CAPACITIVE CMOS READOUT CIRCUITS FOR HIGH PERFORMANCE MEMS ACCELEROMETERS

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CAPACITIVE CMOS READOUT CIRCUITS FOR HIGH PERFORMANCE MEMS ACCELEROMETERS

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Kepenek, Reha

ABSTRACT

CAPACITIVE CMOS READOUT CIRCUITS FOR HIGH PERFORMANCE MEMS ACCELEROMETERS

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This thesis presents the development of high resolution, wide dynamic range sigma-delta type readout circuits for capacitive MEMS accelerometers. Designed readout circuit employs fully differential closed loop structure with digital output, achieving high oversampling ratio and high resolution. The simulations of the readout circuit together with the accelerometer sensor are performed using the models constructed in Cadence and Matlab Simulink environments. The simulations verified the stability and proper operation of the accelerometer system. The sigma-delta readout circuit is implemented using XFab 0.6 μm CMOS process. Readout circuit is combined with Silicon-On-Glass (SOG) and Dissolved Wafer Process (DWP) accelerometers. Both open loop and closed loop tests of the accelerometer system are performed. Open loop test results showed high sensitivity up to 8.1 V/g and low noise level of 4.8 μg/√Hz. Closed loop circuit is implemented on a PCB together

with the external filtering and decimation electronics, providing 16-bit digital output at 800 Hz sampling rate. High acceleration tests showed ±18.5 g of linear acceleration range with high linearity, using DWP accelerometers. The noise tests in closed loop mode are performed using Allan variance technique, by acquiring the digital data. Allan variance tests provided 86 μg/√Hz of noise level and 74 μg of bias drift. Temperature sensitivity tests of the readout circuit in closed loop mode is also performed, which resulted in 44 mg/ºC of temperature dependency.

Two different types of new adaptive sigma-delta readout circuits are designed in order to improve the resolution of the systems by higher frequency operation. The two circuits both change the acceleration range of operation of the system, according to the level of acceleration. One of the adaptive circuits uses variation of feedback time, while the other circuit uses multi-bit feedback method. The simulation results showed micro-g level noise in closed loop mode without the addition of the mechanical noise of the sensor.

Key words: Sensor interface electronics, Capacitive readout circuit, Sigma-Delta Modulator, Closed Loop Systems, MEMS Accelerometers, Inertial Sensors.

ÖZ

YÜKSEK PERFORMANS MEMS İVMEÖLÇERLER İÇİN SIĞASAL CMOS OKUMA DEVRELERİ

Kepenek, Reha
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Yard. Doç. Dr. Haluk Külah
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Şubat 2008, 144 sayfa

Bu tezde yüksek çözünürlüklü, geniş ölçüm aralığı olan, sığasal MEMS ivmeölçerler için sigma-delta tipi okuma devrelerinin geliştirilmesi anlatılmaktadır. Tasarlanan okuma devresinin, sayısal çıkışlı, tam farksal, kapalı devre yapısıyla, yüksek örnekleme ve yüksek çözünürlük elde edilir. Okuma devresi ve ivmeölçer duyargasının modelleri Cadence ve Matlab Simulink ortamlaında hazırlanıp, benzetimleri yapılmıştır. Benzetimler, ivmeölçer sisteminin kararlı ve doğru çalışmasını doğrulamıştır. Sigma-delta okuma devresi XFab 0.6 μm CMOS süreci kullanılarak üretilmiştir. Okuma devresi Silicon-On-Glass (SOG) ve Dissolved Wafer Process (DWP) ivmeölçer yapılarıyla birleştirilmiştir. İvmeölçer sisteminin, açık ve kapalı döngü testleri yapılmıştır. Açık döngü test sonuçları 8.1 V/g'ye kadar yüksek hassasiyet ve 4.8 μg/√Hz'lik düşük gürültü seviyesi göstermiştir. Kapalı döngü devre, dış filtreleme ve seyreltme elektroniği ile birlikte baskı devre kartına

yerleştirilmiş ve 800 Hz örnekleme frekansında 16-bit sayısal çıktı elde edilmiştir. DWP ivmeölçerler kullanılarak yapılan yüksek ivme testleri, ±18.5 g ivme ölçüm aralığında yüksek doğrusallık göstermiştir. Kapalı devre gürültü testleri veriler toplanıp, Allan Variance tekniği kullanılarak gerçekleştirilmiştir. Allan Variance testleri 86 μg/√Hz gürültü seviyesi ve 74 μg sabit kayma değeri göstermiştir. İvmeölçer sisteminin sıcaklık testleri de yapılmış ve 44mg/ºC sıcaklık hassasiyeti gözlemlenmiştir.

Çözünürlüğü artırmak için, yüksek örnekleme frekansı kullanılarak, iki farklı, yeni, uyarlamalı sigma-delta okuma devresi tasarlanmıştır. İki devre de, uygulana ivme değerine göre ivme ölçüm aralığını değiştirmektedir. Uyarlamalı devrelerin biri, geri besleme süresi değişimi kullanırken, diğer devre çok-bitli geri besleme metodunu kullanır. Benzetim sonuçları kapalı döngüde, duyarga gürültüsü katılmadan mikro-g seviyesinde gürültü elde edildiğini göstermiştir.

Anahtar kelimeler: Duyarga Arayüz Elektroniği, Sığasal Okuma Devresi, Sigma-Delta Modülator, Kapalı Devre Sistemler, MEMS İvmeölçerler, Eylemsizlik Duyargası.

To My Sister, Damla

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CHAPTER 1

INTRODUCTION

Silicon-based inertial sensors, including accelerometer and gyroscopes, are one of the most crucial types of Micro-Electro-Mechanical-Systems (MEMS) devices. Due to their low cost, low power, small size, and high reliability, MEMS accelerometers have extensive use, such as in airbag safety systems in automotive area, in digital cameras for picture stabilization, for vibration monitoring in industry, microgravity measurements in space, tilt control and platform stabilization, seismometry, and inertial navigation and guidance [1]. Measurement bandwidth and acceleration needs of these application areas are illustrated in Figure 1.1. From all of these areas, MEMS accelerometers have an increasing vital role in navigational systems. The navigational area needs high resolution, particularly having sub-micro-g resolution accelerometers. In order to achieve sub micro-g resolution, both of the two main components, the sensor and the readout electronics, of an accelerometer system should be designed with extreme attention. Recently, capacitive accelerometers have become very attractive for high precision μg applications due to their high sensitivity, low temperature sensitivity, low power, wide dynamic range and simple structure [2-7]. There is still a necessity of high performance readout circuits to read the extremely small movements of capacitive accelerometers. Therefore, the research presented in this thesis focuses on the navigational purpose readout circuits for capacitive MEMS accelerometer sensors, achieving both high resolution and high range.

A basic explanation of capacitive type accelerometers is given in Section 1.1. In Section 1.2, a general discussion is made on the interface electronics used in capacitive sensing accelerometers. Section 1.3 gives a brief explanation and

comparison of previously designed and implemented accelerometer systems in the literature. Then the accelerometer structures designed and fabricated in METU are discussed in Section 1.4. Finally, Section 1.5 provides the objectives of this research and the organization of thesis.

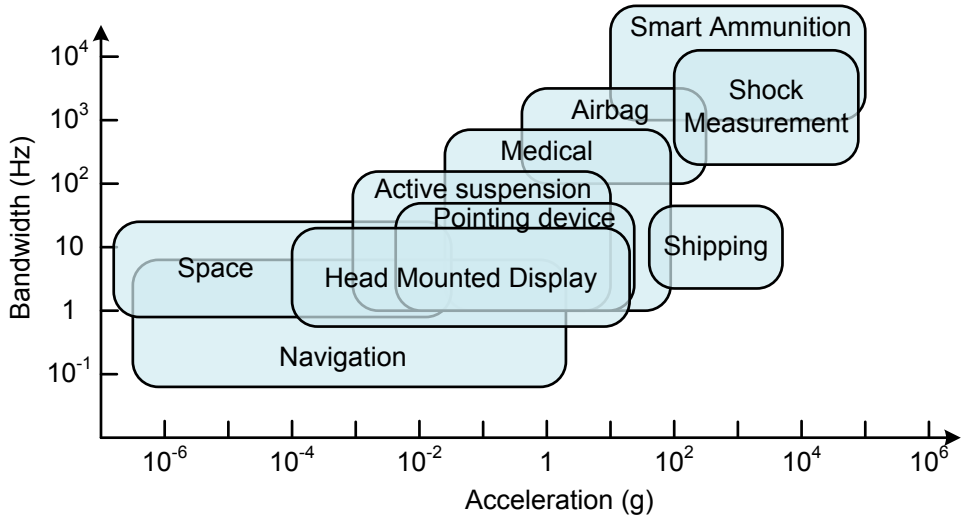


Figure 1.1: The application areas of accelerometers according to the operation range and bandwidth.

1.1. Capacitive Accelerometers

Accelerometers need to measure the movement of an inertial mass in order to detect acceleration. In micro-g level acceleration measurements, displacements of the mass are generally in the order of angstroms. To detect such small displacements, there is a variety of acceleration sensing methods presented in the literature, such as magnetic, tunneling [8], optical, [9] and capacitive sensing. The advantage of capacitive sensing is the ability to obtain highly sensitive and reliable accelerometers, and ease of interfacing with the electronic circuitry.

Basic structure of a capacitive accelerometer is illustrated in Figure 1.2. The accelerometer uses a movable mass, which is connected to base through spring structures. There are also stationary electrode structures on the two sides of the

mass, where the capacitance in between changes according to the displacement of the mass. Commonly, finger-like structures are used to increase the capacitive area between the mass and the electrodes. In order to achieve a highly sensitive capacitive accelerometer, capacitive area should be increased while decreasing the gaps in between the plates. In addition, the mass should be designed large, to accomplish low mechanical noise and high sensitivity. The construction of capacitances on the mechanical structure enables the conversion of a mechanical signal into electrical domain. The next section gives a discussion on basic electronic interface structures, and the capacitive configurations.

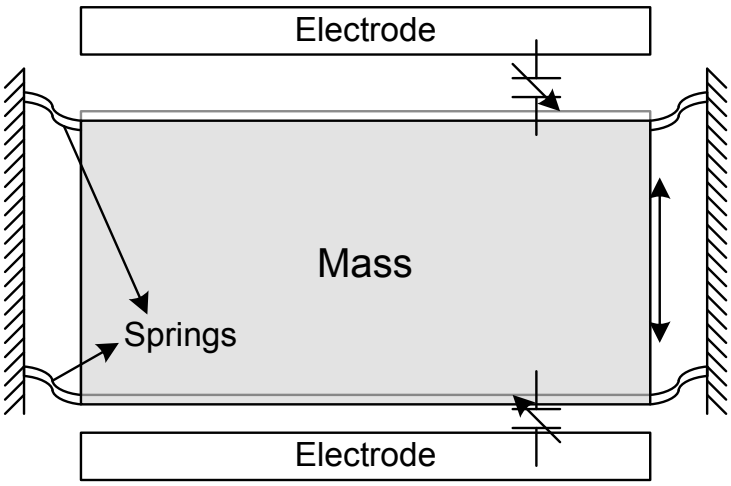


Figure 1.2: Illustration of basic capacitive accelerometer.

1.2. Capacitive Interfaces

There are mainly two capacitive topologies, which are half bridge and full bridge configurations, as shown in Figure 1.3 (a) and (b), respectively. The half bridge configuration is used with single ended readout circuits, either with two sense capacitors or with a sense and a reference capacitor. Square or sinusoidal signals, frequencies of which are much higher compared to the resonance frequency of the accelerometer, are applied at two ends of the half bridge. This creates a charge flow or a voltage at the common node, proportional to the difference of two capacitors.

With this configuration, some non-idealities, such as offset, power supply noises, and other common mode noises are observed, due to the single ended operation.

Full bridge configuration is composed of four capacitors, at least two of which are sense capacitors. In this case, a differential charge flow, or voltage is generated at the sensing nodes of the full bridge. This configuration is used with a differential readout circuitry, and therefore, the common mode noises are not observed, and the configuration has higher sensitivity.

Another capacitor configuration is a pseudo-differential structure as shown in Figure 1.3 (c). In this configuration, the square wave is applied from the common node, and the sensing is performed from the ends of a half bridge structure, which allows the usage of a differential readout circuit, and hence cancelling the common mode non-idealities at the readout circuit.

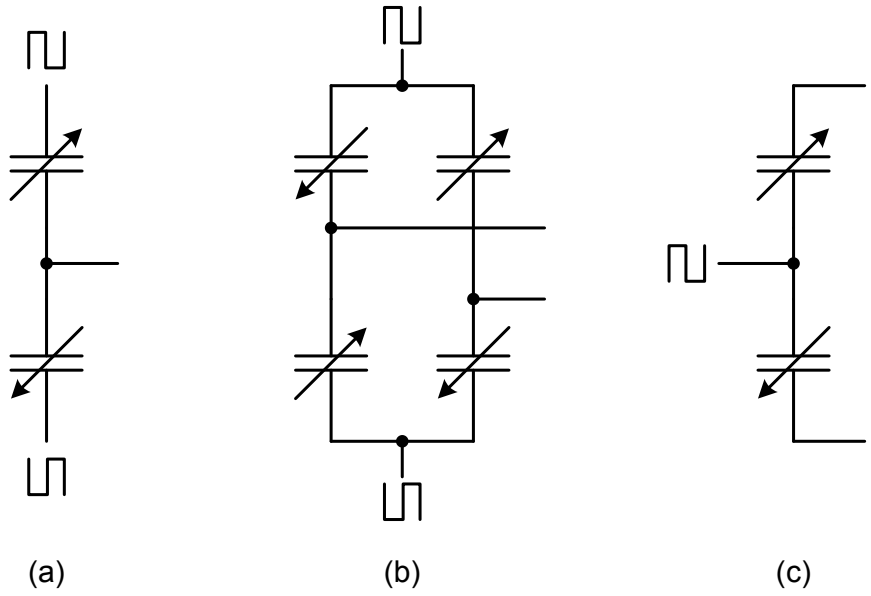


Figure 1.3: Capacitive topologies. (a) Half bridge structure. (b) Full bridge structure. (c) Pseudo-differential half bridge structure.

For reading out the capacitance differences, there are a few main types of readout circuit structures. The readout structures are given with half bridge structures, for the ease of understanding. A basic readout structure, given in Figure 1.4 uses capacitive voltage division between two capacitances [10, 11]. This structure is also

named as ac-bridge amplifier [12, 13, 14], where the voltage created at the sense node of the half bridge is amplified, demodulated and then low-pass filtered to obtain meaningful analog data. The output voltage of the readout circuit is given in Equation (1.1). This circuitry has the disadvantage of having lower performance with high parasitic capacitances; hence, it is not compatible with the non-monolithic structures.

$$V_{out} = V_p \frac{\Delta C}{2C_{s0} + C_p} A_v \tag{1.1}$$

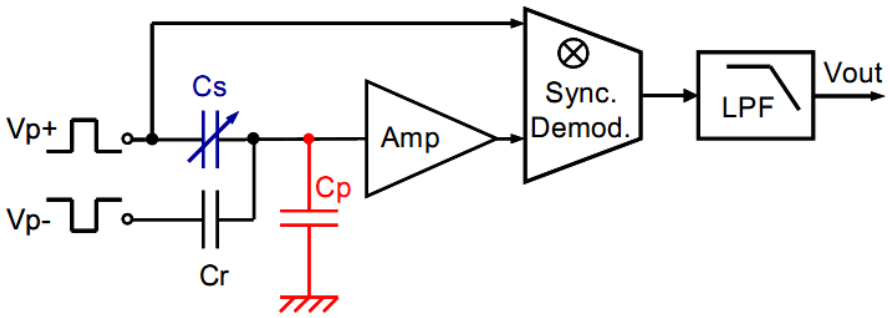


Figure 1.4: AC bridge amplifier structure [12].

Figure 1.5 shows trans-impedance amplifier readout structure, where the capacitors are driven by two sinusoidal signals with 180° phase difference. Sensing node of the half bridge is held at virtual ground by the resistive feedback. The current created due to the capacitance difference flows through the feedback resistance, and a voltage proportional to the capacitance difference is formed, as shown in Equation (1.2). The output is then demodulated and low-pass filtered. This circuitry is most suitable for the resonance mode sensors, because of the need for the sinusoidal drive signal. Moreover, the noise of the circuit is usually dominated by the feedback resistor.

$$V_{out} = 2\pi f_{drive} V_m R_f \Delta C \tag{1.2}$$

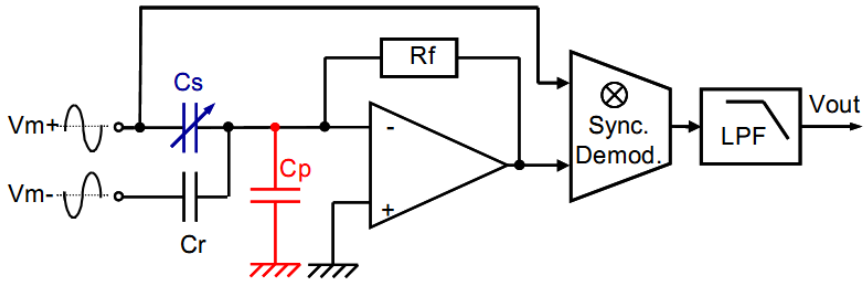
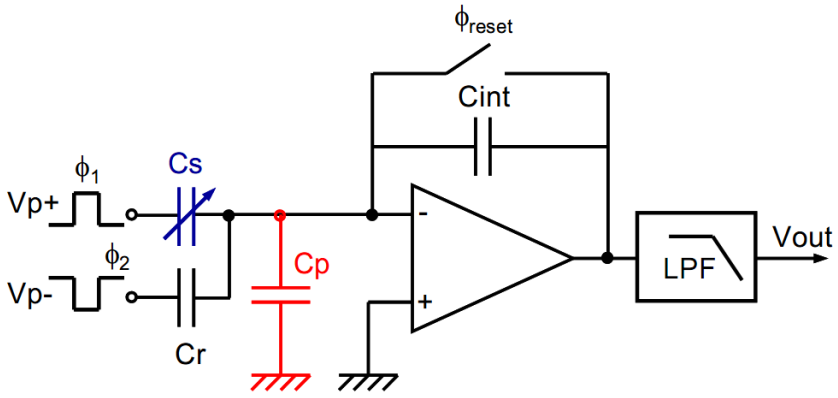


Figure 1.5: Trans-impedance amplifier structure [12].

The readout circuit structure shown in Figure 1.6 is named as a charge integrator, which is the circuit structure selected in this study. Switched capacitor technique is used in the circuitry. In this circuit, the excess charge created due to the capacitance difference, is transferred on to the integration capacitor, C_{int}, and the charge is reset at each readout cycle. The output of the charge integrator should only be low-pass filtered without the need of a separate demodulator. The output of this circuit is independent of the parasitic capacitances, as given in equation (2.1), which makes it suitable for non-monolithic applications. With the use of a switched capacitor circuitry, correlated double sampling (CDS) technique can also be added to the circuitry in order to cancel the low frequency noise sources. Due to these advantages, the switched capacitor readout circuit is the optimum choice for non-monolithic capacitive accelerometers to achieve a high performance accelerometer system.



(1.3)

Figure 1.6: Switched-capacitor charge integrator structure [12].

The next section gives some main examples on these readout circuit structures and capacitive accelerometers existing in the literature, and their system level achievements.

1.3. Previous Work

There are several studies of capacitive accelerometers in the literature. The Figure 1.7 shows the chip photograph of a 3-axis surface micro-machined accelerometer, including the readout circuit on the same chip, which was designed and implemented in University of California, Berkeley [15-17]. There are two sense capacitors, connected in a pseudo differential half-bridge configuration. The readout circuit uses switched capacitor charge integrator to sense the capacitive difference, as shown in Figure 1.8. Since, the sensing nodes of the half bridge structure is floating, an input common mode feedback circuitry is used to set the input common mode voltage. The overall structure is composed of a sigma-delta loop in order to hold the proof mass stationary by applying electrostatic feedback force, which also enables digital output generation. This study achieved 110 μg/√Hz noise with 84 dB dynamic range.

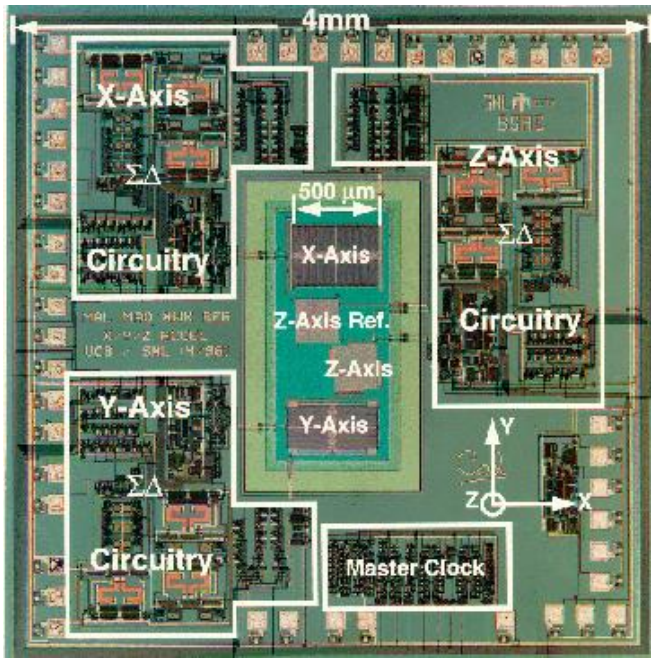


Figure 1.7: Surface micro machined 3-axis monolithic capacitive accelerometer. [15].

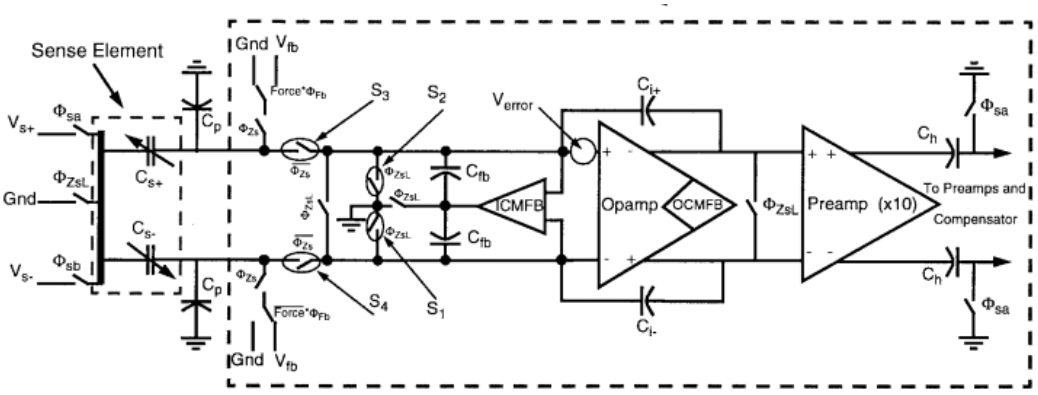


Figure 1.8: Switched capacitor sigma-delta readout circuit designed by University of California, Berkeley [15].

Another surface micro-machined, monolithic accelerometer was designed and implemented in Carnegie Mellon University [18, 19]. The chip photograph of the accelerometer system is given in Figure 1.9. There are 4 separate sense capacitors on the mechanical structure, which allows fully differential configuration. For the readout circuit, ac bridge structure is used, as shown in Figure 1.10. The circuit accomplishes 50 μg/√Hz noise at 400 Hz with ±6g linear range, which results in 106 dB of dynamic range.

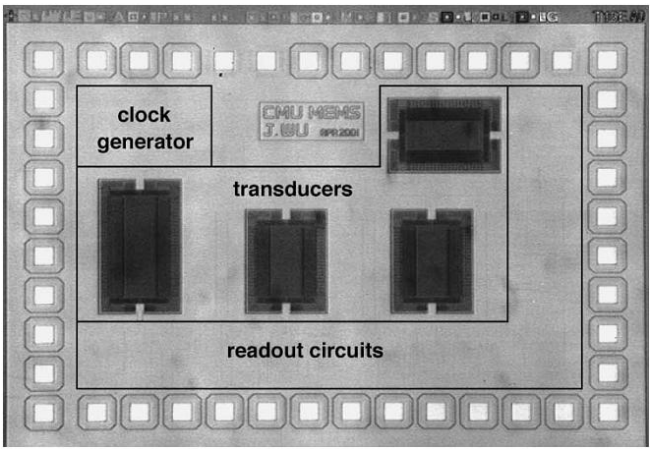


Figure 1.9: The photograph of the surface micro-machined accelerometer chip implemented by Carnegie Mellon University [18, 19].

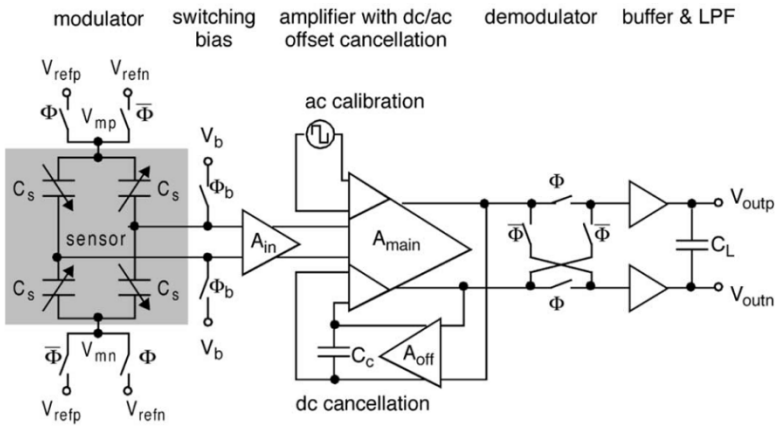


Figure 1.10: Fully differential readout circuit designed by Carnegie Mellon University [18, 19].

In the research carried out in University of Michigan, a z-axis bulk micro-machined accelerometer was designed and implemented, with a large proof mass, as shown in Figure 1.11 [20]. The large proof mass enables high sensitivity and low mechanical noise of the sensor. A fully differential switch capacitor readout circuit is designed and implemented for position sensing with closed loop sigma-delta configuration as shown in Figure 1.12 [21, 22]. Hence, the system achieves noises of 3.5 μg/√Hz in open loop, and 25 μg/√Hz in closed loop force feedback operation, with ±1.35 g acceleration range.

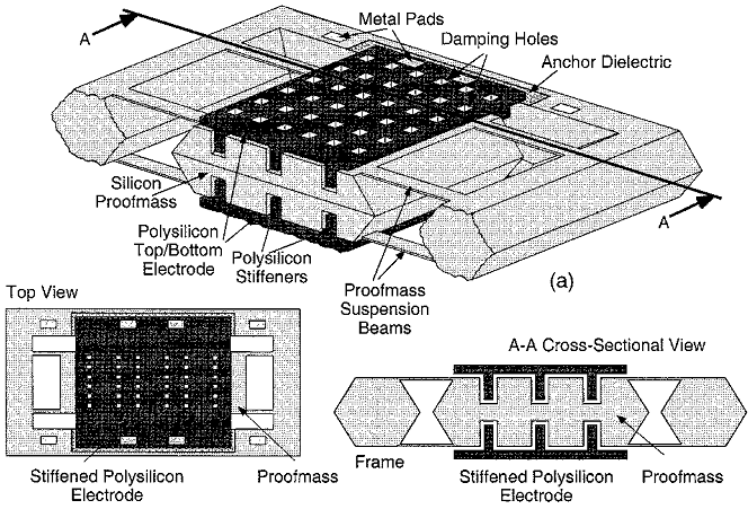


Figure 1.11: Z-axis capacitive accelerometer designed and fabricated at University of Michigan [20].

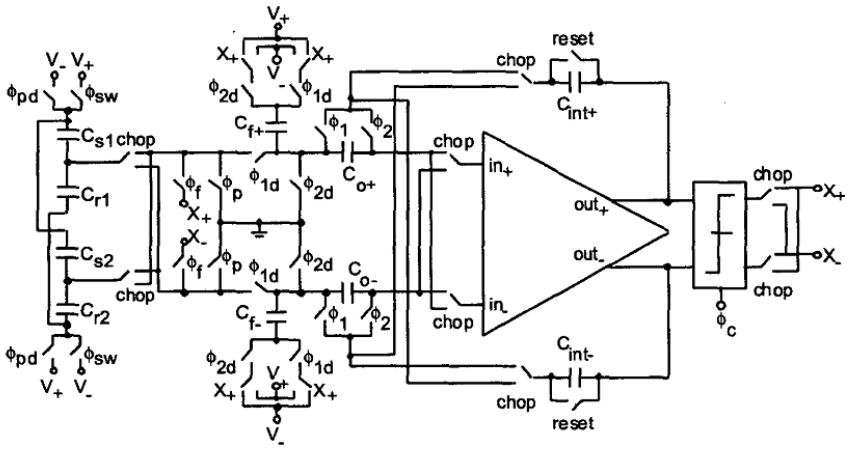


Figure 1.12: Fully differential switched capacitor readout circuit designed in University of Michigan [21].

The research on MEMS accelerometers is also being performed in Georgia Institute of Technology, where an SOI accelerometer structure is fabricated, with large mass and high sensitivity, which is shown in Figure 1.13 [23-25]. The process allows 4 different sense capacitors to be constructed, however all the capacitors are connected at the common node, proof mass of the sensor. This connection of the sense capacitors does not allow construction of full bridge configuration. Therefore, a switching scheme is proposed and implemented to perform the position sensing with 4 sense capacitors, as shown in Figure 1.14. The readout circuit uses switched capacitor charge integration technique, and the system achieves 4.4 μg/√Hz noise at 150 Hz with ±2 g operation range.

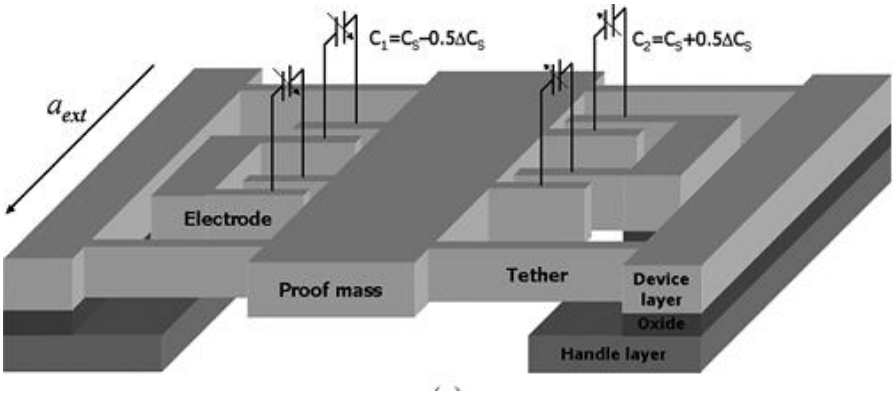


Figure 1.13: Illustration of SOI accelerometer designed and fabricated in Georgia Institute of Technology [23].

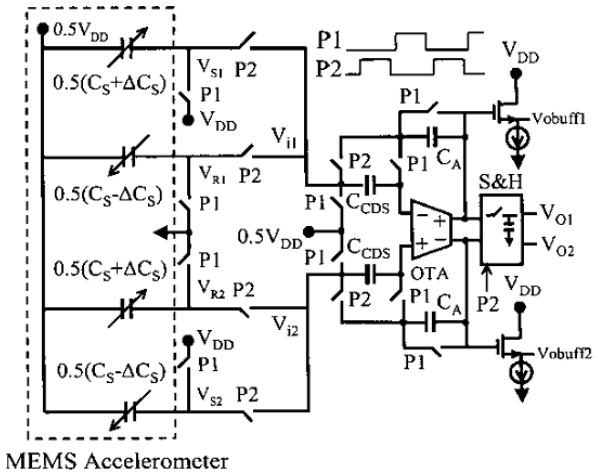


Figure 1.14: Switched capacitor readout circuit with a new switching scheme, designed in Georgia Institute of Technology [25].

Table 1.1 gives a comparison of the performance of some previous capacitive accelerometer studies, existing in the literature, and the proposed achievements of this work. The main performance criteria for an accelerometer are the operation range, resolution and bandwidth. In these studies, both the sensor structure and the readout circuit play an important role, in achieving high performance accelerometer systems. Hence, the purpose of this thesis is to obtain high resolution and wide operational range in closed loop, i.e. improving the dynamic range, by improving the readout circuit structure.

Table 1.1: A comparison of previous studies on capacitive accelerometer systems.

Source	Accelerometer type	Bandwidth	Linear Range	Resolution
M. Lemkin et.al., 1999 [16]	Surf. micro-machined Monolithic, 3-axis,	100	~ ±1 g	110, 160, 990 µg/√Hz
J. Chae, et.al., 2000 [26]	SOG, Lateral	~ 2 kHz	> ±2 g	<100 µg/√Hz
G. Fedder et.al., 2004 [18]	Surf. Micro-machined Monolithic	2 kHz	±6 g	50 µg/√Hz
M. Lemkin, B. Boser, 1996 [27]	Surf. Micro-machined Monolithic	~8 kHz	±3.5 g	500 µg/√Hz
X. Jiang et.al., 2002 [28]	Surf. Micro-machined Lateral	~1.4 kHz	0.125 g	2 µg/√Hz
H. Kulah, 2003 [22]	Surf. – Bulk micromachining	100 Hz	±1.35 g	3.5 µg/√Hz
B. V. Amini et.al., 2004 [23]	Lateral, SOI Bulk micromachining	150 Hz	±2 g	4.4 µg/√Hz
Proposed study of this thesis (closed loop)	*Lateral, Bulk micromachining*	*~ 1 kHz*	*> ±20 g*	*<100 µg/√Hz*

1.4. Accelerometers Fabricated at METU

Accelerometer sensors used in this research were fabricated by MEMS-VLSI research group at Middle East Technical University. There are two main types of sensor structures, one of which is named as Silicon-On-Glass (SOG) accelerometers, as shown in Figure 1.15. The structure is placed on a glass substrate, and the silicon is shaped using DRIE processing [29]. Accelerometers have comb finger structures on each side of the proof mass, which constitutes two differential capacitances. The thickness of the structural layer is 100 μm, which allows large proof mass, hence, high sensitivity and low mechanical noise. However due to the large mass of the sensor, the operational range of the accelerometer is limited, in both open loop and closed loop operation.

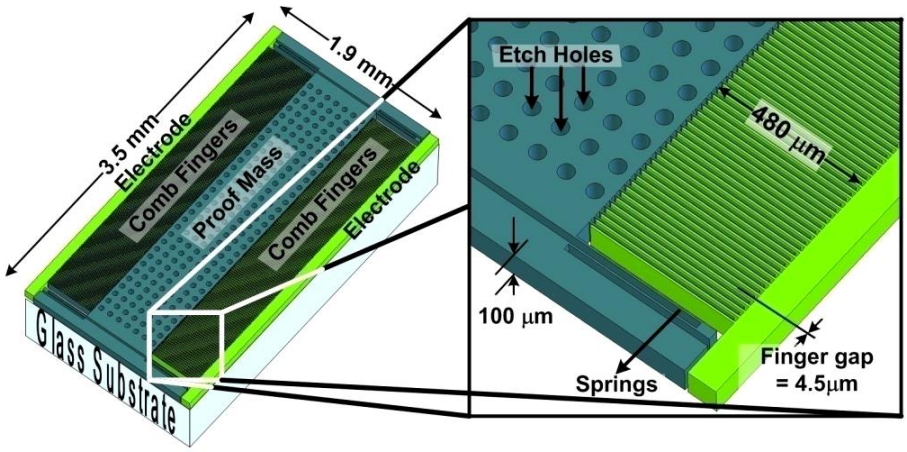


Figure 1.15: Silicon-On-Glass (SOG) accelerometer structure designed and fabricated in METU [29].

The fabrication process of the SOG accelerometer requires only 4 masks. First, a glass substrate is etched to form anchor regions (Figure 1.16 (a)). Then, a shielding metal layer is patterned on a 100μm-thick silicon wafer (Figure 1.16 (b)). This layer prevents DRIE notching and acts as a heat sink during DRIE. Next, the silicon and glass wafers are anodically bonded (Figure 1.16 (c)). Metal contacts are evaporated and patterned, and finally the wafer is etched with DRIE to define the proof mass and sensing electrodes (Figure 1.16 (d, e, f)). Then the shielding layer is removed.

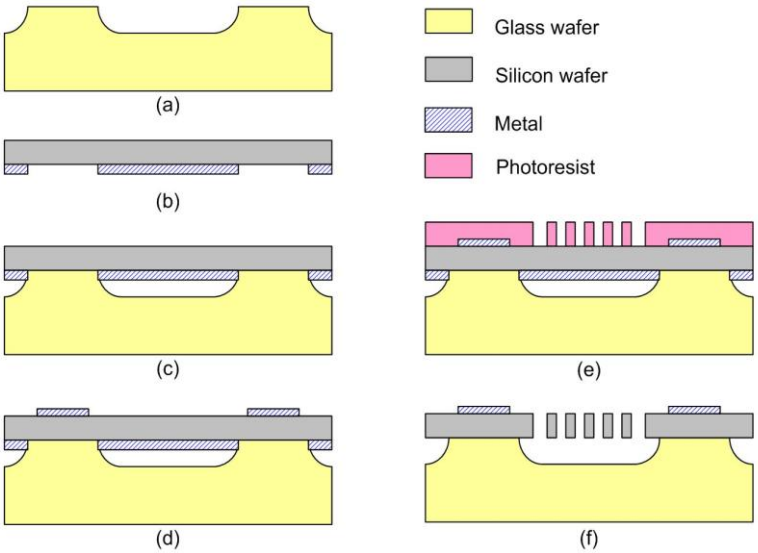


Figure 1.16: Fabrication process of the SOG accelerometer [29].

The second structure fabricated by the research group uses dissolved wafer process (DWP) technique [29], as illustrated in Figure 1.17, which allows smaller gaps between the finger structures. Smaller gaps results in higher sensitivity, due to the increased capacitance. However, the structural thicknesses of these devices are also decreased down to 15 µm, which decreases the sensitivity. The proof masses of the DWP accelerometers are smaller due to the decreased structural thickness. Although this results in higher mechanical noise, the operational linear range of the system is increased up to 20 to 30 g's depending on the designed accelerometer.

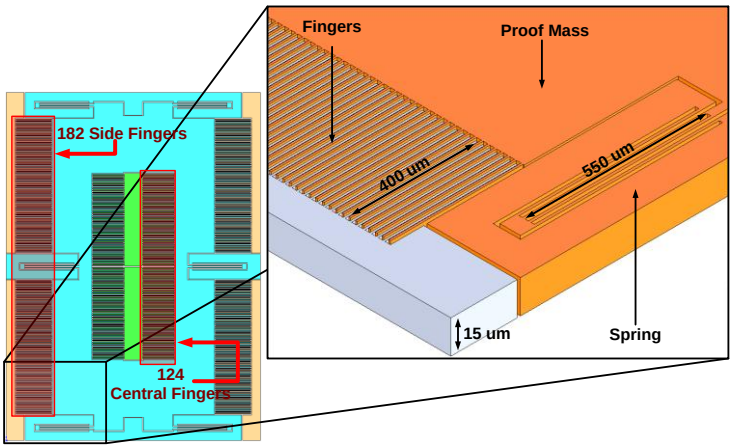


Figure 1.17: Dissolved Wafer Process (DWP) accelerometer structure designed and fabricated in METU [29].

Fabrication process of the DWP accelerometer requires 3 masks. First, a glass substrate is etched to form anchor regions of the accelerometer (Figure 1.18 (a)). After the formation of the anchor regions chromium and gold is sputtered on the glass wafer and patterned to form the electrical connections (Figure 1.18 (b)). Then, a 100µm thick silicon wafer is doped with boron (Figure 1.18 (c))and etched reactively to form the structural layer (Figure 1.18 (d)). Next, silicon and glass wafers are anodically bonded (Figure 1.18 (e)) and the undoped silicon is completely etched (Figure 1.18 (f)). The parameters of two sample accelerometers of the two kinds designed and fabricated in METU are given in Table 1.2.

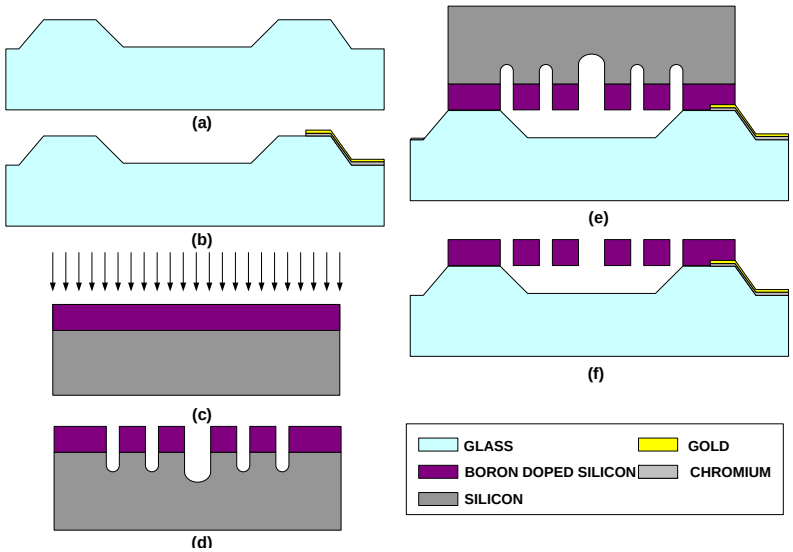


Figure 1.18: Fabrication process of the DWP accelerometer [29].

Table 1.2: Parameters of capacitive accelerometers fabricated at METU.

Parameter	Value (SOG)	Value (DWP)
Mass of proof mass	0.72 milli-g	0.18 milli-g
Resonant frequency	1.53 kHz	1.72 kHz
Proof mass thickness	100 µm	15 µm
Sensing gap	4.48 µm	1.1 µm
Sense capacitance	24.8 pF	16.2 pF
Sense fingers length	500 µm	400 / 350 µm
Number of fingers	290	182 / 124
Sensitivity	1.88 pF/g	0.96 pF/g
Brownian noise	2.81 µg/√Hz	3.62 µg/√Hz

1.5. Objectives and Organization of the Thesis

The main objective of this thesis is to design and implement a readout circuit to achieve high resolution and high dynamic range together with the accelerometer sensors. The following is a summary of the objectives.

- *Design and implementation of a complete accelerometer readout circuit.*

  A sigma-delta closed loop capacitive accelerometer readout circuit is to be designed, and implemented with a resolution in the order of micro-g level, with high dynamic range. The aim is to obtain a low power, low cost, closed loop accelerometer system with a linear range of ±20 g, and resolution below 100 μg.

- *Modeling and simulation of the accelerometer system and verification of operation.*

  Both the accelerometer and readout circuit are to be modeled in MATLAB Simulink and Cadence environments, and the verification of operation and stability of the system is to be done.

- *Development of new readout techniques to improve the performance of the accelerometer system.*

  Adaptive readout structures are to be designed and implemented in order to achieve higher resolution and higher dynamic range.

- *System level testing of the accelerometer with the readout electronics.*
  Full testing of the accelerometer system is to be performed, including sensitivity, linearity, range and noise tests.

Chapter 2 of this thesis gives a brief explanation of the theory of sigma-delta modulators, where the main properties and limitations are discussed.

Chapter 3 presents the modeling of the accelerometer system and obtained simulation results using the constructed models. First, it explains the accelerometer

sensor structure, by defining the sensor parameters. Then, the modeling and simulations of the sensor and readout circuit are examined. Finally, the model constructed in Cadence environment is discussed and the simulation results are given.

Chapter 4 describes the design stage of sigma-delta fully differential readout circuit. After explaining the operation of each block of the readout circuit and supplying the simulation results, the layout considerations and performance limitations are discussed.

Chapter 5 describes the design of adaptive readout circuits. After presenting the operation of two different adaptive readout circuits, the simulation results are given. Finally, a comparison of the readout circuits is given.

Chapter 6 of the thesis provides the test results obtained throughout the research of this subject. First, the implementation of the readout circuit together with the sensor and the external electronics for closed loop operation is explained. Then, the open loop and closed loop test results are given separately.

Lastly, Chapter 7 puts a conclusion to the thesis, and gives a direction for the future work of the research.

CHAPTER 2

THEORY OF SIGMA DELTA MODULATORS

This chapter presents the theory of operation of sigma-delta modulators. Sigma-delta modulators provide high resolution, especially at low bandwidth analog to digital converter applications, with the aid of oversampling and noise shaping concepts. Since the acceleration signals to be measured has low bandwidth, sigma-delta modulation gives great advantage in providing high resolution, with low cost. For applying the modulation technique with a mechanical structure, sigma-delta modulation itself should be understood, primarily. In this purpose, the concepts for comprehending the theory of sigma-delta modulation are explained in this chapter. Section 2.1 gives a brief description of the structure of a first order sigma-delta modulator. The oversampling concept is explained in Section 2.2. Section 2.3 explains the noise-shaping concept in sigma-delta modulators. Section 2.4 gives the application of sigma-delta modulator as an electromechanical system, combined with the accelerometer sensor.

2.1. Sigma – Delta Modulators

Sigma-delta modulation was developed from delta modulation [30]. Delta modulation is an A/D conversion technique, where the output is quantized according to how fast the input signal amplitude varies. Hence, if the output is 1-bit, the bit stream at the output indicates only the sign of the variations of the input signal. Figure 2.1 shows the basic block diagram of a delta modulator. Integrator in the feedback loop is trying to predict the input signal and an error signal is generated after taking the difference between the prediction and the input signal. This error signal is then quantized using a comparator. Depending on the sign of the error

signal, another prediction is made by increasing or decreasing the value at the output of the integrator. On the demodulation side, the 1-bit output stream should be integrated to obtain the quantized signal. Then, with the use of a low-pass filter, the analog input signal can be regenerated. [30, 31]

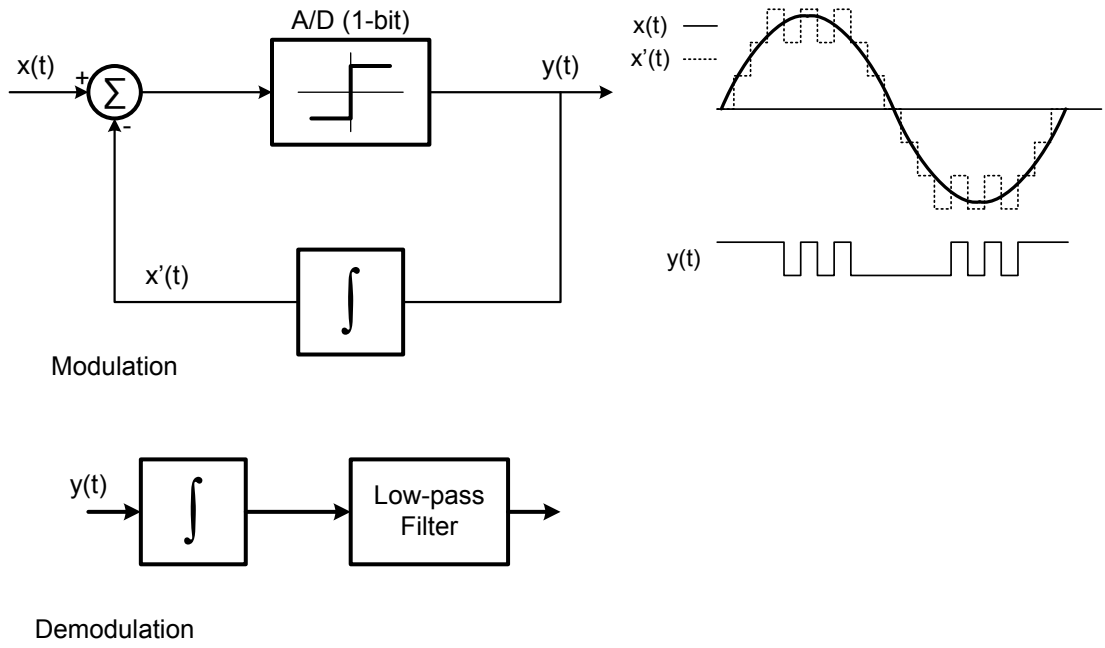


Figure 2.1: Block diagram of the delta modulator structure.

The operations performed in this system are linear, so the integrator stage at the demodulator can be carried to the input stage, as shown in Figure 2.2(a). Moreover, in the block diagram in Figure 2.2(b), the two integrators are combined into one integrator. This structure forms the first order sigma-delta modulator. In this structure, the output is directly dependent on the input signal; hence, the demodulator side only needs a low-pass filter. The operation is also performed using a single integrator on the modulator side; hence, it is much simpler than the delta modulator structure. The output of a sigma-delta modulator is commonly single bit; the resolution in amplitude is carried to the resolution in time, which is achieved by oversampling.

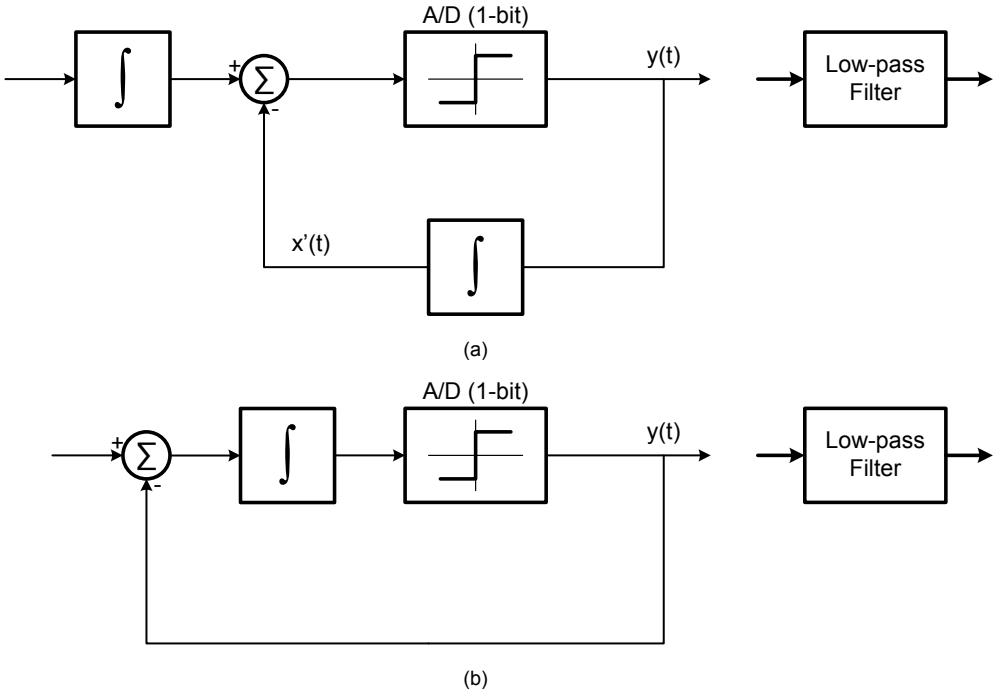


Figure 2.2: Block diagram of Sigma – Delta modulator (a) with two integrators, (b) with the integrator blocks combined into one.

The sigma-delta A/D converters are widely used for high resolution and low bandwidth applications due to the noise shaping and oversampling techniques. Oversampling sigma-delta modulators are extensively used for low frequency analog-to-digital converters especially in audio applications where the over-sampling ratio can be considerably high and the noise rejection is very efficient [32, 33]. In micromechanical accelerometers, since the mechanical bandwidth is usually quite small (<2kHz), sigma-delta conversion can effectively reduce noise and improve overall performance [34-36]. The following sections describe the properties of sigma-delta modulators.

2.2. Oversampling and Quantization

Oversampling is a crucial concept in sigma–delta modulators in order to increase the resolution of the system by increasing the sampling frequency of the system. Oversampling increases the resolution in the time domain, and decreases the in-band

noise. The Nyquist rate A/D converters have a sampling rate twice the bandwidth of the signal frequency; but the oversampling converters use higher sampling rates. The oversampling ratio is defined as in Equation (2.1).

$$M = \frac{f_s}{2f_{BW}} \tag{2.1}$$

where f_s and f_{BW} are the sampling frequency and the signal frequency bandwidth, respectively.

Quantization and the error caused by quantization is a significant point, which should be considered primarily in an A/D system. In Nyquist sampling quantizers, the rms value of the error is given as in Equation (2.2) [31].

$$e_{rms}{}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2\, de = \frac{\Delta^2}{12} \tag{2.2}$$

where, Δ is the quantization level spacing. Hence the quantization error is bounded between $\Delta/2$ and $-\Delta/2$, and have equal probability of taking any value in between.

If there is a dither signal, with sufficiently large in amplitude, the quantization error can be assumed to be a white noise [31]. Using this assumption, for an oversampling quantizer, the noise power inside the signal bandwidth is given as in Equation (2.3).

$$v_{qn,rms}^2 = \frac{e_{rms}^2}{M} = \frac{\Delta^2}{12.M} \tag{2.3}$$

Conceptually, oversampling provides resolution in time, instead of resolution in amplitude. By decimation process, the high-resolution result can be obtained. However, as can be observed from the quantization noise expression given in

Equation (2.3), doubling the sampling frequency results only a 3 dB enhancement in the quantization noise. Therefore, oversampling by itself does not improve the resolution of the system as desired. The sigma-delta modulation, not only does oversampling but also the noise shaping, which decreases the in-band quantization error considerably.

2.3. Noise Shaping

Noise shaping concept is the major purpose of usage of sigma-delta modulation. For a first order sigma-delta modulator, the quantization error is added in the last stage, where analog data is converted to digital, as shown in Figure 2.3.

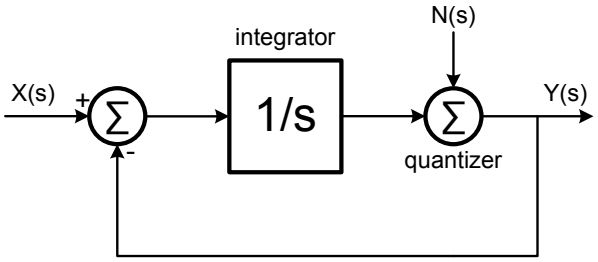


Figure 2.3: Block diagram of the sigma – delta modulator in s-domain, with the quantization error.

The transfer function of the system can be calculated as given in Equation (2.4), which results in a low pass filter characteristic. For calculating the transfer function from input to output, the quantization noise is taken to be zero.

$$\frac{Y(s)}{X(s)} = \frac{1}{s+1} \tag{2.4}$$

For calculating the noise transfer function, input signal is assumed zero. So, the noise of the system becomes as given in Equation (2.5).

$$\frac{Y(s)}{N(s)} = \frac{s}{s+1} \tag{2.5}$$

This result has a high pass filter characteristic. In this way, the quantization noise is shaped and carried to high frequencies. Hence, in-band noise power of the system is decreased by using a sigma-delta structure, compared to an oversampling quantizer. The in-band quantization noise of a sigma-delta modulator is expressed as given in Equation (2.6) [31].

$$V_{qn,rms} = e_{rms} \frac{\pi^L}{M^{L+0.5}\sqrt{2L+1}} \tag{2.6}$$

where, L is the order of the modulator, M is the oversampling ratio and e_{rms} is the rms value of the quantization noise calculated by Equation (2.2). The above equation shows that, as the order of the sigma-delta modulator increases, the more of the quantization noise is carried to high frequencies and the less in-band quantization noise is observed. Figure 2.4 gives the noise transfer function of multi order sigma-delta modulators and makes a comparison between noise shaping of the different order of sigma-delta modulators. As can be observed from this figure, increasing the order of the modulator decreases the in-band noise contribution. Figure 2.5 illustrates the dependence of the in-band quantization of the modulator to the oversampling ratio and the modulator order.

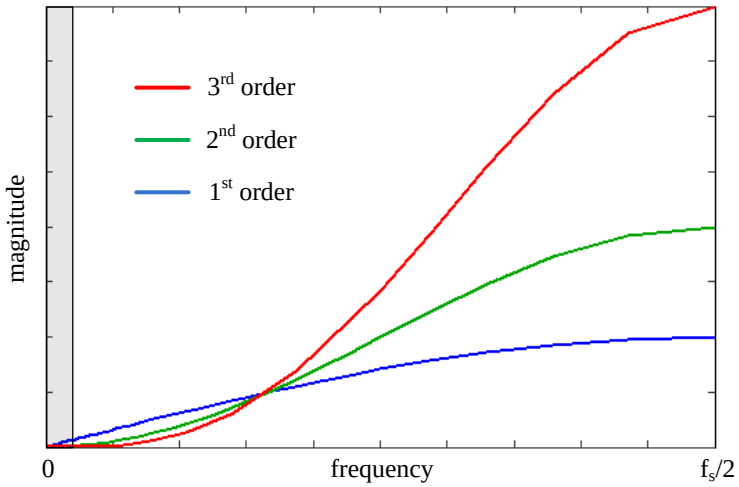


Figure 2.4: Noise response of various order sigma – delta modulators

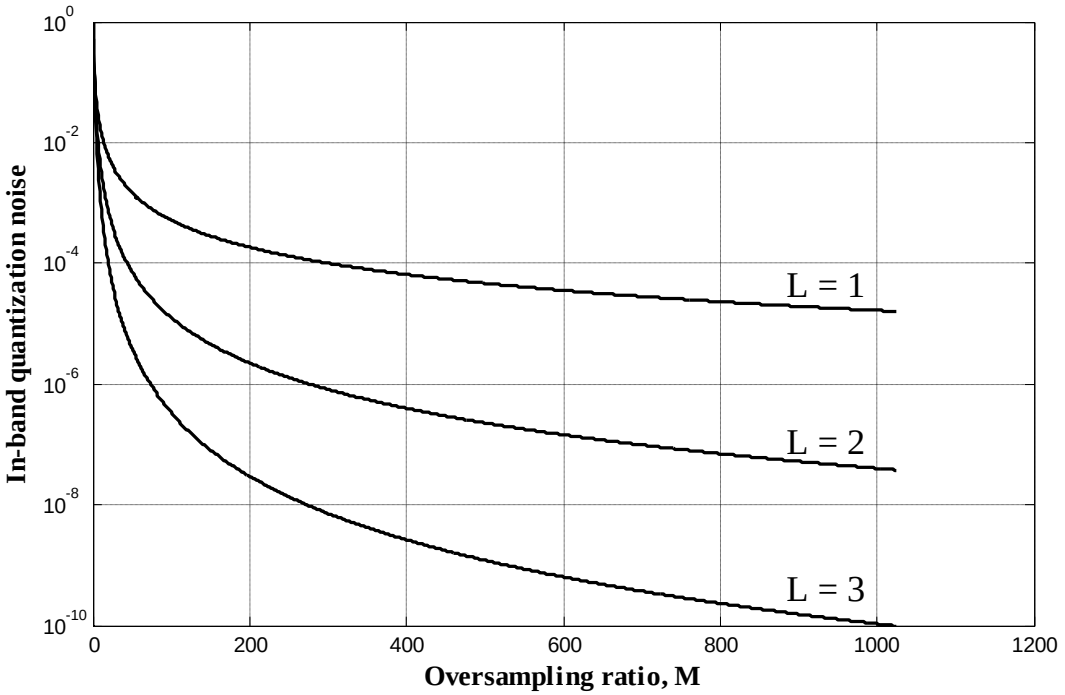


Figure 2.5: In band quantization noise of sigma – delta modulators, depending on the oversampling ratio and modulator order.

2.4. Filtering and Decimation

The instantaneous output of a sigma-delta modulator is generally not meaningful by itself, because of the high quantization noise included at high frequencies, especially in the case of using high sampling rate and low resolution in amplitude quantization. The signals at different stages of a sigma-delta modulator are illustrated in Figure 2.6. The output stream includes the input signal at the low frequency band with the quantization noise. As explained in the previous section, the quantization noise is shaped and mostly carried to the high frequency band. Hence, to extract the signal, from the output data stream, a low pass filtration is needed. The low pass filtration is preferred to be a digital stage, where high quality and low cost filters can be implemented using digital signal processing.

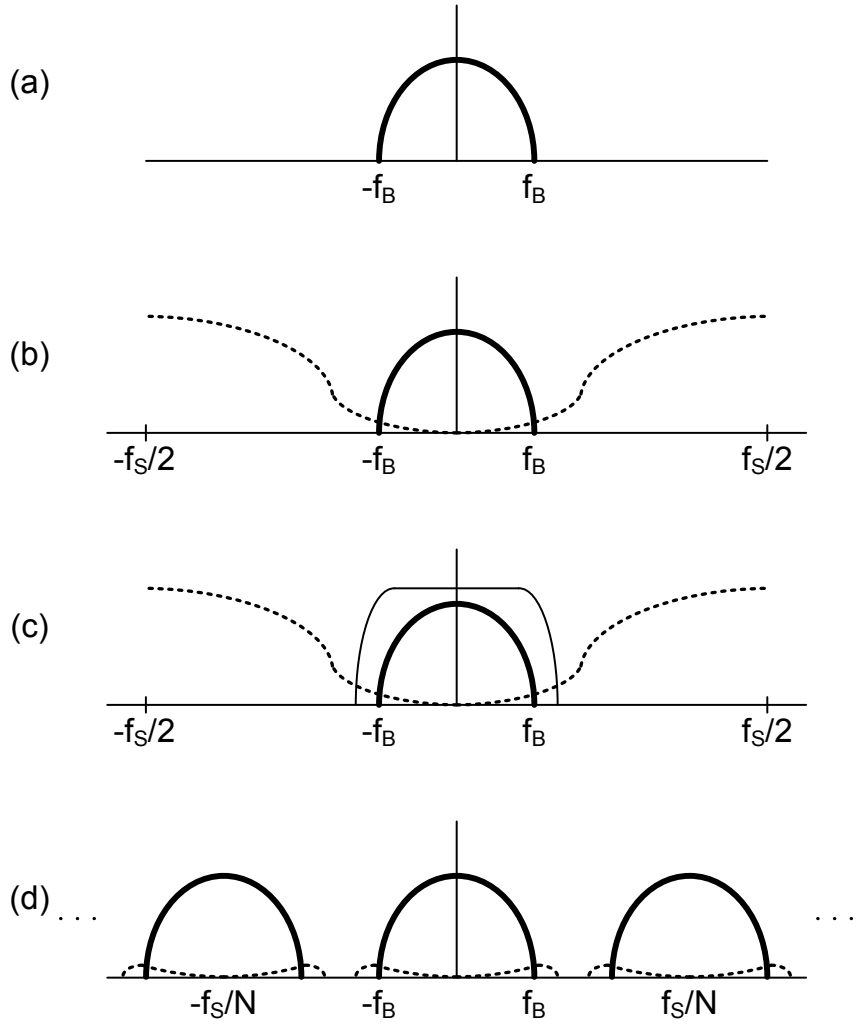


Figure 2.6: (a) Input signal, (b) output of the modulator with the quantization noise, (c) low pass filtration, (d) low pass filtered & decimated output.

The low pass filtered data has a low bandwidth; however, the sampling rate does not change with the filtration process. A sampling rate at the Nyquist frequency is sufficient at the output of the low pass filter. Hence, following the digital filtration stage, a decimation process is generally needed, for removing the unnecessary data, and ease of data processing. In sigma-delta modulator systems, generally the decimation and filtering are carried out in the same stage, which decreases the computation time during digital filtering.

2.5. Electromechanical Sigma – Delta Modulator

Sigma-delta modulators are well suited for low frequency applications, because of the fact that high oversampling ratio is needed for achieving high resolution. Hence, for a mechanical structure, which has a bandwidth in the range below a few kHz, a sigma-delta modulation would result in high resolution. Moreover, a mechanical structure, such as an accelerometer, is a second order integrator by itself, and hence directly can be used as the integrator stage in the sigma-delta modulator structure. As shown in Figure 2.7, the input to the system is acceleration and the feedback is applied in the form of acceleration, with the application of an electrostatic feedback force. The measured parameter from the mechanical sensor is the position. Hence, the usage of a second order mechanical system together with the readout circuit in closed loop, results in a second order sigma-delta loop to be formed. For reading the sensor mass position, generally capacitive techniques are used, where a capacitive change occurs depending on the position of the mass of the mechanical sensor. For reading out the capacitance, an amplifier is needed. For operating at high oversampling ratios, the slew rate and gain bandwidth product of this amplifier carries high importance.

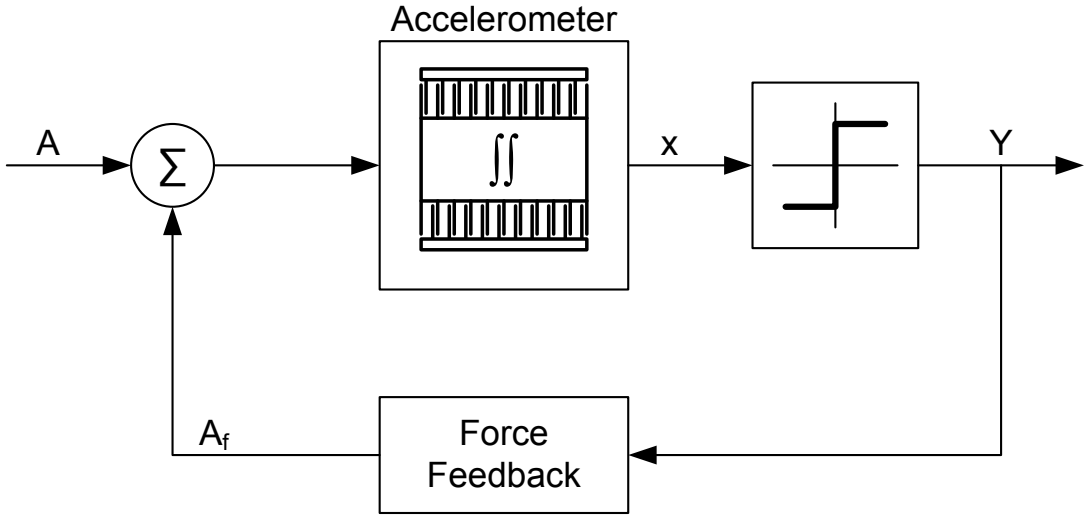


Figure 2.7: The block diagram of the closed loop electromechanical system.

In sigma-delta modulators, multi-bit structures are not preferred commonly due to more complex readout circuit, and the non-linearity of the quantized levels of analog to digital converter. Thus, a single bit output is commonly used, in which the circuitry becomes much simpler and the non-linearity problem caused by the A/D conversion does not exist because of the two-level force feedback. Using a single bit output results in using a single comparator at the output stage following the amplifier. The feedback is applied to the mechanical sensor according to the output generated at the comparator stage. Electrostatic feedback force is applied in either direction of the mechanical sensor, which corresponds to an acceleration value applied to the mechanical mass. In the sigma-delta loop, the displacement of the mechanical mass is held around zero, with feedback pulses at high sampling rate, which results in a motion of the mechanical mass around zero displacement. This motion is called mass residual motion, which is one of the noise sources of the electromechanical sigma-delta modulators. Mass residual motion will be discussed in detail in Chapter 3 and 4.

2.6. Conclusion

This chapter gave a brief explanation of sigma-delta modulators and their significant properties, such as oversampling and noise shaping. Sigma-delta modulation is well suited for the accelerometer application, because of the low bandwidth of acceleration signals, and the integration of the sensor into the loop, forming an electro-mechanical sigma-delta structure. With the use of high oversampling ratios, it is possible to carry the quantization noise to high frequencies, and obtain a high resolution system. The next chapter gives the modeling of the sigma-delta system, together with the readout circuit and the accelerometer, and discusses the stability of the sigma-delta loop.

CHAPTER 3

MODELING & SIMULATIONS

This chapter gives the modeling of the mechanical sensor and the readout circuit in different environments and the simulations performed for understanding the operation of electromechanical sigma-delta modulator system. In section 3.1, a detailed explanation of the accelerometer mechanical system is presented, including the clarification of the parameters included in the transfer function of the system, such as spring constant and damping. Then, the accelerometer models constructed in Cadence environment is explained. Section 3.2 gives the complete system model generated in Matlab Simulink environment. Lastly, in Section 3.3, the closed loop analysis and stability concerns are discussed.

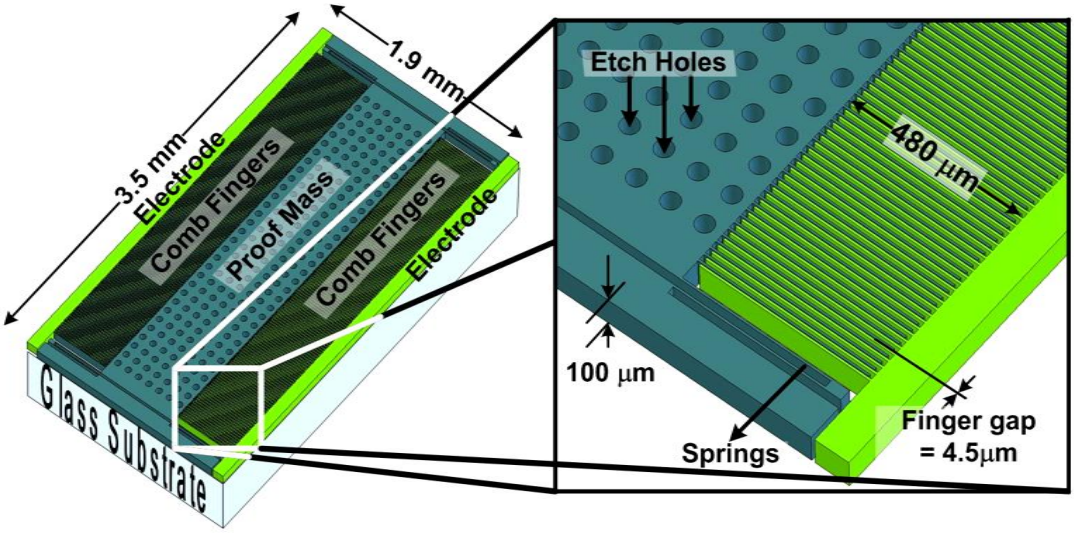
3.1. Modeling the Accelerometer

Both of the sensor structures used in this research has similar lateral comb finger structures to obtain capacitive sensing. Figure 3.1 illustrates the structure of Silicon-On-Glass (SOG) accelerometers designed in the research group, together with the accelerometer parameter dimensions.

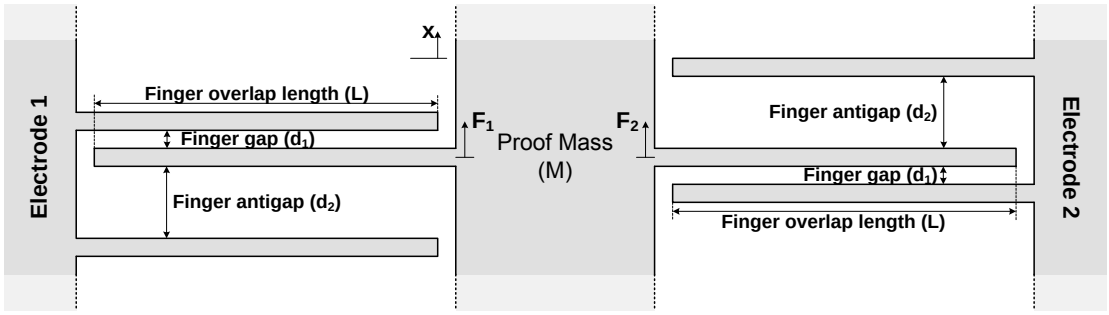
There are two capacitances formed in this structure, between the two electrode fingers and the proof mass fingers. The capacitance value between one of the electrodes and the proof mass is given as,

$$C_{1,2} = \frac{N\varepsilon_0 A}{d_1} + \frac{(N-1)\varepsilon_0 A}{d_2} \tag{3.1}$$

where, N is the number of fingers on one side of the accelerometer, ε_0 is the permittivity of the air, A is the area of the overlapping area of one of the proof mass and electrode finger pair, d_1 and d_2 are the smaller and larger gaps in between the proof mass and electrode fingers.



(a)



(b)

Figure 3.1: (a) The structure of the SOG accelerometer designed in METU MEMS VLSI research group. (b) Illustration of the accelerometer dimensions.

The smaller distance between the fingers, d_1 is called the gap and the larger distance d_2 is called the anti-gap, because of the existence of the anti-gap decreases the sensitivity of the sensor. When a displacement in the position of the proof mass occurs, the gap and anti-gap values change, hence the capacitance values can be given as,

$$C_{1,2} = \frac{N\varepsilon_0 A}{d_1 \mp x} + \frac{(N-1)\varepsilon_0 A}{d_2 \pm x} \tag{3.2}$$

where, x is the displacement of the proof mass from the rest position. For small values of displacements, the capacitance variation can be assumed linearly proportional to the displacement x. The linearity under small displacement can be observed by taking the first two terms of Taylor expansion as follows,

$$C_{1,2(x\to 0)} \cong \frac{N\varepsilon_0 A}{d_1} + \frac{(N-1)\varepsilon_0 A}{d_2} + \left[\frac{N\varepsilon_0 A}{{d_1}^2} - \frac{(N-1)\varepsilon_0 A}{{d_2}^2}\right] x \tag{3.3}$$

If we take the derivative of the capacitance with respect to x, the capacitive sensitivity of the sensor is obtained, dependent on the displacement as in Equation (3.4). In this equation, it is observed that the sensitivity is highly dependent on the finger gap spacings. Hence, smaller the finger gap spacings, higher the sensitivity of the accelerometer.

$$\frac{\partial C_{1,2}}{\partial x} = \frac{N\varepsilon_0 A}{(d_1 \mp x)^2} - \frac{(N-1)\varepsilon_0 A}{(d_2 \pm x)^2} \tag{3.4}$$

Another important parameter of the accelerometer sensor is the electrostatic force generated when potential is applied between the fingers. The significance of this parameter comes from the closed loop operation and applied feedback. The electrostatic pulling force generated between two conducting objects is given by,

$$F = \frac{1}{2}\frac{\partial C}{\partial x} V^2 \tag{3.5}$$

Hence, the force generated between the proof mass and the electrodes becomes as in Equation (3.6). The corresponding acceleration caused by the electrostatic force is given in Equation (3.7), in terms of g's.

$$F = \frac{1}{2}\left[\frac{N\varepsilon_0 A}{(d_1 \mp x)^2} + \frac{(N-1)\varepsilon_0 A}{(d_2 \pm x)^2}\right]\left(V_{elc\,1,2} - V_{pfm}\right)^2 \tag{3.6}$$

$$G = \frac{F}{mg} = \frac{1}{2mg}\left[\frac{N\varepsilon_0 A}{(d_1 \mp x)^2} + \frac{(N-1)\varepsilon_0 A}{(d_2 \pm x)^2}\right]\left(V_{elc\,1,2} - V_{pfm}\right)^2 \tag{3.7}$$

3.1.1. Accelerometer Transfer Function

The accelerometer can be modeled as a basic mass spring damper system as shown in Figure 3.2.

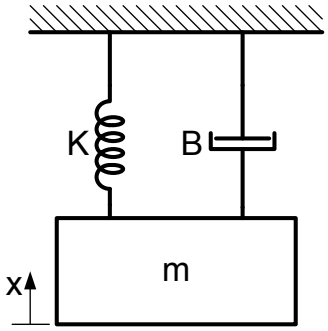


Figure 3.2: Mass-spring-damper system.

For an external acceleration of *a* applied to the sensor, the equations of motion can be shown as in equation (3.8). In this equation *x* is the displacement of the proof mass according to a reference frame placed on the body of the accelerometer, where the electrodes and the anchor points are fixed.

$$F = ma = m\frac{d^2x}{dt^2} + B\frac{dx}{dt} + Kx \tag{3.8}$$

The Laplace transform of the equation gives the Equation (3.9). Hence, the transfer function of the accelerometer is obtained as in Equation (3.10).

$$mA(s) = ms^2X(s) + BsX(s) + KX(s) \tag{3.9}$$

$$H(s) = \frac{X(s)}{A(s)} = \frac{1}{s^2 + s(B/m) + (K/m)} \tag{3.10}$$

The equations (3.11) and (3.12) give the resonance frequency and the quality factor of the accelerometer, respectively.

$$w_0 = \sqrt{\frac{K}{m}} \tag{3.11}$$

$$Q = \frac{w_0 m}{B} \tag{3.12}$$

The magnitude of the accelerometer response is almost constant in the frequency band below the resonance frequency, as shown in Figure 3.3. Hence, the accelerometer is operated in this linear region. Figure 3.3 also shows the dependence of the quality factor on the transfer function. As the quality factor is increased, the peak at the resonance frequency increases, which is the case generally obtained if the mechanical sensor is operated in vacuum environment.

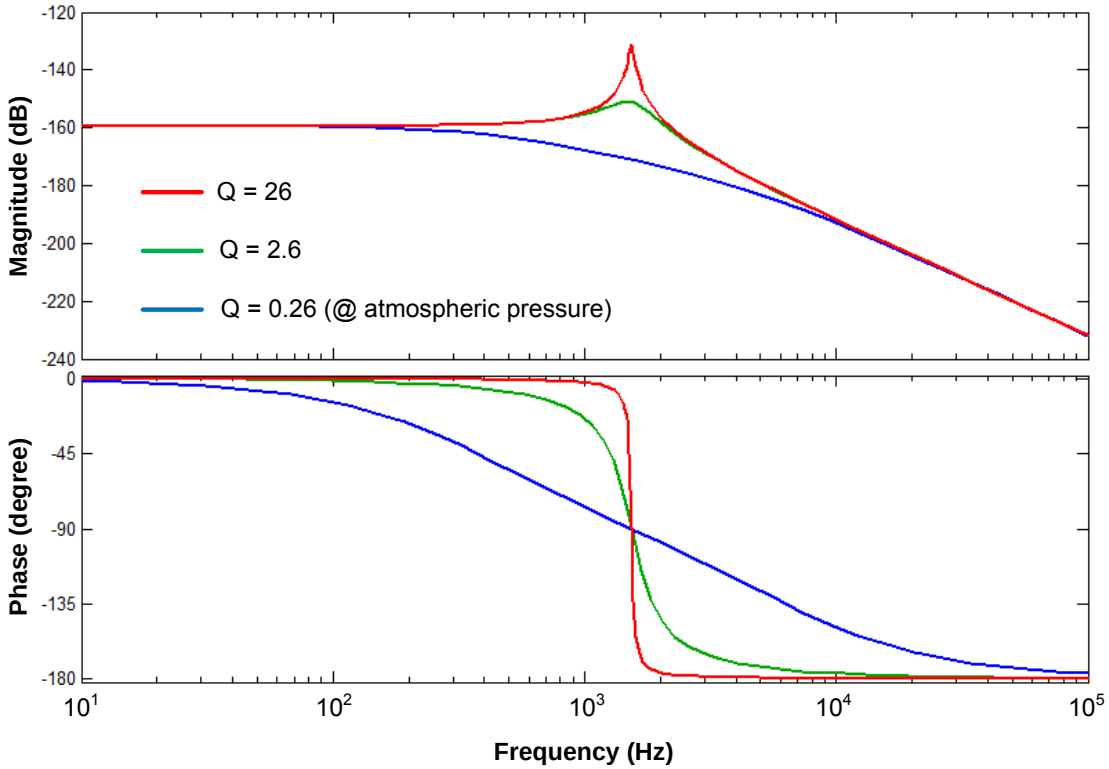


Figure 3.3: Magnitude and phase response of an accelerometer with different quality factors.

In the linear region of the transfer function, at low frequency band, the magnitude of the response is given by Equation (3.13). Hence, the capacitive sensitivity of the accelerometer in open loop is calculated as given in Equation (3.14).

$$H(0) = \frac{\partial x}{\partial g} = \frac{mg}{K} \tag{3.13}$$

$$\frac{\partial C}{\partial g} = \frac{\partial x}{\partial g}\frac{\partial C}{\partial x} = \frac{mg}{K}\left[\frac{N\varepsilon_0 A}{(d_1 \mp x)^2} + \frac{(N-1)\varepsilon_0 A}{(d_2 \pm x)^2}\right] \quad (pF/g) \tag{3.14}$$

3.1.1.1. Spring Constant

The accelerometer sensor uses beam type springs, which differ in size and structure. The beam types used in the accelerometers in this research have the folded beam type structure, as shown in Figure 3.4.

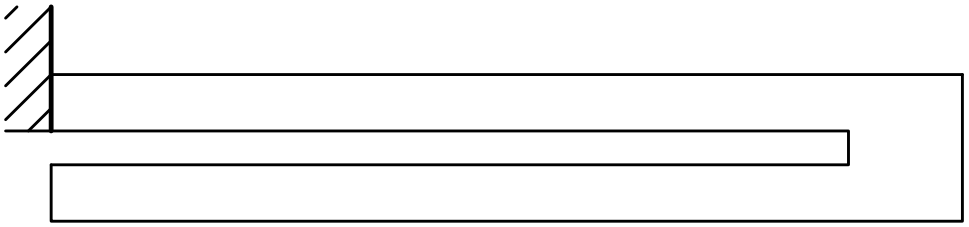


Figure 3.4: Folded beam spring structure.

The spring constant of this beam structure is given as,.

$$K = \frac{1}{2}\left[\frac{Ehw^3}{4l^3}\right] = \frac{Ehw^3}{8l^3} \tag{3.15}$$

where, E is the Young's Modulus, h is the thickness, w is the width, and l is the length of the cantilever beam.

3.1.1.2. Damping

In MEMS devices the two main sources of damping is "Squeeze Film Damping" and "Couette-Flow Damping". Squeeze film damping occurs when two parallel plates move towards each other and compress the fluid molecules in between. Couette-Flow damping results from the movement of two parallel plates in a sliding action. Figure 3.5 illustrates the squeeze film damping and the couette flow damping.

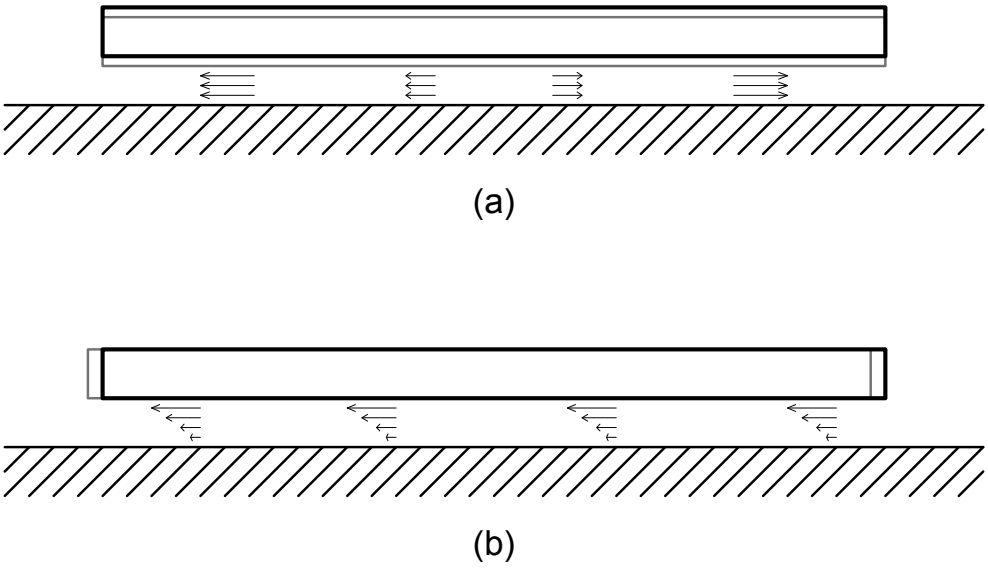


Figure 3.5: Illustration of (a) squeeze film damping, (b) Coutte flow damping.

In the accelerometer structure used in this research, squeeze film damping results from the fingers, where a varying gap structure is used. The movement of fingers does not cause Couette flow damping, however, sliding of the proof mass over the substrate results in a Couette flow damping. Nevertheless, the Coutte flow damping has an ignorable effect when compared with the squeeze film damping, in this structure. Therefore, the total damping constant of the accelerometer can be expressed by only squeeze film damping as given in equation (3.16) [37]

$$B_{squeeze} = c\mu_{eff}\frac{W^3L}{d^3} = c\mu_{eff}W^3L\left[\frac{2N}{d_1^3} + \frac{2(N-1)}{d_2^3}\right] \tag{3.16}$$

where, μ_{eff} is the effective viscosity of the environment, W is the width, L is the length of the rectangular plates, d is the distance between two rectangular plates, d_1 and d_2 are the gap and the anti-gap spacings of the fingers, and c is a factor, which depends on the W/L ratio of the rectangular plates. The dependence of the factor c on the W/L ratio is given in the graph shown in Figure 3.6 [37].

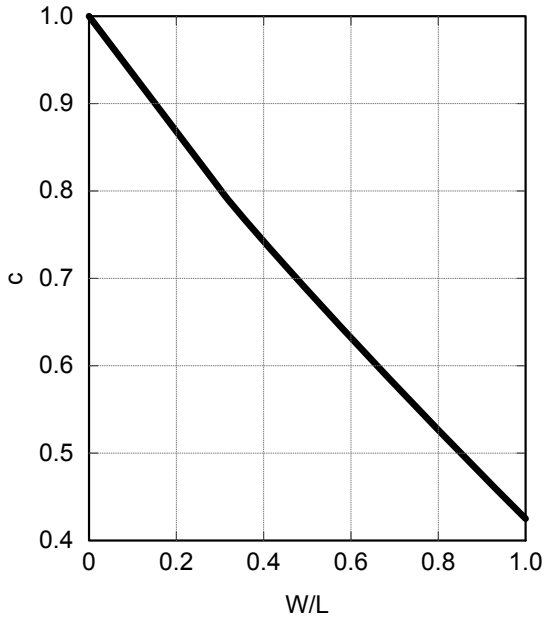


Figure 3.6: The dependence of coefficient c on the dimensions of the plates.

3.1.2. Cadence Modeling of Accelerometer Sensor

In order to observe and simulate the full accelerometer system, both the mechanical sensor and the interface electronics should be modeled in the same environment. One of the ways to implement the model is using the Cadence environment, where the electronic circuitry already exists. In this case, the mechanical structure should be modeled by electrical parameters. Another way is modeling both the interface electronics and the mechanical structure in a seperate environment, such as Matlab.

To obtain an accurate model and simulation results, the accelerometer sensor is modeled in Cadence environment. In this fashion, the overall system could be simulated in the same environment.

The block diagram of the accelerometer model is given in Figure 3.7. The blocks are generated using VerilogA language, except the transfer function block of the

accelerometer. The transfer function is constructed using a second order RLC circuit.

The model is mainly composed of two variable capacitors, the transfer function of the mechanical sensor and the blocks to convert the variables, using the defined equations.

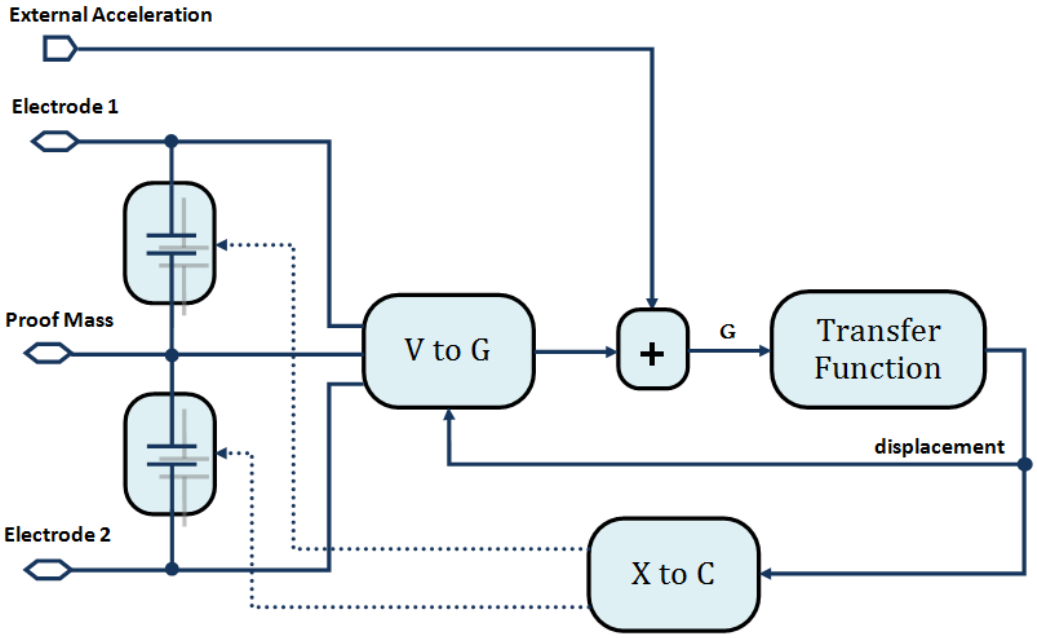


Figure 3.7: Block diagram of the model constructed in Cadence environment.

There are two variable capacitors having values dependent on the accelerometer dimensions and structure, and the instantaneous value of the displacement of the proof mass. The variable capacitors are the interface between the mechanical structure and the electrical circuitry. Variable capacitors are generated using VerilogA language, in which the capacitance value is set by an input value. The capacitance value is calculated in "*X_to_C*" block by using the formula given in Equation (3.2).

The displacement *x* is obtained as an output from the transfer function of the accelerometer. The transfer function block takes total acceleration value as an input,

which is the sum of external acceleration and the acceleration caused by the electrostatic feedback. For obtaining the second order transfer function of the accelerometer, an RLC circuit is constructed. The RLC circuitry for obtaining the transfer function is given in Figure 3.8.

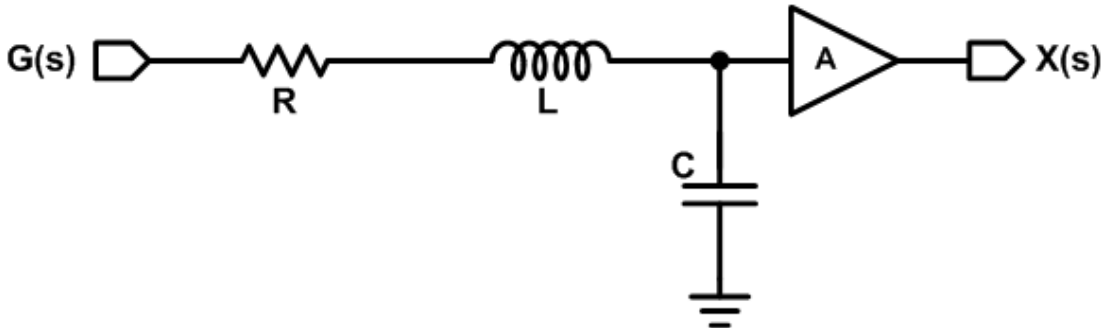


Figure 3.8: RLC circuit constructed for modeling the transfer function of the accelerometer.

For both the input and output of the transfer function block, voltage values are used to represent the acceleration and the displacement. There is also a gain block to set the magnitude of the transfer function properly. For finding the component values, the transfer function of the RLC circuit should be equated to the transfer function of the accelerometer, which is given in Equation (3.17), where acceleration is in terms of g's.

$$\frac{X(s)}{G(s)} = \frac{g}{s^2 + s(B/m) + (K/m)} = \frac{A}{s^2(LC) + s(RC) + 1} \tag{3.17}$$

From this equation, solving for the R, L and C values gives infinite number of solutions. Hence, to obtain a solution, value of R is selected to be 1 Ω. Then, the other parameters can be found as in the Equations (3.18), (3.19) and (3.20), given below.

$$A = \frac{m \cdot g}{K} \tag{3.18}$$

$$C = \frac{B}{K} \tag{3.19}$$

$$L = \frac{m}{B} \tag{3.20}$$

The acceleration value, which is applied to the transfer function block, has two sources. One of the sources is the externally applied acceleration, and the other acceleration source results from the electrostatic force generated from the applied voltages to the accelerometer electrodes and the proof mass. These two sources of acceleration is directly added and given to the transfer function as an input. The external acceleration value is directly an input, where a voltage signal, having the value of acceleration in terms of g's, is applied while performing the simulations. The acceleration created because of the electrostatic force is calculated by the "*V_to_G*" block, using the electrostatic force formula given in Equation (3.7). The net acceleration generated is calculated by taking the difference of accelerations generated on each side of the accelerometer, i.e. $G_1 - G_2$.

The accelerometer model generated in Cadence environment is used with the designed readout circuit, and the simulations are performed. The simulations performed in Cadence environment give accurate results, since the readout circuit is already designed in the same environment. However, the simulation times are so long that complete results cannot be observed. Therefore, for examining the operation and stability of the system, Matlab Simulink models are used, which is discussed in the following section.

3.2. Complete System Modeling in Matlab Simulink

The model of the accelerometer combined with the model of the readout circuit is constructed in Matlab Simulink environment. The block diagram of the model is given in Figure 3.9.

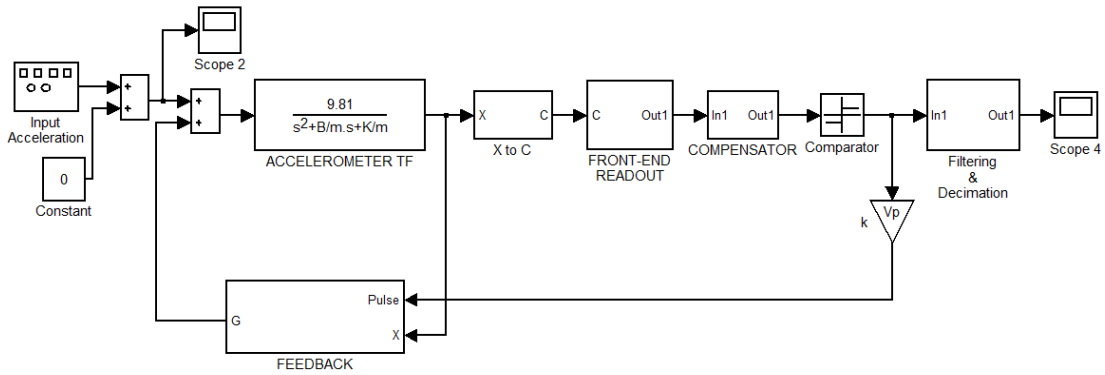


Figure 3.9: Simulink model of the complete electromechanical closed loop system.

In this model, 3 blocks, which are accelerometer transfer function, displacement to capacitance converter "X to C", and the feedback block, represents the accelerometer. The accelerometer transfer function is modeled with a transfer function block in s-domain, as given in Equation (3.10). The acceleration entered into this block is composed of external acceleration and the feedback acceleration. Feedback acceleration is generated by the applied feedback voltage to the electrodes and the proof mass. The internal blocks of the feedback block is shown in Figure 3.10.

The feedback acceleration is generated only when the readout circuit is in feedback phase, timings of which are set by the pulse generator. The direction of the feedback acceleration is defined by the output of the comparator. The magnitude of the force is calculated according to the Equation (3.6), and the net force is then converted to acceleration.

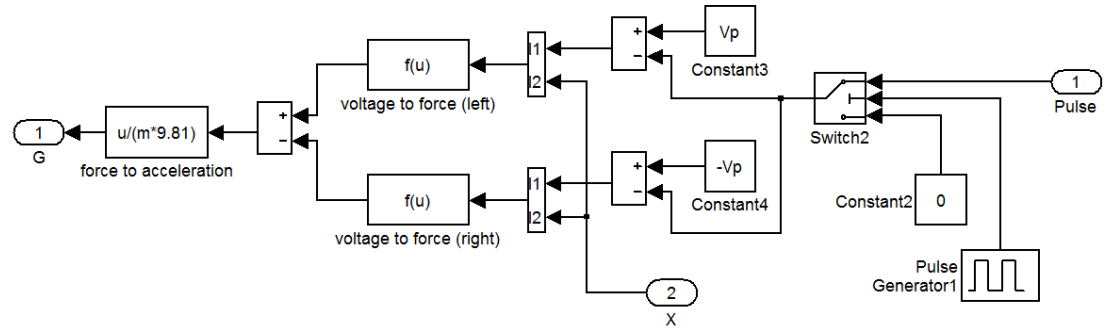


Figure 3.10: Block diagram of the feedback block.

The output of the transfer function gives the displacement as the output, and the displacement should be converted to capacitance value in order to be useful for the readout circuit. The "X to C" block calculates the capacitance on each side of the accelerometer using the displacement value, and gives the capacitance difference at the output. The capacitive difference value is then used in the front-end readout block, to be converted into voltage values in the readout circuit. The model of the front-end readout circuit is given in Figure 3.11. The front-end readout circuit consists of a charge integrator, which is modeled by a gain block. The gain block converts the capacitive difference into the voltage value as given in Equation (3.21).

$$V_{OUT} = \frac{V_{DD}(C_{S1} - C_{S2})}{C_{int}} \tag{3.21}$$

where C_{int} is the integration capacitance value used in the charge integrator block and C_{s1}, C_{s2} are the values of accelerometer capacitances. The saturation of the readout circuit at the supply voltages is also included in the model using a saturation block. The charge integrator block samples the capacitance difference, by transferring the excess charge generated on the sensor capacitances, to the integration capacitances. This operation is performed once in a sampling period. This is modeled in Simulink using a sample and hold block, with proper timings.

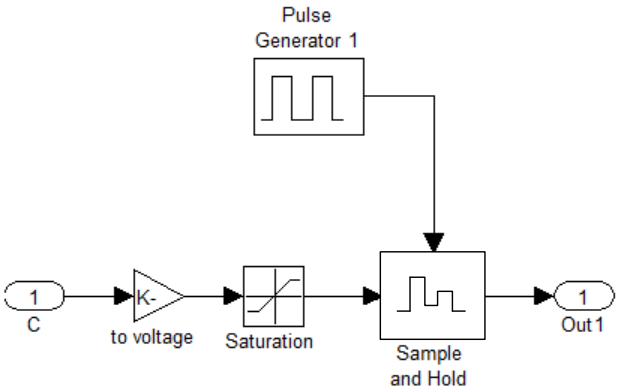


Figure 3.11: Front-end readout circuit modeling.

A compensator block is constructed, the block diagram of which is given in Figure 3.12. The compensator block maintains the stability of the sigma-delta system, by adding a zero to the loop, and carrying the oscillation of the mass to higher frequencies. The block holds the previous output value, and subtracts a ratio of previous data from the current output data. The performed operation is expressed in z-domain as given in Equation (3.22). A detailed discussion on the compensator and stability is given in the following section.

$$H(z)_{comp} = A - Bz^{-1} \tag{3.22}$$

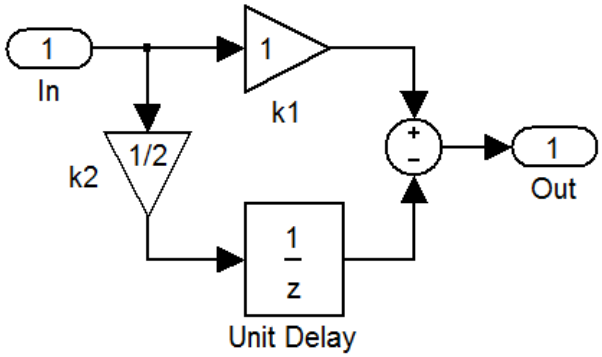


Figure 3.12: Block diagram of the compensator.

After the lead compensator stage, the output value is compared with zero, with the usage of a comparator. The output of the comparator has two levels, either "+1" or "–1". Hence, an output bit-stream is generated at the output of the readout circuit. This bit-stream is supplied back to the feedback block, and the loop is closed.

The output bit-stream carries the acceleration information including a great amount of quantization noise. The quantization noise is at the high frequency, while the acceleration information is in the low frequency band. Therefore, for observing a meaningful output, the bit-stream should be low-pass filtered, using the digital low pass filtration blocks of Matlab Simulink. The low-pass filter should be a sharp filter to eliminate the quantization noise; hence, it will have a complex structure

with very high order. However, using a complex filter structure increases the simulation time incredibly. For decreasing the simulation time, three stages of filtering stages are cascaded, while decimating the signal at each stage, as shown in

Figure **3.13**. In this way, the number of data is reduced at each stage, and much simpler low-pass filter blocks are used.

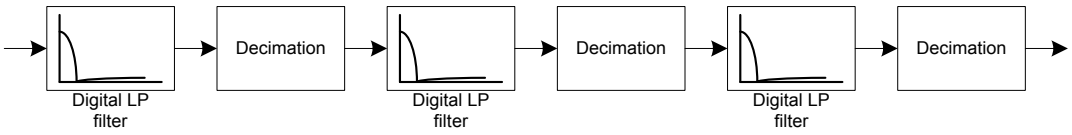


Figure 3.13: Filtering and decimation blocks.

3.3. Closed Loop Response and Stability Analysis

When an accelerometer system is operated in open loop, the bandwidth of the system is defined by the bandwidth of the accelerometer and the measurement range is limited by the finger spacings. According to the Equation (3.14), for increasing the open-loop sensitivity of the accelerometer, it should be designed to have large mass, low spring constant and high capacitance values. All these parameters have effects on decreasing the bandwidth and the range of the system. Moreover, the change of capacitance with respect to the displacement can be assumed to be linear if and only if the displacement value is much smaller than the finger gap spacings. Hence, usage of an open-loop accelerometer results in high amounts of non-linearity of capacitance with respect to the external acceleration.

By using the accelerometer with a closed loop circuitry, the position of the accelerometer is held around the rest position. The output of the system becomes the value of applied feedback force to hold the proof mass position constant. Hence, the output of the system is directly proportional to the applied acceleration, and non-linearity is not observed. In closed loop mode, the range of the accelerometer is not

anymore limited with the finger gap spacings, but the maximum applicable feedback acceleration on the proof mass. For an accelerometer having a low spring constant, closed loop mode results in higher measurement range. Furthermore, in the closed loop system, the bandwidth is not anymore dependent on the accelerometer transfer function. The closed loop bandwidth depends on the closed loop parameters and hence the bandwidth of the system increases in a considerable amount.

The theoretical calculation of the bandwidth of a sigma-delta closed system is not an easy process, and it can vary according to the applied external acceleration. For considering the bandwidth of the system, Figure 3.14 should be considered where a basic block diagram of the sigma-delta loop is given.

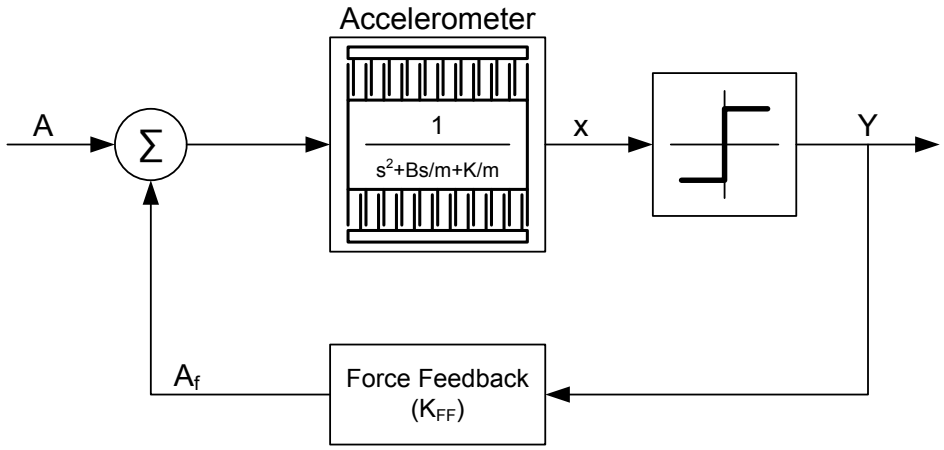


Figure 3.14: Block diagram of the sigma – delta loop.

In this figure, the comparator block is a non-linear element, which gives an output with two levels. The average of the comparator output pulses will converge to the external acceleration value, however the displacement of the proof mass is held in a small value. Hence, this results in a high gain value at the comparator stage. The total gain β from displacement x to feedback acceleration A_f, can be several orders of magnitude larger than (K/m). Hence according to the Equation (3.23), the resonance frequency of the closed response is carried to a high frequency value with

the addition of β. Then, the total closed loop transfer function can have a bandwidth several orders larger than the open loop bandwidth of the accelerometer.

$$\frac{Y(s)}{A(s)} = \left(\frac{1}{K_{FF}}\right)\frac{1}{s^2 + (B/m)s + K/m + \beta} \tag{3.23}$$

where K_{FF} is the factor of conversion of electrostatic voltage to feedback acceleration, and β is a nonlinear function resulting from the comparator and the feedback stages. In the above analysis of the bandwidth of the closed loop system, the delay resulted from the readout circuit is assumed to be zero, which is not the actual case. For calculating the delay caused by the readout circuit, the time between the capacitance readout to the midpoint of feedback time should be considered. Using this delay time, t_d, the phase response of the readout can be given as in Equation (3.24) .

$$\theta_{readout} = -180 \cdot t_d \cdot f \tag{3.24}$$

The accurate way of determining the bandwidth of the closed loop system is observing the output magnitude of the system by sweeping the applied acceleration frequency. A sample result is obtained with a readout circuit of 2μs sampling period and 1.2μs readout delay. For obtaining the frequency response of the closed loop system, accelerations at 1g amplitude at various frequencies are applied to the system and the results are as shown in Figure 3.15. The magnitude of the output at the input frequency is observed with proper filtering, and hence the frequency response is obtained. The result shows that the magnitude of the frequency response is kept constant up to a frequency much higher than the resonance frequency of the accelerometer. Increasing the input frequency results in increasing the contributed

quantization noise to the signal, hence the response becomes distorted at higher frequencies.

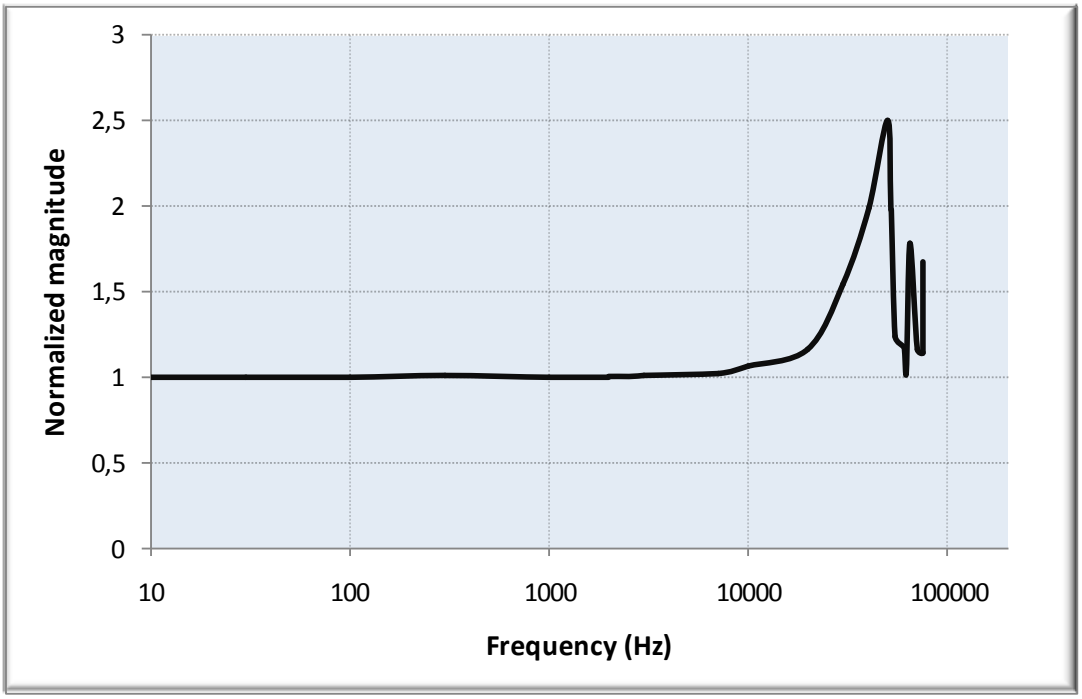


Figure 3.15: Closed loop frequency response of the electromechanical system.

The closed loop system aims to hold the proof mass by applying a pulse stream of feedback force, which creates an oscillation on the proof mass position. The generated oscillation is randomized by the changing value of the input, and hence, creates an undeterminable motion of the proof mass. This motion is called Mass Residual Motion.

For analyzing the closed loop operation and mass residual motion, one should consider the oscillation conditions. There are two conditions for oscillation in a closed loop feedback system. The Figure 3.16 shows the block diagram of the basic feedback circuitry. The first condition of oscillation is the magnitude condition, where the magnitude of the loop gain $H(jw).K$ should be set to unity. The second condition is the phase condition, where the total phase of the closed loop system must be set to 360 degrees.

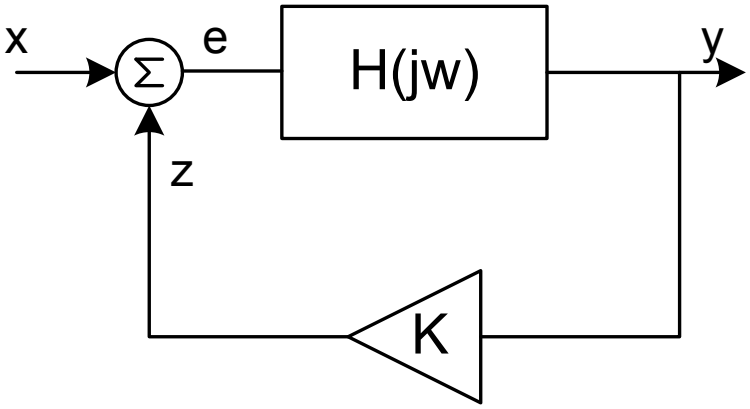


Figure 3.16: Block diagram of a basic feedback system.

For the analysis of oscillation, the input acceleration is assumed zero, and proof mass oscillation is considered. In the sigma-delta closed loop system, a single bit feedback is applied as feedback to the accelerometer. The applied feedback has two levels, without regarding the amplitude of the displacement of the proof mass. This creates an infinite gain element, which has non-linearity due to the saturation. Independent of the amplitude of the displacement of the proof mass, the feedback force to be applied will remain the same. Hence, in this case, the amplitude condition settles to the desired value of unity automatically.

Since the amplitude condition is already satisfied by the system, the main concern for oscillation is the phase of the system. 180 degrees of phase difference results from the negative feedback. Hence, the condition that should be satisfied can be given as in Equation (3.25). There are three sources of phase difference, which are the accelerometer itself, the phase of the readout circuit and the lead compensator circuitry. The lead compensator is used for adding a zero to the system and hence carrying the proof mass oscillation frequency to a higher value. As the mass residual motion is carried to higher frequencies, the amplitude of the oscillation decreases and the contribution of this motion into the signal band are reduced.

$$\theta_{total} = -180° + \theta_{sensor} + \theta_{readout} + \theta_{compensator} = -360° \quad (3.25)$$

From the transfer function of the accelerometer, the phase of the mechanical sensor can be extracted as given in Equation (3.26). The most part of the phase is caused by the accelerometer, which converges to 180 degrees at high frequencies.

$$\angle H(jw) = \angle\left[\frac{1}{(jw)^2 + \frac{B}{m}jw + \frac{K}{m}}\right] = -\frac{360}{2\pi}tan^{-1}\left(\frac{\frac{B}{m}w}{\frac{K}{m} - w^2}\right) \quad (3.26)$$

As discussed previously, the readout phase delay is given by the time between the sampling of the displacement value through the measurement of capacitances, and the midpoint of the feedback time. Hence, the readout phase was given as in Equation (3.24). The phase of the readout circuit starts to become considerable at much higher frequencies.

The lead compensator is an important block for the stability of the system and decreasing the mass residual motion. It has a structure, which can be shown in z-domain as given in Equation (3.22). The phase of the lead compensator is expressed as shown in Equation (3.27). The parameters A and B should be defined according to the needs of the closed loop system. If the oscillation frequency is assumed much larger than the accelerometer resonance frequency, the phase lag of the accelerometer can be assumed 180 degrees. Hence, to obtain 180 degrees in total, the sum of the phases of readout circuit and lead compensator should be equal to zero, i.e. the phase lag of the readout circuit should be equal to the phase lead value of the compensator.

$$\theta_{comp} = \frac{360}{2\pi} \cdot tan^{-1}\left[\frac{B \cdot sin\left(\frac{2\pi f}{f_s}\right)}{A - B \cdot cos\left(\frac{2\pi f}{f_s}\right)}\right] \tag{3.27}$$

There is an achievable limit of oscillation frequency, which is the quarter of the sampling frequency. This maximum oscillation frequency results from the second order nature of the accelerometer. For a basic second order system, having zero damping and spring constant, used in the sigma delta structure, the signals are illustrated in Figure 3.17.

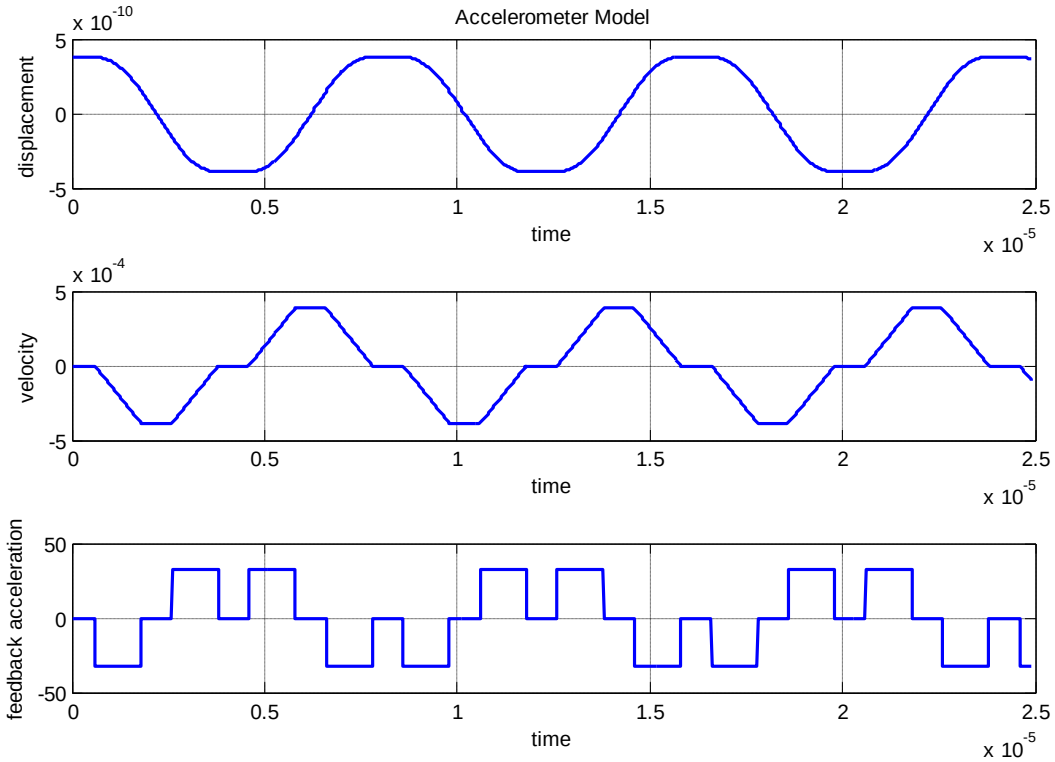


Figure 3.17: Basic illustration of displacement, velocity and feedback acceleration for a sigma delta loop.

By analyzing the signal waveforms, it can be said that the minimum period of the oscillation is four times the sampling period. This fact can be explained by examining the waveforms. Initially, assume that the displacement of the proof mass is slightly above zero position. A feedback force will be applied on the opposite direction, and give acceleration to the proof mass. The applied acceleration will cause the velocity of the proof mass to increase, and stay constant after the acceleration. The next feedback pulse should be in the opposite direction with the previous one, because of the proof mass is moved to one side with the effect of the previous feedback pulse. The second feedback pulse will only make the velocity of the proof mass zero, but cannot make it start to move on the opposite direction. Hence, third feedback pulse will be in the same direction with the second one, and will move the proof mass to zero position. The next two feedback pulses will be on the opposite direction. Hence, the cycle repeats in four feedback pulses. This results in a maximum oscillation frequency of quarter of the sampling frequency.

The phase responses of the accelerometer and readout blocks are given in Figure 3.18. In the given graphs, the readout circuit is taken to have 500 kHz sampling frequency and 1.2 μsec readout to feedback delay and some compensator responses are shown with different coefficients.

The total phase of the system without the compensator is given in Figure 3.19. In this configuration, the oscillation settles at the frequency around 32 kHz, which results to have high amplitude of displacement. With the usage of a lead compensator with the proper coefficients, the phase response of the closed loop system becomes as shown in Figure 3.19. Hence, in this case, the frequency of oscillation increases up to $f_s/4$.

The main concern about the mass residual motion is its contribution on the noise in the signal band. The calculation of the noise due to mass residual motion is given in the next chapter.

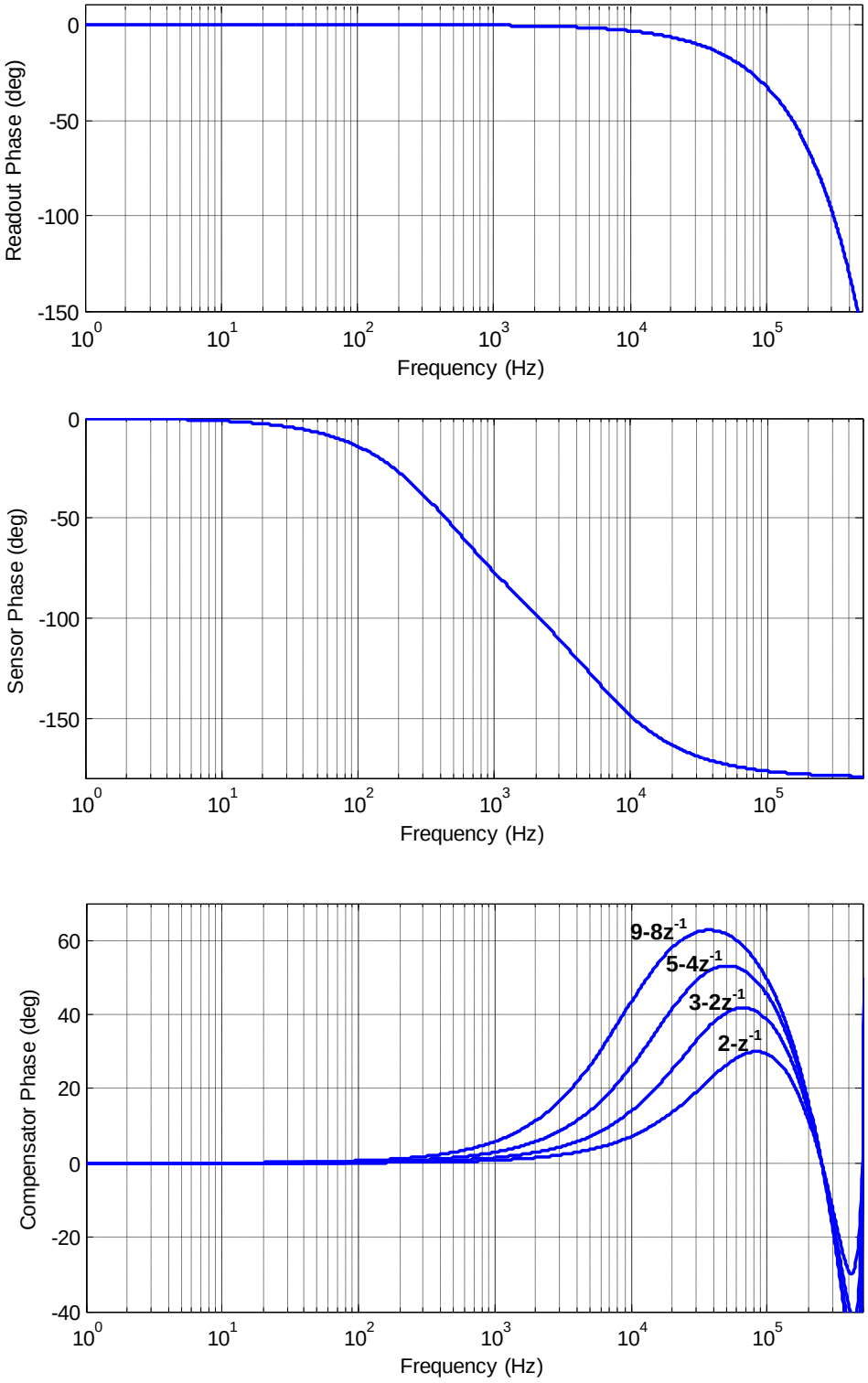
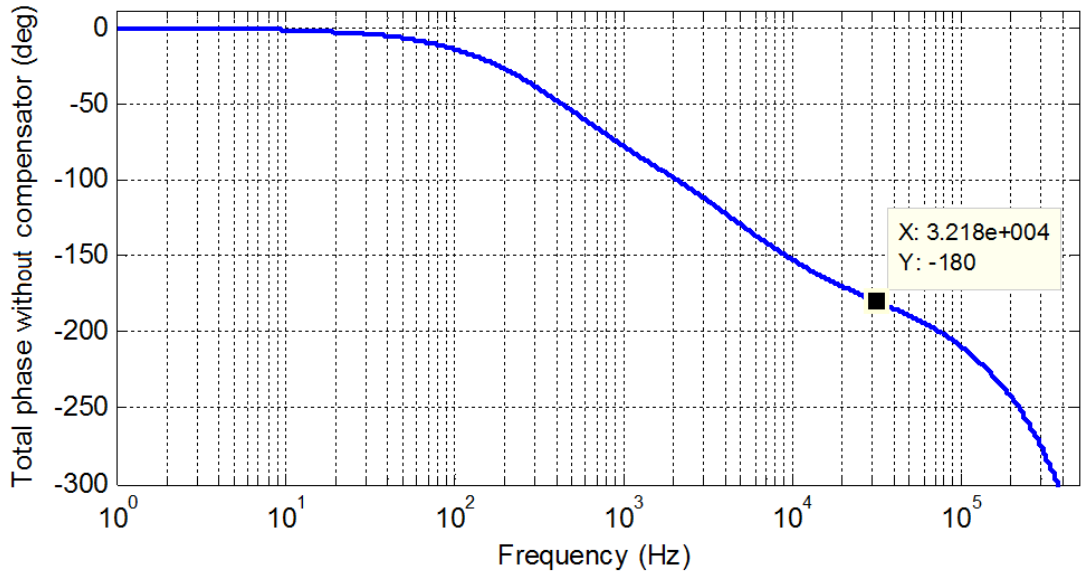
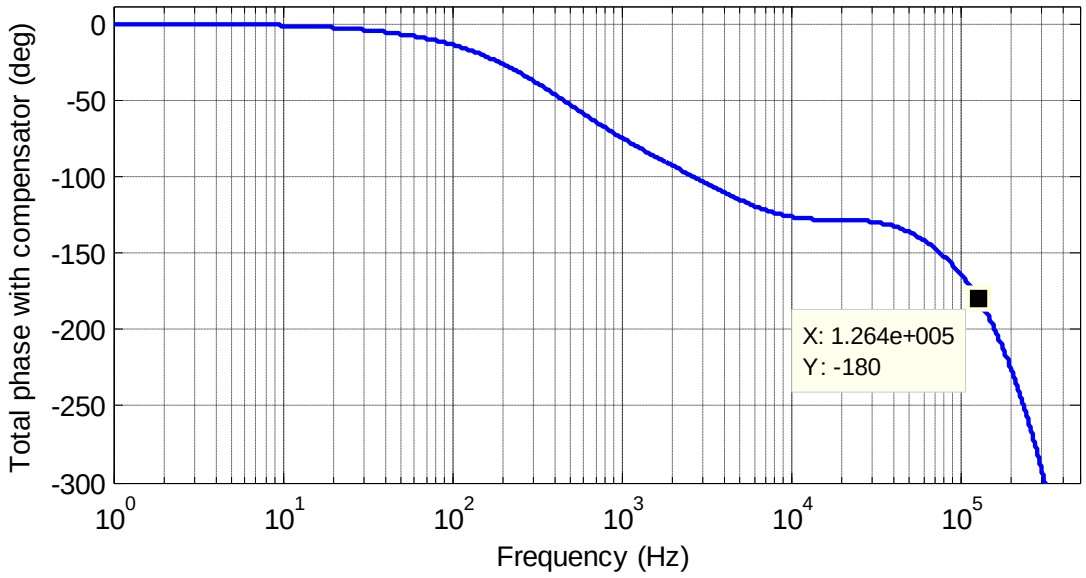


Figure 3.18: The phase responses of the blocks in the closed loop system.



(a)



(b)

Figure 3.19: Total phase of the of the system (a) without the lead compensator (b) with the lead compensator.

3.4. Conclusion

This chapter gave the model of the accelerometer and the readout circuit constructed in Cadence and Matlab environments. Then, closed loop stability analysis of the system is given, and the necessity of the lead compensator structure is explained. Using these models and analysis a readout circuit is designed, which is described in next chapter. The next chapter also gives the performance limitations of the system according to the designed readout circuit.

CHAPTER 4

READOUT CIRCUIT DESIGN

The displacements of an accelerometer sensor are commonly in the order of an angstrom, and the capacitive differences are below atto-farads. In order to detect such small capacitive differences, a high-resolution readout circuit is required. The most effective solution for non-monolithic capacitive accelerometers is the use of a switched capacitor sigma-delta type readout circuit, to achieve high resolution and high linearity with digital output. The aim is to design a closed loop, low noise readout circuit, with low power consumption. Since the accelerometers used in this study have capacitive sensitivities around 1 pF/g, to achieve micro-g resolution, the readout circuit should be capable of detecting below 1 atto-farad capacitive differences. Thus, an electro-mechanical sigma-delta readout circuit is designed and implemented. In later study, another regular sigma-delta structure is designed and implemented with minor improvements and addition of a compensator circuit in the first design. This second design achieved significant results in terms of noise performance, together with the sensor, both in open loop and closed loop mode. With the gathered knowledge and experience on sigma-delta readout circuits, two new readout circuits employing adaptive sigma-delta techniques are designed, to improve the performance of the accelerometer systems, further. The design of the adaptive readout circuits will be discussed in the next chapter. This section describes the second regular sigma-delta readout circuit design.

In Section 4.1, the general structure and operation of the readout circuit is explained. Section 4.2 describes internal blocks of the readout circuit, supplying the circuit schematics and simulation results. Section 4.3 gives the overall simulation results of the readout circuit with the accelerometer models in Cadence and Matlab environments. Section 4.4 gives information on layout considerations, and in

Section 4.5 performance limitations of the readout circuit and the accelerometer system is described. Finally a conclusion is made in Section 4.6.

4.1. Structure of the Readout Circuit

The complete block diagram of the sigma-delta readout circuit is given in Figure 3.2. The mechanical sensor is included in the sigma-delta loop and hence the overall system constitutes an electromechanical structure. Besides using readout circuit in the closed loop, it can also be operated in open loop mode. In open loop mode, in one sampling period, the readout circuit measures the capacitance difference of the accelerometer and gives a differential analog output voltage and no feedback force is applied to the sensor. In closed loop mode, there are two phases in a sampling period, which are sense and feedback phases. The capacitive difference is sensed in the sense phase, and an analog voltage is formed. Then, the differential analog voltage is quantized in two levels using a comparator, and according to the result, an electrostatic feedback force is applied to the proof mass, in the feedback phase of the sampling period.

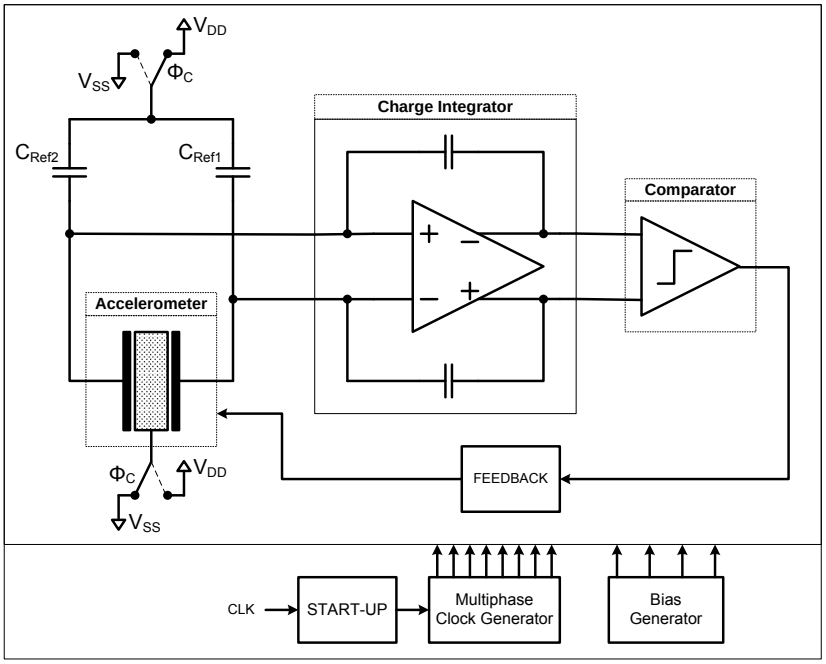


Figure 4.1: Block diagram of the fully differential sigma-delta readout circuit.

Oversampling ratio of a sigma-delta system should be high to achieve high resolution. Therefore, the components of the readout circuit should be designed to operate at the highest possible frequency. Designed readout circuit operates at 500 kHz sampling frequency, using its on-chip clock generator circuitry, which can be increased up to 700 kHz by applying an external clock source. Hence, the speeds of the components are designed to be able to operate with this frequency. Using this clock source, multiphase clocks are generated for operating various parts of the circuit and the switch timings.

The readout circuit has a fully differential structure for reducing the effects of common mode noise sources, such as the power supply noise. The initial stage of the readout circuit is a charge integrator circuitry, including a switch capacitor network. The switch capacitor network, together with the charge integrator, provides the measurement of the sensor capacitor values by charge transferring. The capacitive difference on the accelerometer is converted to differential analog voltage at the charge integrator stage, which uses an Operational Trans-conductance Amplifier (OTA) for performing the operation. In this stage, correlated double sampling (CDS) technique is also employed, for reducing the low frequency noise and offset at the input stage of the charge integrator.

The differential voltage at the output of the charge integrator is then supplied to the compensator stage, which is needed for the stable operation in closed loop mode. After the compensator, a latching comparator is used for deciding on the sign of the differential signal. The output of the comparator is used as the closed loop output of the readout circuit. It is also used for applying feedback voltages between the accelerometer electrodes and proof mass.

The readout circuit also includes a start-up circuitry, which is used to bring the proof mass of the sensor to the rest position in the case of large deflections at start-up.

4.2. Description of the Main Blocks of the Readout Circuit

This section describes the readout circuit blocks including the simulation results. There are mainly four blocks of the readout circuit, first of which is the charge integrator block. The OTA used in the charge integrator block is one of the most critical components, which enormously affects the performance parameters of the readout circuit. The lead compensator used following the charge integrator block satisfies the stability of sigma delta loop, and decreases the mass residual motion by adding a zero to the system and carrying mass residual motion frequency to a higher value. Another critical component is the comparator block, which must operate precisely, and at a high rate.

4.2.1. Switched – Capacitor Network

The switched capacitor circuitry shown in Figure 4.5 is used in order to perform both readout and feedback, in different time intervals. This circuitry also employs correlated double sampling (CDS) to decrease the low frequency noises of the circuit.

There are two kinds of switch structures used in the switched capacitor network. The first kind of switch is the complementary CMOS switch as shown in Figure 4.2. This kind of switch is used in stationary switches, which are not switched during the operation of the readout circuit. Because of these switches are not operational during the circuit operation, there is no charge injection problem. However, the problem to be considered is the resistances and parasitic capacitances of the switches. At high current passing nodes of the readout circuit, the W/L ratios of the transistors are designed large, so that the resistance of the switch is kept low. However increasing the gate area of the transistors increases the parasitic capacitances. Hence, the switch transistors have the minimum length, with large widths. The W/L ratios of switches change depending on the connected node and the current passing through the switches. The resistance of a switch depending on its W/L ratio is given in Figure **4.3**.

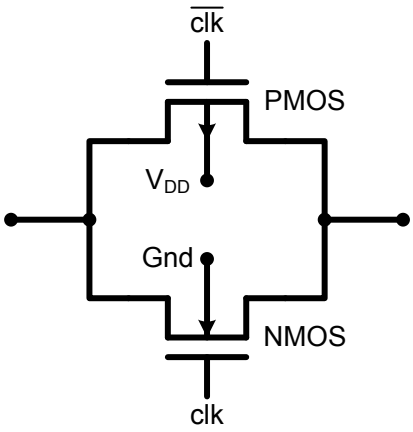


Figure 4.2. Complementary CMOS switch.

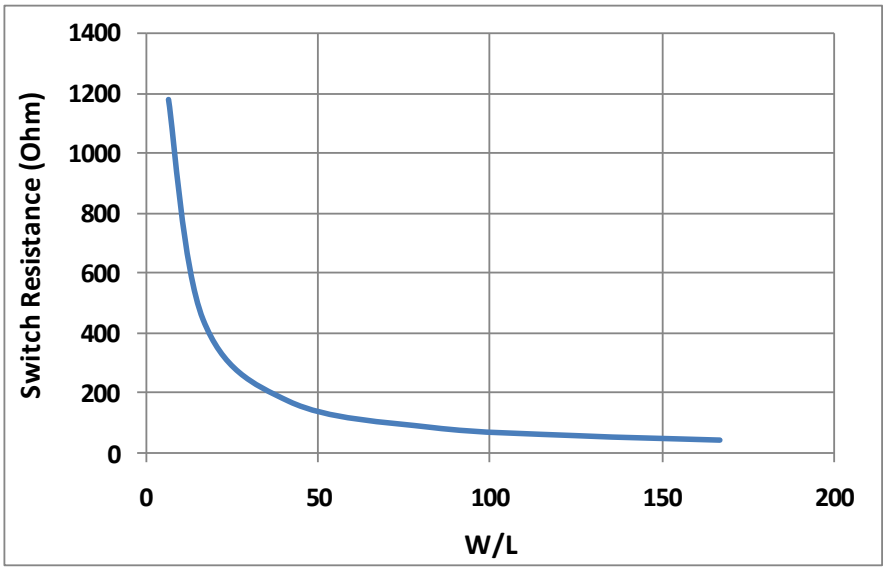


Figure 4.3. Switch resistance versus W/L ratios of the transistors.

The second type of switch is the complementary switch with dummy switches, as shown in Figure 4.4. This switch is used for the switch structures, which are functional during the readout circuit operation. To overcome the charge injection and charge feed through problems, dummy switches are used. The dummy switches M3 – M6 have the half size of the switch transistors M1 and M2. By applying the inverse of the control signals to the dummy switches, the injected charges are collected on the dummy transistors.

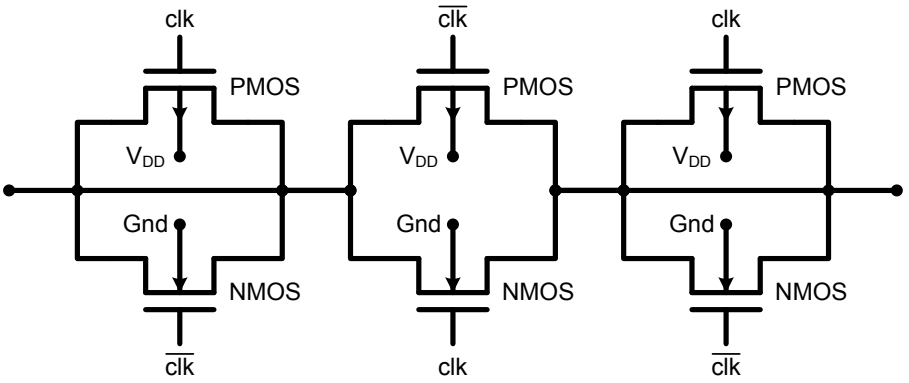


Figure 4.4. Complementary CMOS switch with dummy transistors.

4.2.1.1. Readout and Feedback Switching Timings

The switch capacitor network is shown in Figure 4.5. For understanding the operation of switching and charge transfers, first assume that the Correlated Double Sampling (CDS) technique is not applied, which means "pcds" and "pcdsn" switches are short-circuited and "phcd" switch is kept off. The timings of the signals applied to the switches are shown in Figure 4.6.

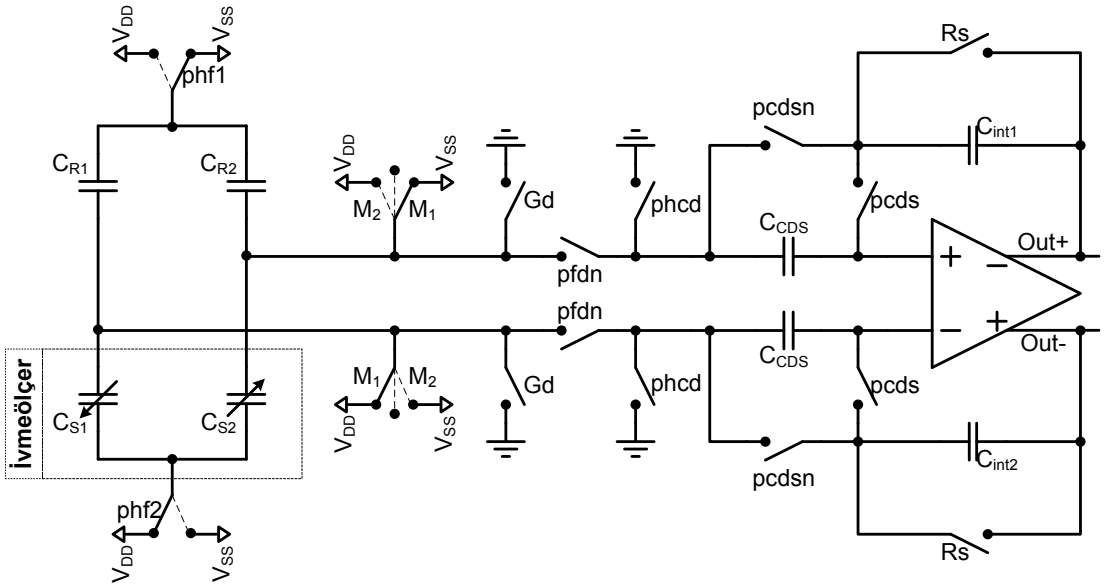


Figure 4.5: Schematic view of the switched capacitor network and the charge integrator stages.

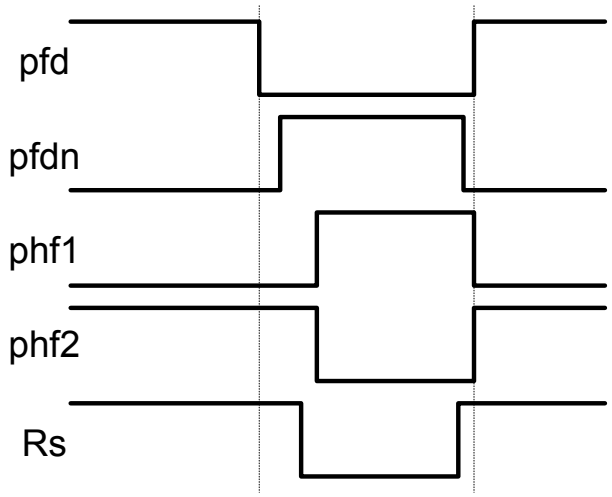


Figure 4.6. Timing diagram of the signals used in the readout circuit.

The readout operation has two main phases of operation, readout and feedback phases. In the readout phase, the charge due to the sensor capacitance difference is transferred to the charge integrator and a proportional output voltage is generated. Then, after the comparator block settles to a valid output, the circuit enters to feedback phase. In the feedback phase, the sensor is disconnected from the charge integrator and an electrostatic voltage is applied to the sensor electrodes.

At the beginning of the readout phase, *"Rs"*, *"pfdn"* and *"Gd"* switches are on. Hence, the integration capacitors, C_{int}, are reset and the input and output nodes of the OTA are set to mid-point voltage. After switching *"Rs"* and *"Gd"* off, the voltages at the top and bottom nodes of the full bridge capacitor structure switches from high to low and low to high, respectively. At this instant, charge transfer to the integration capacitors takes place. Hence, at the charge integrator stage, the differential output voltage related with the full bridge capacitance difference is generated. After this generated voltage being stable and read by the comparator, the circuit enters to feedback phase. When the circuit is in feedback phase, the connection between the readout blocks and the sensor is cutoff by switching *"pfdn"* switch off. Before starting to apply the feedback force, the top and bottom nodes of the full bridge structure switch their states, and stay constant during the feedback phase. Then, feedback voltage is applied at the electrodes of the sensor. During the

feedback, the proof mass voltage is held at 0 V. According to the last generated output of the comparator, 5 V is applied to one of the electrodes of the sensor, which creates a pulling force from one of the electrodes of the accelerometer. At the end of the feedback phase, *"Gd"* switch is turned on, so the electrode nodes are pulled to mid-point voltage. Then, the readout phase starts again by turning *"pfdn"* switch on.

4.2.1.2. Correlated Double Sampling

CDS technique is a useful technique for decreasing the low frequency noises and the offset created at the input node of the OTA. The switching timings for CDS operation are given in Figure 4.7. While the circuit is in feedback phase and the integration capacitors are reset, the output voltage of OTA is sampled on the CDS capacitors. The sampled voltage includes any noise and offset created by the amplifier. When the readout is performed, the CDS capacitors are connected series to the input of the OTA, hence the sampled offset and noise is subtracted from the signal in the readout phase. Hence, the sampled low frequency noise and the offset are reduced. Although the addition of CDS switches and capacitors contributes to a little amount of noise on the readout circuit, the CDS technique improves overall noise performance of the readout circuit.

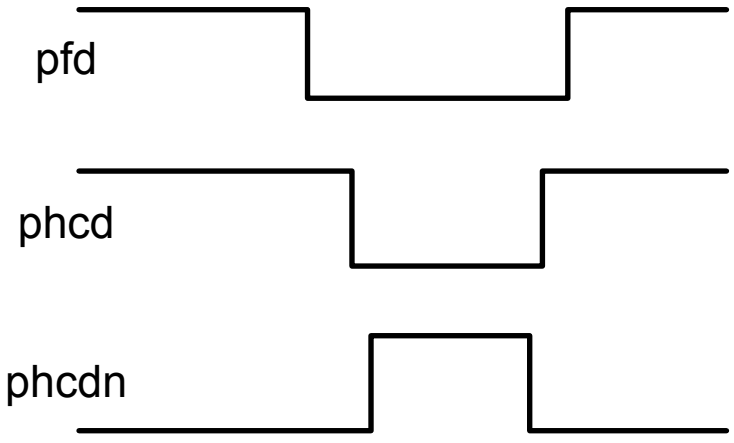


Figure 4.7. Complementary CMOS switch with dummy transistors.

4.2.2. Charge Integrator Operation

The charge integrator circuit constitutes the first stage of the readout circuit. In this part, only the operation of the charge integrator is discussed with the basic configuration as given in Figure 4.8. The switched capacitor network, placed before the charge integrator stage, will be discussed in the following section.

Figure 4.8 shows the full bridge capacitor structure with the fully differential charge integrator. The full bridge capacitors are composed of two sensing capacitors of the accelerometer and two reference capacitors which are chosen to have the same value with the sensor rest capacitances.

The charge integrator block includes a fully differential OTA, which drives the integration capacitors, C_{int}. It also includes a bias generator for biasing the amplifier. The function of the charge integrator block is to convert the capacitance difference of the accelerometer to a differential analog voltage at the output nodes of the OTA.

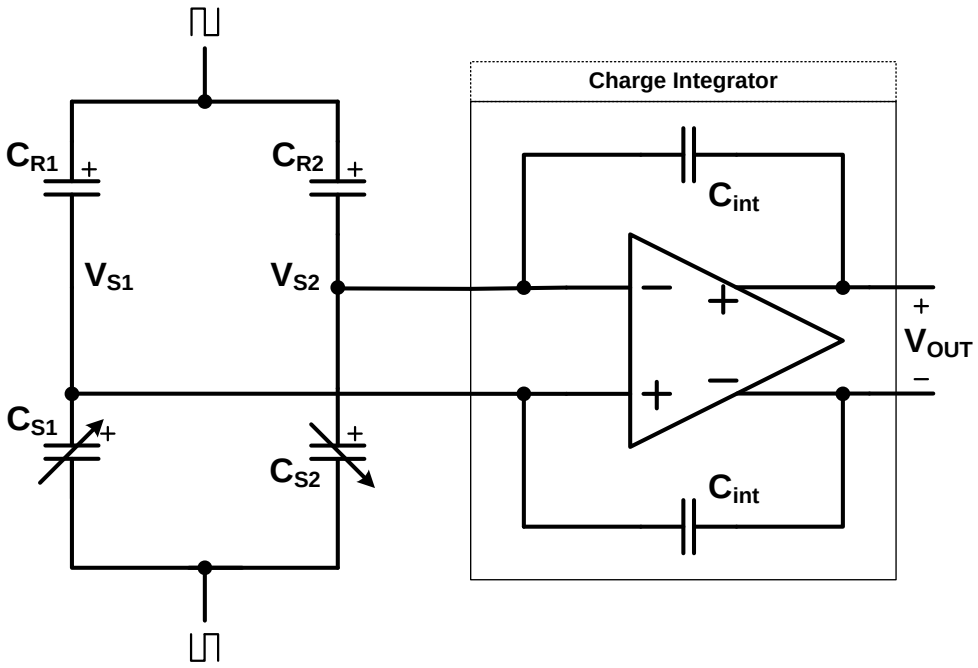


Figure 4.8. Basic schematic of the charge integrator circuit.

The operation principle of the charge integrator block is based on charge transfer from the bridge capacitors to the integration capacitors. Square wave is applied to the top and bottom electrodes of the bridge configuration. The square wave applied to the bottom node is in the opposite phase with the square wave at the top node. The readout is performed at the instant of the applied square waves change states. Let us now consider the time when the signal at the top node switches from high to low; hence, the bottom node signal switches from low to high. Before the switching time, assume that all the capacitor voltages are set to $V_{DD}/2$, which is 2.5 V. After the switching, the charge must be conserved. The Equations (4.1) to (4.4) gives the initial and final charges of each capacitor.

$$Q_{CR1,i} = C_{R1} \times V_{DD}/2 \quad \rightarrow \quad Q_{CR1,f} = C_{R1} \times (-V_{S1}) \tag{4.1}$$

$$Q_{CR2,i} = C_{R2} \times V_{DD}/2 \quad \rightarrow \quad Q_{CR2,f} = C_{R2} \times (-V_{S2}) \tag{4.2}$$

$$Q_{CS1,i} = C_{S1} \times V_{DD}/2 \quad \rightarrow \quad Q_{CS1,f} = C_{S1} \times (-V_{S1}) \tag{4.3}$$

$$Q_{CS2,i} = C_{S2} \times V_{DD}/2 \quad \rightarrow \quad Q_{CS2,f} = C_{S2} \times (-V_{S2}) \tag{4.4}$$

Here, because of the high amplifier gain, the input nodes of the amplifier will be held at the same voltage. After equating the voltages at these nodes, the charge transferred Q_T to the integration at each node is calculated as in Equations (4.5) to (4.7).

$$V_S = V_{S1} = V_{S2} \tag{4.5}$$

$$\begin{aligned} Q_{T1} &= \left(Q_{CS1,i} - Q_{CS1,f}\right) - \left(Q_{CR1,i} - Q_{CR1,f}\right) \\ &= C_{S1}(V_{DD}/2 - V_{S1} + V_{DD}) - C_{R1}(V_{DD}/2 + V_{S1}) \end{aligned} \tag{4.6}$$

$$\begin{aligned} Q_{T2} &= \left(Q_{CS2,i} - Q_{CS2,f}\right) - \left(Q_{CR2,i} - Q_{CR2,f}\right) \\ &= C_{S2}(V_{DD}/2 - V_{S2} + V_{DD}) - C_{R2}(V_{DD}/2 + V_{S2}) \end{aligned} \tag{4.7}$$

The charge transferred to the integration capacitors, generates a voltage at the output nodes of the charge integrator. Calculation of the differential output voltage V_{OUT} is given in equations (4.8) and (4.9).

$$V_{OUT} = V_{Cint\,1} - V_{Cint\,2} = \frac{Q_{T1} - Q_{T2}}{C_{int}} \tag{4.8}$$

$$V_{OUT} = \frac{(3V_{DD}/2 - V_S)(C_{S1} - C_{S2}) - (V_{DD}/2 + V_S)(C_{R1} - C_{R2})}{C_{int}} \tag{4.9}$$

If the voltage V_S is assumed to be $V_{DD}/2$, and the reference capacitors are selected to be equal, the output equation simplifies to Equation (4.10).

$$V_{OUT} = \frac{V_{DD}(C_{S1} - C_{S2})}{C_{int}} \tag{4.10}$$

For the V_S voltage assumption to be true, the reference capacitors should be selected equal to the sensor rest capacitances. The relation between the value of reference capacitors and V_S voltage can be given as in the Equation (4.11). This equation can be derived by equating the total charge transferred to the integration capacitors to zero, i.e. $Q_{T1} + Q_{T2} = 0$.

$$V_S = \frac{V_{DD}}{2}\left(\frac{3C_S - C_R}{C_S + C_R}\right) \tag{4.11}$$

Hence, the reference capacitors being not equal to the value of the accelerometer rest capacitors, results in the change of scale factor. Moreover, by having the Vs voltage different from $V_{DD}/2$, it can get out of the input common mode range of the amplifier, which results in improper operation of the amplifier.

4.2.2.1. Operational Transconductance Amplifier (OTA)

The operational transconductance amplifier (OTA) used in the charge integrator is a critical component for the sampling rate and noise considerations. In order to operate the circuit at high sampling frequency, the slew rate of the OTA is the most significant parameter. Moreover, OTA is the component, which dissipates most of the power in the readout circuit. Thus, a low noise, low power and high slew rate OTA is needed. For this purpose, a folded cascode, fully differential OTA is designed. This structure utilizes high power supply rejection ratio (PSRR), high gain-bandwidth product and low noise.

The cascode structure has the advantages of having high open-loop gain, high supply rejection ratio and lower noise compared to other amplifier structures. The reason for choosing folded cascode structure instead of telescopic structure is to obtain higher output voltage swing and wider input common mode range. However, folded structure has relatively higher noise and higher power consumption than the telescopic structure.

There is a trade of between noise and the speed of the amplifier for setting the widths of the input transistors. Increasing width of the input transistors increases the gate capacitances and hence, decreases the slew rate and the unity gain frequency of the amplifier. Besides, decreasing noise results in higher currents in the branches; therefore increases the power dissipation of the circuit. A high slew rate, low noise, low power dissipation OTA was designed considering all these requirements and tradeoffs.

The schematic of the folded cascode OTA is given in Figure 4.9. M1 and M2 transistors are input differential pair, which provides the gain on the folded branch. M3 and M4 transistors source the current to the folded branch with high output resistance. The open loop gain expression of the folded cascode OTA is given in Equation (4.12).

$$|A_v| \approx g_{m1}\{[(g_{m7} + g_{mb7})r_{O7}(r_{O1}//r_{O5})]//[(g_{m9} + g_{mb9})r_{O9}r_{O11}]\} \quad (4.12)$$

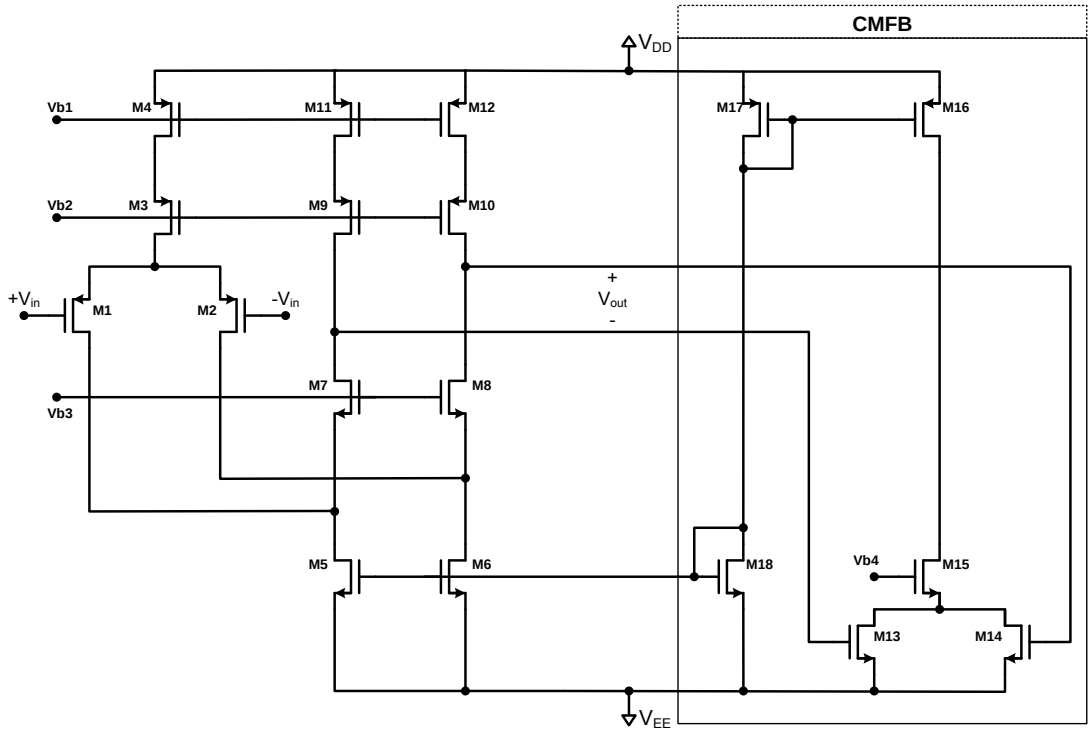


Figure 4.9. Schematic view of the folded cascode OTA.

The input transistors M1 and M2 should have higher trans-conductance for obtaining higher gain. Therefore, the input transistors M1 and M2 should carry higher currents. For the gain of the amplifier to be high, the output resistances of the transistors M9 to M12 should be high, and since output resistance is inversely proportional to the current, currents of the transistors M5 to M14 should be low. Hence, in order to obtain high gain, the W/L ratios of the input transistors are designed to be high, and W/L ratios of M13 and M14 transistors are designed low. Table 4.1 shows the W/L ratios of the transistors.

The noise of the OPAMP is an important factor in order to achieve a high-resolution readout circuit. The main noise sources of the amplifier are the noises from the input transistors M1, M2, as shown in Equation (4.13). Wide transistors are used as the input transistors for decreasing the noise. The trans-conductance of transistors M13 and M14 are kept low by having a lower bias current. For the transistors M5 to M8, through which a high current flows, the trans-conductance is decreased by keeping the *W/L* ratios low and increasing the biasing V_{GS} voltages.

Table 4.1: Size of the transistors used in the OTA circuit.

Transistor	W/L
M1, M2 (PMOS)	800 / 4 μm
M3 (PMOS)	1200 / 4 μm
M4 (PMOS)	800 / 4 μm
M5, M6 (NMOS)	93 / 4 μm
M7, M8 (NMOS)	152 / 4 μm
M9, M10 (NMOS)	177 / 4 μm
M11, M12 (PMOS)	80 / 4 μm
M13, M14 (PMOS)	40 / 4 μm
M15 (NMOS)	8 / 4 μm
M16 (PMOS)	8 / 4 μm
M17 (PMOS)	32 / 4 μm
M18 (NMOS)	29 / 4 μm

$$V_n{}^2 = 8kT\left(\frac{2}{3g_{m1,2}} + \frac{2\left(g_{m5,6} + g_{m7,8}\right)}{3\left(g_{m1,2}\right)^2} + \frac{2g_{m13,14}}{3\left(g_{m1,2}\right)^2}\right) \tag{4.13}$$

Because of having high output resistance, the output common mode voltage of the OTA is not stable at the mid-point voltage and highly dependent on the circuit and process parameters and bias voltages. Hence, with a little disturbance of circuit parameters, the output common mode settles to the supply voltages. In order to keep the common mode voltage at the mid-point voltage, a common mode feedback (CMFB) circuitry is needed. The CMFB circuitry measures the common mode output of the amplifier and gives a feedback to the amplifier to settle it to the desired value. For this purpose, a parameter proportional to the common mode voltage should be obtained. This is achieved by using two transistors M13 and M14 operating in deep triode region, gates of which are connected to the outputs of the OTA, and sink a total current proportional to the common mode output voltage. The current expressions of the transistors in deep triode region are given in Equations (4.14) and (4.15).

$$i_{DS,14} = K_n\left(v_{GS,14} - V_{TN} - \frac{v_{DS}}{2}\right)v_{DS} \approx K_n(v_{OUT+} - V_{TN})v_{DS} \tag{4.14}$$

$$i_{DS,13} = K_n \left(v_{GS,13} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \approx K_n (v_{OUT-} - V_{TN}) v_{DS} \quad (4.15)$$

where, M13 and M14 transistors have the same v_{DS} voltage. When the drain source voltages of the transistors are assumed sufficiently low, then the sum of the drain source currents of the transistors become linearly dependent on the sum of the voltages applied at the gates of the transistors as given in Equation (4.16).

$$i_{DS,15} = i_{DS,14} + i_{DS,13} = K_n (v_{OUT+} + V_{OUT-} - 2V_{TN}) v_{DS} \quad (4.16)$$

The deep triode operation of these transistors is ensured by the transistor M15, which operates in saturation region. When the gates of the deep triode transistors are connected to the differential output of the OTA, the total current passing through is proportional to the common mode voltage. After obtaining this current value, it should be fed back to the amplifier; the current is mirrored with a factor to the M5 and M6 transistors of the amplifier. In this way, if the common mode voltage increases, M5, M6 transistors sink more current and pull the common mode voltage at the output to a lower value. Therefore, it keeps the common mode voltage at a value defined by the CMFB circuitry.

AC simulation results of the amplifier are given in Figure 4.10. As seen in the simulation results, the bandwidth of the amplifier is narrow, but since the amplifier is operated in closed loop, the decrease of open loop gain at higher frequencies is not significant. Instead, gain bandwidth product is an important parameter, in the design of the OTA.

Noise of the amplifier is another critical parameter of the OTA. The input referred noise simulation result of the amplifier is given in Figure 4.11. The design of the circuit is optimized in order to minimize the noise, and hence, 4.4 nV/√Hz thermal noise is achieved. The noise levels could be further decreased by increasing the

widths of the input transistors, however this would cause high power dissipation, and a decreased speed due to the high input capacitances. Table 4.2 summarizes the simulation results of the OTA.

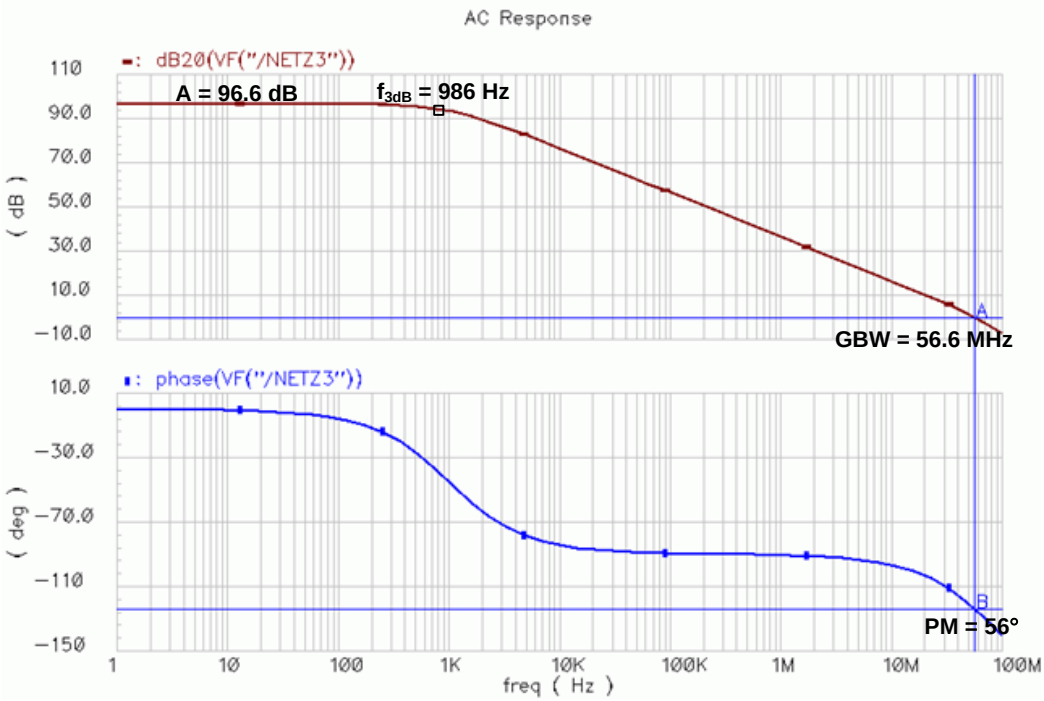


Figure 4.10. AC simulation results of the folded cascode OTA.

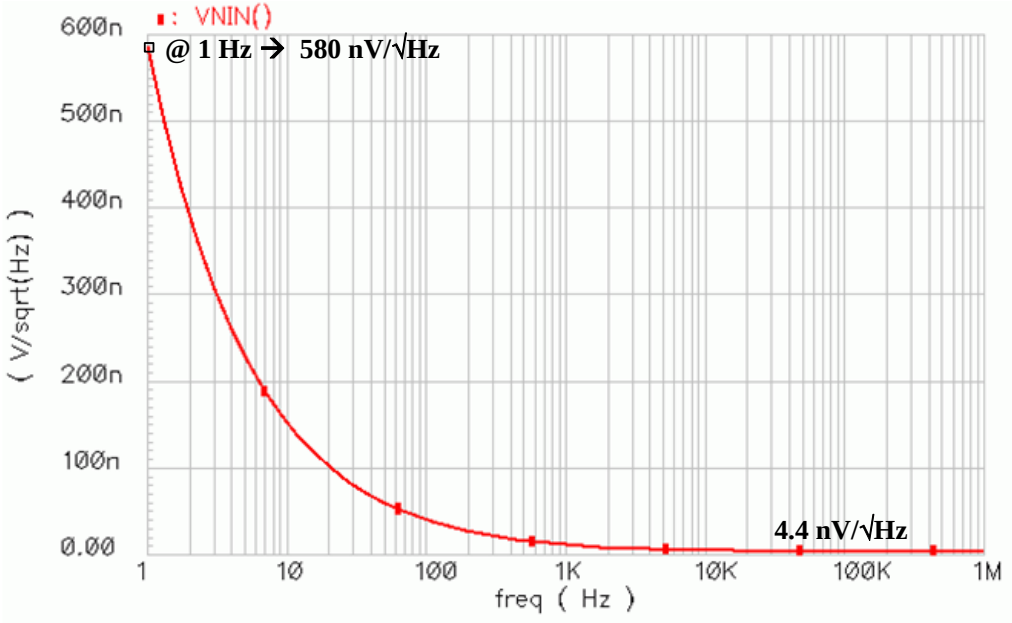


Figure 4.11. Noise simulation results of the folded cascode OTA.

Table 4.2: Summary of the simulation results of the folded cascode OTA.

Parameter	Value
Gain	96.6 dB
Bandwidth	986 Hz
GBW	56.6 MHz
Phase margin	56°
Power Dissipation	5.6 mW
Input referred noise (@ 10MHz)	4.4 nV/√Hz
Input referred noise (@ 1 Hz)	580 nV/√Hz

4.2.2.2. Bias Generator

The folded cascode OTA needs supply voltage and temperature independent bias voltages for proper operation. For generating bias voltages of the folded cascode amplifier, a bias-voltage generator circuit, given in Figure 4.12 was designed. The transistors M1 to M8 generate the two bias voltages V_{b1} and V_{b4}. The transistors from M9 to M14 generate the other bias voltages V_{b2} and V_{b3} and the transistors M3 to M6 are biased by these voltages. The currents I_{DS1} and I_{DS2} are defined by the W/L ratios of M1 and M2 and the value of R. In addition, these currents are guaranteed to be equal by the current mirroring action of M7 and M8. Table 4.3 gives the W/L ratios of the transistors used in the bias generator.

The bias generator circuit itself has another stable state where all the transistors are in cutoff; hence, for operating in normal condition, it needs a start-up circuit. The start-up circuit is constituted by the transistors M15 to M18. After the supply is turned on, M15 pulls the V_{b1} voltage low, then the currents start to flow through the transistors, and when the V_{b3} becomes higher, M18 makes M15 to enter into cutoff, so the start-up circuit does not consume any power while the bias generator starts to operate.

Figure 4.13 gives the simulation results of the bias generator between -40°C/+75°C. The most critical bias voltage, which affects the operation of OTA mostly, is V_{b1}. Therefore, the temperature response of the circuit is optimized for V_{b1} voltage, where a parabolic behavior of temperature dependency is obtained. The temperature

dependencies at room temperature are given on the figure, which shows a low temperature dependency of V_{b1} bias voltage.

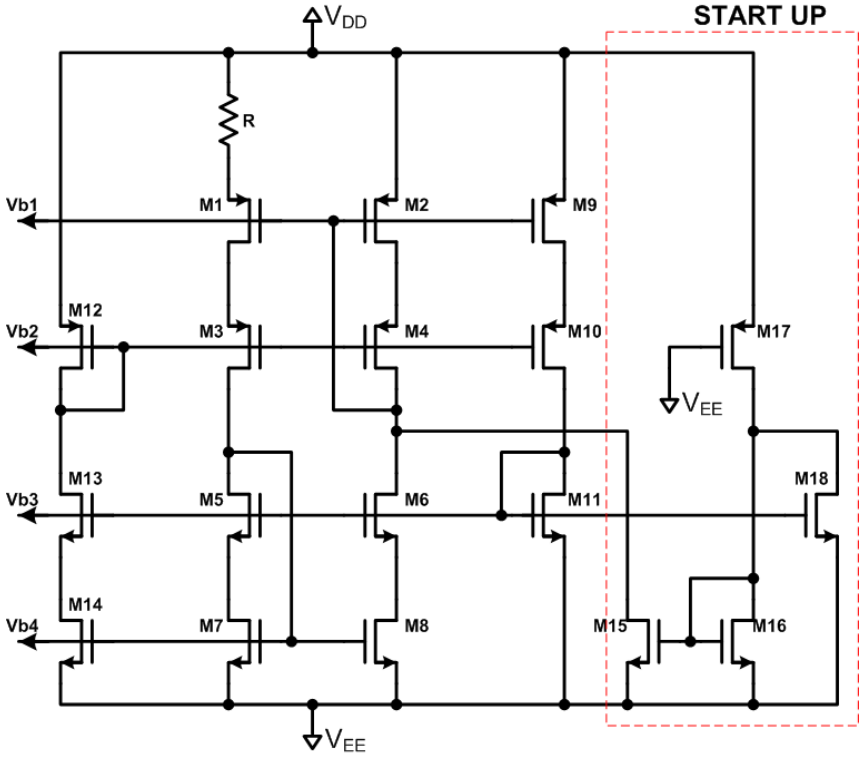


Figure 4.12. Schematic view of the bias generator circuit.

Table 4.3: Size of the transistors used in the bias generator circuit.

Transistor	W/L
M1 (PMOS)	160 / 4 µm
M2 (PMOS)	80 / 4 µm
M3, M4 (PMOS)	150 / 4 µm
M5, M6 (NMOS)	150 / 4 µm
M7, M8 (NMOS)	16 / 4 µm
M9 (PMOS)	80 / 4 µm
M10 (PMOS)	200 / 4 µm
M11 (NMOS)	7.6 / 4 µm
M12 (PMOS)	21 / 4 µm
M13 (NMOS)	200 / 4 µm
M14 (NMOS)	16 / 4 µm
M15 (NMOS)	3 / 2 µm
M16 (NMOS)	1 / 4 µm
M17 (PMOS)	1 / 30 µm
M18 (NMOS)	0.8 / 0.8 µm

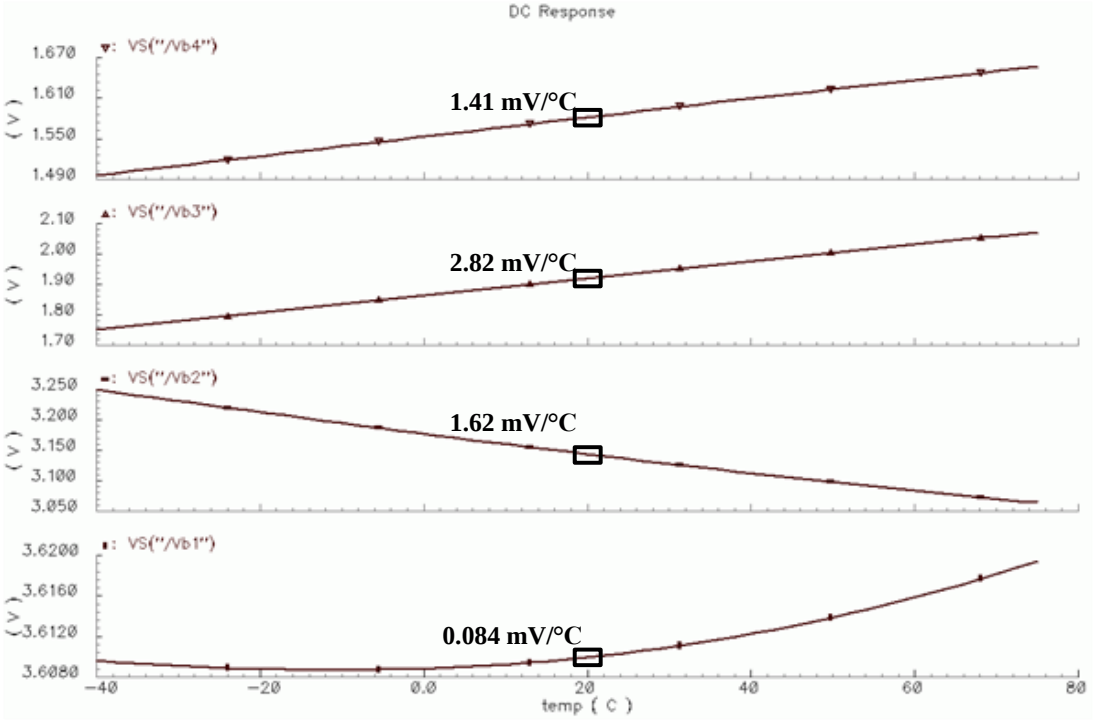


Figure 4.13. Temperature simulation results of the bias generator circuit.

4.2.3. Lead Compensator

Sigma-delta modulators operate at high sampling frequencies to accomplish high resolution. However, high frequency operation brings some stability problems. In electro-mechanical sigma-delta systems, the mass residual motion should be settled at high frequency for the system to be stable and having low amplitude of residual motion. However, the transfer function of the closed loop system can result the system to settle at a lower frequency because of the poles arising from the mechanical structure and the readout circuit. Therefore, generally it is required to add a zero into the sigma-delta loop. In this study, adding a zero to the system was realized using a switched capacitor lead compensator circuit. The schematic view of the lead compensator circuit is shown in Figure 4.14, which uses a differential structure.

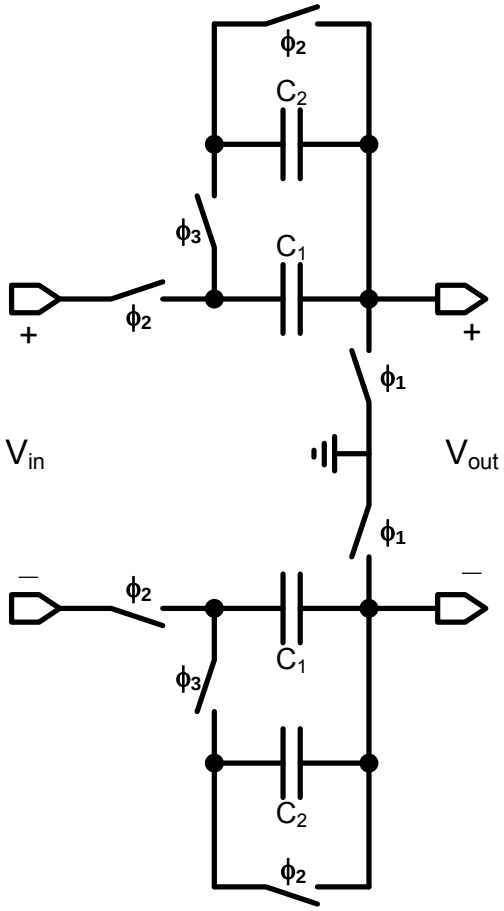


Figure 4.14. Schematic of the lead compensator circuitry.

The switching timings of the lead compensator are given in Figure 4.15. At the time between t_0 and t_1, where ϕ_1 and ϕ_2 signals are both high and ϕ_3 is low, the input signal is sampled on the C_1 capacitors. Then, ϕ_2 switches are turned off, disconnecting the input from the compensator capacitors. At the time t_2, ϕ_3 switches are turned on, therefore the charge on the C_1 and C_2 capacitors are shared with the C_3 and C_4 capacitors.

At the t_3 instant, ϕ_3 and ϕ_1 switches are turned off, then ϕ_2 is turned on, hence the input is connected to the C_1 and C_2 capacitors, which are keeping a factor of the previous input voltage value. Thus, the output of the compensator becomes the input value subtracted with a factor of the previous input value, as given in equation (4.17).

$$V_{OUT} = V_n - V_{n-1}\frac{C_1}{C_1 + C_2} \tag{4.17}$$

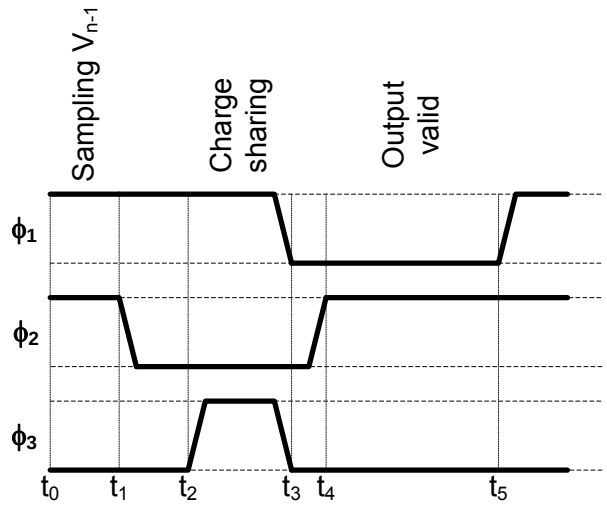


Figure 4.15. Timing diagram of the lead compensator, type 1.

4.2.4. Comparator

In the sigma-delta loop, a high precision, high speed comparator is needed, to obtain a high sampling rate and high resolution in overall readout circuit. Since, sample based operations are performed in the readout circuit, the comparator should compare the output voltages of the charge integrator stage at a single instant in the sampling period, and keep the result until the next sample. Consequently, a dynamic latching comparator is used, which compares its inputs at the rising edge of a clock signal, and keeps the output value until the falling edge of the same clock signal.

The schematic of the dynamic latching comparator circuit is given in Figure 1.1, and the W/L ratios of the transistors are given in Table 4.4. The operation of the circuit can be described as follows. When the Clk is low, the comparator is in pre-charge

phase and both outputs of the comparator are low, and there is no current flowing through the branches. As soon as the Clk signal is switched to high, it compares the input voltages and gives an output accordingly. Cross-coupled M3 and M4 transistors result in faster decision of the comparator. After the decision is made, M5 and M6 cut the currents on the branches, and the output is stored until the Clk is made low.

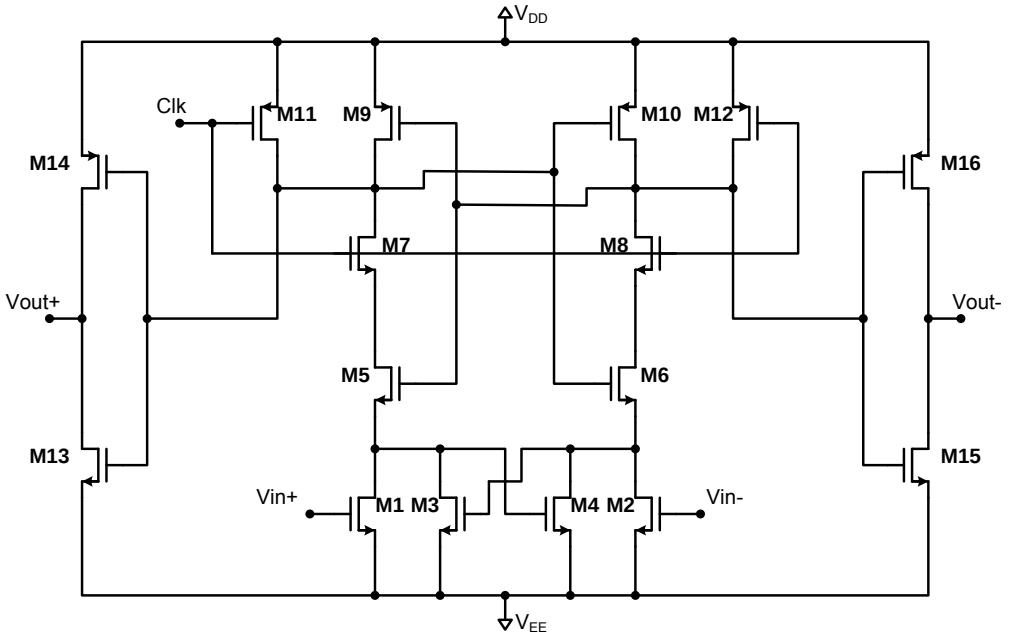


Figure 4.16. Schematic view of the dynamic comparator.

Table 4.4: Size of the transistors used in the comparator circuit.

Transistor	W/L
M1, M2 (NMOS)	4 / 4 μm
M3, M4 (NMOS)	40 / 4 μm
M5, M6 (NMOS)	8 / 4 μm
M7, M8 (NMOS)	10 / 4 μm
M9, M10 (PMOS)	20 / 4 μm
M11, M12 (PMOS)	8 / 4 μm
M13, M15 (NMOS)	4 / 4 μm
M14, M16 (PMOS)	10 / 4 μm

The offset voltage of the comparator is simulated in a temperature range of -40°C to 60°C. A 3 μV/°C dependency on temperature is observed, as shown in Figure 4.17. The temperature dependency of the offset voltage results in a dependency of output bit-stream to the temperature. However, the effect of the offset voltage on the output temperature dependency is in the order of a few micro-g's per degree.

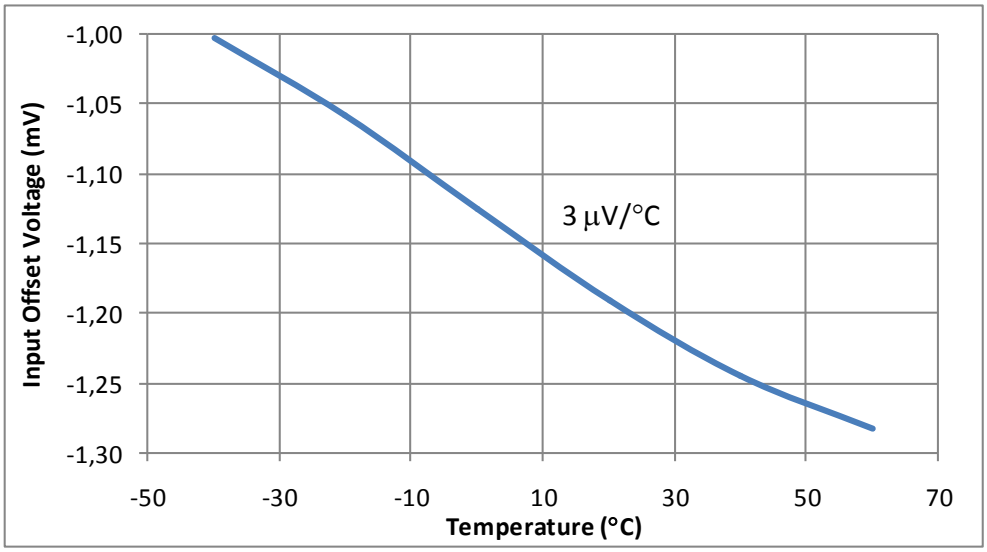


Figure 4.17. Input offset voltage of the comparator versus temperature.

4.2.5. Start-up Circuit

If there is a high deflection on the proof-mass position, with the effect of a large input acceleration or because of a non-ideality, the force feedback applied during the normal closed loop operation of the circuit may not be enough for holding the proof mass at the midway between the electrodes. For holding the proof mass in the case of large deflections, a start-up circuit is used. The schematic of the start-up circuit is given in Figure 4.18. The output of the charge integrator stage is used as the input of the start-up circuit. At the input of the start-up circuit, there are two comparators, which have internal offset values of 1 V at the inputs. Hence, if differential output of the charge integrator exceeds the range +1V, -1V, the OR gate gives a high value,

and the capacitor is discharged. In this way, the clock of the readout circuit is turned off, until the capacitor is charged again through the PMOS transistor. The PMOS transistor has a low W/L ratio, so that the charging of the capacitor takes longer time. In this period, constant feedback force is applied to the accelerometer. The charging time of the capacitor is designed to be around 40μsec.

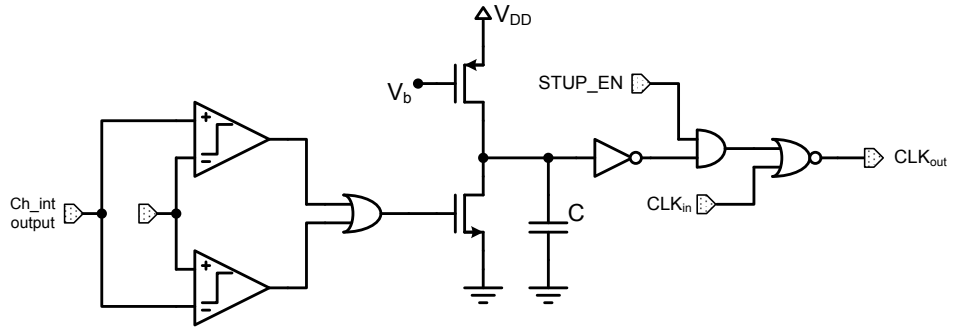


Figure 4.18. Schematic view of the start-up circuit.

4.2.6. Multiphase Clock Generator

The multiphase clock generator creates the switching signals and phases of the readout circuit, as shown in Figure 4.19. The circuit uses a single-phase clock signal for generating the various phases of clock signals. The clock source is supplied from the on-chip 500kHz clock generator circuit. The clock input can also be supplied from an external clock source, which can be increased up to 700kHz. Increasing the frequency higher than 700 kHz results in incorrect generation of clock timings, hence the readout circuit does not operate properly. For generating the multiphase clock signals, first a pulse is generated, where the width of the pulse is independent of the input clock period. Therefore, changing the period of the input clock signal does not change the pulse with, but only the frequency of the pulse. Then this pulse is shifted many times by using the delay elements, hence multiphase pulses are generated. The delay elements used are composed of two inverters and a capacitor in between. Then, these pulses are used to generate various signals needed for the readout circuit, by the use of basic logic operations. All the pulses are

independent of the clock period, so when the period of the input clock signal is increased, only the feedback duration is increased but the readout timings are kept constant. The simulation result of the output waveforms of the multiphase clock generator is given in Figure 4.20.

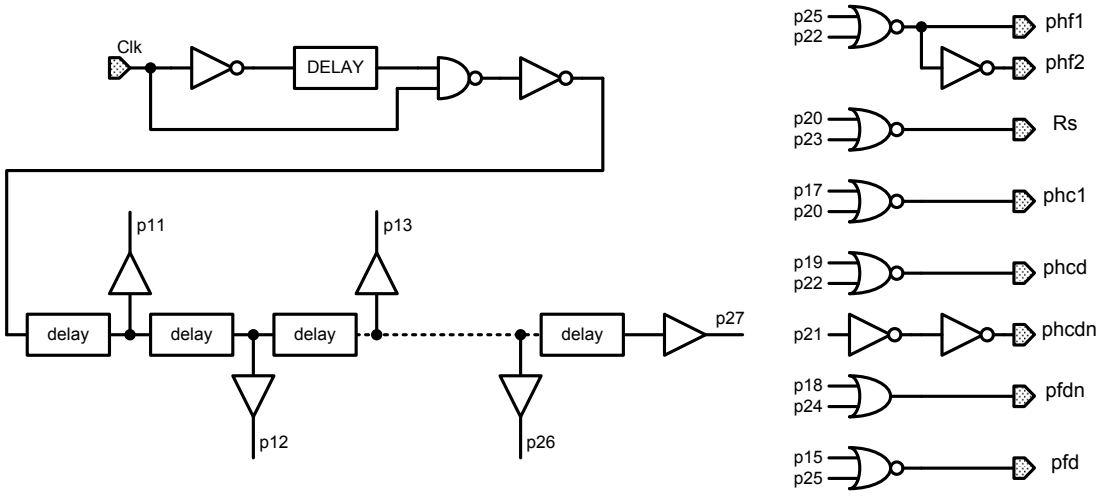


Figure 4.19. Schematic view of the multiphase clock generator circuit.

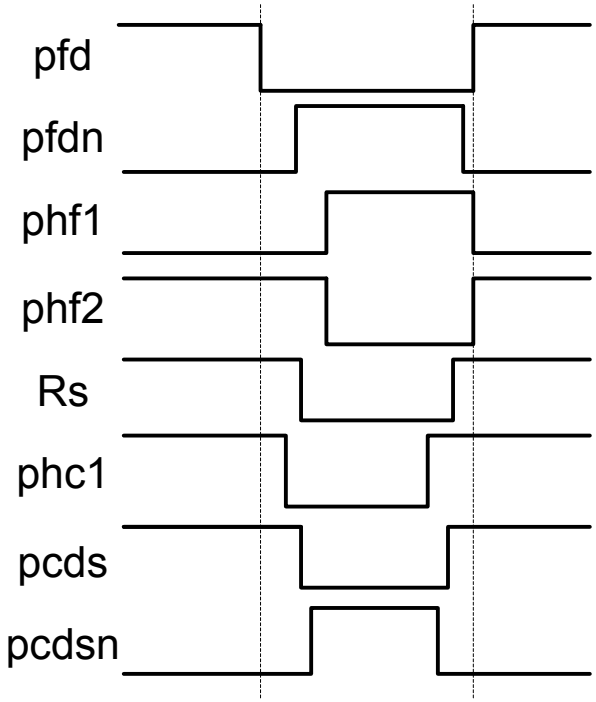


Figure 4.20. Timing diagram of the signals generated by the multiphase clock generator.

4.2.7. Test Structures and Control Signals

There are various testing structures for making different parts of the readout circuit available to be tested. First test structure included in the circuit is for controlling timing signals generated by the multiphase clock generator, as shown in Figure 4.21. This circuit consists of 8 multiplexers, which are controlled by a single signal "Ext_tim". When the control signal is low, the readout circuit uses the internally generated timing signals and when "Ext_tim" is high, the 8 pins are used as inputs to the circuit and readout circuit uses externally applied timing signals.

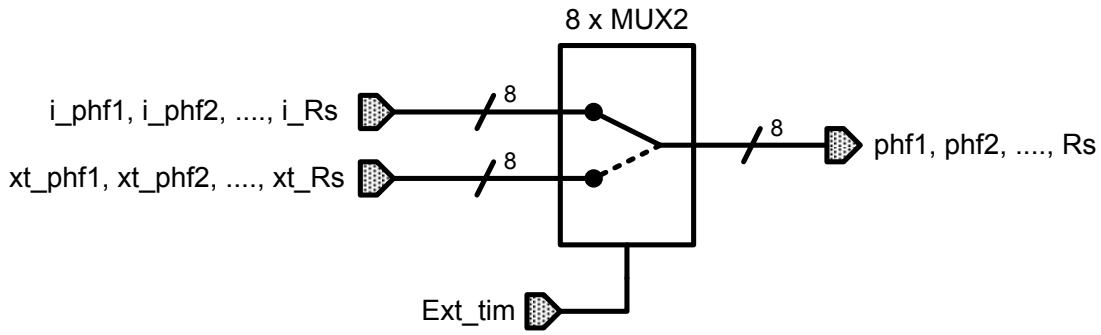


Figure 4.21. Schematic view of multiplexer structures, used for applying external timing signals.

As a second test structure, for observing the internally generated timing signals, one pad is used, and 8 timing signals are decoded using the circuit shown in Figure 4.22. The selection signals are the same signals, which are used for selecting the internal reference capacitors; hence, no additional pads are used for selecting the timing signal to be observed.

Another test structure, the sample and hold circuitry, is implemented to observe and test the open loop operation of the readout circuit. Buffer op-amps with sample and hold capacitances are used as shown in Figure 4.23. This circuit enables observing the sampled analog outputs at a longer duration of the sampling period, provides driving of high external capacitances.

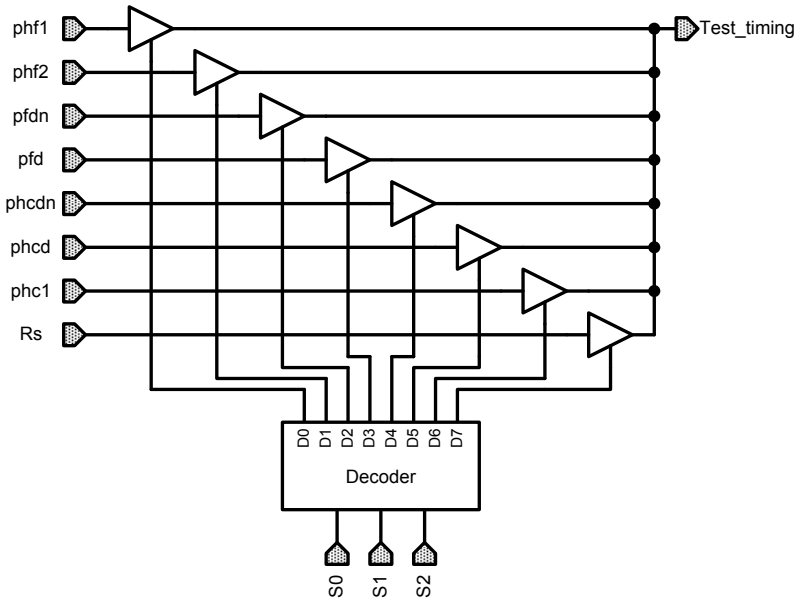


Figure 4.22. Schematic view of the test structure for observing the internal signals.

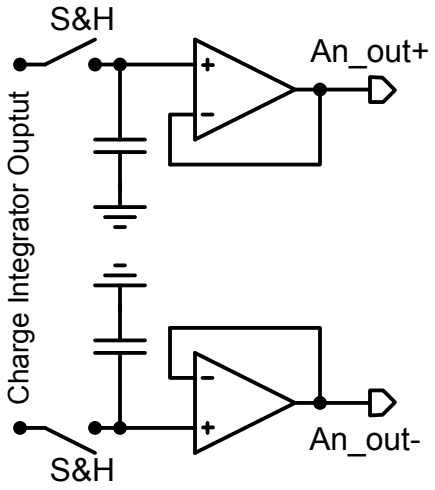


Figure 4.23. Schematic view of the sample and hold circuitry.

For increasing the testability of the circuit, there are also various selection signals to set the capacitor values and to enable and disable various parts of the circuitry. The reference capacitors, which are used in the full bridge structure with the accelerometer capacitances, are implemented in the chip, and are selectable, using 5 control signals, enabling 5 different sized capacitor. The sizes of the capacitors are as binary coded, with minimum sized capacitor having value of 0.875 pF and the

largest capacitor having 14 pF value. Therefore, a maximum of 27.125 pF of reference capacitor value can be selected. Similarly, the integration capacitors used in the charge integrator stage is selectable by 4 control signals up to 15 pF, with 1 pF increments.

4.3. Overall Circuit Simulation Results

After the design of individual block diagram of the readout circuit, the simulations of the overall system is performed, to observe the operation of the readout circuitry. The simulations are performed in Cadence environment with the model of the mechanical sensor, both in open loop and closed loop modes. The open loop simulation results are given in Figure 4.24. In this simulation, 1 kHz of sinusoidal input acceleration is applied to the system, and the charge integrator differential output is observed. Capacitive difference on the sensor follows the input acceleration signal with a phase delay. The analog output samples are observed to be proportional to the capacitive difference.

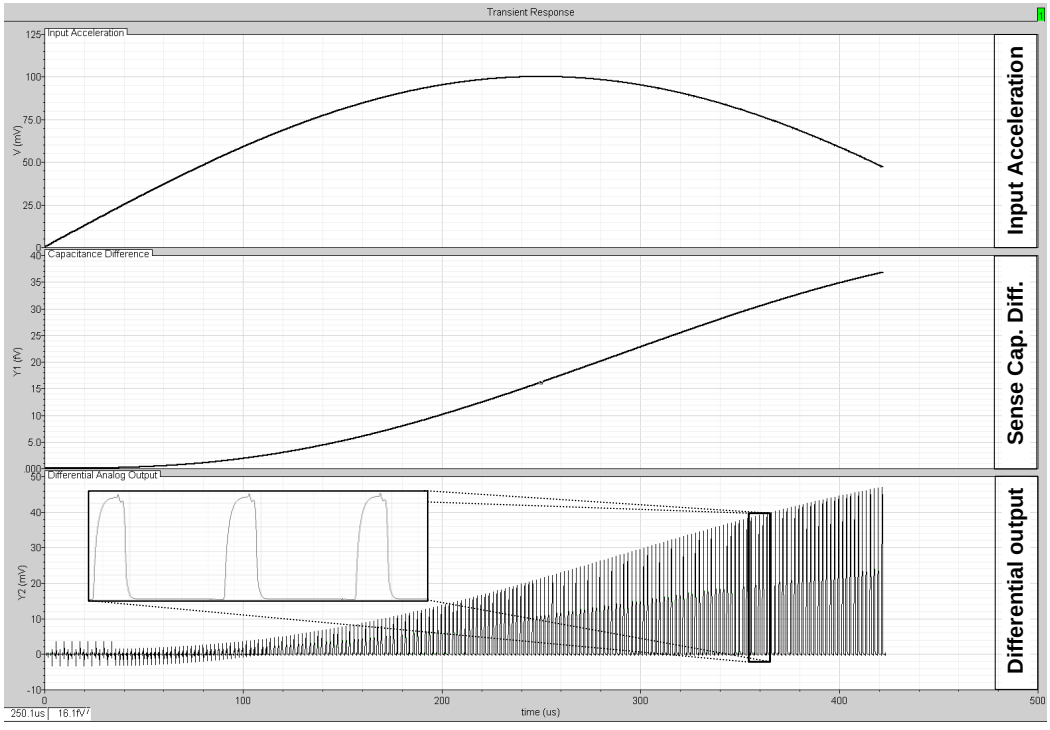


Figure 4.24: Open loop simulation results of the sigma delta readout circuit together with the model of the SOG accelerometer.

Figure 4.25 gives the closed loop simulation results of the readout circuit combined with the mechanical sensor model. In this simulation, a 1 kHz, 1 g amplitude of input acceleration is applied to the system. The displacement of the proof mass and digital output signals are observed. The average value of output pulses increase for increasing input accelerations. The residual motion of the proof mass is observed to be around 1 nm in amplitude.

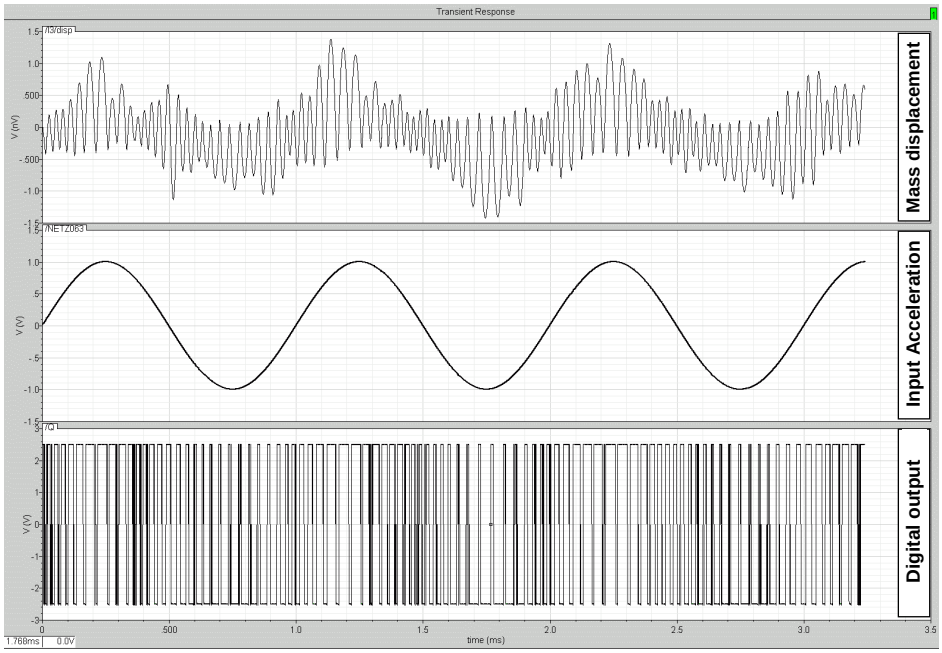


Figure 4.25: Closed loop simulation results of the sigma delta readout circuit together with the model of the SOG accelerometer

The simulation times in Cadence environment cannot exceed a few milliseconds due to the long computation time. Simulations performed in Matlab environment gives much fast results accurately. The model of the readout circuit with the accelerometer is given in Figure 3.9. With this model a simulation is performed using 1 kHz, 1 g amplitude of input acceleration. The simulation results are given in Figure 4.27. The density of the output bit-stream is observed to be changing in parallel with the input acceleration. The simulation results of Cadence and Matlab are consistent.

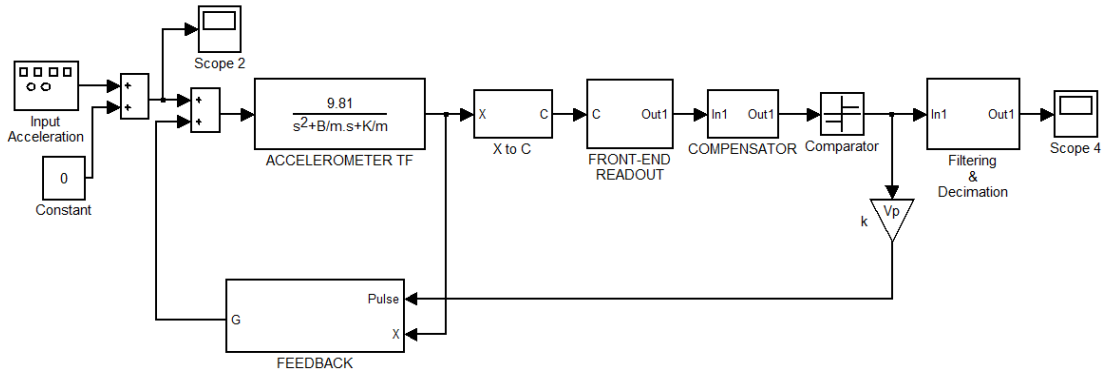


Figure 4.26: Simulink model of the complete electromechanical closed loop system.

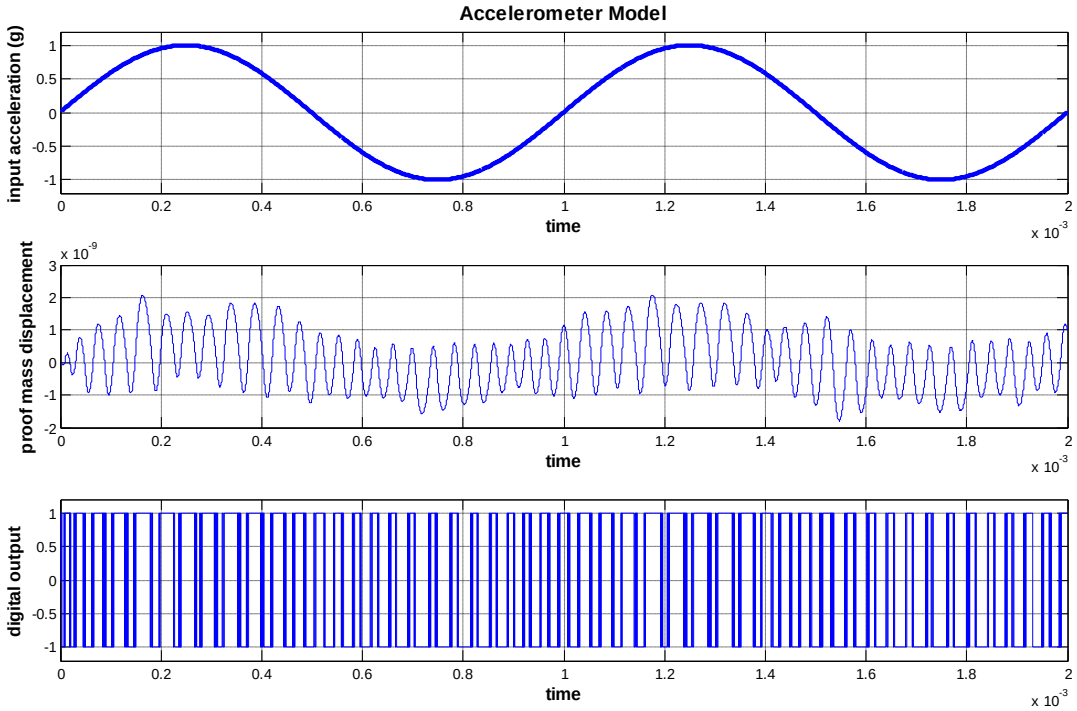


Figure 4.27: Simulation results of the accelerometer system using the model created in Matlab.

4.4. Layout Considerations

The layout of the readout chip is drawn and the chip is implemented with 0.6µm XFAB CMOS process. The layout of the sigma-delta readout chip is given in Figure 4.28, including the floor plan of the chip.

Since the readout circuit has a fully differential structure, the layout should be drawn fully symmetrically, in order to reduce any differential offset, parasitic impedance and other non-idealities in the circuit. The analog blocks and the digital blocks of the circuit are separated as much as possible, by placement and the usage of guard rings around the blocks. The guard rings are used for isolating the part of the circuit, and reducing the substrate noise, due to the other components of the readout circuit.

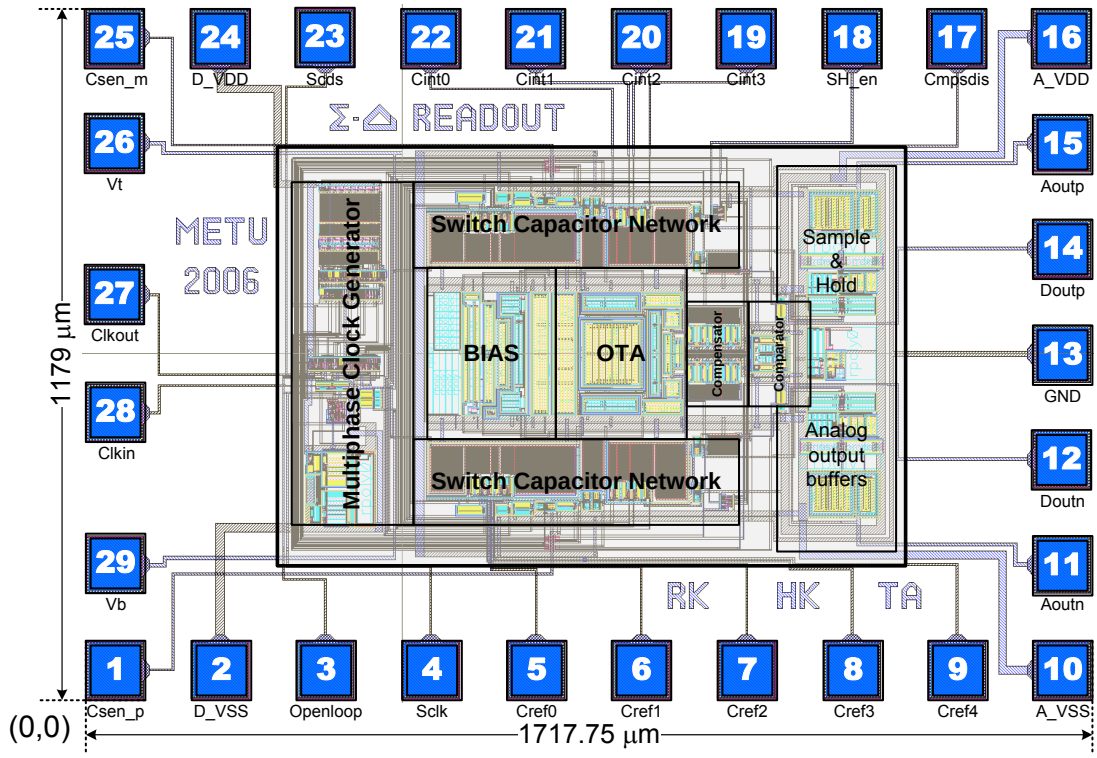


Figure 4.28: Layout view and floor plan of the fully differential readout circuit chip.

4.5. Performance Limitations

There are various parameters, limiting the performance of the readout circuit together with the accelerometer. These limitations include the noise sources, which are the readout circuit noise due to the OTA, switches and other circuit components; sigma – delta loop noises, such as the quantization noise and mass residual motion; and the mechanical noise due to the accelerometer. These noise sources limit the minimum measurable acceleration value. On the other end, maximum operation range is limited by the sensor dimensions in open loop mode and by maximum applicable feedback force in closed loop mode. In addition, offsets are created due to the non-linearity in both readout circuit and accelerometer. In the following subsections, these non-idealities limiting the performance of the system will be discussed.

4.5.1. Mechanical Noise

Mechanical noise exists on any mechanical structure, as the force applied on the mass of the mechanical structure. This mechanical noise, which is also called Brownian noise, is due to the thermal motion of the molecules. Brownian noise has a white noise characteristic with the noise amplitude in terms of acceleration given in equation (4.18).

$$a_{n,mech} = \frac{\sqrt{4k_B TB}}{m} \qquad (m/s^2) \tag{4.18}$$

where, k_B is Boltzmann's constant, T is the temperature, B is the mechanical damping constant and m is the mass of the mechanical structure. Hence, in order to achieve low noise mechanical devices, the mass of the device should be selected to be large or the structure should have low damping constant. Decreasing the damping constant can be achieved by decreasing the pressure of the environment. However, the vacuum condition can result in stability problems.

4.5.2. Readout Circuit Noise

The noises resulting from the readout circuit are noise due to the amplifier, and kT/C noise created due to the switching of the capacitors. The thermal noise of the OTA was already calculated in section 4.2.2.1, as given in Equation (4.13). When this OTA is used in a switched capacitor structure, the thermal noise is filtered according to the capacitor values. The basic switched capacitor charge-integrator structure is shown in Figure 4.29. The thermal noise of this circuitry is given as in Equation (4.19) [14].

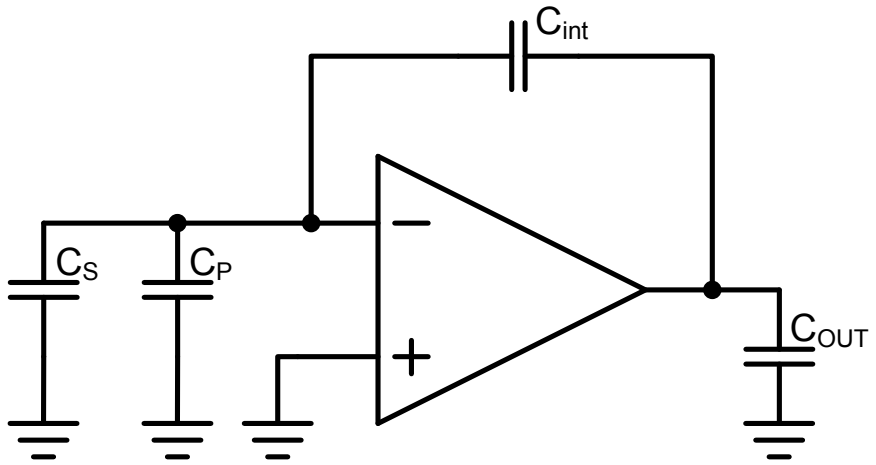


Figure 4.29. Schematic view of the basic switched capacitor charge integrator structure.

$$V_{n,readout} = \sqrt{\frac{16}{3}\frac{C_S + C_P}{C_{int}}\frac{k_B T}{C_{OUT} f_S}} \quad (V/\sqrt{Hz}) \tag{4.19}$$

where, k_B is the Boltzmann's constant, T is the temperature, f_S is the sampling frequency of the readout circuit, and the capacitors are as shown in Figure 4.29. In the figure, C_S is the sensor capacitance; C_P is the parasitic capacitance at the input of the amplifier, C_{int} is the integration capacitor and Cout is the load capacitance at the output of the amplifier. According to the equation (4.19), increasing the value of

integration capacitor C_{int}, decreases the noise of the readout circuit, which is inversely proportional with the square root of C_{int}. However, capacitance to voltage sensitivity of the readout is inversely proportional with the value of C_{int}. Hence, if SNR of the circuit is considered, decreasing the value of integration capacitor, increases the SNR of the circuit.

Another source of noise at the readout circuit is the kT/C noise, which mainly results from switching of the integration capacitors. Hence the kT/C noise expression is given as in equation (4.20).

$$V_{n,kT/C} = \sqrt{\frac{4k_B T}{C_{int} f_S}} \quad (V/\sqrt{Hz}) \tag{4.20}$$

4.5.3. Open Loop Mode Non-Linearity and Operation Range

In open loop operation of the readout circuit, differential capacitance is measured by the readout circuit. However, the relation between the capacitance and proof mass displacement is linear only if the displacements are very small in amplitude, i.e. are ignorable when compared with the finger gap spacings. The Equation (3.2) gives the relation between capacitance difference and displacement of proof mass, which was already discussed in the previous chapter. Figure 4.30 gives the graph of differential capacitance versus displacement, where the highly non-linear dependence can be observed. The finger gap spacings of the accelerometer used to obtain the graph, is 4.5µm. Hence, the linearity for small displacements is observed in this graph. The capacitance non-linearity increases enormously, as the displacement becomes comparable with finger gap spacings.

$$\Delta C = C_1 - C_2 = \frac{N\varepsilon_0 A}{d_1 - x} + \frac{(N-1)\varepsilon_0 A}{d_2 + x} - \frac{N\varepsilon_0 A}{d_1 + x} - \frac{(N-1)\varepsilon_0 A}{d_2 - x} \tag{4.21}$$

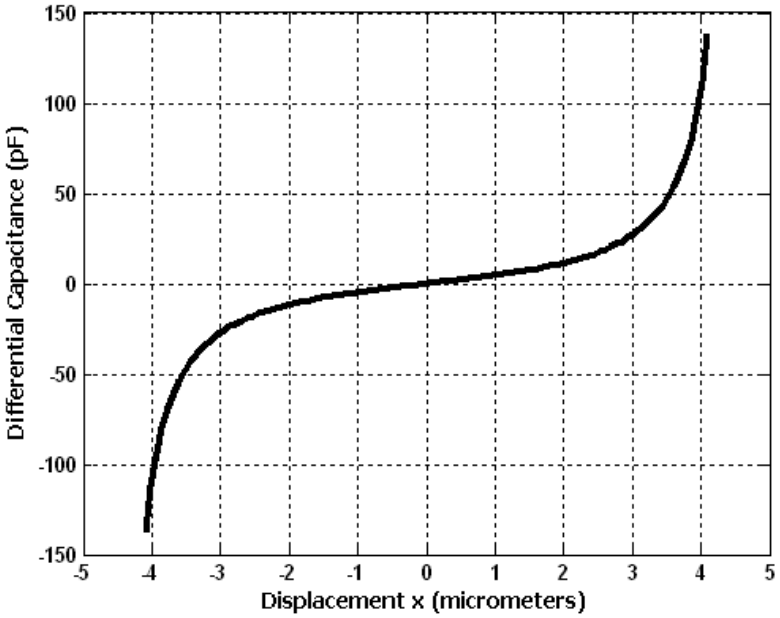


Figure 4.30. Differential capacitance versus displacement graph for a capacitive accelerometer.

The operation range is limited by the finger gap spacings in open loop mode. From the scale factor of the accelerometer at low frequencies, if the value of finger gap spacing is substituted to displacement *x*, maximum operational acceleration range is calculated, as shown in Equation (4.22).

$$a_{max\ ,openloop} = \frac{Kx_{max}}{mg} = \frac{Kd_1}{mg} \quad (g) \tag{4.22}$$

4.5.4. Closed Loop Operational Input Acceleration Range

The input acceleration range of the closed loop system is mostly dependent on the accelerometer parameters. The maximum input acceleration is determined by the maximum feedback force that can be applied to the accelerometer sensor. Equation (4.23) gives the feedback acceleration applied to the sensor proof-mass related to the electrostatic voltage applied to one of the electrodes. In this equation, *m* is the

proof-mass, g is the gravitational acceleration, and x is the amount of displacement of the proof-mass from the rest position.

$$a_f = \frac{1}{2mg}\frac{\partial C}{\partial x}V^2 \quad \text{(g)} \tag{4.23}$$

Since, feedback is not applied full time, but only in the feedback phase, for the sense electrodes, the maximum feedback acceleration is obtained by multiplying a_f by feedback time to total readout time ratio. Hence, one can obtain equation (4.24), which is fully dependent on accelerometer parameters except the feedback ratio and feedback voltage. Since the feedback voltage is supplied from the power source, it cannot be easily changed. The remaining parameter to set the operation range using the readout circuit is the feedback time ratio. As seen from the equations, the acceleration range is linearly proportional with the feedback duration ratio.

$$a_{max} = \frac{T_f}{T_{tot}}a_f = \frac{T_f}{T_{tot}}\frac{1}{2mg}\frac{\partial C}{\partial x}V^2 = \frac{T_f}{T_{tot}}\frac{1}{2mg}\left[A\varepsilon\left(\frac{N}{(d_1-x)^2} - \frac{N-1}{(d_2+x)^2}\right)\right]V^2 \tag{4.24}$$

Where, A is the overlap area of one finger of the accelerometer, and ε is the permittivity of air. Other accelerometer parameters used in equation (4.24) are illustrated in Figure 4.31.

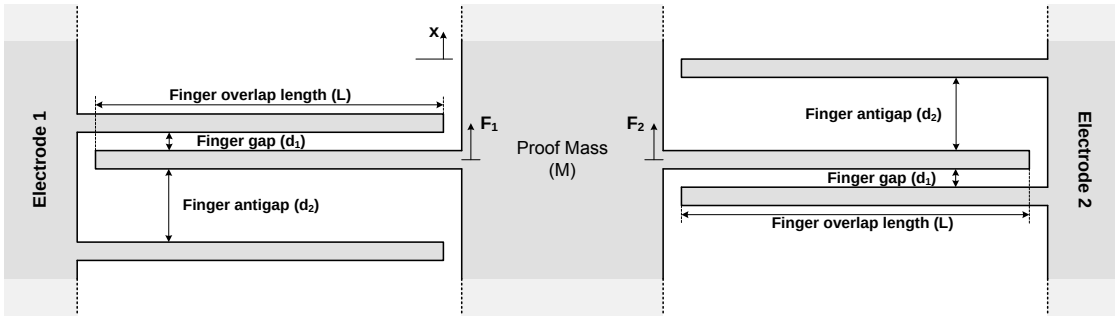


Figure 4.31. Illustration of the sensor fingers and parameters.

4.5.5. Quantization Noise

The quantization noise of a second order sigma-delta system is given as in equation (4.25).

$$V_{qn,rms} = e_{rms} \frac{\pi^2}{M^{2.5}\sqrt{5}} \tag{4.25}$$

In this equation, L is the order of the sigma delta system; M is the oversampling ratio, e_{rms} is the rms value of unshaped quantization noise. For single bit quantization of $\Delta/2$ and $-\Delta/2$, e_{rms} becomes $\Delta/\sqrt{12}$. For the case of accelerometer readout circuit, Δ is $2a_{max}$. Hence, for a second order sigma-delta readout circuit, the quantization noise can be shown as in equation (4.26).

$$V_{qn,rms} = \frac{a_{max}}{\sqrt{15}} \frac{\pi^2}{M^{2.5}} \tag{4.26}$$

Equation (4.26) shows that quantization is highly dependent on oversampling ratio. Therefore, for decreasing the quantization noise, increasing the frequency has a significant effect.

4.5.6. Mass Residual Motion

The proof-mass of the sensor is being held in a constant position using one-bit feedback pulses. This creates a motion around the rest position of the proof-mass. The motion becomes random when a varying input acceleration is applied to the sensor. However, for calculation of the amplitude of the mass residual motion, zero input acceleration is assumed. In this case, with proper lead compensator usage, the mass residual motion settles to the frequency $f_s/4$, as discussed in the previous chapter, where f_s is the sampling frequency of the readout circuit.

The critical parameter is the magnitude of the mass residual motion and its contribution to the acceleration noise in the bandwidth of interest. The displacement magnitude of the residual motion can be found from the feedback acceleration multiplied with the transfer function of the sensor at the oscillation frequency, as in the equation (4.27) given. For calculating the contribution of the mass residual motion to the noise in the bandwidth of interest in terms of acceleration, the equation (4.28) is given. Here, an assumption is made such that the mass residual motion is uniformly distributed in the frequency between 0 and the mass residual oscillation frequency. Since various inputs will be given to the system, the residual motion changes its frequency according to the input magnitude, and hence a white noise assumption can be made to the mass residual motion.

$$x_{rm} = a_{max} \left| \frac{1}{(j2\pi f)^2 + (B/m)(j2\pi f) + (K/m)} \right| \tag{4.27}$$

$$N_{rm} = \sqrt{\frac{f_{BW}}{f}} \left(\frac{K}{m}\right) x_{rm} \quad \text{(g)} \tag{4.28}$$

If the mass residual motion has a frequency of $f_s/4$, the equations can be approximated as in the equations (4.29) and (4.30).

$$x_{rm} = \frac{a_{max}}{\left(\frac{2\pi f_s}{4}\right)^2} \tag{4.29}$$

$$N_{rm} = \sqrt{\frac{4f_{BW}}{f_s}} \left(\frac{K}{m}\right) \frac{a_{max}}{(2\pi f_s/4)^2} \tag{4.30}$$

Hence, both decreasing maximum feedback acceleration and increasing the frequency of the readout circuit decreases the noise caused by the mass residual motion.

4.6. Conclusion

In this chapter, the design and simulations of the sigma-delta readout circuit and the performance limitations of the system are given. Table 4.5 gives the main parameters and the noise sources of the designed circuit with both the SOG and DWP accelerometers. The results show that mass residual motion and quantization noise dominating the noise sources. Hence, to decrease these noises, a higher sampling rate operation should be obtained, in order to increase the resolution of the system. Considering the case, new adaptive readout circuits are designed to increase sampling rates and achieving higher performance, which are explained in the following chapter.

Table 4.5: Readout circuit parameters and design achievements.

Parameter	**Value (with SOG)**	**Value (with DWP)**
Closed loop acceleration range	±4 g	± 19 g
Noise due to mass residual motion (1 kHz BW)	54 μg (1 kHz BW) 1.7 μg/√Hz	324 μg (1 kHz BW) 10.5 μg/√Hz
Quantization noise	10.3 μg/√Hz	48.9 μg/√Hz
Capacitance Sensitivity	0.3 – 5 V/pF	
Power consumption	16 mW	
Sampling rate	500 kHz	
Readout circuit noise	0.94 μV/√Hz	

CHAPTER 5

ADAPTIVE SIGMA DELTA READOUT CIRCUITS

To achieve higher performance in terms of resolution, the sigma-delta readout circuits need higher frequency operation, since most of the noise sources are dependent on the sampling frequency and decreases with the increasing frequency. However, increasing the sampling frequency of the readout circuit is not an easy process. To increase the sampling frequency, the speed of the circuit components should be increased, which is mostly limited by the used process. Another way of increasing the sampling frequency is to decrease the feedback duration of the sampling period, without decreasing the sense duration. However, decreasing the feedback time decreases maximum applicable feedback force, hence, decreases the operation range of the closed loop system.

To increase the sampling frequency, without decreasing the operation range of the readout circuit, two novel techniques are proposed and the readout circuits are designed and simulated. These readout circuits will be fabricated after this thesis study and the test results will be obtained. Therefore, only the design and the simulation results are discussed in this thesis. The readout circuits use adaptive techniques, where they change their operation state according to the rough magnitude of the input acceleration. This chapter presents the design and simulation results of these adaptive readout circuit designs. Section 5.1 presents the operation principle of the two readout circuits. Section 5.2 provides the explanation of some significant blocks of the readout circuits and gives the simulation results of these circuit blocks. Section 5.3 gives simulation results of the readout circuits. The complete simulations are performed in Matlab Simulink environment, and the operations of the readout circuits are verified. Section 5.4 gives the layouts of the

designed circuits. Finally, Section 5.5 gives a comparison of the designed circuits in terms of some noise components and the operation range, and concludes the chapter.

5.1. Operation Principle of the Readout Circuits

The readout circuits employ the sigma-delta structure, including a feedback mechanism, which improves the resolution and dynamic range of the system. The improvements are achieved by decreasing the mass residual motion and quantization noise. The main issue for decreasing the mass residual motion and quantization noise is increasing the readout sampling frequency. The limiting cases for achieving higher sampling frequency are the OTA speed, and the feedback duration needed to attain desired operation range. The OTA is designed to have best performance in order to have high speed, high current drive capability, low noise and low power. Hence, it has a feasible limit of speed, which prevents decreasing the readout time further. Another way of increasing the sampling rate is to decrease feedback duration. However, decreasing the feedback duration decreases the maximum average feedback force applied to the sensor. Therefore, the operation range is reduced. Figure 5.1 illustrates the increasing sampling frequency and decreasing feedback acceleration, with the change of feedback duration, and without changing the sense duration.

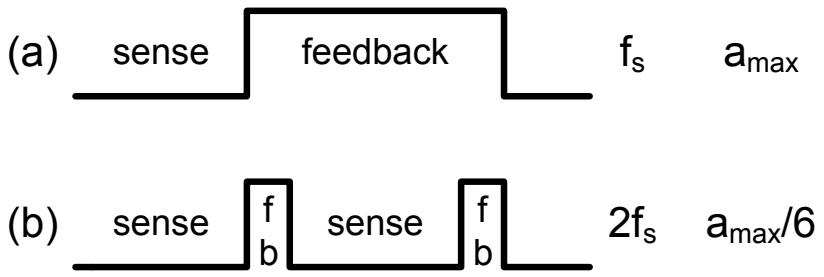


Figure 5.1. Illustration of the effect of decreasing feedback time. (a) with 60% feedback duration. (b) with 20% feedback duration.

5.1.1. Sigma-Delta Readout Circuit with Adaptive Feedback Duration

It is required to increase the sampling frequency without reducing the operation range. To achieve this, one method is to decrease the feedback duration for small input accelerations, and gradually increase the feedback duration according to the acceleration. In this way, the accelerometer system has high resolution for small accelerations and lower resolutions for higher acceleration ranges. Hence, both high resolution and high range is achieved, not at the same time but with the same system.

The circuit has almost the same operation with the second order sigma-delta system. However, it has variable feedback time, which is digitally controlled according to the input acceleration range. The circuit includes a digital control mechanism for applying feedback related with the magnitude of the input acceleration. The system has 15 different operation ranges, which is divided linearly. Range value is hold in a 4-bit register. If the range is 0, the circuit reads the position of the proof mass in the sense phase in 7 clock cycles and generates a feedback pulse and applies a positive or negative feedback accordingly to the sensor in 1 clock cycle duration. This generates a 12.5% of feedback duration, with a readout frequency of 2.5 MHz, if a 20MHz clock is used. At the maximum range, sense phase is again 7 clock cycles, and the feedback duration increases to 31 clock cycles. So, 82 % of the readout duration is spent for feedback and the readout frequency decreases to 513 kHz, with a 20 MHz clock frequency. Figure 5.2 illustrates the sense feedback timings for different operation ranges of the readout circuit.

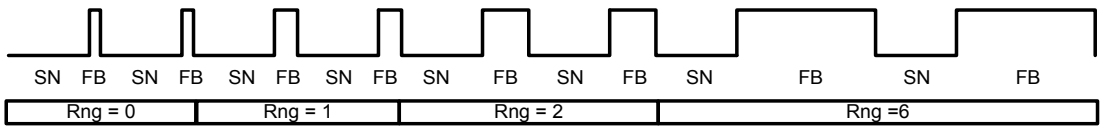


Figure 5.2. Illustration of the sense and feedback timings for different acceleration ranges, for the varying feedback-time readout circuit.

The feedback duration is increased if the range is positive, which means the input acceleration is positive. At the beginning, the proof mass makes a positive displacement, and a feedback force is applied in negative direction. However, when the proof mass passes over to the negative position with the feedback, the circuit does not enter to feedback phase after sense phase; but it enters to another sense phase without giving any feedback. The reason of not applying a feedback force on the other direction is to decrease the mass residual motion, since it is known that there is already acceleration, pulling the mass to the positive position. Hence, the proof mass is pulled back by the already existing external acceleration.

For determining the operation range, the digital output history of the circuit is examined. The feedback pulses for 128 clock periods are counted and an average value of acceleration is extracted from the data. If this acceleration value is not in the range of operation, the circuit changes state by changing the feedback time duration, and increases its acceleration range.

For counting the feedback force, a digital counter is used, and it counts at each clock cycle according to the feedback pulse. The counter counts for 128 clock cycles. If the clock frequency is applied as 20 MHz, this corresponds to 6.4 μsec. Since the maximum frequency of the applied acceleration is 500 Hz, in 6.4 μsec, the range of the system cannot change abruptly; so this duration does not create any problem.

5.1.2. Sigma-Delta Readout Circuit with Multi-bit Feedback

Another way of decreasing the feedback time, without decreasing the operation range is using separate electrodes in the sensor, to apply electrostatic feedback force. From the sense electrode, regular sigma-delta technique is applied, with short feedback time, and hence with high resolution, and the high acceleration range is guaranteed by applying multi-bit feedback from the feedback electrodes. Hence, the designed readout circuit uses a different kind of accelerometer sensor, which has 3 sets of electrodes, with a single proof mass, a basic illustration is given in Figure 5.3. One of these 3 sets of electrodes is used for reading the position of the proof

mass, and also applying feedback with short duration. With short feedback duration, high sampling frequency is achieved up to 2.5 MHz. This set of electrodes can be named as “sense electrodes”, even though they are both used for sensing and applying feedback.

The remaining 2 electrodes are used just for applying feedback force. The feedback force that will be applied from one set of electrode can take 3 values, positive, negative or no feedback force. When the electrodes of the accelerometer is arranged such that one set of feedback electrodes is twice the size of the other feedback electrode, 7 evenly distributed values of feedback force can be generated using only the feedback electrodes. If the feedback acceleration that can be generated by the smaller electrode is *a*, then the total feedback acceleration that can be applied from feedback electrodes ranges from +3*a* to -3*a*.

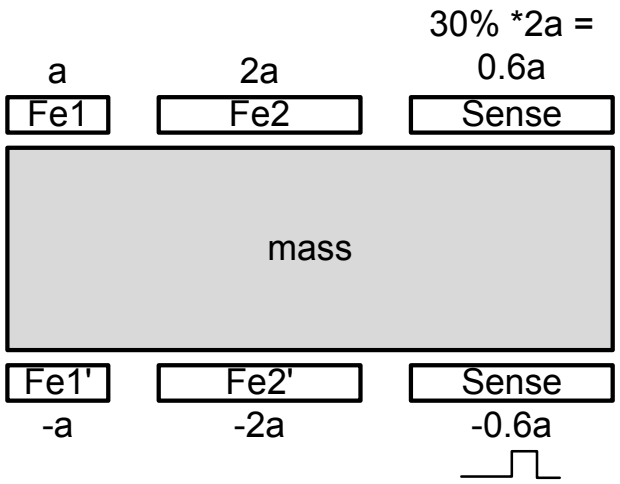


Figure 5.3. The structure of the accelerometer sensor, to be used with the multi-bit adaptive sigma-delta circuit structure.

For obtaining a suitable size for the sense electrodes, the average maximum feedback force that can be applied from the sense electrodes should be considered. To cover all values of acceleration, the maximum feedback acceleration from sense electrodes must be at least *a*/2. So, if the acceleration applied from the feedback electrodes is zero, the sigma-delta system constituted with the sense electrodes will

cover the range between +*a*/2 and -*a*/2. For instance, if a feedback acceleration of *a* is applied from feedback electrodes, then the operation range is changed to between +3*a*/2 and +*a*/2. Assuming the feedback duration is the 25% of the total sampling period, the feedback acceleration that can be applied is 25% of the full time feedback acceleration. Hence, to obtain a feedback acceleration of *a*/2, twice the size of smaller feedback electrode should be used, for the sense electrodes. However, for safe operation, the size of the sense electrodes should be selected larger than twice of the size of smaller feedback electrodes, or the feedback time should be a bit more than 25%. For this purpose, the feedback duration is chosen to be 30%. Hence, the accelerometer sensor can have electrode size ratios of 1:2:2.

After obtaining the sensor structure that can be used for the readout circuit, the basic principle of operation of the readout circuit should be explained. The block diagram of the readout circuit is given in Figure 5.4. The readout circuit uses the same sigma-delta structure, which is composed of a charge integrator, a compensator and a comparator. The charge integrator senses the capacitance difference of the sense electrodes, by transferring the charge difference created on the sensor capacitances to the integration capacitors. After passing from a lead compensator, the read value is entered to a comparator. Hence, according to the result of the comparator, either a positive or negative feedback is applied to the sense electrodes in the feedback time of the sampling period.

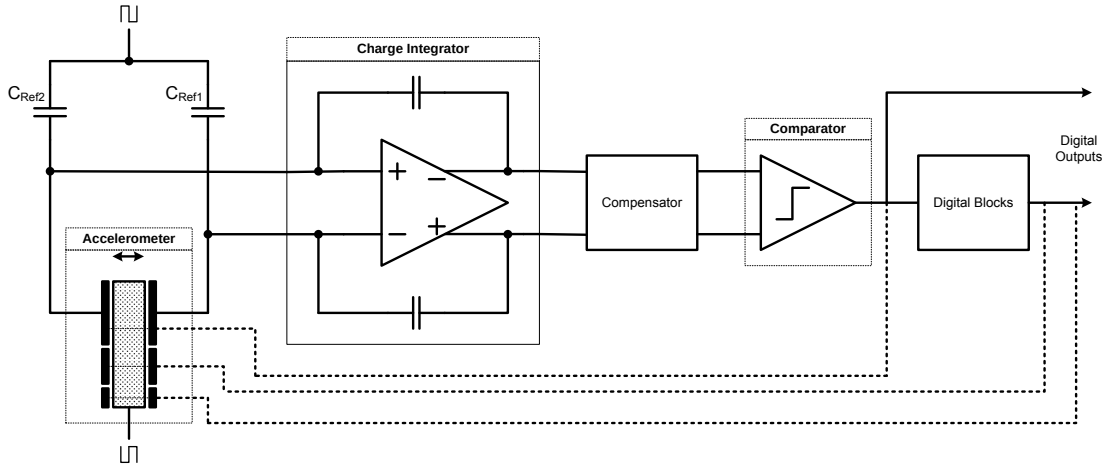


Figure 5.4. Block Diagram of the readout circuit.

For determining the feedback force to be applied from the feedback electrodes, a digital control block is used. This block counts the applied feedback to the sense electrodes in a period of 128 clock cycles, and if the applied feedback is exceeding a previously defined value, the system increases the applied feedback to the feedback electrodes.

5.2. Description of the Main Blocks of the Readout Circuit

This section describes the readout circuit blocks, which differentiate from the circuit blocks used in sigma-delta readout circuit designs explained in Chapter 4. There are mainly 4 blocks of the readout circuit, most of which are the same with the previous readout circuits. The OTA is improved in these readout circuits, having a better performance in terms of speed and noise, and using a different structure of Common Mode Feedback. The other component changed is the lead compensator circuit, which uses a different kind of capacitor switching mechanism. The main changes of the circuits are made structurally by timings or feedback control, which are controlled by the digital blocks of the readout circuit.

5.2.1. Operational Trans-conductance Amplifier (OTA)

The folded cascode fully differential OTA structure is used also in the adaptive readout circuits. A better design in terms of noise and speed is achieved. Also, the structure of the CMFB circuitry is changed, as shown in Figure 5.5. The sizes of the transistors used in the OTA circuit is given in Table 5.1.

For decreasing the flicker noise of the amplifier, the area of the transistors M5 and M6 are increased, while keeping the W/L ratio low, in order to keep the thermal noise of the circuit low.

The CMFB circuitry used in the previous designs, highly depend on the process parameters, and does not include a reference for setting the common mode voltage, which results in setting the common mode of the circuit to a value not exactly at the

mid-point voltage. The output nodes of the OTA are connected to the gates of the two transistors (M15, M16) of the CMFB circuit. These transistors are operated in deep triode region; hence, the sum of the drain currents of these transistors is proportional to the sum of the voltages at the output nodes of the OTA. With the diode connected PMOS transistor, the first stage of the CMFB circuit generates a voltage depending on the sum of the voltages at the output nodes of the OTA. This stage is replicated, with the inputs of the transistors are grounded. The replicated stage generates a reference voltage. Then, in the second stage, a diode loaded differential amplifier is used. Diode loaded structure is used to obtain wide bandwidth, low gain amplifier, and hence maintain the stability of the CMFB circuit. The output of the CMFB circuit biases the bottom NMOS transistors of the OTA, and hence keeps the output common mode very close to the reference voltage.

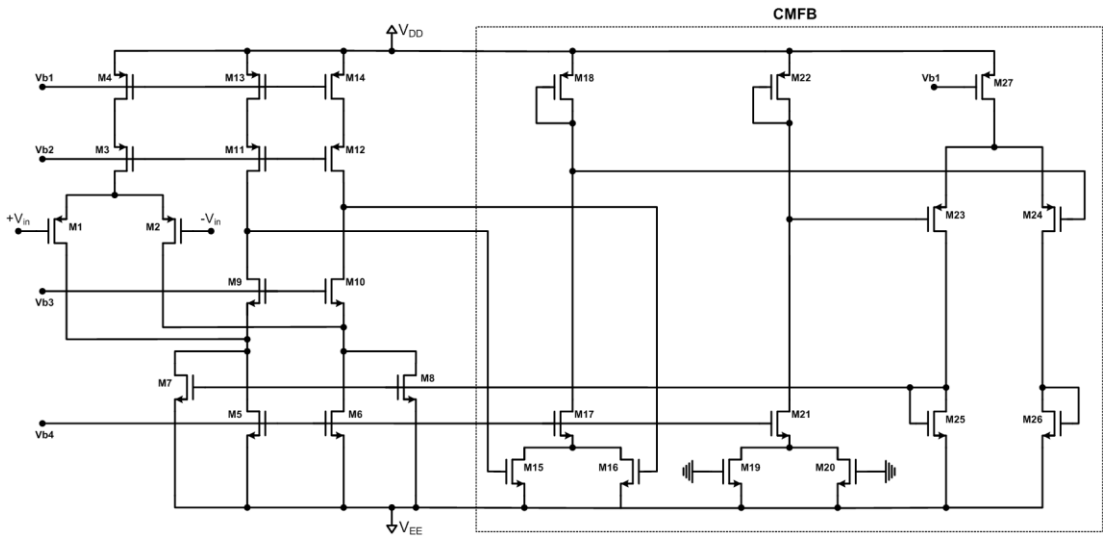


Figure 5.5. Schematic view of the folded cascode OTA.

AC simulation results of the amplifier are given in Figure 5.6. As seen in the simulation results, the bandwidth of the amplifier is narrow, but since the amplifier is operated in closed loop, the decrease of open-loop gain at higher frequencies is not significant. Instead, gain bandwidth product is an important parameter, in the design of the OTA.

Table 5.1: Size of the transistors used in the OTA circuit.

Transistor	W/L
M1, M2 (PMOS)	600 / 3 µm
M3 (PMOS)	400 / 3 µm
M4 (PMOS)	400 / 3 µm
M5, M6 (NMOS)	116 / 8 µm
M7, M8 (NMOS)	8 / 8 µm
M9, M10 (NMOS)	98 / 3 µm
M11, M12 (PMOS)	120 / 3 µm
M13, M14 (PMOS)	50 / 3 µm
M15, M16, M19, M20 (NMOS)	3 / 5 µm
M17, M21 (NMOS)	8 / 4 µm
M18, M22 (PMOS)	3 / 10 µm
M23, M24 (PMOS)	125 / 3 µm
M25, M26 (NMOS)	3 / 5 µm
M27	13 / 3 µm

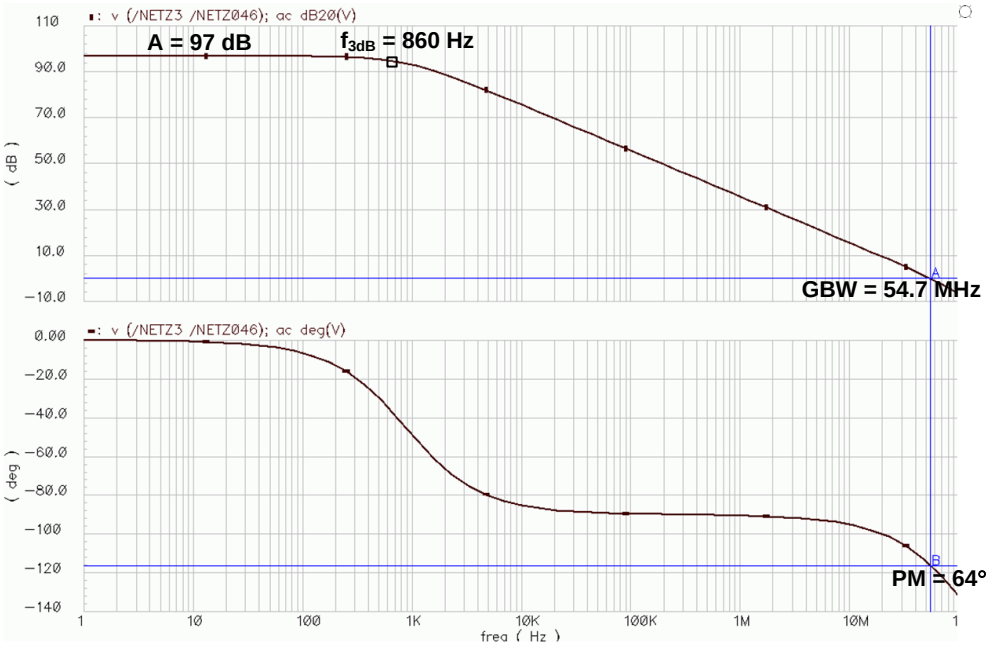


Figure 5.6. AC magnitude and phase response of the OTA.

Noise of the amplifier is another critical parameter of the OTA. The noise simulation result of the amplifier is given in Figure 5.7. The low frequency noise performance of the OTA is considerably improved in this design. The summary of the simulation results of the OTA is given in Table 5.2.

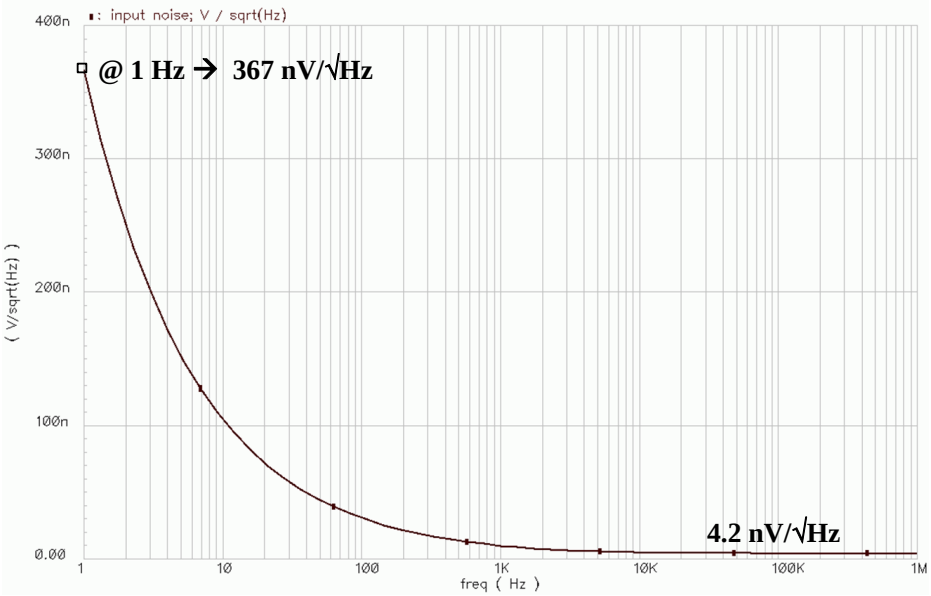


Figure 5.7. Simulation results for the input referred noise of OTA.

Table 5.2. Summary of the simulation results for the folded cascode amplifier.

Parameter	Value
Gain	97 dB
Bandwidth	860 Hz
GBW	54.7 MHz
Phase margin	64°
Power Dissipation	3.5 mW
Input referred noise (1 MHz BW)	4.2 nV/√Hz
Input referred noise (@ 1 Hz)	367 nV/√Hz

5.2.2. Lead Compensator

The schematic of the lead compensator structure is given in Figure 5.8. The compensator operates in 4 non-overlapping clock phases as shown in the timing diagram given in Figure 5.9.

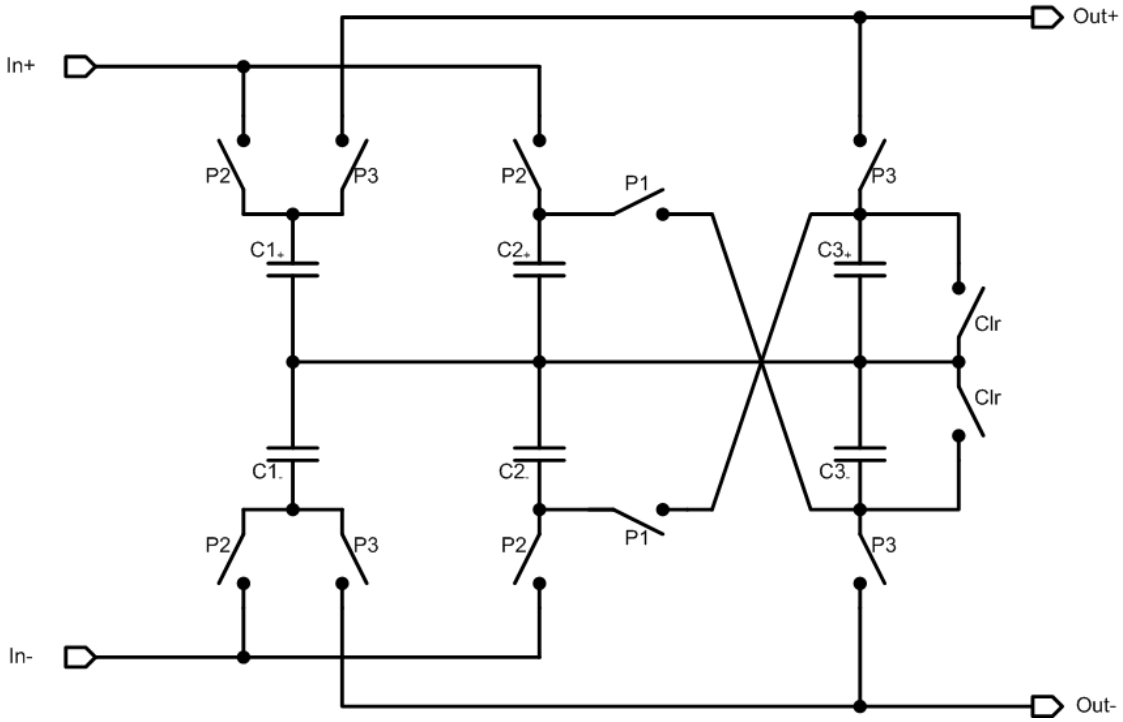


Figure 5.8: Schematic view of the lead compensator circuit.

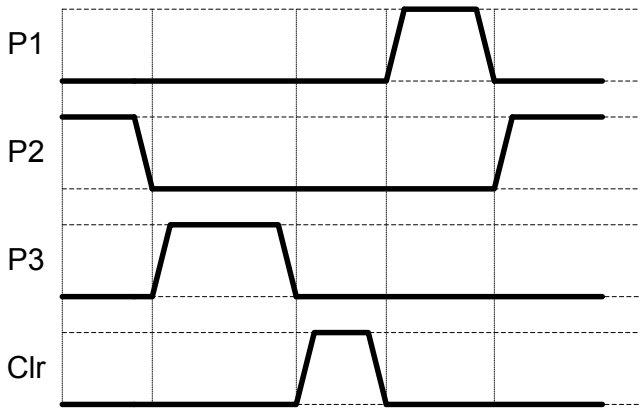


Figure 5.9: Compensator switching timing diagram.

Assume that 'P1' signal is at high state, and all other signals are at low state. Also, assume that C2 capacitors are charged with the previous value of the voltage read out by the charge integrator stage, named as V_{n-1}. Another assumption is that the C3 capacitors are discharged. In that case, with P1 switch closed, C2 and C3 capacitors

are paralleled inversely. After the charge sharing, the resultant voltage on C3 will be as given in Equation (5.1).

$$V_{C3} = -V_{n-1}\frac{C_2}{C_2 + C_3} \tag{5.1}$$

Next, in the 'P2' phase, C1 and C2 capacitors are charged to the output voltage of the charge integrator, V_n. Following this, in 'P3' phase, C1 and C3 capacitors are directly connected to the output and the compensator output is provided. After the output is provided, the C2 still stores the voltage. In 'Clr' phase, C3 capacitors are discharged. The cycle again starts from the 'P1' phase, C2 shares the charge with C3 and the cycle repeats.

The voltage resulting from the charge sharing of C1 and C3 in the 'P3' phase becomes as in Equation (5.2).

$$V_o = \frac{C_3\left[V_n C_1 - V_{n-1}\left(\frac{C_2}{C_2 + C_3}\right)\right]}{C_1 + C_3} \tag{5.2}$$

If all the capacitors are selected to be 1 pF, which is the case used in the readout circuit, the output becomes as in Equation (5.3). The equation (5.4) is the z-domain representation of this expression.

$$V_o = \frac{2V_n - V_{n-1}}{4} \tag{5.3}$$

$$V_o(z) = \frac{2 - z^{-1}}{4} \tag{5.4}$$

5.2.3. Digital Blocks

Digital blocks for the readout circuits mainly consist of a ring oscillator, a digital control and a multiphase clock generator circuits as shown in Figure 5.10. The ring oscillator generates a 20 MHz clock signal needed for the operation of circuit. The clock signal can also be supplied from an external source. The digital control circuit controls the feedback and sense timings, the operation range of the readout circuit, and counts the feedback pulses and gives to the output. Multiphase clock generator block provides clock signals for all the switches used in the readout circuit.

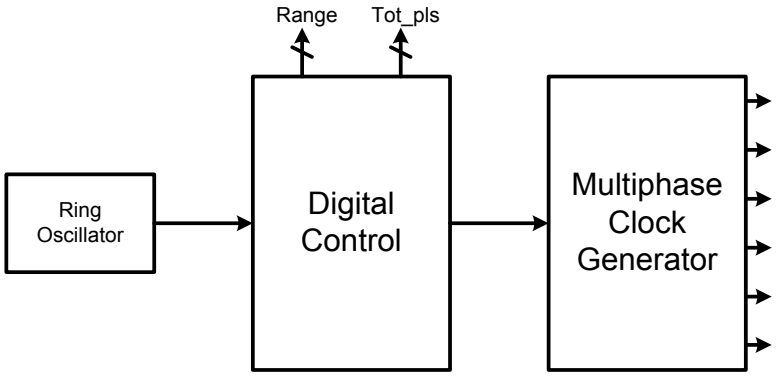


Figure 5.10: Block diagram of the digital part of the readout circuit.

The digital blocks of the readout circuit consists of two parts. One of those parts is for generating the multiphase timing signals, which are needed in various parts of the circuit. The other part is for controlling the feedback mechanism, and generating the necessary feedback signals.

5.2.3.1. Timing Signal Generation

The sense phase of the both readout circuits are completed in seven clock cycles. For the readout circuit with adaptive feedback duration, the feedback time depends on the operating range value, hence on the input acceleration value. For this circuit, the feedback duration can vary from 1 clock cycle to 31 clock cycles. For the multi-

bit readout structure, the duration of the feedback cycle is selected externally from the digital *rng<0:1>* inputs. The feedback duration can take values of 1, 3, 7 and 17 clock cycles, which corresponds to 12, 30, 50 and 71 percent of feedback durations. These timings are controlled by using a counter, and other sequential and combinational logic circuitry.

There are various timing signals used in different parts of the readout circuit. For generating these signals, initially, three major timing signals, ϕ_1, ϕ_2, ϕ_3 are generated. These timing signals are high for one clock cycle period, during the sense phase, as shown in the timing diagram in Figure 5.11. After generating these three signals, they are given to inverters as delay elements; hence, the delayed versions of the signals are generated. After obtaining these, for each timing signal needed in the circuit, RS latch circuit is used, where the set and reset times of the latches are defined by the three major signals and their delayed versions.

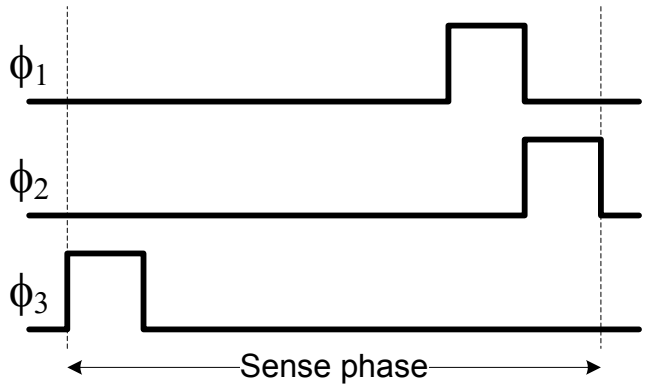


Figure 5.11: Timing diagram of generated major timing signals.

5.2.3.2. Digital Control Circuit

For the multi-bit readout structure, the digital control circuit is used for both defining the sense and feedback phases, by a counter, and averaging the output bit-stream in a defined period. The averaging is used for determining the feedback to be applied to the sensor. For averaging, a signed magnitude counter is used, which

is reset in each 128 clock cycles. If the feedback is in negative direction, the counter counts -1, and for positive feedback, it counts +1. When the readout circuit is in sense phase, the counter does not count. Hence, at the end of this 128 clock cycles, an average output value is generated. This value is compared with a previously defined value, and if it is higher than that value, an additional feedback is applied from the additional electrodes of the sensor. The feedback duration of the circuit can be set to 4 different values, and for each feedback ratio the compared value of counted feedback pulse changes accordingly, as shown Table 5.3. As seen, when the output value reaches around 85% of the maximum feedback time value, additional feedback is applied to the sensor.

Table 5.3: Feedback duration ratios and the compared values of the readout circuit.

Feedback ratio	**Feedback ratio (%)**	**Compared value of counted pulse**	**Compared value (%)**	**Compared value / feedback ratio**
1/8	12.5 %	14/128	10.9 %	87.2 %
3/10	30 %	32/128	25 %	83.3 %
7/14	50 %	51/128	39.8 %	79.6 %
17/24	70.8 %	78/128	60.9 %	86.0 %

When the electrode ratio of the accelerometer sensor is 1:2:2, where the last 2 stands for the sense electrodes, the input acceleration coverage can be illustrated as given in Figure 5.12.

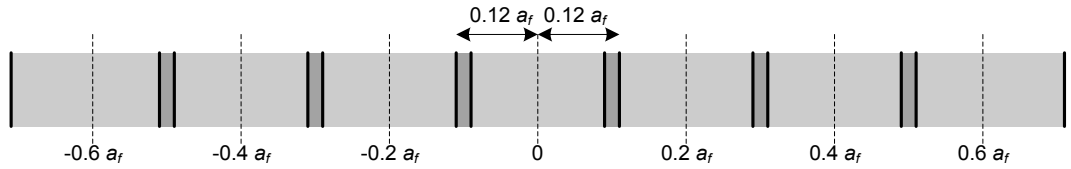


Figure 5.12: Illustration of the input acceleration coverage according to different operation ranges.

5.3. Simulation Results Using Matlab Simulink

Matlab simulations for the circuit with adaptive feedback duration are performed using the same models of the previous sigma-delta readout circuits, which are given in Chapter 3 of the thesis. The feedback duration and timings of the model is changed for different input accelerations and the simulations of the circuit are performed.

The simulation results of the circuit are performed using Matlab Simulink model of the circuit for observing the system operation. The Simulink model of the circuit is given in Figure 5.13. The model uses accelerometer as a second order transfer function. The input is applied in the form of acceleration and at the output of the accelerometer proof-mass displacement value is obtained and converted to capacitance. Then, the readout circuit block converts the capacitance to voltage, which includes the readout gain, saturation voltages and the timings of the readout circuit. After passing from the compensator stage, the signal is entered to the comparator stage. At the feedback part of the model, there are three different blocks, for applying feedback from three different electrodes. First feedback block applies feedback in a time-multiplexed fashion according to the comparator output of the circuit. The other blocks apply constant voltages to the electrodes, which are used when high value of acceleration is applied to input. Basically, additional feedback blocks generate offset feedback acceleration.

Two different simulations are performed with the simulink model. First, zero acceleration is applied and the mass residual motion of the system is observed, as shown in Figure 5.14. With an applied input acceleration of 1 micro-g the rms value of mass residual motion becomes 7 picometers.

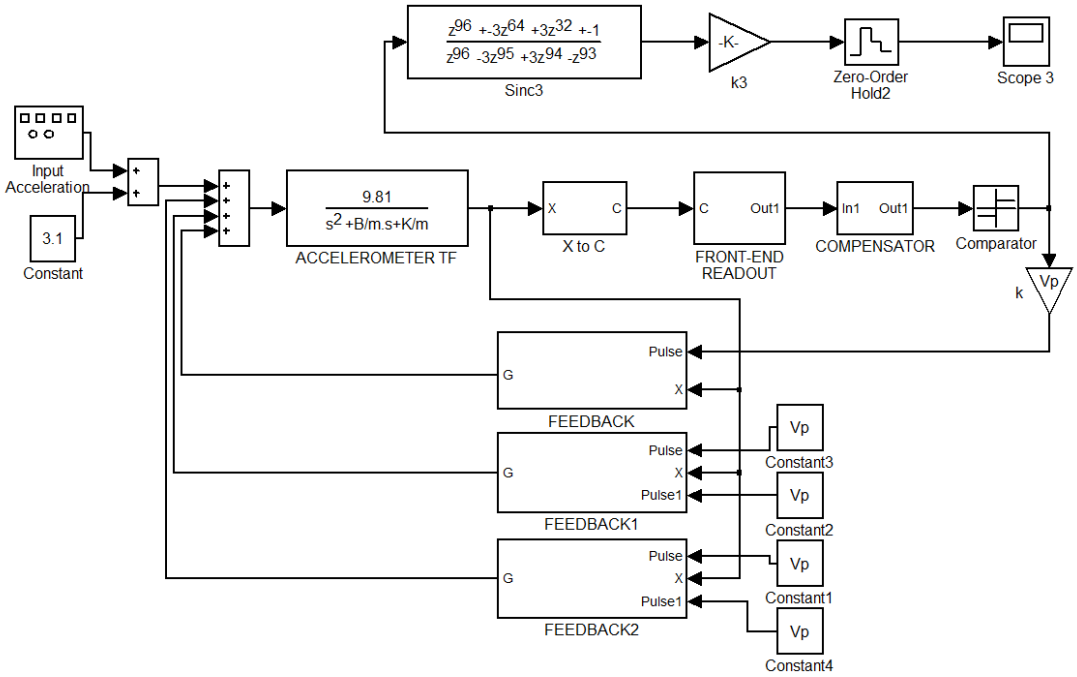


Figure 5.13. Simulink model of the accelerometer system.

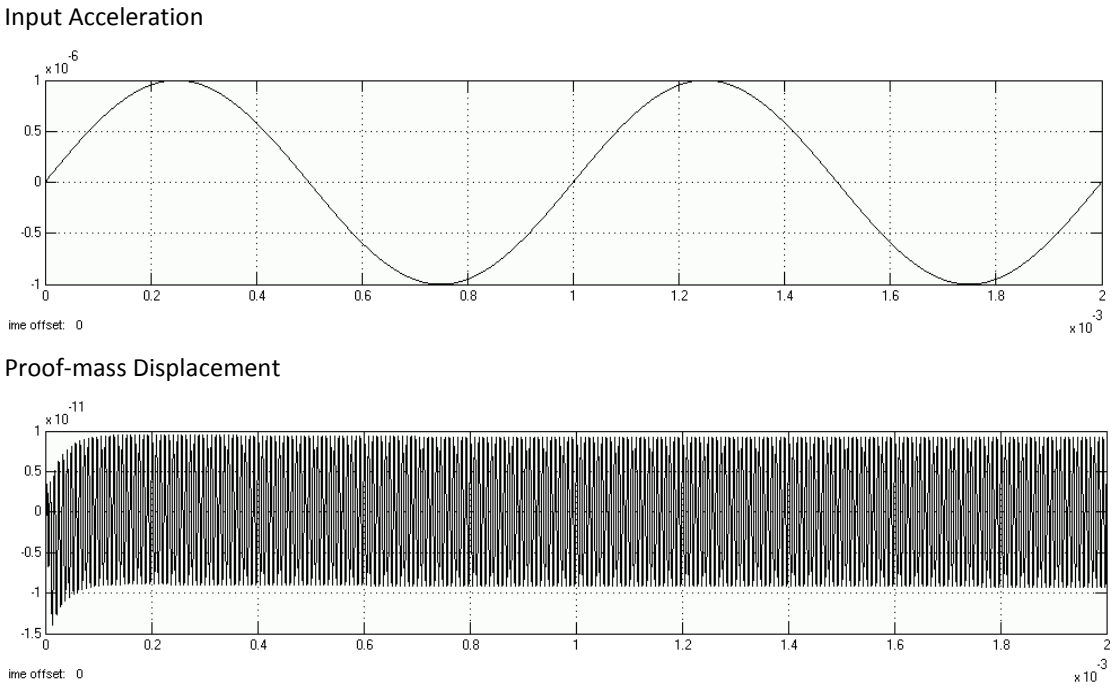


Figure 5.14. Simulink simulation results for observing mass-residual motion.

Another simulation is performed with 0.4 g peak input acceleration. The results are shown in Figure 5.15. It is observed that the average value of the output bit stream changes according to the input acceleration value.

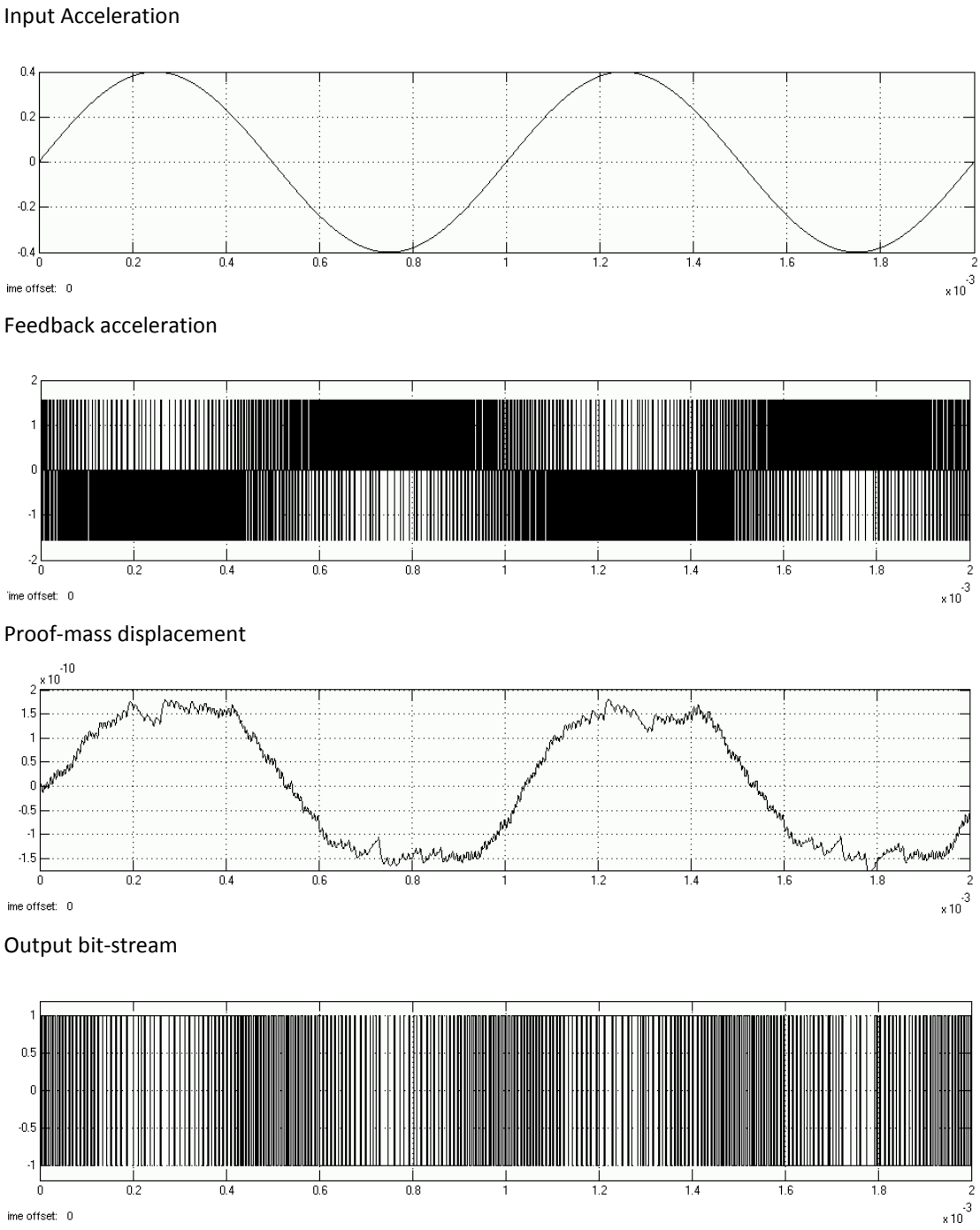


Figure 5.15. Simulink simulation results of the readout circuit.

5.4. Layouts

Figure 5.16 (a) and Figure 5.16 (b) give the layouts of the adaptive readout circuits with varying feedback time and with multi-bit feedback, respectively. Both of the readout circuits are designed with XFab 0.6µm 2 metal – 2 poly CMOS process. The total area of each chip is 2440 x 1180 μm^2 including the pads. The pin descriptions of the readout circuits are given in Appendix B.

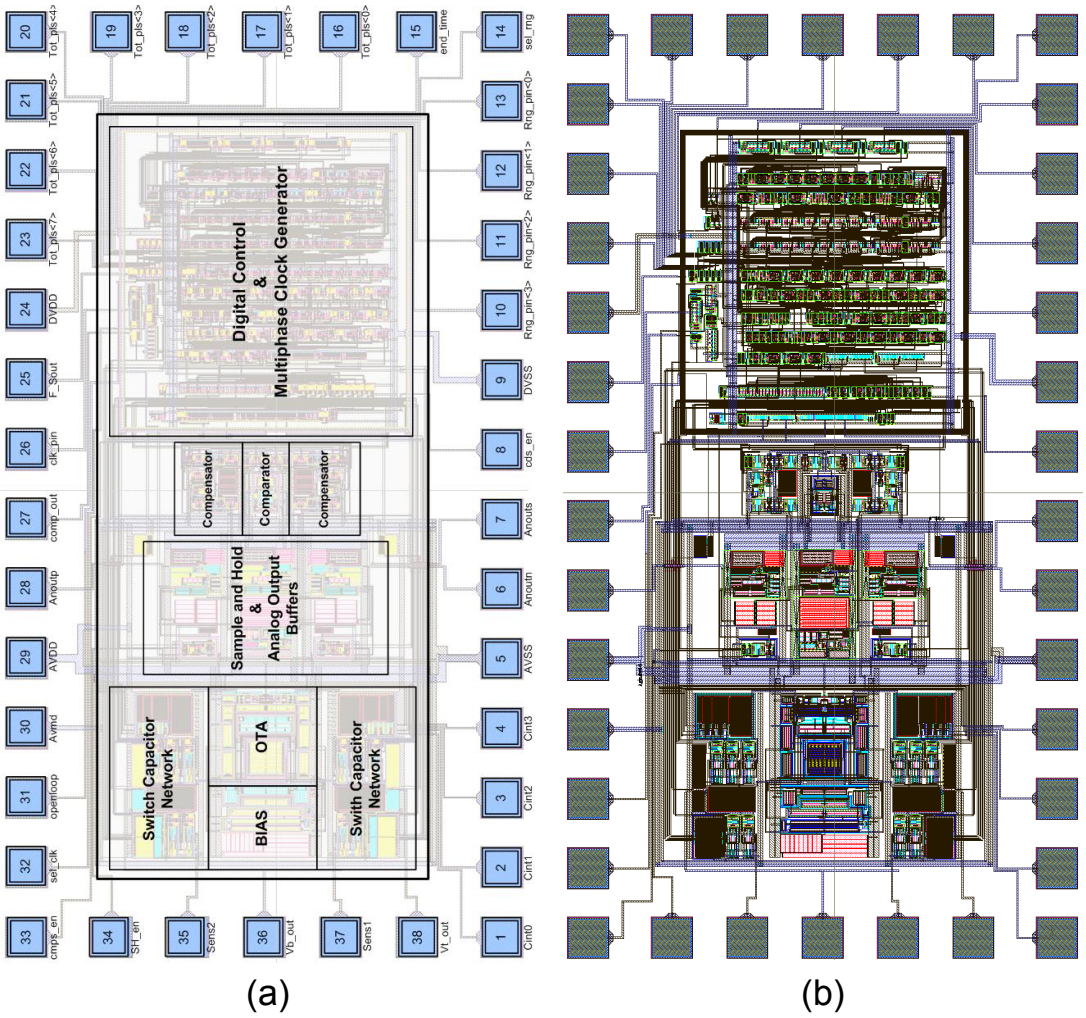


Figure 5.16: Layout of the adaptive readout circuits with (a) varying feedback time, (b) multi-bit feedback.

5.5. Comparison of Readout Circuits and Conclusion

There are 3 different versions of sigma-delta readout circuits designed. First design has a classical sigma-delta readout circuit structure, where feedback duration ratio is 0.6, and a sampling frequency of 500 kHz.

The second design is an adaptive sigma-delta structure, which changes the feedback duration according to the input acceleration value. If the input acceleration is around zero, the feedback duration is kept shortest. Because of the sense phase is constant, decreasing the feedback duration results in increasing sampling frequency. Hence, maximum acceleration is decreased and sampling frequency is increased, which both results in decreasing the mass residual motion and quantization noise. For also obtaining wide operation range, when the input acceleration value is increased, the feedback duration is increased. This results in having higher noise as the input acceleration is increased. For zero input acceleration, the sampling frequency is increased to 2.5 MHz, while the feedback duration ratio is 0.125. For the maximum acceleration value, feedback duration ratio increases to 0.82, and the sampling frequency is decreased down to 513 kHz.

The last design also employs low feedback duration ratio, but achieves the desired input acceleration range by applying feedback from separate electrodes. The feedback duration ratio is selectable in this circuit, and designed to operate best for the feedback duration ratio of 0.3. In this case, since feedback is applied from the 40% of the electrode, a_{max} is decreased down to $0.12a_f$. However, the maximum acceleration that can be applied to the sensor as feedback can be found by adding the feedback acceleration supplied from feedback electrodes and the a_{max}, which is the maximum acceleration value at the sense electrodes. Hence, $0.72a_f$ is obtained as the input acceleration range. In the case of this circuit, there is no increase in the noise while increasing the range of the system. The sampling frequency of this circuit is 2 MHz when operated with 0.3 feedback duration ratio.

A comparison of the noises of these three circuits is given in Table 5.4 and Table 5.5. Here, a sample accelerometer sensor is selected, and all the calculations are made according to that sensor.

Table 5.4: Comparison of Sigma-Delta readout circuit in terms of quantization noise and mass residual motion.

Calculated according to SOG Accelerometers **M = 0.719e-6 kg, K = 67**		**Sampling Frequency f_s**	**Quantization Noise** $\frac{a_{max}}{\sqrt{15}}\frac{\pi^2}{M^{2.5}}$	$\frac{a_{max}}{\left(\frac{2\pi f_s}{4}\right)^2}$	N_{rm} **(1kHz BW)** $\sqrt{\frac{4f_{BW}}{f_s}}\left(\frac{K}{m}\right)x_{rm}$	**Linear Range**
S-D Readout Circuit		500 kHz	10.3 µg	0.636 Å	54 µg	± 4g
S-D with feedback pulse width modulation	**0 g**	2.5 MHz	0.185 µg	0.0045Å	0.171 µg	± 5.3g
	High g	513 kHz	9.67 µg	0.805 Å	67.5 µg	
S-D with multi-bit feedback		2.0 MHz	0.11 µg	0.0051 Å	0.194 µg	± 4.7g

Table 5.5: Comparison of Sigma-Delta readout circuit in terms of noise sources.

Calculated according to SOG Accelerometers **M = 0.719e-6 kg, K = 67**		**Quantization & Mass Residual Motion Noise**	**Mechanical Noise**	**Readout Circuit Noise**	**Expected Total Noise**
S-D Readout Circuit		55 µg/√Hz	2.81 µg/√Hz	1.22 µg/√Hz	55 µg/√Hz
S-D with feedback pulse width modulation	**0 g**	0.252 µg/√Hz	2.81 µg/√Hz	0.55 µg/√Hz	2.87 µg/√Hz
	High g	68.2 µg/√Hz	2.81 µg/√Hz	1.22 µg/√Hz	68 µg/√Hz
S-D with multi-bit feedback		0.223 µg/√Hz	2.81 µg/√Hz	0.61 µg/√Hz	2.87 µg/√Hz

The next chapter gives the implementation and test results of the regular sigma-delta readout circuit, which were explained in Chapter 4.

CHAPTER 6

IMPLEMENTATION AND TESTS

This chapter presents the implementation of the readout circuits and the test results of the system. There are 2 chips implemented and tested, both of which are sigma-delta type fully differential readout circuits. With the second readout chip, the performance of the circuit is improved, and a compensator circuit is included. Section 6.1 of this chapter shows the implementation of the readout circuits together with the accelerometer sensors, and describes the implemented external electronics, used for filtering and decimating the output signal. Section 6.2 gives the open loop test results of the readout circuit, which includes linearity, sensitivity and noise tests with and without the accelerometer. Section 6.3 gives the closed loop test results. Closed loop tests include linearity and sensitivity of the accelerometer system, dynamic response, high acceleration tests, noise and temperature tests.

6.1. Implementation of the Readout Circuit

The first readout circuit is designed and implemented using XFAB 0.6μm, two metal, two poly CMOS process. The photo of the chip is given in Figure 3.2. The readout chip has 38 pads, with total dimensions of 2440x1180μm^2. A test structure of some analog blocks of the readout circuit is also implemented separately, which is placed inside the area of the readout circuit, as seen in Figure 3.2. The chip is bonded to a 44 pin smd package. A PCB is designed and manufactured, as shown in Figure 6.2 and the package is soldered on the PCB. The accelerometer is also bonded on the PCB, so that it is placed near the readout circuit as much as possible. In this way, parasitic capacitances at the sense nodes are kept low.

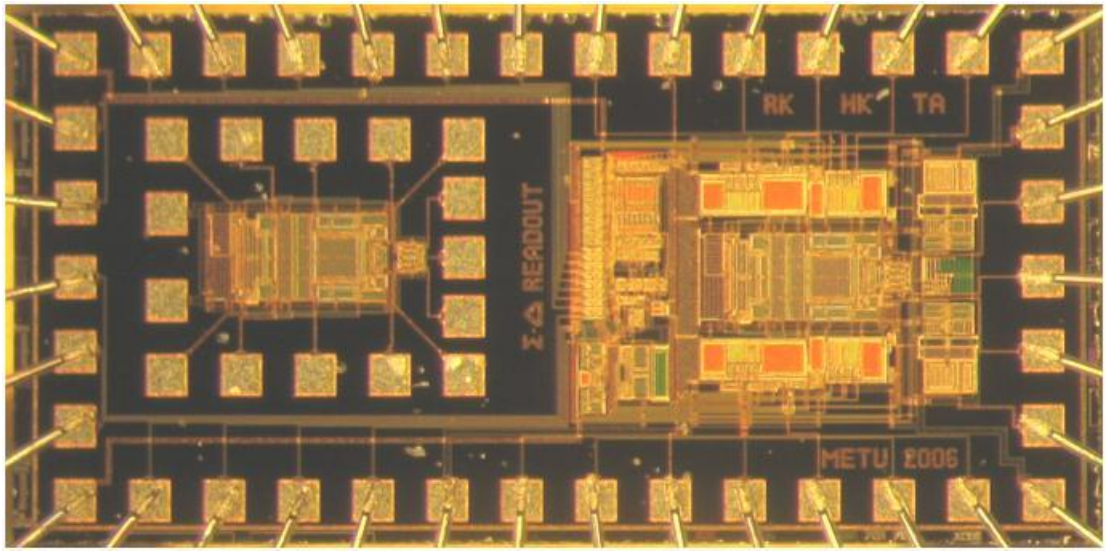


Figure 6.1: Photo of fully differential sigma-delta capacitive accelerometer readout circuit.

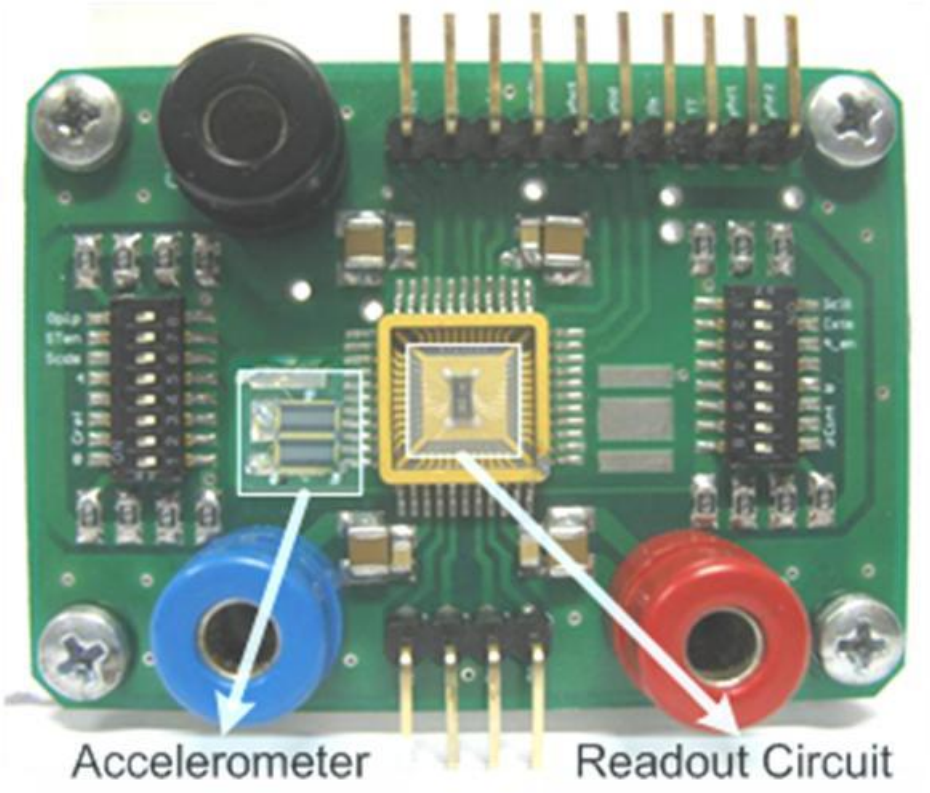


Figure 6.2: Printed Circuit Board used for the tests of the readout circuit and the accelerometer.

A better way is to wire-bond the accelerometer inside the same package with the readout circuit. Hence, in the later times of this research, the second readout chip and accelerometer is placed in the same package. The photograph of the second readout chip is shown in Figure 6.3, which has 29 pads and has dimensions of 1180x1120μm^2. An alumina substrate PCB is implemented and placed in the package, as shown in Figure 6.4. Using this package, which isolates the system from the electromagnetic noise sources with the metal covering, minimizes the parasitic capacitances and impedance in between readout circuit and accelerometer. This package is mounted on a PCB as shown in Figure 6.5. This PCB includes the filtering and decimation circuitry. Hence, the closed loop tests are mostly performed using this PCB. The open loop and closed loop tests performed are given in the next sections separately.

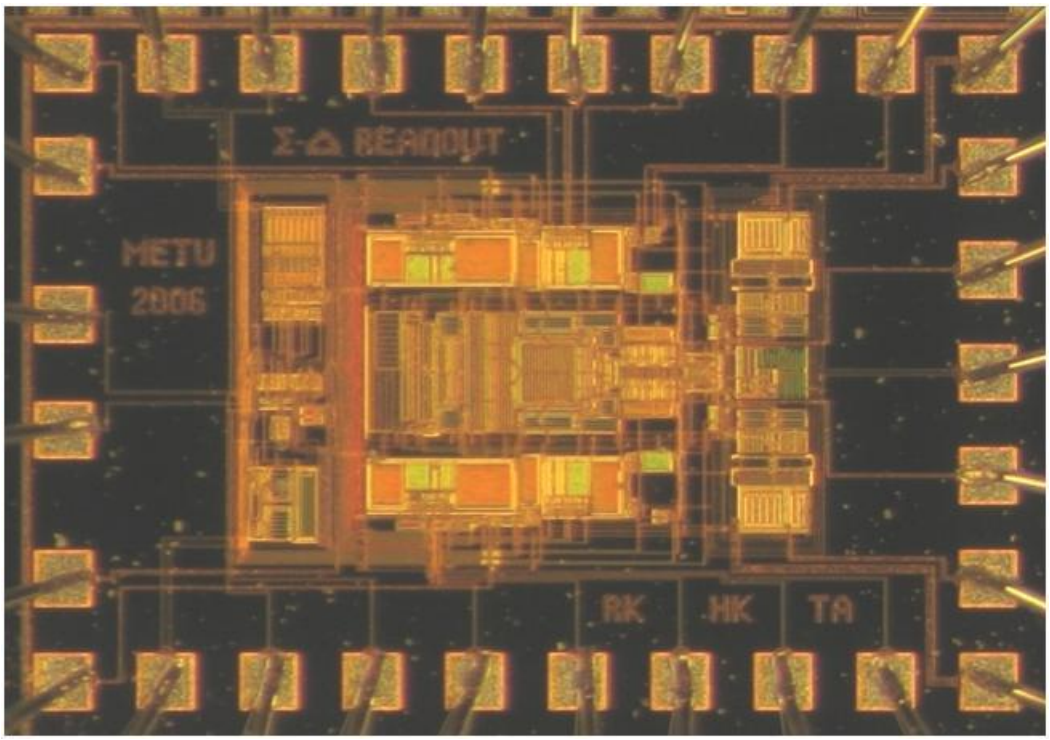


Figure 6.3: Photograph of the second readout chip.

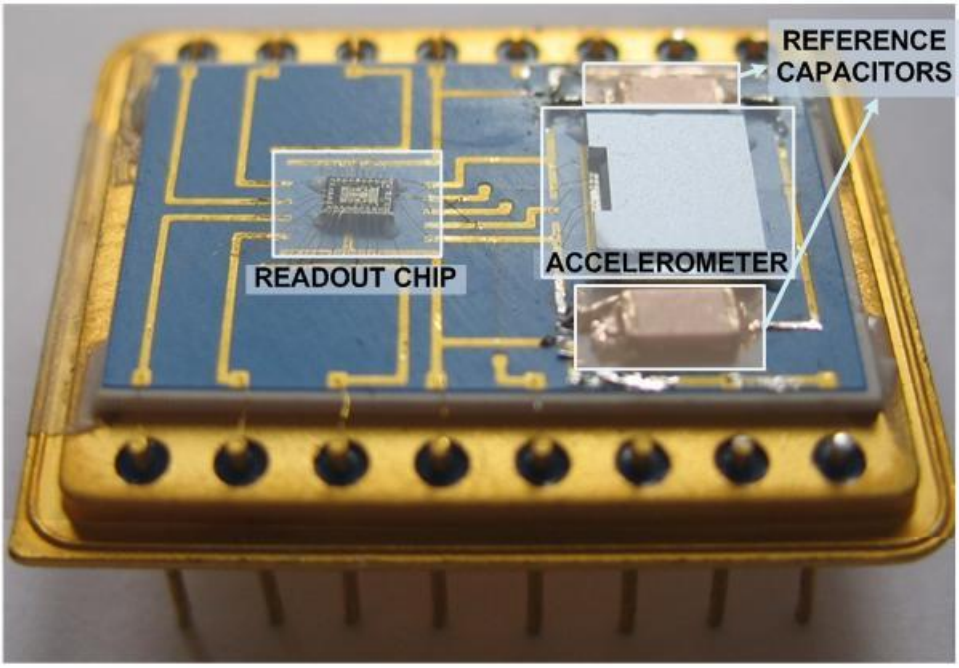


Figure 6.4: The accelerometer and the readout circuit wire-bonded in the same package, using an alumina substrate PCB.

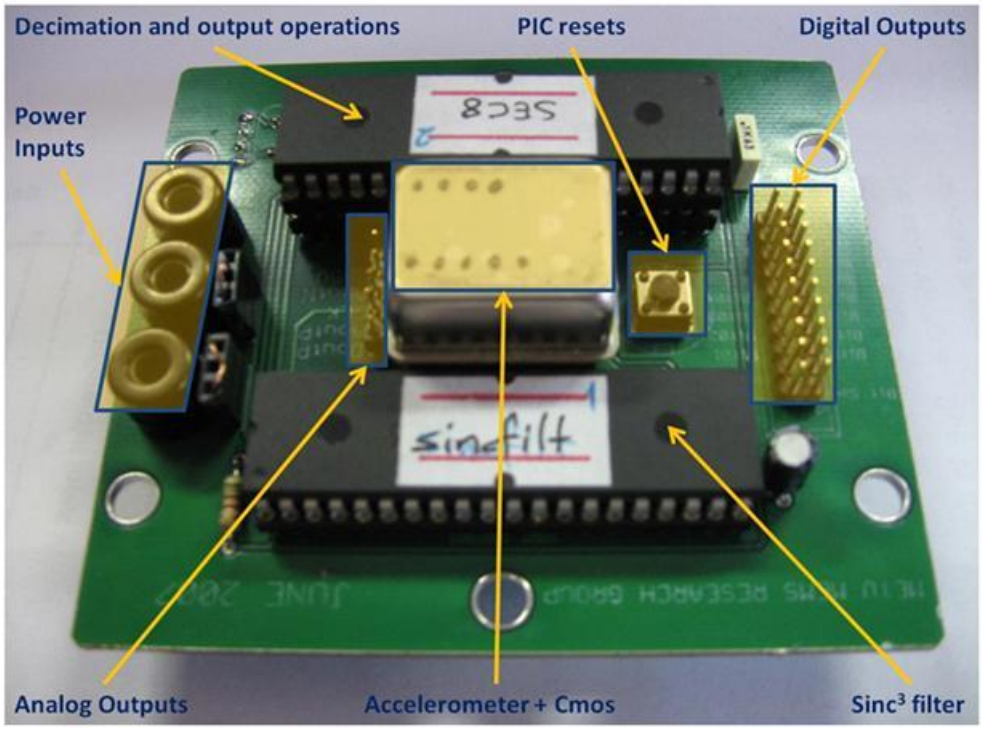


Figure 6.5: Accelerometer system together with the external filtering and decimation circuitry, placed on a PCB.

6.2. Open Loop Test Results

For checking the functionality of the readout circuit, open loop tests are performed initially. The open loop tests include the tests with and without the accelerometer sensor.

6.2.1. Sensitivity of the Readout Circuit

First test is performed without the accelerometer, where input capacitive full-bridge structure is constructed using 4 external capacitors. Then the differential analog output of the circuit is observed. In this test, since the capacitor values have some tolerances around 10%, first, value of each capacitor is measured using an impedance analyzer. Then, by using various capacitor values, several data points are collected. Test are performed with 4pF and 8pF integration capacitors. The results of the test are shown in Figure 6.6, which give the capacitance to voltage sensitivity of the readout circuit. The theoretical sensitivities are 0.625V/pF and 1.25V/pF for 8pF and 4pF integration capacitors, respectively. The experimental results show 1.16 V/pF and 0.54 V/pF sensitivities as seen in Figure 6.6.

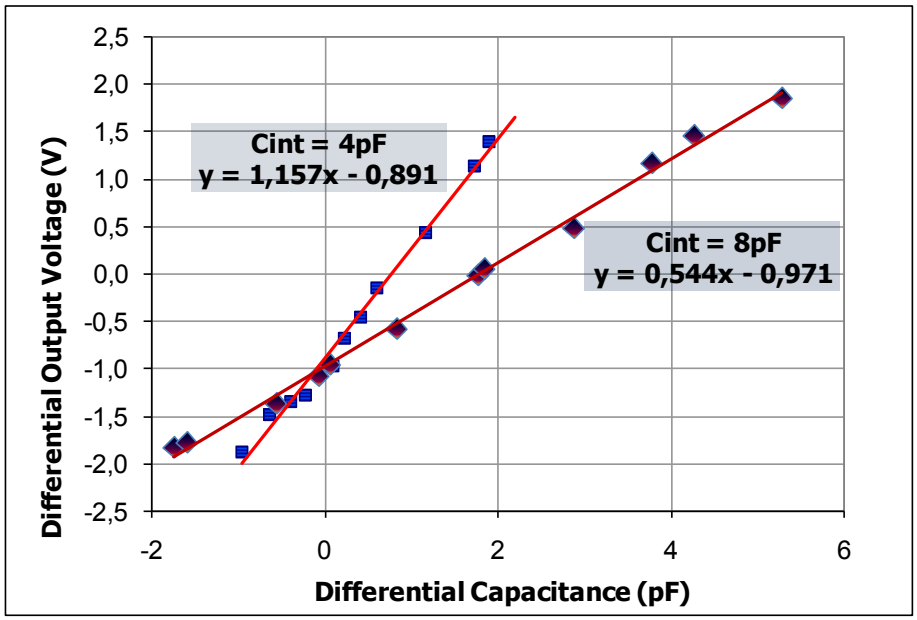


Figure 6.6: Sensitivity test results of the readout circuit.

As it is observed from the graph, there is an offset and non-linearity on the data. These errors are mostly caused by the parasitic capacitances of the test environment. Another reason of this non-linearity is the changing scale factor, because of the changing total capacitance, while trying to change the differential value of the capacitors. The dependence of the scale factor on the full-bridge capacitor values was given in Chapter 3.

Another test is performed for observing the dependence of differential output voltage to the integration capacitors, while there is a constant input capacitance difference. The results of the test are shown in Figure 6.7. The test is performed for two different input capacitance differences, in opposite signs. In the graph, the x-axis show the inverse of the integration capacitor value. Theoretically, the output voltage is linearly dependent on the inverse of integration capacitors. The results of this test show the linear dependence of the output differential voltage. However, it is observed that the output voltage starts saturating at the differential output voltage of around ±1.2 V.

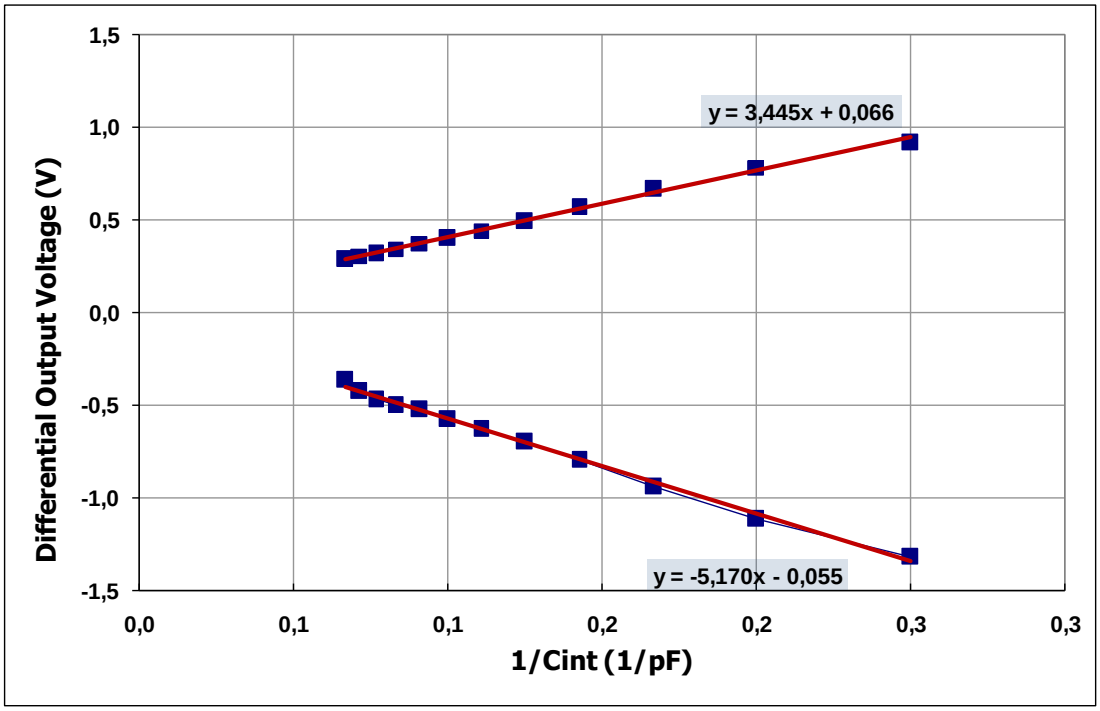


Figure 6.7: Differential output voltage versus inverse of the integration capacitance.

6.2.2. Sensitivity of the System Using Accelerometer

For observing the operation and sensitivity of the readout circuit with the accelerometer, an SOG type accelerometer is bonded to the PCB. The parameters of the accelerometer used were given in Table 1.2 in Chapter 1. The system is placed on a rotating head, and accelerations in the range of -1g and +1g is applied by changing the angle of the accelerometer according to the gravitational acceleration. The differential output of the circuit is measured using a multimeter. The test is repeated using different integration capacitor values. By collecting the data at various angles, with different integration capacitor values, the test results shown in Figure 6.8 is obtained. The test result show high linearity on acceleration in the differential output range of -0.8V and +0.8V. The sensitivity of the system reaches up to 4.37 V/g.

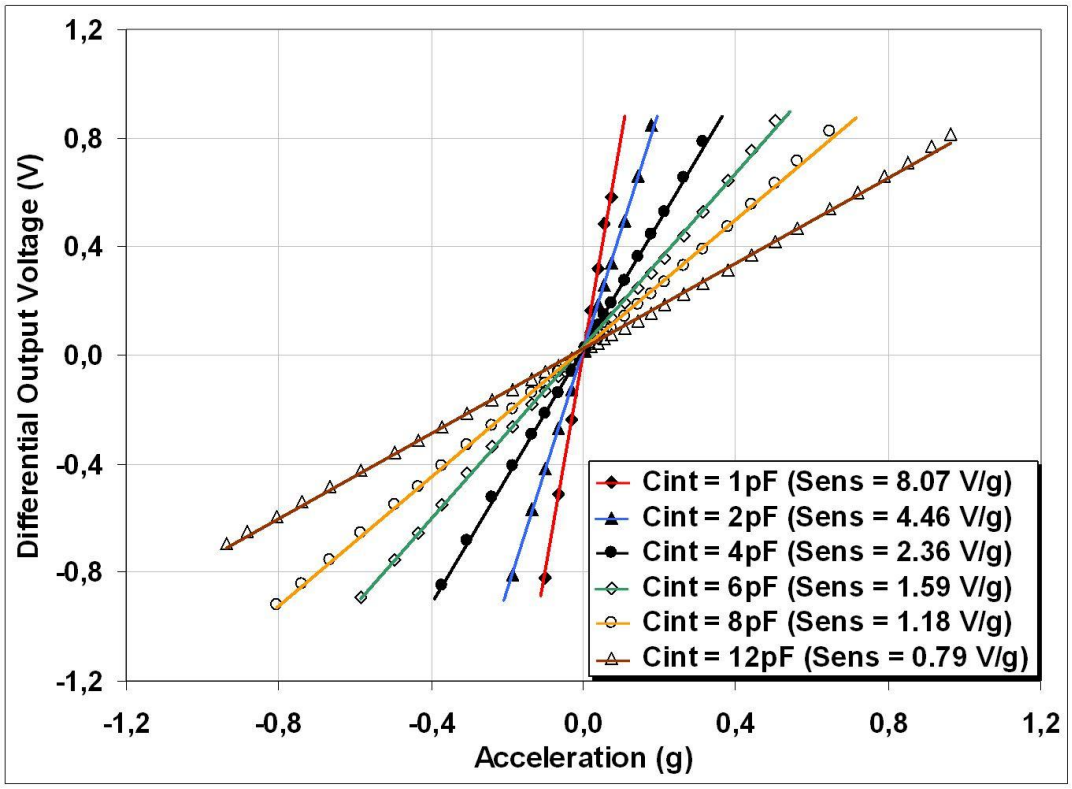


Figure 6.8: Open loop sensitivity tests of the readout circuit together with the accelerometer.

6.2.3. Noise Tests

The noise tests of the circuit alone by itself and with the accelerometer are performed separately. The open loop noise tests with the accelerometer are performed using the same SOG accelerometer used in open loop sensitivity tests. The noise test setup is shown in Figure 6.9. For measuring the noise of the circuit, the readout circuit and the external circuitry for measuring noise is placed in a metal box, to prevent any electromagnetic interference on the circuits. The noise measurement is performed using "Agilent 35670A Dynamic Signal Analyzer"

The block diagram of the external circuitry used for noise measurements are also shown in Figure 6.9. With this circuit, the differential output is converted into single-ended output using a difference amplifier. Then, the signal is low pass filtered using a second order low pass filter, and the noise signal is amplified using a low noise amplifier structure. The output of the last stage amplifier is connected to the Dynamic Signal Analyzer through a coaxial cable. Batteries are used as the power supply of the circuitry in order to eliminate the supply noise.

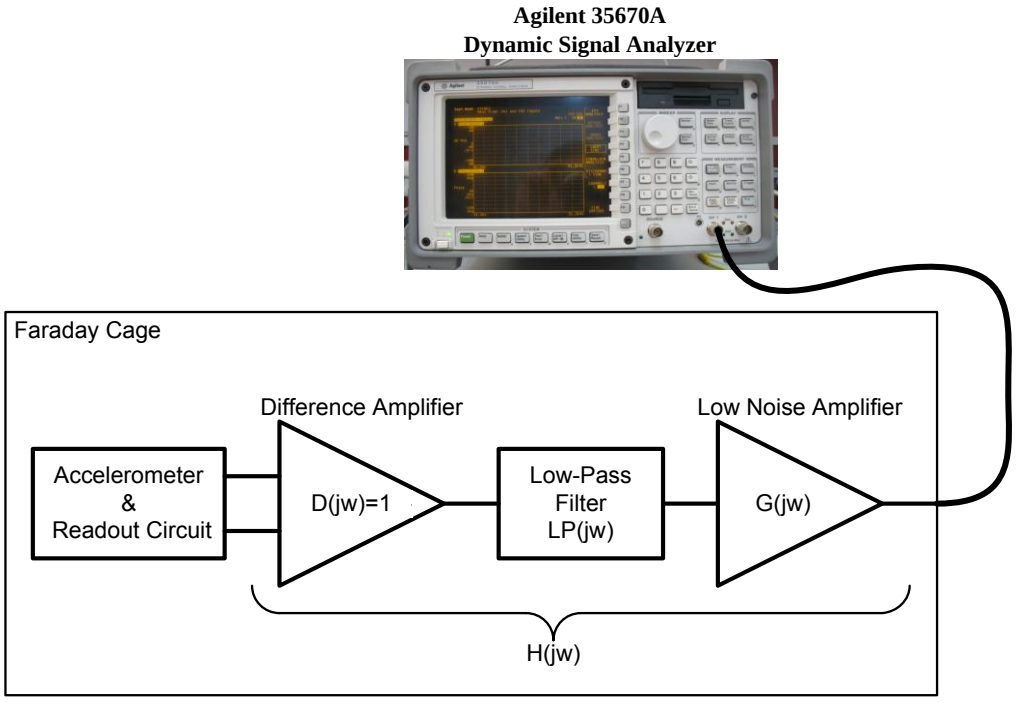
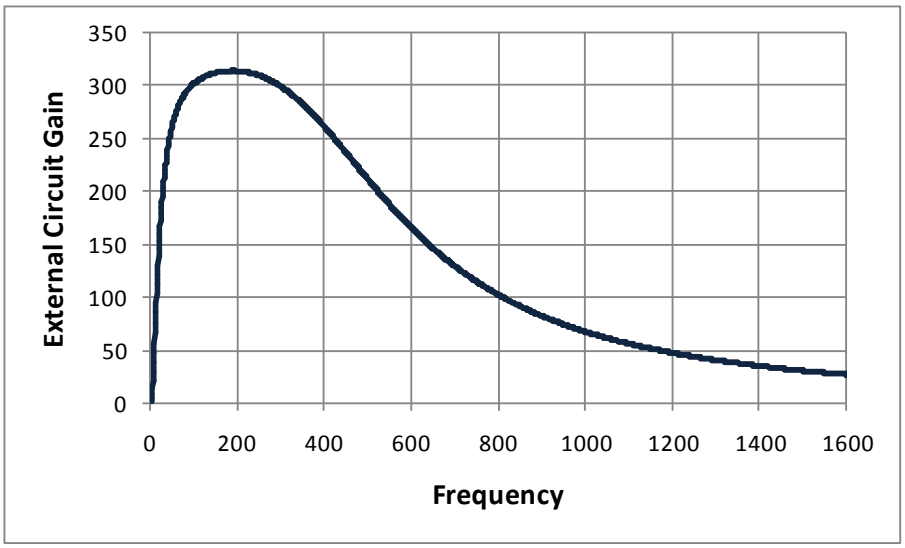
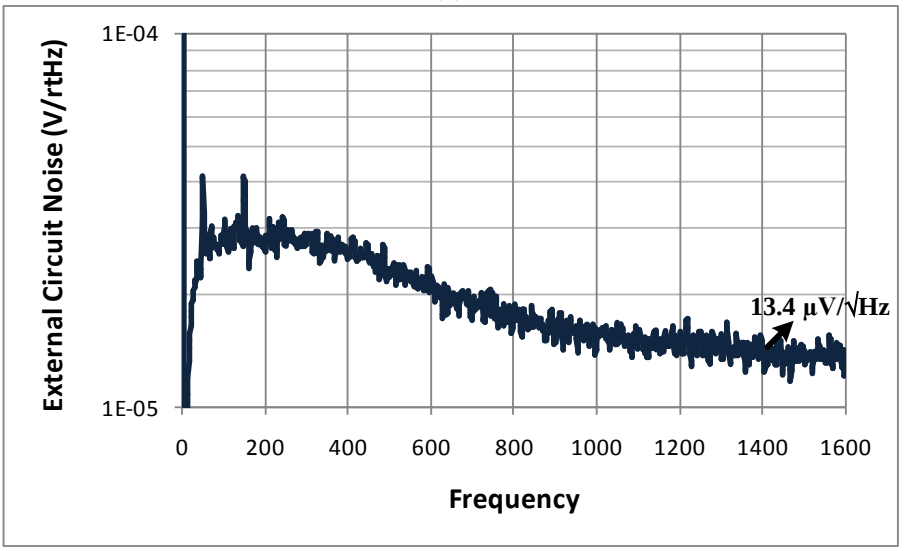


Figure 6.9: Test setup for noise measurements of the readout circuit.

To obtain the noise characteristic of the readout circuit, the total gain H(jw), and noise response of the external circuitry is primarily measured. The measured gain and noise characteristics of the external noise circuitry are shown in Figure 6.10. Then, total noise of the readout circuit with the external noise circuitry is measured. For obtaining the noise response of the readout circuit, squared noise of the external circuitry is subtracted from squared value of total noise and divided by the gain of the external circuitry at each frequency, as in Equation (6.1).



(a)



(b)

Figure 6.10: (a) Gain of the external circuitry, (b)Noise of the external circuitry.

$$V_{n,acce}(jw) = \sqrt{\frac{V_{n,tot}^2(jw) - V_{n,ext}^2(jw)}{H_{ext}^2(jw)}} \tag{6.1}$$

With this noise measurement setup, the noise of the readout circuit and the open loop noise with accelerometer are measured. The noise test results of the readout circuit are shown in Figure 6.11, including the tests with and without the accelerometer. The noise of a resistance is also measured and shown in Figure 6.11, for being a reference in the noise measurements. The test results show that the readout circuit has 0.81 µV/√Hz of noise. When this noise value is multiplied by the scale factor, it corresponds to a noise value of 1.22 µg/√Hz. When the noise of the readout circuit with the accelerometer is measured, 4.8 µg/√Hz noise level is obtained.

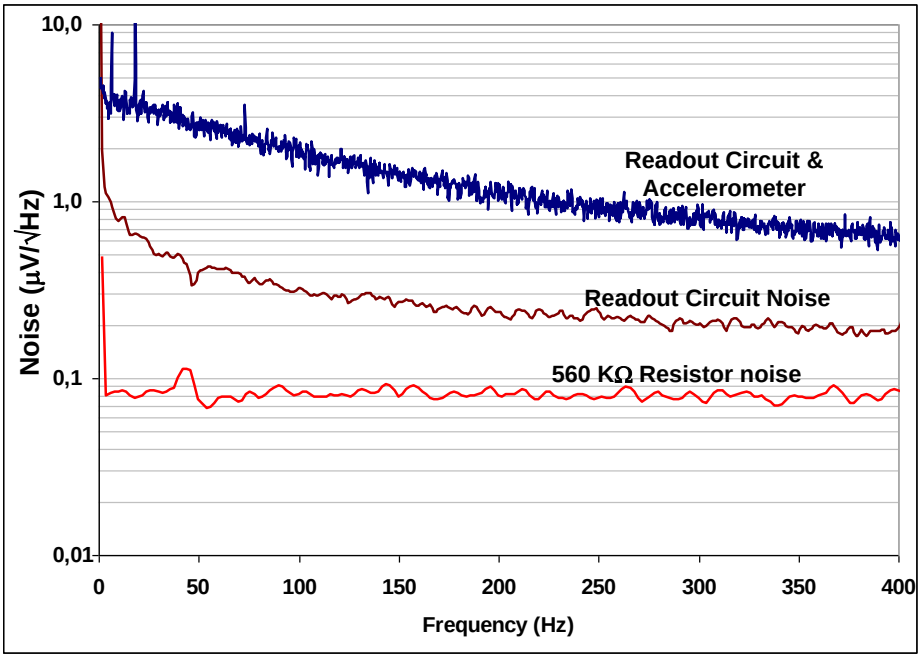


Figure 6.11: Open loop noise test results of the readout circuit, with and without the accelerometer.

6.3. Closed Loop Tests

Closed loop readout tests include linearity and sensitivity tests, dynamic response test, high acceleration test, noise and bias drift tests.

6.3.1. Closed Loop Linearity and Sensitivity

First test for measuring the sensitivity of the closed loop system is performed using the readout circuit with SOG accelerometer. The single bit output of the comparator is acquired with an oscilloscope. With this way, a maximum of 32768 single-bit data could be acquired at once. The system is placed on a rotating head, and 32768 data point is acquired and saved at various angle positions, applying accelerations from -1g to +1g. For each position, the average value of the acquired data is calculated. After calculating the accelerations from the measured angles, the graph in Figure 6.12 is obtained. The graph shows the ratio of high pulses to the total, in percentage, which can be named as pulse density.

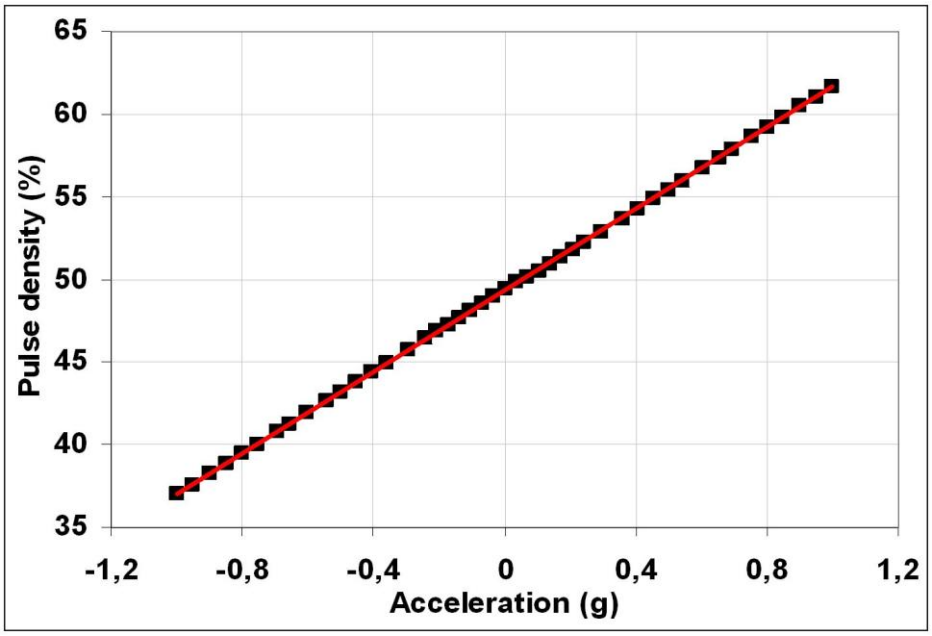


Figure 6.12: Closed loop linearity and sensitivity test results of the accelerometer system, with SOG accelerometer.

Later, using DWP process accelerometers, with the PCB given in Figure 6.5, the linearity tests are repeated. The circuitry on the PCB used for this test includes two PIC microcontrollers for filtering and decimating output bit-stream. At the output of the microcontrollers, 16-bit data is obtained at 800 Hz sampling frequency. Both the readout circuit and the accelerometer are bonded in the same package, and the package is placed on the PCB. For performing the linearity tests, PCB is mounted on a rotating head. 16-bit output data is acquired using a data acquisition system with a computer. The rotating head is rotated 30 degrees for each measurement. The data is acquired at 12 positions, completing the 360 degrees, which corresponds to 7 different acceleration values. Data is acquired for 1 minute at each position. The result obtained by 12 position measurements is shown in Figure 6.13. The decimal equivalent of 16-bit output data, which is obtained by averaging the 1 minute data for each position, versus acceleration is shown in Figure 6.13, where the acceleration is calculated according to the position angle. The scale factor according to the decimal value of output data is found as 1660 per g, where the output can range from 0 to 64000.

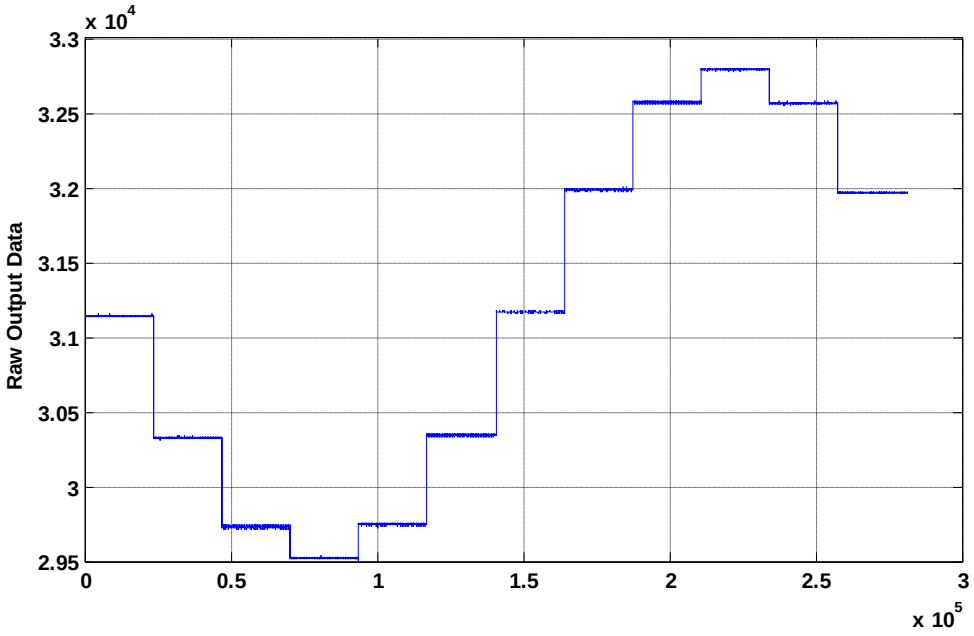


Figure 6.13: Output data versus time graph of the linearity test results of the closed loop accelerometer system, with 12 angular positions.

As seen on the Figure 6.14, R^2 non-linearity is found as 0.0035%. If the system is assumed linear also for high acceleration values, the measurement range can be calculated from the scale factor obtained, by dividing the total output value range to the scale factor. This calculation results in an operating range between -19g and +19g. If the closed loop operation range of the SOG accelerometer is calculated similarly from the previous closed loop linearity test, it is calculated as ±4g.

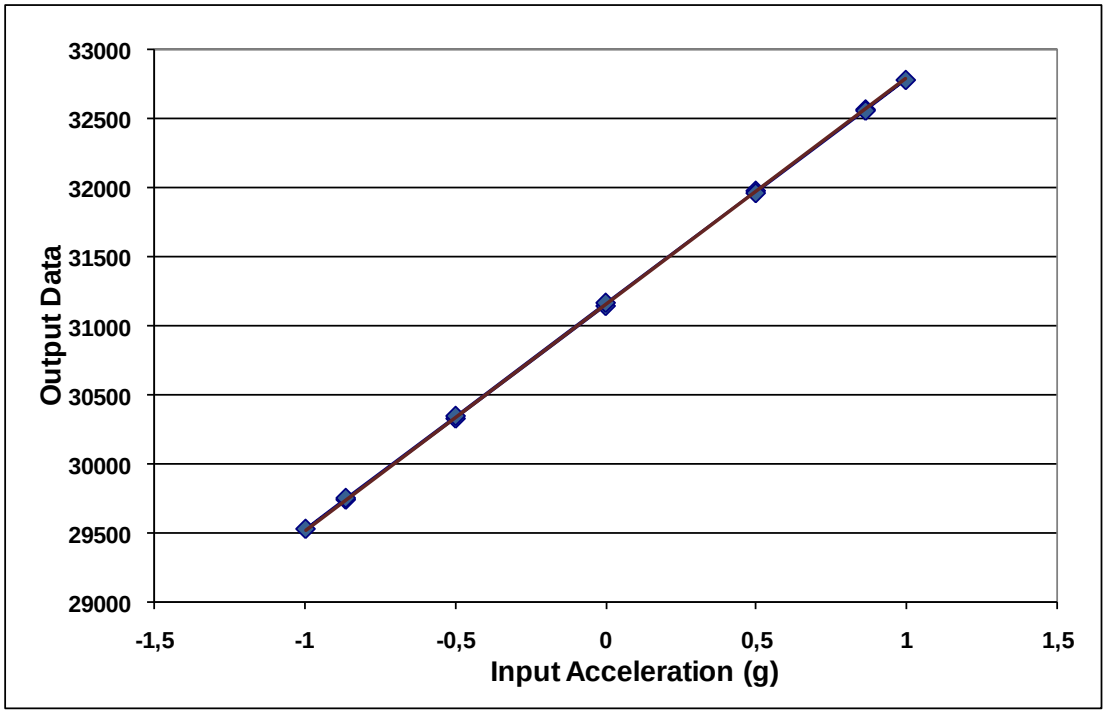


Figure 6.14: Averaged output data versus acceleration.

6.3.2. Closed Loop Dynamic Response

With this test, the response of the accelerometer system to a sinusoidal input is observed. For applying a sinusoidal acceleration, the system is placed in a rate table. The PCB is placed near the border of the plate of the rate table, so that the distance between the accelerometer and the center of the rate table is maximized. Then, a rotational vibration is applied on the accelerometer. Since the amplitude of

motion is small, the acceleration can be assumed linear, in the direction parallel to the boundary of the circle of the rate table plate, which is illustrated in

Figure **6.15**. The rate table sets the amplitude of sinusoidal vibration displacement. Knowing the positional amplitude of the vibration, the acceleration can be calculated by taking the twice derivative of the position, as given in Equation (6.2).

$$a(t) = \frac{d^2}{dt^2}x(t) = \frac{d^2}{dt^2}\left(\frac{\Delta x}{2}\sin(2\pi f t)\right) = \frac{\Delta x}{2}(2\pi f)^2 \sin(2\pi f t) \tag{6.2}$$

The acceleration is applied at 10 Hz, with 3 different amplitudes of 70 mg, 140 mg and 210 mg. The data is collected for 5 seconds, using the data acquisition board of "National Instruments". The acquired data is processed in Matlab Simulink using the digital low pass filtration blocks as explained in Chapter 3. Hence, the filtered output waveform is obtained as shown in Figure 6.16.

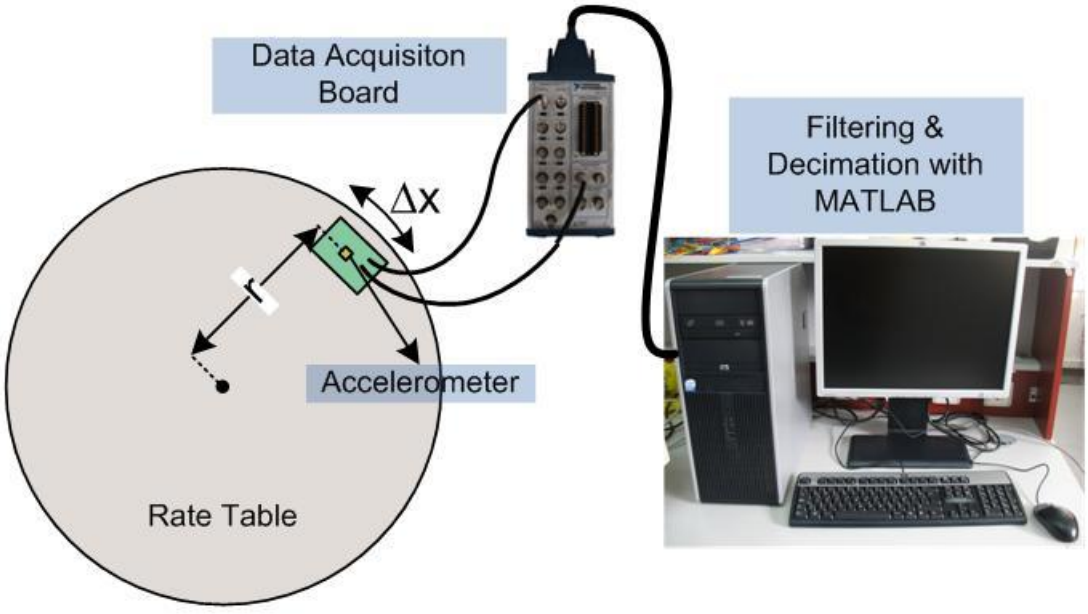


Figure 6.15: Test setup for measuring the dynamic response of the accelerometer, using the rate table.

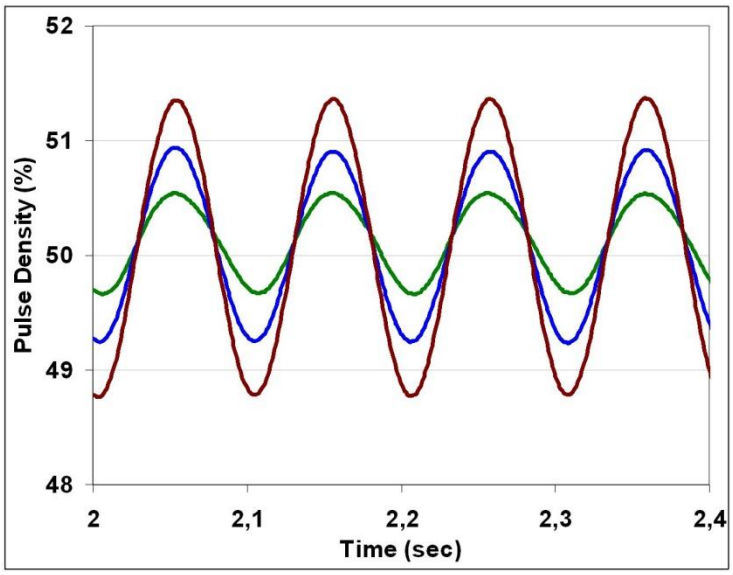


Figure 6.16: Differential analog outputs of the readout circuit, with 70mg, 140 mg and 210 mg amplitude sinusoidal inputs.

6.3.3. High G Acceleration Tests

Using a rotating head, maximum acceleration that can be applied on the accelerometer cannot exceed the gravitational acceleration. Hence, to apply higher values of acceleration, centrifugal force is used. For this purpose, the accelerometer system is mounted on a centrifuge table. The applied acceleration to the system can be expressed as in equation (6.3).

$$a_{cent} = w^2 \cdot r \tag{6.3}$$

where, *r* is the length of the arm of centrifugal table and *w* is the angular speed of the table.

The test setup prepared for the centrifuge test is illustrated in Figure 6.17. For mounting the PCB on the centrifuge table, a durable fixture is prepared as shown in Figure 6.18. With this fixture, it is able to change the direction of the applied

acceleration, just by rotating the top part of the fixture. After the PCB is mounted, 16-bit parallel data cables are connected to the data acquisition system through the slip rings of the centrifuge table. The data is acquired and observed real time on the computer.

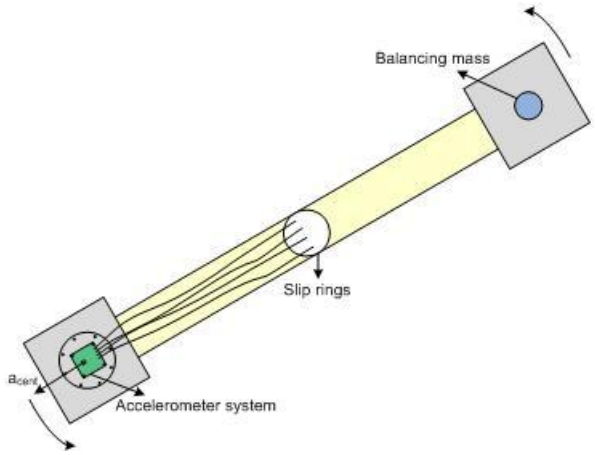


Figure 6.17: Illustration of high acceleration tests performed on centrifuge table.

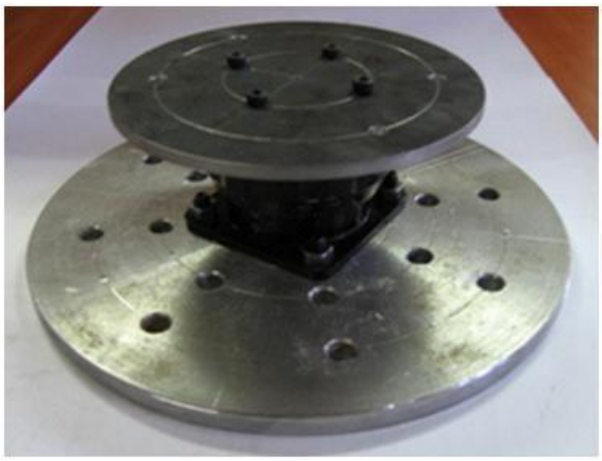


Figure 6.18: Fixture constructed for mounting the PCB on the centrifuge table.

The centrifuge table is rotated to achieve accelerations of ±4g, ±6g, ±8g, ±10g. Hence, the output of the accelerometer is observed as given in Figure 6.19. In this figure, the starting and ending of the rotation is shown. The output of the circuit is given in terms of applied acceleration in g's, which is normalized by multiplying with the scale factor.

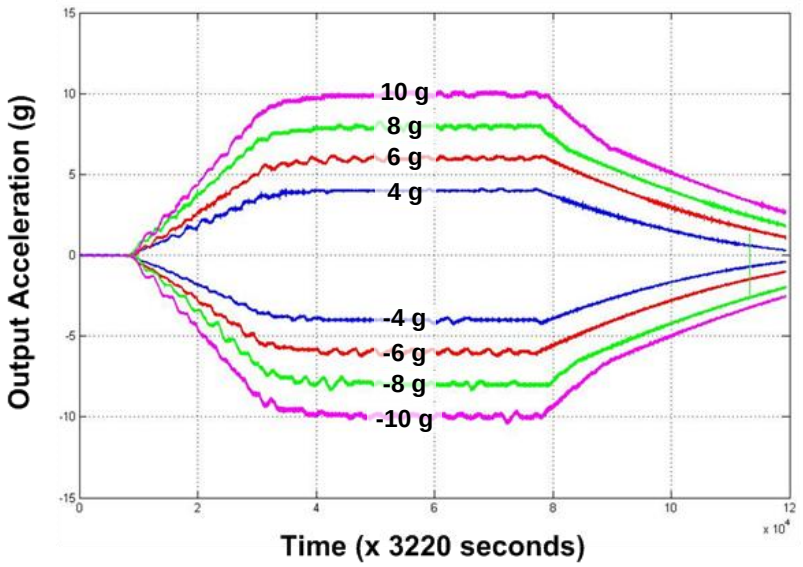


Figure 6.19: High acceleration test results of the closed loop accelerometer system.

Then, the average of each data is calculated at different accelerations, so the linearity plot is obtained as given in Figure 6.20. R^2 non-linearity of the closed loop system is 0.0004% as shown in the plot.

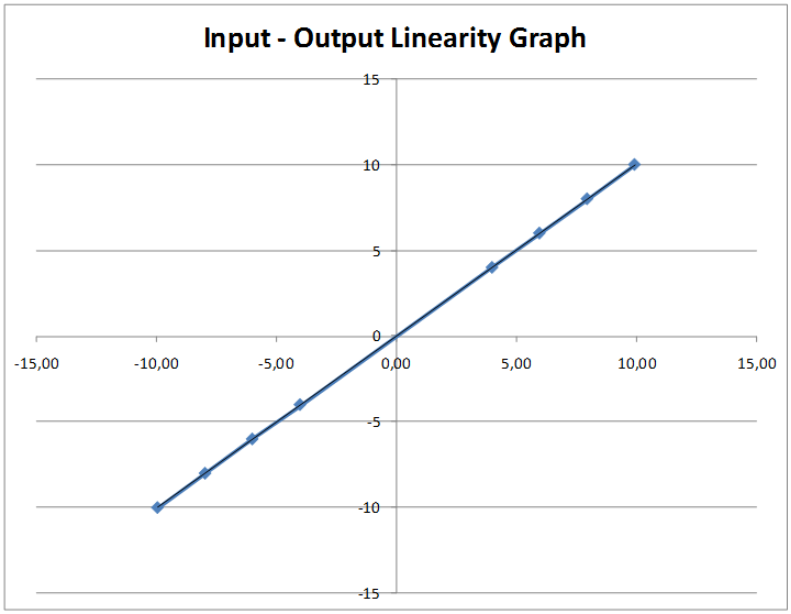


Figure 6.20: Linearity graph obtained from high acceleration tests.

6.3.4. Noise Tests

The closed loop noise tests are performed with two different methods. The first method is directly measuring the output bit-stream, after passing through a low pass filter. With this method, test setup is prepared as illustrated in Figure 6.21. For measuring the noise, "Agilent 35670A Dynamic Signal Analyzer" is used. The results of the noise test are shown in Figure 6.22. As it is expected, the noise of the closed loop system increases with the increasing frequency, because of the shaped quantization noise. Figure 6.22 also includes the open loop noise test results and makes a comparison in between. The open loop test results are higher than the results given earlier, since the used accelerometers in this test is DWP accelerometers and both the scale factor and mechanical noise of the accelerometer is different.

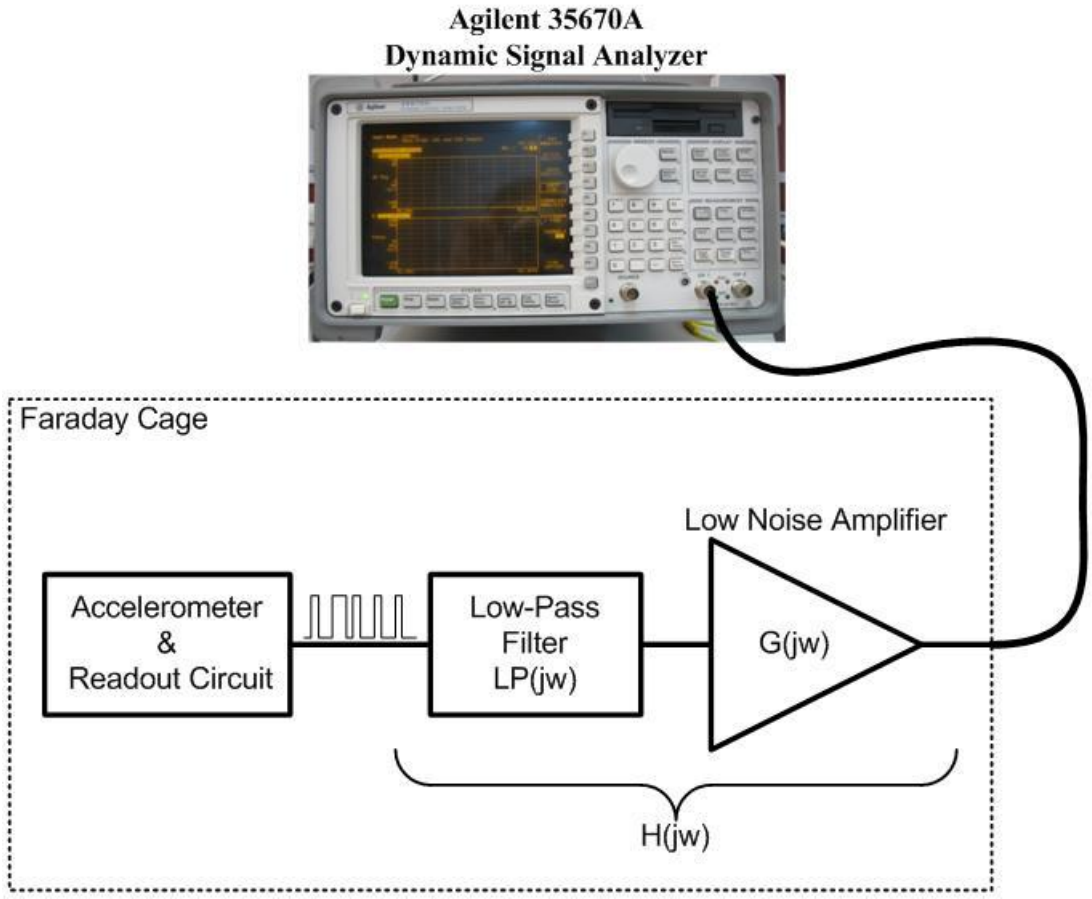


Figure 6.21: Illustration of the test setup constructed for closed loop noise tests.

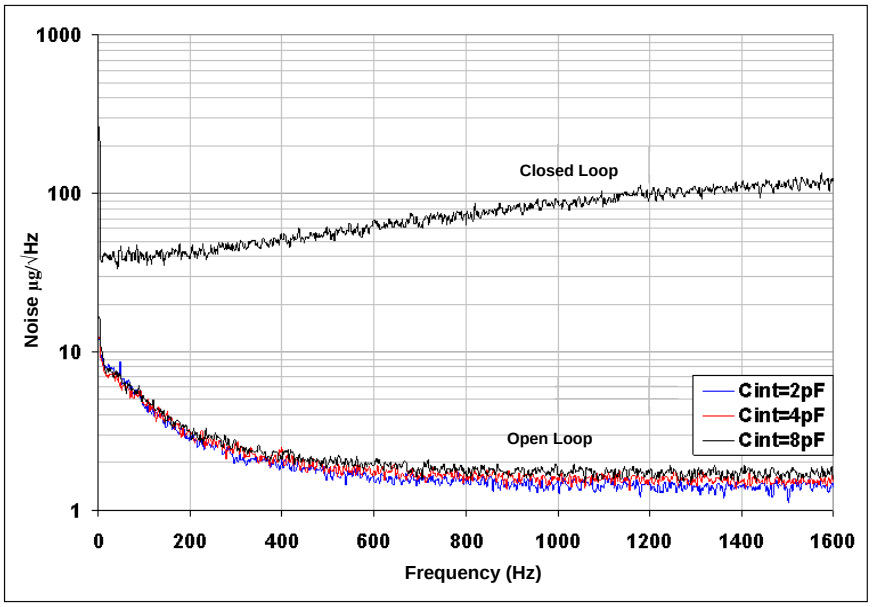


Figure 6.22: Differential analog outputs of the readout circuit.

With the second method of measuring the closed loop noise, 16-bit filtered and decimated output, using the PIC microcontrollers, are acquired for an hour, using a data acquisition board.

Then, "Allan Variance" method is used to extract the noise and bias drift values of the accelerometer system. The collected data is processed and Allen-variance graph is plotted. Figure 6.23 shows a sample plot of Allan variance analysis graph. By using the 6 different parts of this plot, various sources of non-idealities can be found as shown in Figure 6.23 and Table 6.1. By using ∂ and τ values at any point in the specified region, one can find the parameters given in Table 6.1 using the given equations. Allan Variance is a commonly used technique for determining the noise and bias drift of various systems. Hence, there are commercial software programs for processing the raw data according to Allan Variance method. By using one of these software programs, Alavar 5.2, Allan Variance plot of the acquired data is obtained, as shown in Figure 6.24. From the Allan Variance plot, the bias drift is calculated as 74µg and the noise of the system is calculated as 86µg/√Hz.

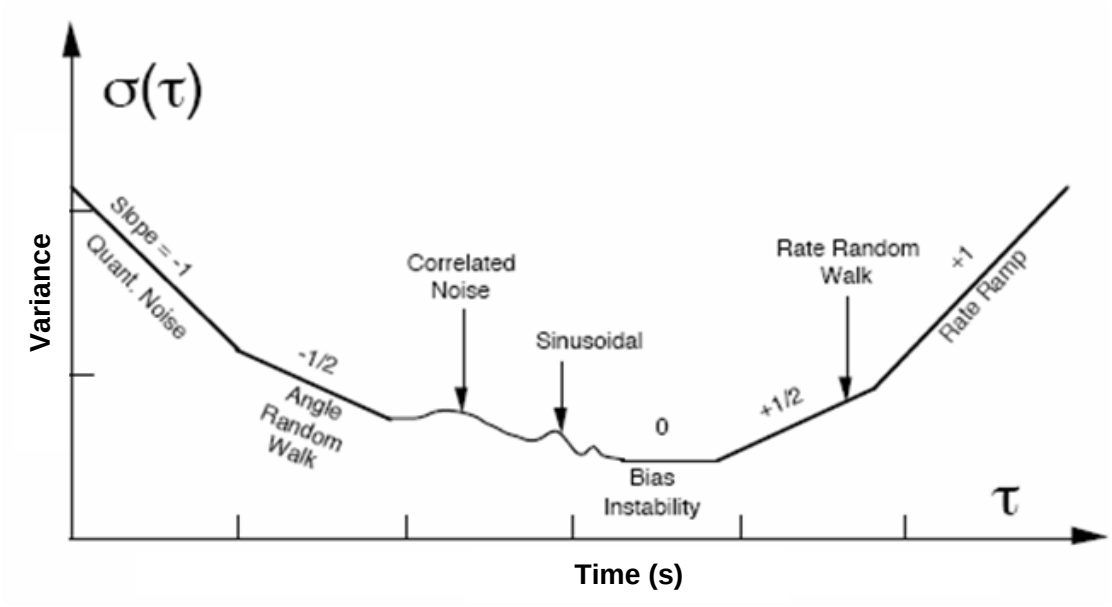


Figure 6.23: Sample Allan Variance graph.

Table 6.1. Regions in Allan variance graph and their meanings.

Region Name	Symbol	Equation	Region Slope
Quantization Noise	Q	$\partial_a = \sqrt{3}.Q/\tau$	-1
Angle Random Walk	N	$\partial_{WN} = N/\sqrt{\tau}$	-1/2
Sinusoidal	W_0	$\partial_S = w_O.\sin^2(\pi f_0\tau)/(\pi f_0\tau)$	sinusoidal
Bias Instability	B	$\partial_B = 0.6648\,B$	0
Random Walk	K	$\partial_{RW} = K\sqrt{\tau/3}$	1/2
Ramp	R	$\partial_R = R\tau/\sqrt{2}$	1

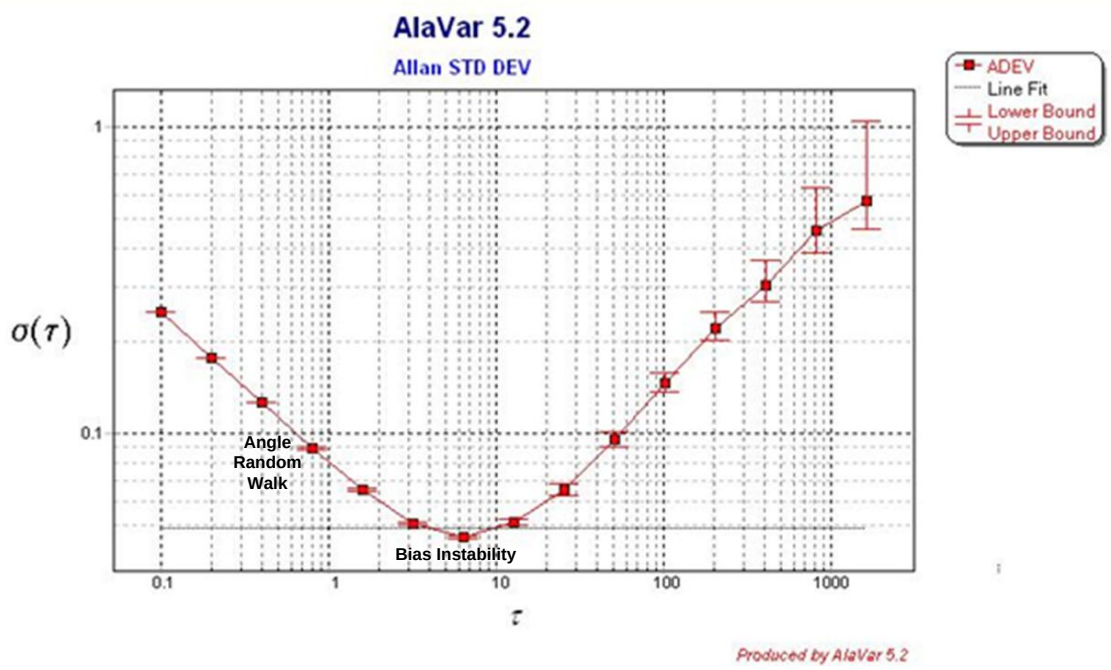


Figure 6.24: Allan variance graph obtained from the tests.

6.3.5. Temperature Tests

For measuring the temperature dependency of the system, a temperature sensor chip, designed in the research group is used. The temperature sensor has 0.05°C of maximum inaccuracy, and -165°C to 200°C measurement range. The closed loop output of the system is acquired with the data acquisition board while changing the temperature of the system. The temperature data is given as analog voltage, and it is collected using an HPVEE program, with a multimeter. The results are shown in Figure 6.25. It is observed that the output of the system is highly dependent on the temperature, where one degree change in the temperature results in 44 mg corresponding change at the closed loop output of the system. The temperature dependency may result from both the temperature dependency of the accelerometer and the readout circuit components.

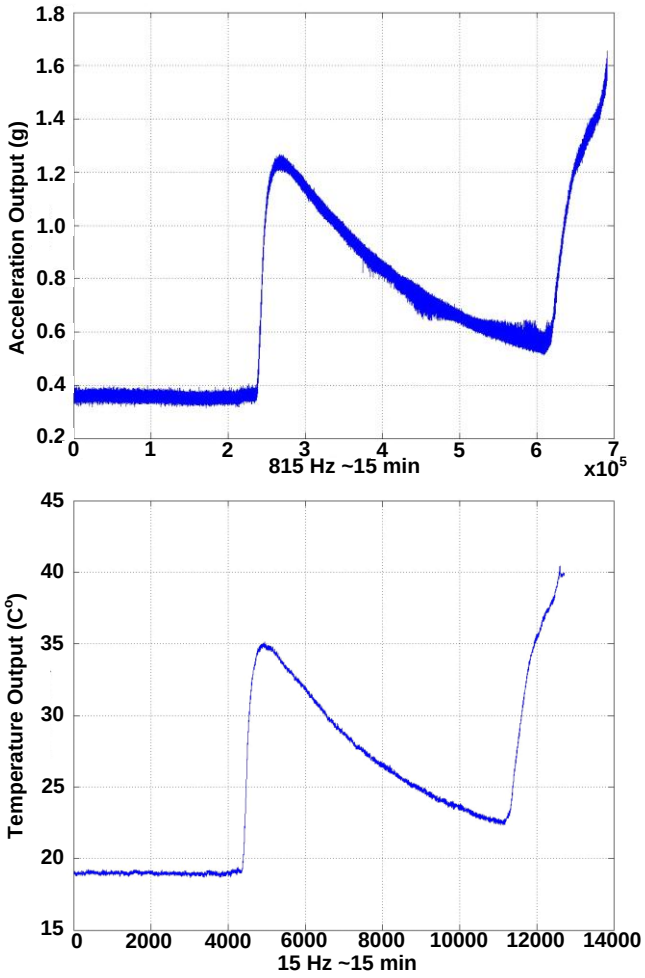


Figure 6.25: Linearity graph obtained from high acceleration tests.

6.4. Conclusions

The test results of the readout circuits showed high sensitivity, high resolution in open loop mode with SOG accelerometers. The closed loop tests were performed using DWP accelerometers and high operation range with low noise of below 100 µg is obtained. However, there are some temperature dependency problems of the readout circuit, and can be solved using a temperature sensor together with the accelerometer and performing temperature compensation at the digital output data.

Table 6.2. Summary of system level test results with SOG and DWP accelerometers.

Test	Test Result (SOG)	Test Result (DWP)
Open loop sensitivity (C_{int} = 4 pF)	2.36 V/g	0.53 V/g
Open loop noise	4.8 μg/√Hz	8.8 μg/√Hz
Closed loop sensitivity	12.5%/g pulse density	2.6%/g pulse density
Closed loop range	±4 g	±18.5 g
Closed loop noise	~50 μg/√Hz	86 μg/√Hz

CHAPTER 7

CONCLUSION AND FUTURE WORK

This thesis presented the design and implementation of a high performance readout circuit for capacitive MEMS accelerometers. The following is a summary of the accomplishment of this research.

- *The design of a complete accelerometer readout circuit.*

  A sigma-delta closed loop capacitive accelerometer readout circuit was designed, with 0.6μm XFAB CMOS process. The first readout circuit implemented was fully functional, and open-loop noise results of 4.81 μg/rtHz were obtained using SOG type accelerometers. To improve the first readout circuit with minor changes, and with the addition of a lead compensator to guarantee the system stability, a second version of the readout circuit was implemented using the same CMOS process.

- *The modeling and simulation of the accelerometer system and the verification of the operation.*

  The models of the accelerometer were constructed in both Cadence and Matlab Simulink environment. The model constructed in Simulink included the modeling of sigma-delta readout circuit together with the accelerometer sensor. This model and the performed simulations gave a better understanding of electromechanical sigma-delta modulating concept, and they were used for observing the system stability. The Accelerometer model constructed in Cadence environment gives accurate simulations results. However, due to long simulation times, the use of this model is not practical for simulations. For future research, if the readout circuit is

designed with mixed signal circuitry in Cadence, which gives simpler models for the digital structures in the readout circuit, the simulation times will be considerably reduced. Hence, more accurate closed loop complete system simulation results can be obtained.

- *The development of new readout techniques to improve the performance of the accelerometer system.*

  Two adaptive readout circuit structures were designed, which were verified to improve the performance of the closed loop system. The first adaptive circuit design decreased the quantization noise and mass residual motion by making the circuit available to operate at higher sampling frequencies. Operation at higher frequency was achieved by decreasing the feedback time of the readout. The feedback time of the circuit was decreased only for low input accelerations. For the circuit to be capable of applying adequate feedback force at high input accelerations, the feedback time was lengthened. Hence, the resolution was decreased at high input accelerations. This resulted in a high resolution at low input acceleration values and lower resolution at high input accelerations.

  The second adaptive readout circuit design uses multi-bit feedback to the accelerometer, and hence increases the resolution of the system, by decreasing the feedback time and increasing sampling frequency. However, this readout circuitry needs a multi-electrode accelerometer structure, to be able to apply the multi-bit feedback to the accelerometer.

- *The implementation and tests of the sigma-delta readout circuit together with the sensors.*

  Using the sigma-delta readout circuit, low noise open loop and closed loop test results were obtained. With the circuitry combined with DWP accelerometers, an operational range of around ±18.5 g was obtained and verified with the tests. The closed loop test results showed high linearity in

this operational range. The noise of the system was measured as 86 μg/√Hz, and a bias drift of 74 μg was obtained.

There was a bias drift at the output in the first 5-10 minutes of the closed loop tests. The reason of this drift was understood after the temperature tests of the accelerometer system were performed. It was observed that the output of sigma-delta loop was highly dependent on the temperature of the environment.

7.1. Future Directions

A micro-g resolution closed loop readout circuitry, together with the accelerometer, is still a need for navigational purposes. In order to achieve higher resolution, the first thing is to increase the sampling frequency of the readout circuit by employing different structures, or increasing the speed of the readout circuitry by speeding up the components used in the readout. While increasing the sampling frequency, the stability of the system should be taken into consideration. The stability can be verified using the models of accelerometer system.

The noise sources of the mechanical sensor and readout circuit should be added in the MAtlab Simulink model of the accelerometer, in order to achieve more accurate modeling, and the observation of non-idealities.

High temperature dependency of the system is a problem, and hence the temperature independence of the. Readout circuit components and the accelerometer should be improved. Another way of solving this problem is to use temperature compensation for the output data of the readout circuit.

The new readout techniques can be used to increase the performance of accelerometer systems. One of these techniques can be a multi-bit structure, which has already been designed. After the implementation of this readout circuit, it needs to use a multiple electrode accelerometer structure. Hence a properly sized multiple electrode accelerometer is needed.

Another readout circuit using multi-bit feedback can be designed, where, to prevent non-linearity, time-based quantized feedback can be applied. Hence, instead of using multi-bit quantization in magnitude domain, it would be used in time domain. However, with this configuration, the linearity of the analog to digital conversion stage should be taken into consideration.

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