COMMON MODE VOLTAGE AND CURRENT REDUCTION IN VOLTAGE SOURCE INVERTER DRIVEN THREE PHASE AC MOTORS

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ABSTRACT

COMMON MODE VOLTAGE AND CURRENT REDUCTION IN VOLTAGE SOURCE INVERTER DRIVEN THREE PHASE AC MOTORS

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In this thesis various reduced common mode voltage (RCMV) pulse width modulation (PWM) techniques and active/passive common mode voltage (CMV) reduction methods for voltage source inverter driven three-phase AC motors are theoretically and practically investigated. A novel RCMV-PWM method, the near state PWM (NSPWM) method is proposed for operation at high modulation index. At low modulation index, a modified version of an existing RCMV-PWM method, AZSPWM1, termed as MAZSPWM, is proposed to mitigate the voltage reflection problem of the method. An optimum modulation algorithm combining NSPWM and MAZSPWM with seamless transition is proposed. The proposed RCMV-PWM methods significantly reduce CMV but they suppress common mode current (CMC) partially. Utilization of a common mode inductor together with RCMV-PWM methods is effective in suppressing the CMC. In the study, in addition to the CMV characteristics, various practical performance characteristics such as voltage linearity, inverter output current ripple, inverter DC-link current ripple, and output line-to-line voltage pulse pattern are also analyzed. The study involves analysis, computer simulations, and detailed laboratory experiments.

Keywords: PWM, inverter, common mode, near state PWM, motor, EMI

ÖZ

GERİLİM KAYNAKLI EVİRİCİLERLE SÜRÜLEN ÜÇ FAZLI ALTERNATİF AKIM MOTORLARINDA ORTAK MOD GERİLİMİ VE AKIMININ AZALTILMASI

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Bu tezde gerilim kaynaklı eviriciden sürülen üç fazlı AC motorlar için çeşitli ortak mod gerilimi düşürücü (OMGD) darbe genişlik modülasyon (DGM) yöntemleri ve aktif/pasif ortak mod gerilimi (OMG) düşürücü yöntemler teorik ve pratik olarak incelenmektedir. Yüksek modülasyon indisi bölgesi için yeni bir OGMD-DGM yöntemi olan yakın komşu (YKDGM) yöntemi önerilmiştir. Düşük modülasyon indisi bölgesinde, mevcut bir OMGD-DGM yöntemi olan AZSPWM1'in geliştirilmiş hali olan MAZSPWM, yöntemin gerilim yansıması problemini gidermek üzere önerilmiştir. YKDGM ve MAZSPWM yöntemlerini birleştiren ve geçişleri yumuşak olan optimum bir modülasyon algoritması önerilmiştir. Önerilen OMGD-DGM yöntemleri, OMG'yi etkin bir şekilde azaltmakta ancak ortak mod akımını (OMA) kısmen bastırmaktadır. OMGD-DGM yöntemleri ile birlikte ortak mod indüktörünün kullanılması OMA'yı etkili biçimde bastırmaktadır. Bu çalışmada, OMG karakterstiklerine ek olarak, gerilim doğrusallığı, evirici çıkış akım dalgacığı, DC-bara akımı dalgacığı ve faz-arası çıkış gerilimi darbe şablonu gibi değişik pratik başarım karakteristikleride analiz edilmektedir. Bu çalışma, analiz, bilgisayar benzetimi ve laboratuvar deneylerini kapsamaktadır.

Anahtar Kelimeler: DGM, evirici, ortak mod, yakın komşu DGM, motor, EMI

To my family

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CHAPTER 1

INTRODUCTION

1.1. Adjustable Speed Drives

In modern life, electrical motors are widely utilized to generate motion from electrical energy. There are many kinds of electrical motors available at a wide range of power ratings for various domestic and industrial applications. In the past DC motors were widely preferred since control of a DC motor is easy and its speed can be controlled by changing its terminal voltage. However they have disadvantages against AC induction motors such as their initial and maintenance costs. AC motors are economical but it is impossible to control an AC motor efficiently by directly feeding it from the AC grid. Therefore Adjustable Speed Drives (ASD) were developed. ASDs generate AC output voltage at required magnitude and frequency for the induction motor. They are widely utilized for driving AC motors especially in industrial processes where variable speed control and high energy efficiency are required [1] and in high quality motion control applications where precise torque, speed, and position control are required. With the development of ASDs, utilization of AC motors has spreaded widely and today the three-phase AC induction motor is the most common motor type utilized in industry and at long term great majority of AC motors are expected to be driven by ASDs.

In Figure 1.1, a standard three-phase inverter drive circuit diagram is illustrated. In the drive illustrated in the figure between the rectifier and AC line, inductive filters are utilized to draw low harmonic distortion current from the AC grid. The DC voltage is obtained by rectifying the line voltage by a three-phase diode rectifier. In

order to decrease the voltage ripple over the DC bus, large electrolytic capacitors are utilized and smooth DC bus voltage is obtained. The DC bus voltage is converted from DC to AC by the two-level, three-wired, three-phase Voltage Source Inverter (VSI) and the AC output voltage is applied to the motor terminals [2]. VSIs are power electronic devices that can generate AC voltage at required magnitude and frequency, and they are utilized in AC motor Adjustable Speed Drives (ASD). In motor drive applications, VSIs increase the quality of motor speed control and motor efficiency by adjusting the frequency and magnitude of output voltage in a wide range with high accuracy. VSIs are composed of semi-conductor switches. In normal operation modes of circuit, these switches are either at conduction or cut-off just like ideal switches. Therefore output voltages of VSIs fed by constant DC bus voltage have rectangular waveform.

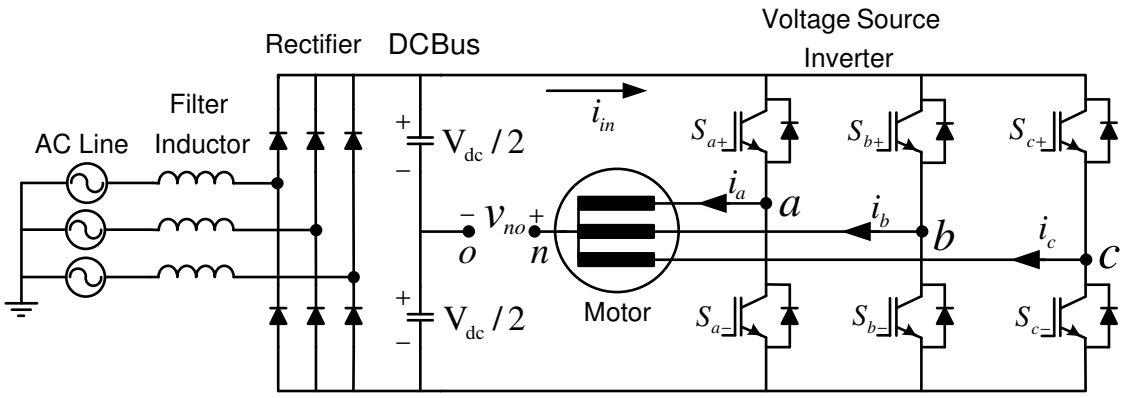


Figure 1.1 The circuit diagram of a three-phase inverter drive with diode rectifier front-end.

In order to obtain output voltage at desired magnitude and frequency, the VSI switches are turned on and off utilizing the required pulse pattern. When the switching frequency is low (lower than kHz) and the motor leakage inductance is small, the harmonic content of motor current is strong and results vibrations, noise, and losses. Therefore the switching frequency is increased as the switching losses permit [3]. In practical applications the switching frequency is typically 10-20 kHz for kW power levels, and 1-5 kHz at MW levels. The two-level inverter based ASD

circuit topology illustrated at Figure 1.1 is widely utilized in applications involving less than several MW power levels.

In the two-level VSI the most common switching method is Pulse Width Modulation (PWM). This method is based on the principle of generating a sinusoidal voltage at a fundamental frequency by adjusting the width of inverter output voltage pulses by utilizing constant switching frequency ($f_s=1/T_s$) [4]. In order to obtain these pulses, a triangular carrier wave at the switching frequency is compared with a modulation wave at the desired frequency and magnitude, and the coinciding points reveal the switching instants of switches (Figure 1.2). In high carrier frequency to fundamental frequency ratio applications (typically for a ratio larger than 20) there is no need to synchronize the modulation signal with the carrier wave [4]. Therefore there is one unique modulation wave for each leg, but the triangular carrier wave is common for all legs. The upper and lower switches of all legs complement each other ($S_{a+}=1 \rightarrow S_{a-}=0$). For $S_{a+}=1$ the output voltage is $+V_{dc}/2$, and for $S_{a+}=0$ output voltage (V_{ao}) is $-V_{dc}/2$. To prevent short-circuit faults, during switch state transitions logic signals of both switches are disabled (set to 0) for an interval named the dead-time, t_d. During this period, the load current flows through the anti-parallel free-wheeling diodes instead of the semiconductor switches, and the polarity of the output current defines the output voltage polarity (if $i_a > 0$, $V_{ao} = -V_{dc}/2$ and if $i_a < 0$, $V_{ao} = V_{dc}/2$). By this way at the output of the VSI, rectangular voltage pulses are obtained. Since each phase output voltage can take 2 different values, a two-level three-phase VSI can take $2^3=8$ different states. The average of these voltage pulses over a T_s PWM period forms a waveform which is equal to the reference (modulation) signal.

In the basic sinusoidal PWM method the reference signals of all phases are sinusoidal. However in other PWM methods the reference signal of each phase is shifted with an offset signal which is the same for all phases [5]. For these PWM methods, the average value of the output phase voltage pulses over a T_s switching period forms a waveform not equal to a pure sinusoidal signal (unless the offset signal is zero). However the average value of the line-to-line voltage pulses is sinusoidal since all phase signals are shifted (up or down) equally. Each PWM

method has unique performance attributes and the performance attributes of these PWM methods will be investigated in the following chapter.

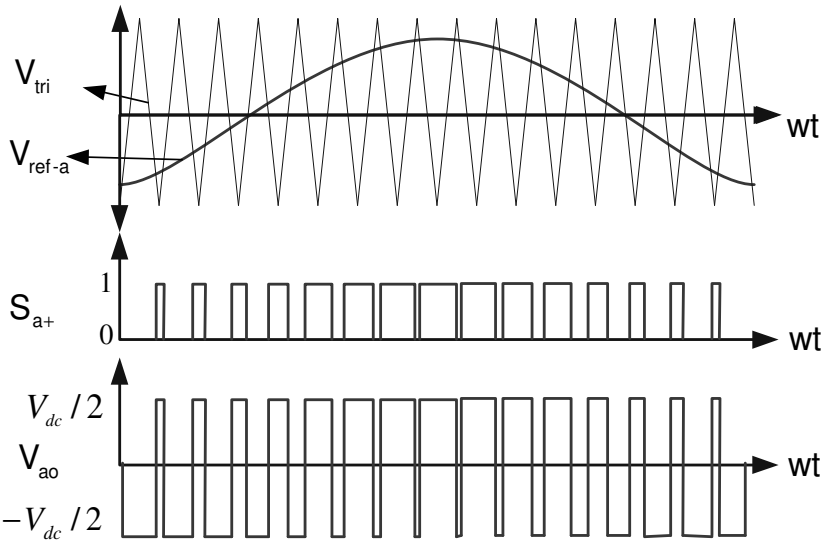


Figure 1.2 Generation method of the PWM signals and the corresponding phase voltage waveform for phase “a”.

In the VSI, power semiconductor devices are utilized as switches. The controlled switch is typically a modern power transistor and the anti-parallel diode is a fast recovery diode. While in the early development stages of the VSI technology Darlington configuration based Bipolar Junction Transistors (BJTs) were employed, at later stages faster and therefore more efficient transistors have been developed. IGBTs (Insulated Gate Bipolar Transistor) and power MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) have been invented and put to use in inverter drives over the last two decades. Reduction of the turn-on and turn-off transition times of the semiconductor switches, increases the efficiency and allows switchings at higher frequencies. Typically modern IGBTs have turn-on and turn-off times in the range of 0.1-1 μs. The DC bus voltage is approximately 550 V for the drives fed by standard utility line-to-line voltage of 400 Vrms. For such conditions, the rate of change of the VSI output voltage is approximately 0.5-5 kV/μs. In Figure 1.3, the experimental inverter output phase voltage expanded waveform and the

corresponding phase current of a 4 kW VSI during the turn-on instant is illustrated. The phase current is nearly constant during turn on instant and has positive polarity with a magnitude of 5A. The inverter turn-on time is 200 ns in this application which results in a dv/dt of approximately 3 kV/µs. Due to this rapid change, the output voltage generated by a VSI is composed of pulses with sharp edges and these pulses result undesired effects on the motor.

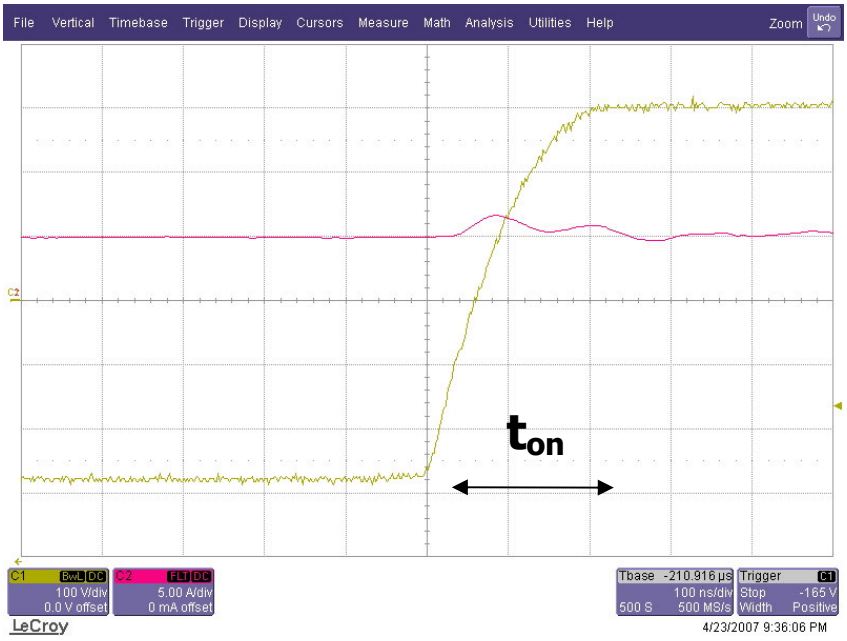


Figure 1.3 The experimental inverter output phase voltage expanded waveform and the corresponding phase current of a 4 kW VSI during the turn-on instant.

One of the important unwanted effects of the sharp edged PWM pulses is the overvoltage appearing across the motor terminals due to the voltage reflection in long cable applications. These overvoltages can have more damaging effect when there are instantaneous polarity reversals on the inverter output line-to-line voltages [6]. Due to these overvoltages, insulating breakdown occurs generally at the first coil of the stator phase windings and when this repeatedly occurs, it eventually leads to motor failure.

The Common Mode Voltage (CMV) and Common Mode Current (CMC) [7] are other important unwanted effects of the sharp edged PWM pulses and they are the main topics of this thesis and their effects and mitigation methods are investigated in detail.

1.2. Common Mode Voltage and Current

The common mode voltage is defined as the potential of the star point of the load with respect to the center of the DC bus of the VSI (V_{no} in Figure 1.1) and can be expressed in the following.

$$v_{no} = (v_{ao} + v_{bo} + v_{co})/3 \tag{1.1}$$

Since the two-level three-phase VSI can not provide sinusoidal voltages and has discrete output voltages, the instantaneous value of the common mode potential is different from zero and may take the values of $\pm V_{dc}/6$ or $\pm V_{dc}/2$ depending on the state of the inverter switches [8]. During the switching instants the change of CMV has always magnitude of $V_{dc}/3$.

Since CMV is defined according to the switch states, during switching instants it shows a rapid change. This rapid change results catastrophic problems especially at the motor drive applications [7]. Since the distances between the motor windings, rotor frame and the motor chassis are short, there are equivalent parasitic capacitances existing between these layers which are effective at high frequencies. Simply, these capacitances can be modeled as an equivalent capacitance. In Figure 1.4 the simplified common mode equivalent circuit of an inverter drive and an induction motor is illustrated [9]. The equivalent parasitic capacitance of the motor (C_{eq}) forms a RLC series resonant circuit together with the equivalent inductance (L_{eq}) and resistance (R_{eq}) parameters of the equivalent circuit of inverter drive [9]. In practical applications, for safety reasons the conductive motor chassis is grounded.

Therefore, high CMVs with high dv/dt result in parasitic CMC flowing through this parasitic capacitance from the motor to the ground at high frequencies.

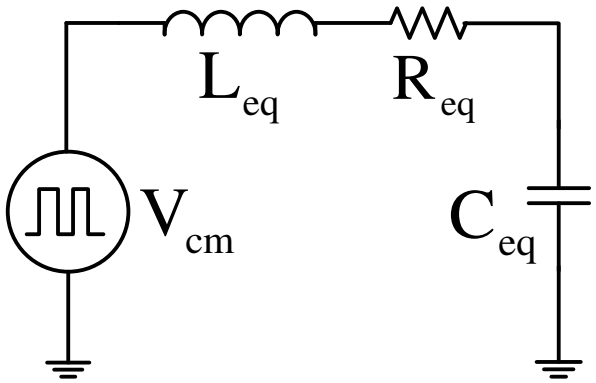


Figure 1.4 Simplified common mode equivalent circuit of an inverter drive and an induction motor [9].

In some applications the peak value of the CMC can be comparable with the rated current of the motor [10]. In the example in Figure 1.5, experimental common mode voltage and leakage current (approximately equal to CMC) waveforms are illustrated, which are observed in a 4 kW induction motor driven by an ASD with 500V DC bus voltage and no mitigation method is applied. In this operation the rms value of the load current is approximately 3 A at no load while the leakage current is approximately 1 A peak which is very high. These large CMV/CMC values result fluting type bearing failures [7] in a short time. Since CMV and CMC create emission at high frequencies, they result in EMI at both the AC grid which feds the drive and the electronic circuits of the drive itself. Therefore unwanted nuisance trips (including at the drive itself) and failure of the electronic circuits may occur [7]. Due to these unwanted effects, reduction of the effects of CMV and CMC is necessary. Therefore various mitigation techniques have been developed.

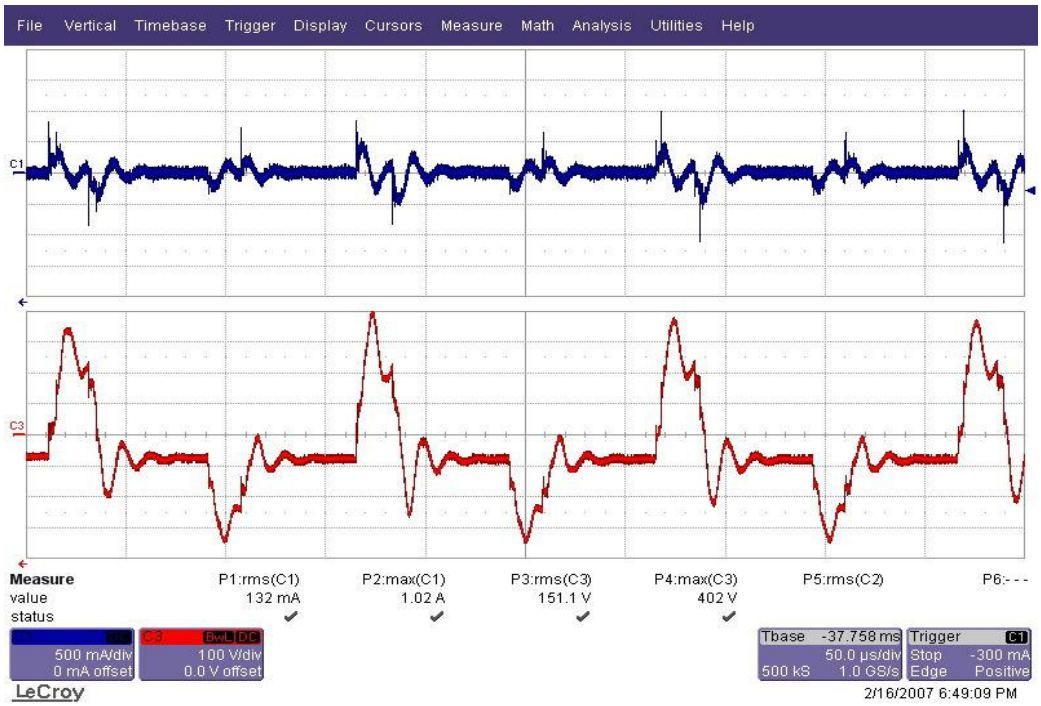


Figure 1.5 Experimental CMV (red) and leakage current (blue) waveforms.

Adding active or passive filters [9], [11], [12] between the inverter drive and the motor is the most common technique to effectively reduce CMV and CMC. However there are some drawbacks to utilizing filters such as increasing size and cost.

Optimization of the PWM pulse pattern also reduces CMV and CMC but so far the developed PWM methods that reduce CMV/CMC [13], [14] have practical constraints and limited performance attributes. Although some methods are theoretically (ideally) viable, due to practical constraints, they result in performance degradation rather than improvement [13], [14]. The practical implementation of some methods is problematic as such methods result high harmonic content at load current [8]. Similarly some methods result high peak overshoots at line-to-line voltages at the motor phase winding terminals when the ASD and the AC motor are distant from each other (long cable applications) [15]. In this thesis a new PWM pulse pattern optimization technique is proposed without any practical constraints and with high PWM performance attributes. Utilizing this method reduces CMV and CMC partially and decreases filter requirement of the inverter drive.

1.3. Scope of The Thesis

This thesis mainly focuses on CMV/CMC reduction in three-phase two-level VSI based drives, by means of PWM pulse pattern optimization. The most important contribution of this thesis involves the development of a novel reduced common mode voltage PWM method, the Near State PWM (NSPWM) method for three-phase two-level VSIs which has no practical implementation constraints and yields superior PWM performance attributes such as resulting in low harmonic stresses at the AC and DC side of the VSI.

The second contribution involves investigation of the important performance attributes of Reduced Common Mode Voltage PWM (RCMV-PWM) methods and standard PWM methods by means of theoretical, analytical and numerical analysis, computer simulations and laboratory experiments.

The third contribution involves theoretical investigation of active and passive CMV/CMC mitigation methods and experimental investigation of the effects of passive filters on CMC. This study is for the purpose of comparing the passive and PWM pattern based CMV/CMC reduction methods and do a global evaluation.

The Active Zero State PWM (AZSPWM1) method [13] which is one of the most popular RCMV-PWM methods has a performance constraint, such that it has problematic line-to-line output voltage pulse pattern. The fourth contribution of this thesis involves the development of a modification algorithm for the AZSPWM1 method, which eliminates its performance constraint. This section also evaluates the overvoltage attributes of all discussed PWM methods.

The final contribution of this thesis is the development of a PWM algorithm that combines various PWM methods and results in overall superior performance depending on the optimization criteria chosen by the user. It is illustrated that the algorithm combines various PWM methods and the combination involves seamless transition between methods such that the output performance is not disturbed.

The organization of this thesis is as follows. In the second chapter, standard PWM methods and RCMV-PWM methods for the two-level three-phase VSI are reviewed and a novel RCMV-PWM method (NSPWM) is introduced. Important PWM performance characteristics, such as the voltage linearity and input/output ripple characteristics and practical applicability of NSPWM and other PWM methods are investigated.

In the third chapter, computer simulations of the PWM methods are provided to verify the theoretical and analytical results of the second chapter. In this chapter important performance characteristics such as inverter input and output harmonic content and CMV of all RCMV-PWM methods and standard PWM methods are compared.

In the fourth chapter, harmful effects of the common mode voltage and the common mode current are discussed. Generating mechanism and different types of CMC and bearing currents are discussed in detail. Active and passive common mode voltage and current suppression methods are reviewed. Effects of PWM pulse pattern optimization on CMV/CMC is compared with other mitigation methods.

In the fifth chapter, the laboratory experimental set-up which is used in this thesis and the implementation of the NSPWM are described. Experimental results composed of measurements of the CMV and CMC of important PWM methods are provided. The effects passive common mode filters on the CMC are investigated in this chapter. CMV/CMC performance of commercial two-level and three-level ASDs are studied and compared with the prototype VSI which is constructed in this thesis. Line-to-line voltage waveforms at the terminals of the motor are studied with the long cable test for important PWM methods. Finally the combination of CMV and CMC reduction techniques is proposed for optimum overall performance.

The sixth chapter summarizes research results related to this thesis.

CHAPTER 2

PWM METHODS AND CHARACTERISTICS

2.1 Introduction

Voltage source inverters are utilized in practical motor drive applications since their invention. In the past, the voltage source inverters were operated in the square wave operation mode. In the square wave operation mode, the inverter phase and therefore line-to-line output voltages have square wave shapes. In Figure 2.1 the line-to-line output voltage of V_{ab} and its fundamental component in this operation mode is illustrated for the conventional three-phase two-level inverter [2]. This operation mode has drawbacks such that the inverter output voltage has low order harmonics with large magnitude (such as 5^{th}, 7^{th}) which are also seen at the motor currents. In spite of these drawbacks, the square wave operation was preferred in the early inverters because of its very low number of switchings, hence low switching losses. The semiconductor switches which were utilized in the early inverters had long turn-on and turn-off times resulting very high switching losses. Therefore by utilizing these switches, switching at high frequencies was practically impossible and instead of the PWM, the square wave operation was preferred.

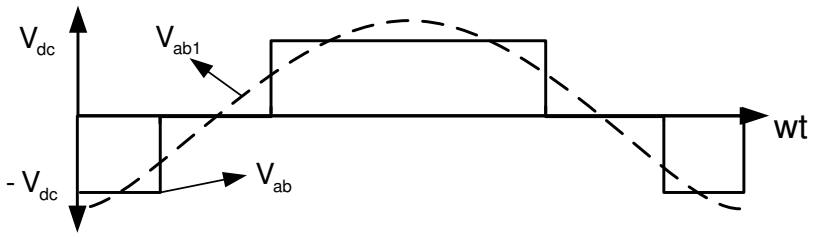


Figure 2.1 Inverter output line-to-line voltage waveform and its fundamental component when square wave method is utilized.

As the semiconductor technology has evolved, faster semiconductor switches have been developed. Today IGBT switches with low turn-on and turn-off times are widely utilized in VSIs. Development of faster semiconductor switches significantly reduced the switching losses of the inverter drives and this reduction enabled operation at higher switching frequencies. Therefore utilization of PWM methods (Figure 1.2) in inverter drives had been possible at various power ratings and the square wave operation had been obsolete except at very high power ratings. Today PWM methods are widely preferred in three-phase motor drives due to their superior characteristics. In the PWM mode operation, an AC motor does not draw low order current harmonics (such as 5^{th}, 7^{th}, 11^{th}, etc.). The lowest order harmonic on the motor current occurs at the switching frequency of the inverter. Since this frequency is practically high (order of kHz), current harmonics are damped by the motor windings and are not problematic as in the square wave operation case.

In the PWM approach, the inverter switches are turned on and off within a carrier period in an appropriate manner and switch pulse patterns are generated. Various PWM methods with unique switch state pulse patterns have been developed with unique characteristics. In this chapter conventional PWM methods are reviewed, new PWM methods are introduced and their performance attributes are theoretically and analytically investigated. Finally, a thorough performance comparison of all the discussed PWM methods is provided.

2.2 PWM Basics, Scalar and Vector Implementations

Based on the implementation technique, PWM methods are classified as scalar or space vector PWM methods. In the scalar implementation, a modulation reference signal is compared with a triangular carrier signal and the intersections define the switching instants. PWM pulses of one phase were given in Figure 1.2 for a fundamental cycle. In Figure 2.2 the phase voltage reference signals, triangular carrier signal, inverter upper switch signals and output line-to-line voltage pulses of all phases are illustrated for a PWM period. In practice, PWM periods are very small (100 μs for 10 kHz operation) compared to the fundamental period (20 ms for 50 Hz operation). Therefore the reference signals can be assumed as constant throughout the PWM period. The magnitude of the reference signal (V_{ref}) of any phase (phase-x) is proportional to the duty cycle of the upper switch of the corresponding phase (d_{x+}) and defined as (2.1) where V_{dc} is the DC-bus voltage. [16].

$$d_{x+} = \frac{1}{2}\left(1 + \frac{2V_{ref}}{V_{dc}}\right) \qquad x \in \{a, b, c\} \tag{2.1}$$

Since upper and lower switches of all phase legs complement each other and the duty cycle of the lower switch of the phase-x (d_{x-}) is defined as (2.2).

$$d_{x-} = (1 - d_{x+}) \tag{2.2}$$

The performance characteristics of a modulation method are primarily dependent on the modulation index M_i (voltage utilization level) which is defined as (2.3) [5]

$$M_i = \left(\frac{2}{\pi}\right)\frac{V_{1m}}{V_{dc}} \tag{2.3}$$

where V_{1m} is the magnitude of the reference signal fundamental component.

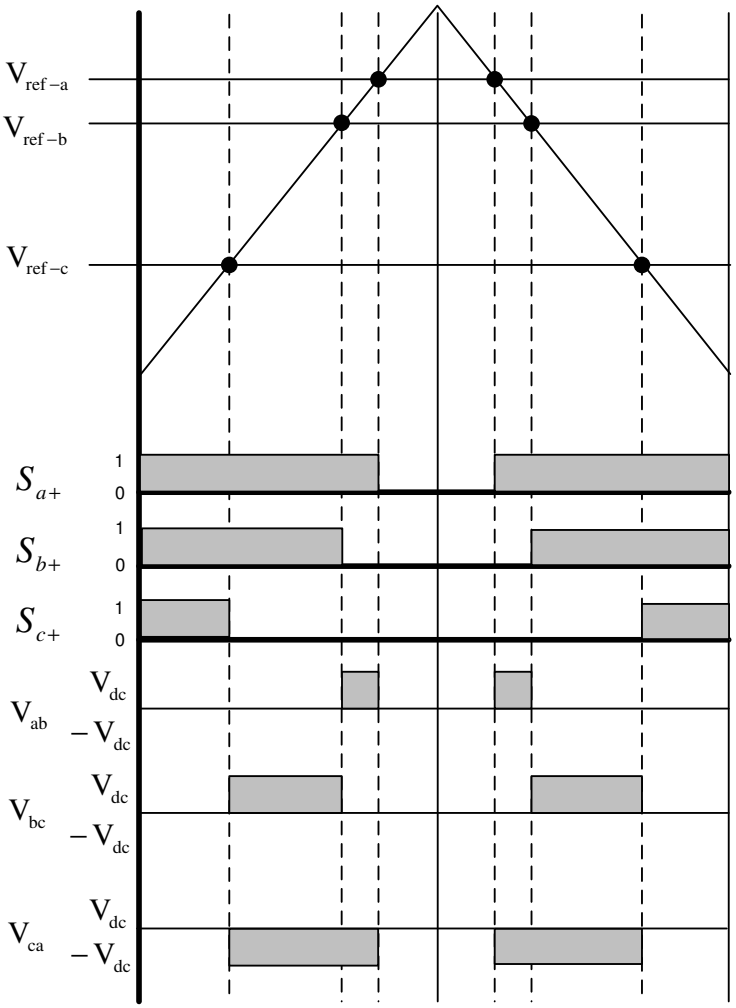


Figure 2.2 Scalar implementation of a PWM method and the resulting output line-to-line voltages.

When implementing the PWM methods and analyzing the VSI output voltages, the space vector approach can be utilized. In the space vector approach the reference and the inverter output voltages are transformed to space vectors via the following complex variable transformation [16].

$$V = (2/3)\times(V_a + aV_b + a^2V_c) \tag{2.4}$$

In the above equation $a = e^{j2\pi/3}$ is the phase shift operator. Since there are eight possible inverter states available, the vector transformation yields eight voltage

vectors as shown in Figure 2.3. Of these voltage vectors, six of them (V_1, V_2, V_3, V_4, V_5, and V_6) are active voltage vectors, and two of them (V_0 and V_7) are zero voltage vectors. The active voltage vectors result in non-zero line-to-line voltage at least between two phases and the zero voltage vectors result in zero line-to-line voltage between all the phases. In the space vector analysis the duty cycles of the voltage vectors are calculated according to the vector volt-seconds balance rule defined in (2.5) and (2.6) and these voltage vectors are applied with the calculated duty-cycle.

$$V_i t_i + V_j t_j + V_k t_k = V_{ref} T_s \tag{2.5}$$

$$t_i + t_j + t_k = T_s \tag{2.6}$$

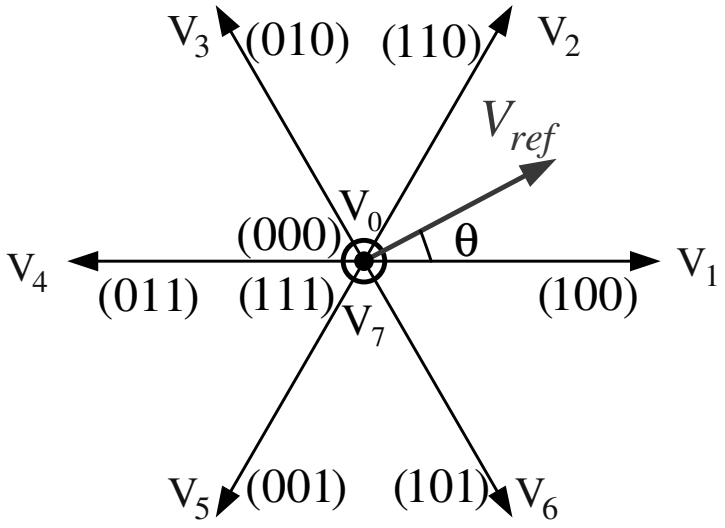


Figure 2.3 Voltage space vectors of the two-level inverter.

The sequence of the voltage vectors is selected based on a specified performance criterion such as the switching count and the vectors are programmed accordingly. Each PWM method utilizes different voltage vectors and sequences and the utilized voltage vectors alternate throughout the vector space. Therefore, the vector space is

divided into segments. There are 6 A-type and 6 B-type segments available (Figure 2.4). Investigations reveal that all PWM methods utilize either A-type or B-type segments, and the utilized voltage vectors of these PWM methods alternate at the boundaries of the corresponding segments.

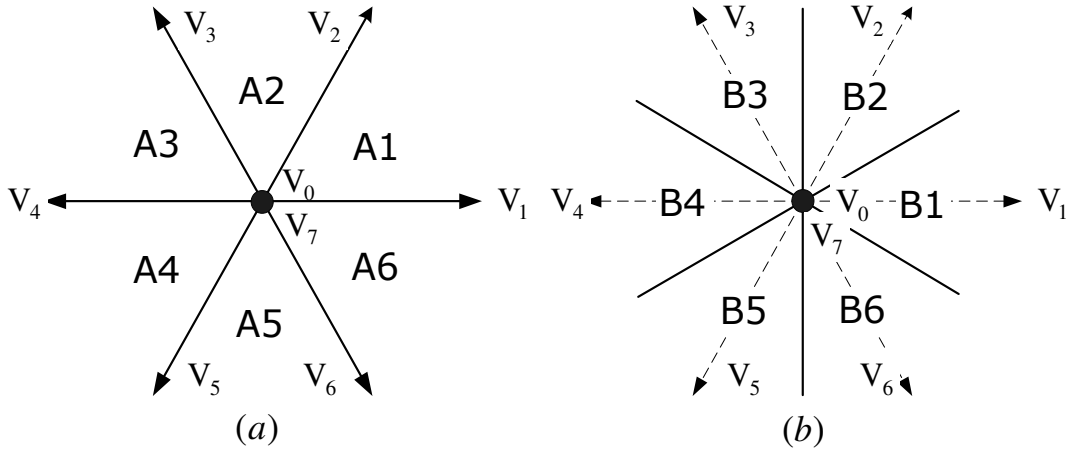


Figure 2.4 Voltage space vectors and 60^{o} sector definitions:
(a) A-type, (b) B-type regions.

2.3 Standard PWM Methods

In PWM based VSIs, a reference signal is utilized and compared with the carrier triangular signal. The shape of this reference signal is equivalent to that of the corresponding required inverter output phase voltage with a proportional magnitude. In practice, the neutral point of the motor is always isolated. Therefore even the potential of the neutral point of the motor is non-zero; zero sequence currents can not flow since there exists no current path. This isolation allows the injection of a wide range of a zero-sequence voltage to the inverter phase voltages. In order to optimize the waveform quality, to decrease switching losses, or to provide wider voltage linearity range, zero-sequence signal injection is applied by shifting the reference signals of all phases up or down with a same amount as illustrated in Figure 2.5 [16]. In the given diagram $V_{ref\text{-}a}$', $V_{ref\text{-}b}$' and $V_{ref\text{-}c}$' are the sinusoidal reference signals of phase-a, phase-b and phase-c respectively before zero sequence signal (V_{zs}) is

injected. The zero sequence signal (V_{zs}) is a function of the sinusoidal reference signals and is added to all phase reference signals equally. By this injection the reference signals of phases (V_{ref-a}, V_{ref-b} and V_{ref-c}) which are going to be compared with triangular carrier signal are obtained.

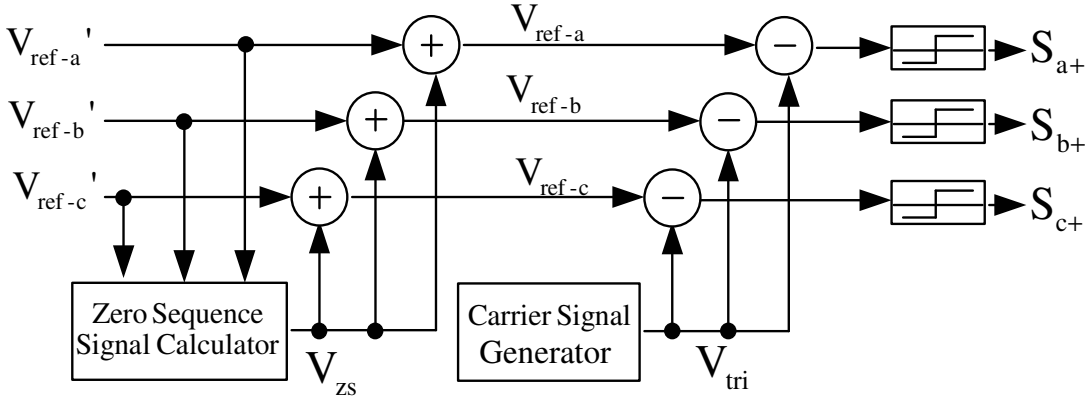


Figure 2.5 Zero sequence signal injection diagram for PWM methods [16].

Standard PWM methods have been developed by the zero-sequence signal injection principle and are classified according to their reference signals. Theoretically infinitely many PWM methods can be generated by injecting zero-sequence signals but only few of them are utilized in practice. The most common PWM methods which are generated by zero-sequence injection are Space Vector PWM (SVPWM) and Discontinuous PWM (DPWM) methods [5]. In this section, these two methods will be investigated in detail. Although in these methods, average value of the output phase voltage pulses over a T_s period forms a waveform not equal to a pure sinusoidal signal; the inverter output line-to-line voltages are not affected from this injection since all the three phases are shifted up or down with a same amount.

In vector implementation, regardless of the injected zero sequence signals, the active voltage vectors and their duty cycles are not affected at all. In Figure 2.6, the voltage space vectors of a standard PWM method which is generated by the zero-sequence signal injection principle is illustrated. In those applications the zero sequence

injection only changes the partitioning of the zero voltage vectors V_0 and V_7 [5]. This partitioning can be applied such that one of these two zero voltage vectors may not be utilized at all (discontinuous PWM). However total duty cycles of the zero voltage vectors (the total zero vector time) are same and therefore CMV is not substantially affected by the zero sequence injection.

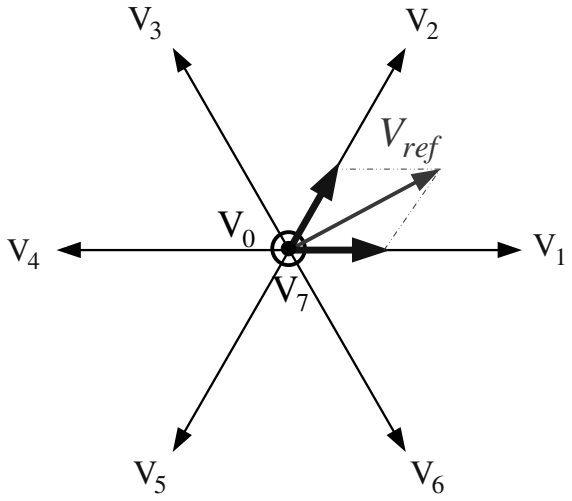


Figure 2.6 Voltage space vectors of a standard PWM method.

2.3.1 Space Vector PWM (SVPWM)

SVPWM modulation signals are generated by selecting the phase reference signal with the smallest magnitude and adding half of this signal to all phases [16]. By this injection, at steady-state the peak value of the modulation signal is decreased without changing the magnitude of the fundamental component of the modulation signal. Therefore phase voltages with a peak fundamental value greater than half DC bus can be generated and this method is widely preferred in the motor drive applications. SVPWM is classified as a Continuous PWM (CPWM) method since in SVPWM the modulation signal peak value is always smaller than peak of the triangular carrier wave and inverter switches of all three phases are always switched on and off within a PWM cycle. In Figure 2.7 SVPWM reference signals (V_{refa}', V_{refb}', V_{refc}') and the injected zero sequence signal (V_{zs}) are illustrated for $M_i = 0.78$.

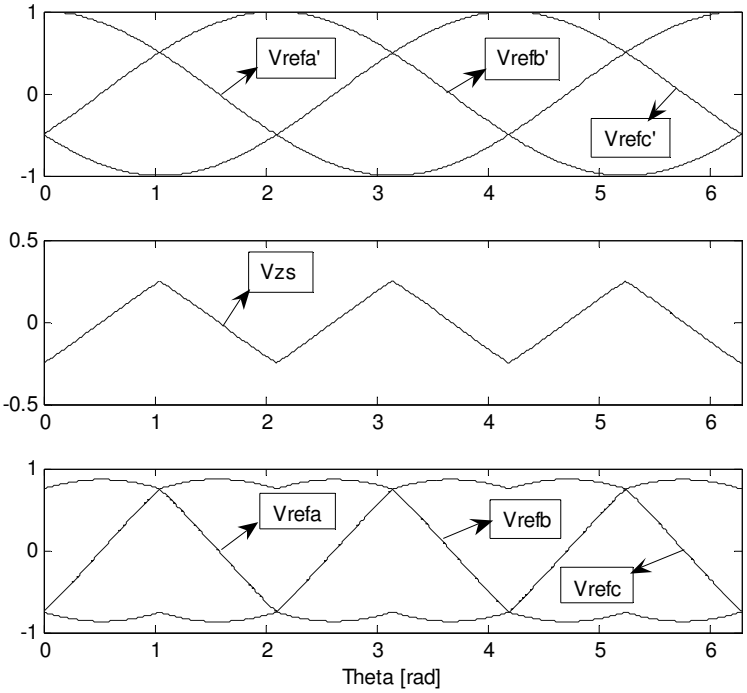


Figure 2.7 SVPWM reference signal and injected zero sequence signal for $M_i = 0.78$.

When the space vector approach is utilized, adjacent states along with zero states are utilized to generate the required voltages, and the zero states are made equal (d_0 and d_7), the resulting pulse pattern becomes identical to the above discussed SVPWM method. This is the reason this method is termed SVPWM. In Figure 2.8 inverter switch state pulse pattern and CMV pulse pattern of SVPWM are given for the region A1. Note that when SVPWM is utilized, CMV can be $V_{dc}/2$ in magnitude [8].

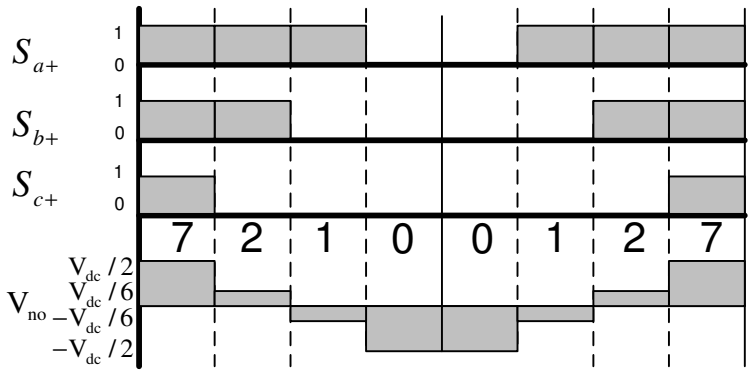


Figure 2.8 Inverter switch state PWM pulse pattern of SVPWM for the region A1.

2.3.2 Discontinuous PWM (DPWM)

In generation of the reference signals of DPWM methods a zero sequence signal is injected such that reference signal of at least one phase is always clamped to the positive or negative DC bus. The clamped phase is alternated throughout the fundamental cycle. In DPWM methods clamped phase is not switched throughout a PWM period. Therefore the switching losses are decreased. There are various DPWM methods available differing from each other by the selection of the clamped phase [17]. For example in DPWM1 the phase signal which is the largest in magnitude is clamped to the DC bus with the same polarity. DPWM1 has the least switching losses among all DPWM methods at unity power factor [17]. In Figure 2.9 the DPWM1 reference signal and the zero sequence injected are illustrated for M_i=0.78.

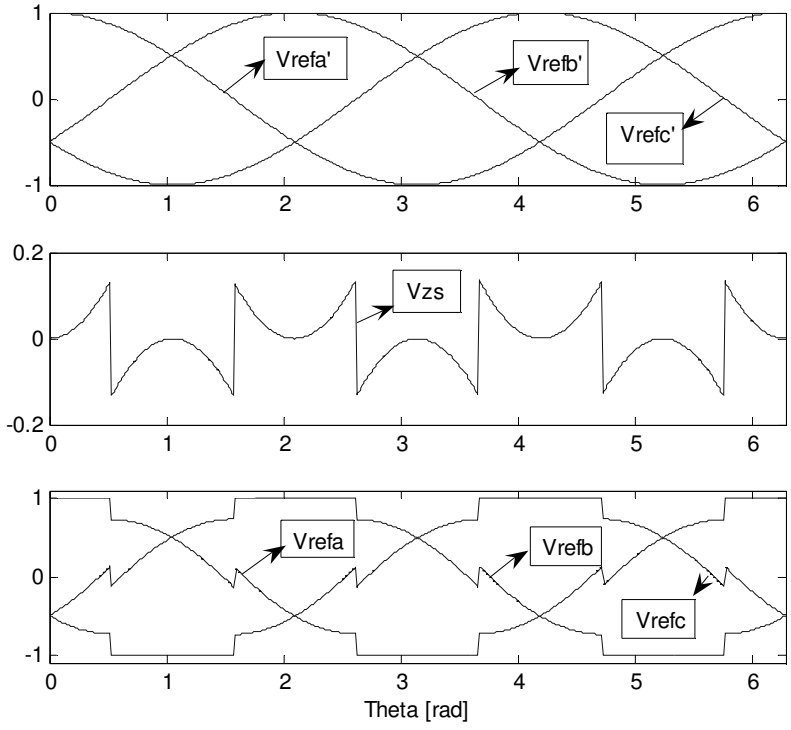


Figure 2.9 DPWM1 reference signal and zero sequence injected.

In the space vector implementation, when one of the zero vectors (either V_7 or V_0) is not utilized, the same pulse pattern as DPWM can be obtained. In Figure 2.10 inverter switch state pulse pattern and CMV pulse pattern of DPWM1 is given for region A1 ∩ B2 ($30^o \leq \theta \leq 60^o$). Note that when DPWM is utilized, CMV can be $V_{dc}/2$ in magnitude [8].

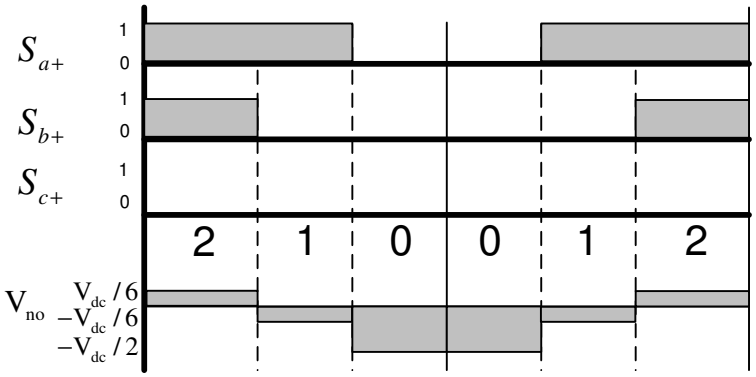


Figure 2.10 Inverter switch states and the PWM pulse pattern of DPWM1 for the region A1∩B2.

2.4 Reduced Common Mode Voltage PWM Methods

In the conventional PWM methods, which are based on the principle of injecting a zero sequence signal to the reference signal, utilization of the zero voltage vectors is mandatory. Therefore when utilizing any of these PWM methods, CMV rises to $V_{dc}/2$ in magnitude. In order to avoid this high CMV, various Reduced Common Mode Voltage (RCMV) PWM methods have been developed. All of these RCMV-PWM methods are based on the principle of avoiding utilization of the zero voltage vectors (V_0 and V_7). For this purpose, the space vector approach is widely utilized in the development and analysis of the RCMV-PWM methods. RCMV-PWM methods utilize only active voltage vectors (V_1, V_2, V_3, V_4, V_5, V_6) and the duty cycles of these vectors are calculated by volt-seconds balance. The choice of the voltage vectors of the RCMV-PWM methods is unique. There are three important RCMV-

PWM methods available which are Active Zero State PWM (AZSPWM) [13], Remote State PWM (RSPWM) [14], and Near State PWM (NSPWM) [15]. In the following, these methods will be described in detail.

2.4.1 Active Zero State PWM (AZSPWM)

In the Active Zero State PWM (AZSPWM) methods, two opposing active voltage vectors with equal duration are utilized to create effectively a zero voltage vector.

In the AZSPWM methods, the choice and the sequence of the active voltage vectors are the same as in CPWM. However, instead of the real zero voltage vectors (V_0 and V_7), two active opposite voltage vectors canceling the effects of each other are utilized [13]. Here, three choices exist. Any of the pairs V_1V_4, V_2V_5, or V_3V_6 can be utilized. For each region (A1-A6), of the three pairs only one is favorable while the other two pairs result in performance problems (adjacent pairs are favorable due to low harmonic distortion) [13]. The voltage vectors of AZSPWM are given in Figure 2.11. For a reference voltage vector in the region A1, only the V_3V_6 pair is favorable since these vectors are adjacent to the active voltage vectors V_1 and V_2. The duty cycles of AZSPWM methods are given in (2.7), (2.8), and (2.9) for a reference voltage vector in the region Ai. In the defined equations $\theta = w_e t$ is the angle of the reference voltage vector. The sequence of the active zero voltage vectors defines the two types of the AZSPWM methods.

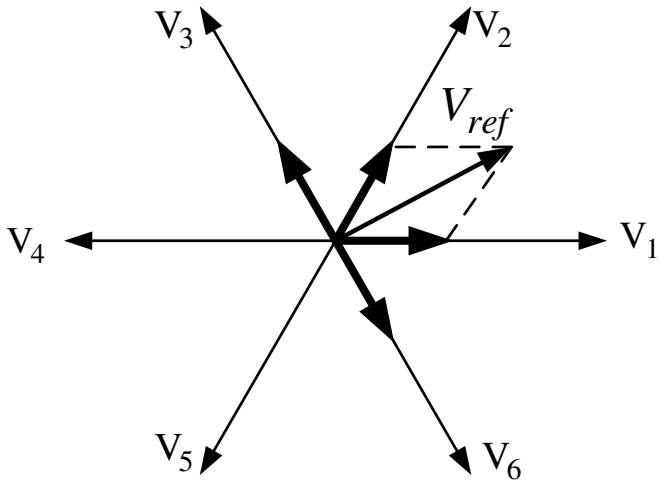


Figure 2.11 The AZSPWM voltage space vectors.

$$d_{i+1} = \frac{2\sqrt{3}}{\pi} M_i \sin(\theta - \frac{(i-1)\pi}{3}) \tag{2.7}$$

$$d_i = \frac{2\sqrt{3}}{\pi} M_i \sin(\frac{i\pi}{3} - \theta) \tag{2.8}$$

$$d_{i-1} = d_{i+2} = (1 - d_{i+1} - d_i)/2 \tag{2.9}$$

The AZSPWM1 method proposed in [13] involves only 60^o jumping vectors. For example, as shown in Table 2.1, in the region A1 the sequence 3216123 is utilized and results in 60^o output voltage vector rotation during every commutation. The AZSPWM2 method utilizes the sequence 6213126 and it results in 120^o jumps in the output voltage vectors during commutation from the active vectors (V_1 and V_2) to the active zero vectors (V_3 and V_6) [8]. In Table 2.1 the sequence of voltage vectors for both methods are listed for all regions. Inverter switch state pulse patterns and CMV pulse patterns of AZSPWM1 and AZSPWM2 are given in Figure 2.12 for region A1. The CMV is reduced when utilizing AZSPWM1 or AZSPWM2 methods and equal to $-V_{dc}/6$ or $+V_{dc}/6$ [8], [13].

Table 2.1 Voltage vector sequences of AZSPWM methods.

	A1	A2	A3	A4	A5	A6
AZSPWM1	3216123	4321234	5432345	6543456	1654561	2165612
AZSPWM2	6213126	1324231	2435342	3546453	4651564	5162615

The performance characteristics, advantages and disadvantages of AZSPWM1 and AZSPWM2 are different from each other. The most important disadvantage of AZSPWM2 is the practical implementation constraints. As seen from Figure 2.13 in AZSPWM2 simultaneous switchings are required. For example in region A1, V_2 is applied just after V_6; that means phase-b should be turned on just at the same time as phase-c is turned off. However due to dead-time between switchings and the unequal switch transient times, this simultaneous switching can not be realized. During the dead-time, instantaneous voltage of the corresponding phase is not defined by the switch states and is defined by the polarity of the phase current. Therefore according to the polarity of the phase currents unwanted zero states may occur, causing high common mode voltage. For example, in region A1 if both i_b and i_c are negative (according to the polarity definitions in Figure 1.1), CMV is $V_{dc}/2$ during the dead-time as Figure 2.13 illustrates. Even if the dead-time compensation is done accordingly, due to the non-idealities of the switches, switching at the same instant is practically impossible.

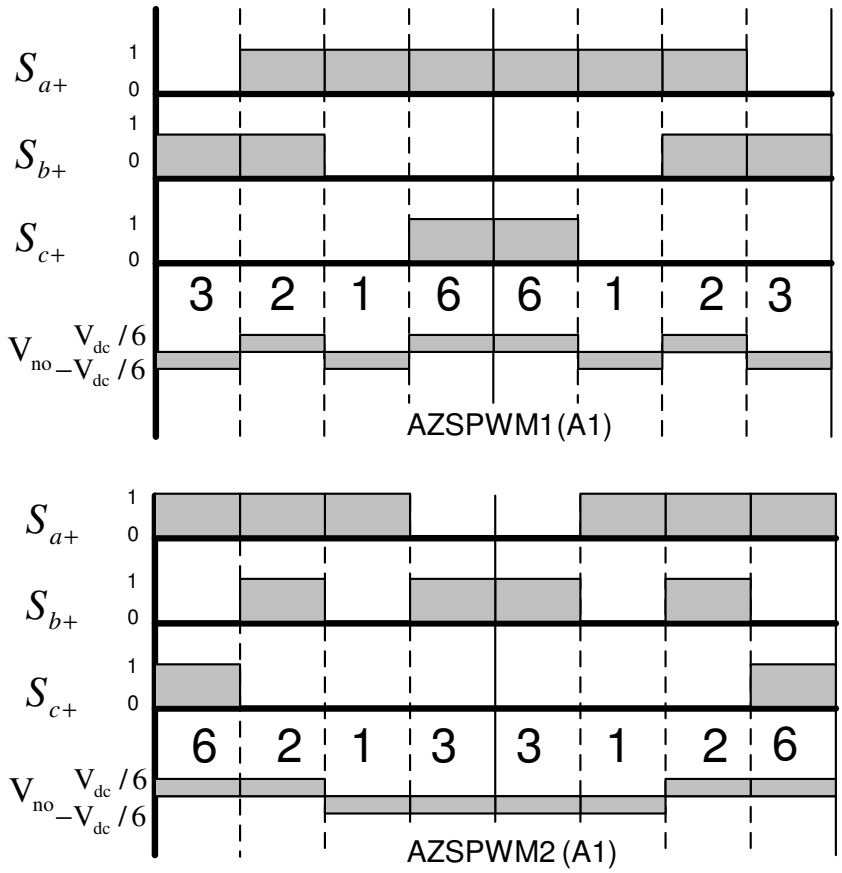


Figure 2.12 PWM pulse patterns of AZSPWM1 and AZSPWM2 in region A1.

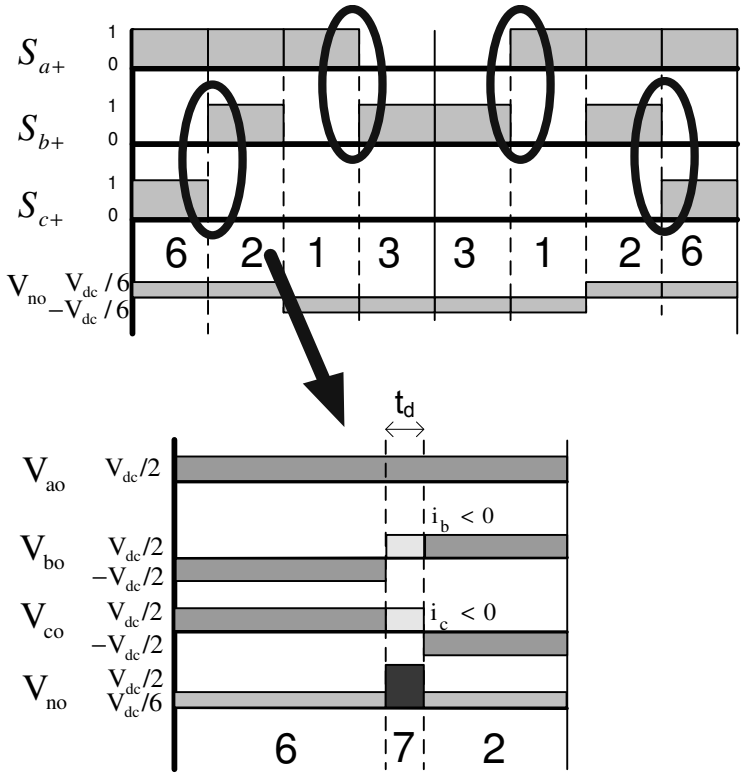


Figure 2.13 The inverter dead-time related performance problems of AZSPWM2.

2.4.2 Remote State PWM

The Remote State PWM (RSPWM) methods [14] synthesize the output voltage from three inverter voltage vectors that are 120^o apart from each other (most remote vectors). RSPWM methods [14] utilize the vector group $V_1V_3V_5$ and/or $V_2V_4V_6$ in various sequences. In Figure 2.14 the voltage space vectors of RSPWM are illustrated. In Figure 2.14.a voltage vector group of "$V_1V_3V_5$" is utilized and in Figure 2.14.b voltage vector group of "$V_2V_4V_6$" is utilized to synthesize the reference voltage vector (V_{ref}).

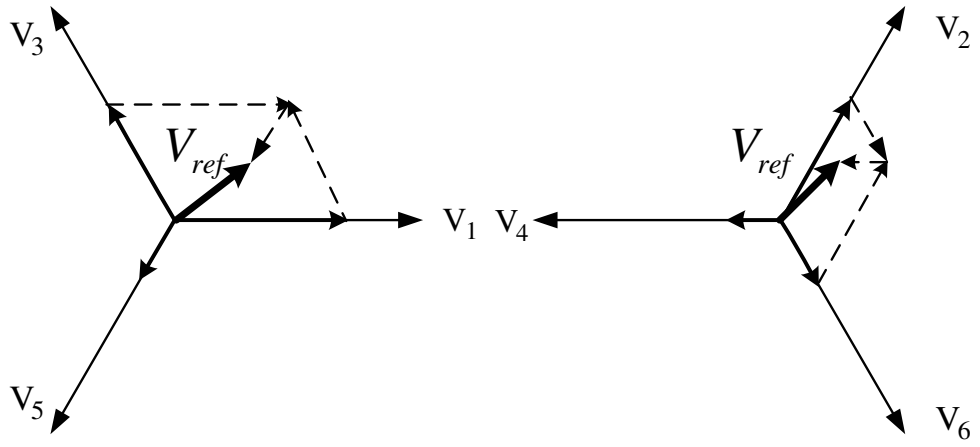


Figure 2.14 The RSPWM voltage space vectors utilizing: (a) V_1, V_3, V_5 (b) V_2, V_4, V_6.

RSPWM methods are divided into three subgroups according to their utilization of the voltage vector groups and their sequences [8].

RSPWM1 is the simplest way of the implementation of RSPWM. RSPWM1 utilizes only one vector group (either $V_1V_3V_5$ or $V_2V_4V_6$) and applies the vectors in a fixed sequence throughout the voltage vector space. Thus, there exist three sequence possibilities and three pulse patterns per group, yielding a total of six pulse patterns. Although there are six different pulse pattern possibilities available, all of them are symmetrical and the performance attributes of all of them are equivalent to each other over a fundamental cycle. Therefore from now on only the sequence (V_3-V_1-V_5-V_1-V_3) is considered as RSPWM1.

In RSPWM2, only one group of voltage vectors is utilized throughout the voltage vector space. However, in this case unlike RSPWM1 variable sequence is selected. With the output voltage distortion minimization being the performance criterion, the sequence is varied in a specific manner. Two patterns yielding high output current quality performance are displayed in Table 2.2 as RSPWM2A (utilizes $V_1V_3V_5$) and RSPWM2B (utilizes $V_2V_4V_6$). Since these two pulse patterns are symmetrical and

the performance attributes of both of them are equivalent to each other over a fundamental cycle and from now on RSPWM2A is considered as RSPWM2.

RSPWM3 involves utilization of both vector groups (alternating each group every 60^o) and also applies variable sequence as shown in Table 2.2 according to the region definitions of Figure 2.4.b (B-type regions). Utilizing this combination of remote state voltage vectors provides optimum output current quality performance and widest voltage linearity range. As a general rule RSPWM3 utilizes the voltage vectors V_i, V_{i+2} and V_{i-2} for region Bi and the duty cycles of these voltage vectors are calculated in the following.

$$d_i = \frac{1}{3} + \frac{2}{\pi} M_i \cos(\theta - \frac{(i-1)\pi}{3}) \tag{2.10}$$

$$d_{i+2} = \frac{1}{3} + \frac{2}{\pi} M_i \cos(\theta - \frac{(i-3)\pi}{3}) \tag{2.11}$$

$$d_{i-2} = \frac{1}{3} + \frac{2}{\pi} M_i \cos(\theta - \frac{(i+1)\pi}{3}) \tag{2.12}$$

Table 2.2 Voltage vector sequences of RSPWM methods.

	A1	A2	A3	A4	A5	A6
RSPWM1	31513	31513	31513	31513	31513	31513
RSPWM2A	31513	13531	13531	15351	15351	31513
RSPWM2B	42624	42624	24642	24642	26462	26462
	B1	B2	B3	B4	B5	B6
RSPWM3	31513	42624	13531	24642	15351	26462

In Figure 2.15 inverter switch state pulse pattern and CMV pulse pattern of RSPWM3 are given for region B1. Note that when RSPWM3 is utilized, CMV is reduced and fixed at $-V_{dc}/6$ throughout the B1 region [8]. The CMV characteristics of RSPWM methods are tabulated in Table 2.3. The RSPWM1 method (assuming

sequence V_3-V_1-V_5-V_1-V_3) has a constant CMV of -V_{dc}/6 throughout the fundamental cycle. Similarly RSPWM2A and RSPWM2B have constant CMVs of -V_{dc}/6 and V_{dc}/6, respectively. The CMV of RSPWM3 alternates at every 60^o periods between -V_{dc}/6 and V_{dc}/6 (Table 2.3)

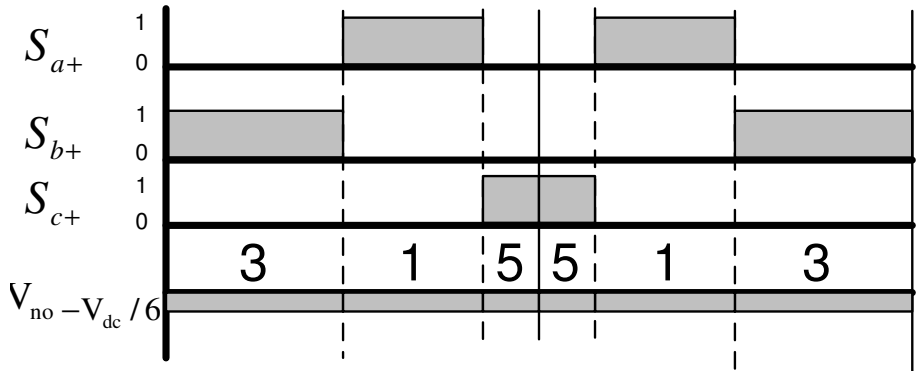


Figure 2.15 PWM pulse pattern of RSPWM3 in region B1 and the resulting CMV pattern.

Table 2.3 Common mode voltages of RSPWM methods.

	A1	A2	A3	A4	A5	A6
RSPWM1	-V_{dc}/6					
RSPWM2A	-V_{dc}/6					
RSPWM2B	V_{dc}/6					
	B1	B2	B3	B4	B5	B6
RSPWM3	-V_{dc}/6	V_{dc}/6	-V_{dc}/6	V_{dc}/6	-V_{dc}/6	V_{dc}/6

All RSPWM methods have practical constraints similar to the AZSPWM2 method such that simultaneous switchings are required at each switching instant. For the same reasons this simultaneous switchings can not be implemented and unwanted zero states may occur. As Figure 2.16 illustrates when $V_1V_3V_5$ voltage vectors are utilized, if a simultaneous switching is required between two phases with positive phase currents (according to the polarity definitions in Figure 1.1), CMV of –V_{dc}/2 is generated (similarly when $V_2V_4V_6$ voltage vectors are utilized CMV of V_{dc}/2 is generated, if simultaneous switching is required between two phases with negative

phase currents). Therefore implementations of the RSPWM methods are also problematic.

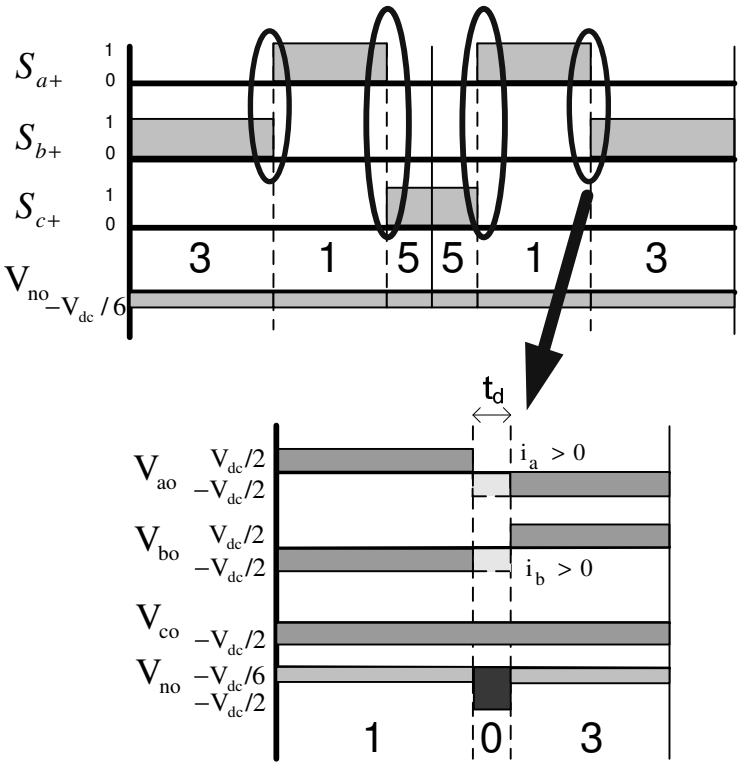


Figure 2.16 The inverter dead-time related performance problems of RSPWM3.

2.4.3 Near State PWM (NSPWM)

Developed throughout the research studies of this thesis, the Near State PWM (NSPWM) method utilizes a group of three neighbor voltage vectors to match the output and reference volt-seconds [15]. These three voltage vectors are selected such that the voltage vector, closest to reference voltage vector and its two neighbors (to the right and left) are utilized. Therefore, the utilized voltage vectors are changed in every 60^o throughout the vector space. Defined with indices, voltage vectors V_{i-1}, V_i, and V_{i+1} are utilized for region Bi. For example, for the region between 30^o and 90^o (B2), the applied voltage vectors are V_1, V_2, and V_3 (Figure 2.17). Investigations of

the voltage vectors of NSPWM and RSPWM shows the relationship between these two methods. RSPWM2A utilizes V_1, V_3 and V_5 while NSPWM utilizes V_1, V_2 and V_3 in the region B2. At low modulation index, the equation set of the duty cycles of RSPWM has a valid solution. However at higher M_i the duty cycle of V_5 is calculated as less than "0" in region B2. Negative duty cycle of V_5 corresponds to utilization of V_2 which is the opposite voltage vector of V_5. By utilizing V_2 instead of V_5, the NSPWM vectors are obtained.

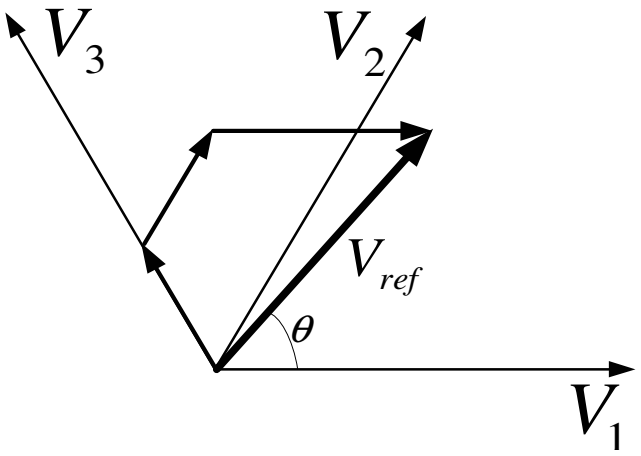


Figure 2.17 Illustration of the NSPWM space vectors for B2.

Utilizing the near state voltage vectors; the complex variable volt-seconds balance equation and the PWM period constraint for NSPWM are given in generalized form for region Bi (2.13 and 2.14) where T_s is the PWM period [15].

$$V_{i-1}t_{i-1} + V_i t_i + V_{i+1}t_{i+1} = V_{ref}T_s \tag{2.13}$$

$$t_{i-1} + t_i + t_{i+1} = T_s \tag{2.14}$$

Normalizing the voltage vector on-time values, to the PWM period the vector duty cycles are found as $d_k = t_k / T_s$, where k: i-1, i, i+1. Utilizing the above equations, the duty cycles of the required voltage vectors are calculated for region Bi as follows.

$$d_{i-1} = 1 - \frac{2\sqrt{3}}{\pi} M_i \sin(\theta - \frac{(i-2)\pi}{3}) \tag{2.15}$$

$$d_i = -1 + \frac{3}{\pi} M_i \cos(\theta - \frac{(i-2)\pi}{3}) + \frac{3\sqrt{3}}{\pi} M_i \sin(\theta - \frac{(i-2)\pi}{3}) \tag{2.16}$$

$$d_{i+1} = 1 - \frac{3}{\pi} M_i \cos(\theta - \frac{(i-2)\pi}{3}) - \frac{\sqrt{3}}{\pi} M_i \sin(\theta - \frac{(i-2)\pi}{3}) \tag{2.17}$$

The above equations yield a valid solution at high modulation indices and at low M_i there is no solution. With the constraints of minimum switching count, no simultaneous switchings of phase legs, and minimum CMV, only the sequence as a general form of V_{i+1}-V_i-V_{i-1}-V_i-V_{i+1} remains feasible for region Bi. For example, between 30^o and 90^o (B2), the optimal sequence is V_3-V_2-V_1-V_2-V_3. In this sequence, state changes occur only between adjacent states and this is the only sequence which does not require simultaneous switching of the inverter legs. The sequence of NSPWM is shown in Table 2.4 for region definitions of Figure 2.4.b.

Table 2.4 Voltage vector sequences of the NSPWM method.

	B1	B2	B3	B4	B5	B6
NSPWM	21612	32123	43234	54345	65456	16561

The switch state and CMV pulse patterns of NSPWM are given in Figure 2.18 for region B2. The CMV is $+V_{dc}/6$ or $-V_{dc}/6$ when NSPWM method is utilized. Also NSPWM has discontinuous behavior such that as Figure 2.18 illustrates, in region B2 phase-c is locked to the negative DC bus. The locked phase is alternating at every 60^o of the vector space. Therefore NSPWM is a discontinuous PWM method and its switching losses are less than those of continuous PWM methods.

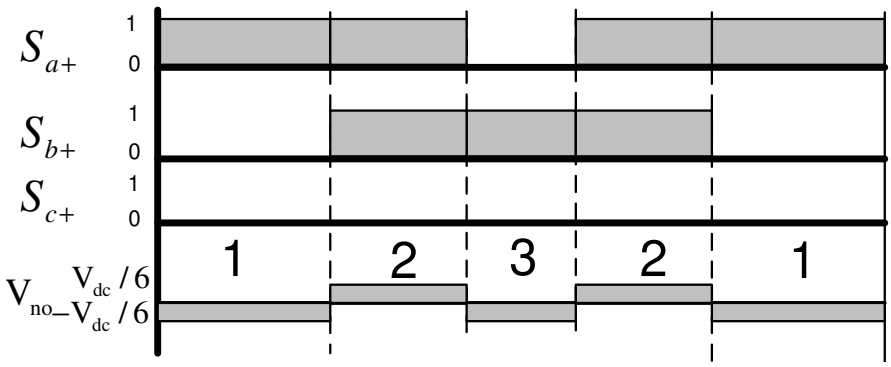


Figure 2.18 Inverter switch state and PWM pulse pattern of NSPWM in region B2.

The PWM pulse pattern of NSPWM can also be implemented by scalar implementation. The modulation signals of NSPWM are exactly the same as those of DPWM1. Therefore on-off state duty cycle of each phase is equal for DPWM1 and NSPWM. However for DPWM1, the PWM pulses of each phase are located at the edges of the PWM carrier period but for NSPWM, the PWM pulses of one phase are located at edges and those of the other phase are located at the center of the PWM carrier cycle (Third phase is always locked). Therefore the voltage space vectors of NSPWM and DPWM1 differ. Generation of the pulse pattern of NSPWM is achieved by utilizing two carrier waves (V_{tri} and $-V_{tri}$) instead of one carrier wave. The choice of the triangle to be compared with the modulation signals is region dependent and is given in Table 2.5. For example in B2, the modulation signal of phase *"b"* is compared with V_{tri} while the modulation signal of phase *"a"* is compared with $-V_{tri}$ (phase "c" is locked) and the pulse pattern of NSPWM in B2 results.

Table 2.5 NSPWM region dependent carrier signals.

	B1	B2	B3	B4	B5	B6
Phase a	Locked	$-V_{tri}$	$-V_{tri}$	Locked	V_{tri}	V_{tri}
Phase b	V_{tri}	V_{tri}	Locked	$-V_{tri}$	$-V_{tri}$	Locked
Phase c	$-V_{tri}$	Locked	V_{tri}	V_{tri}	Locked	$-V_{tri}$

Figure 2.19 illustrates the reference voltages of all three-phases and the triangular carrier wave for NSPWM method at M_i=0.78 and M_i=0.39 (θ=70^o). At high M_i where NSPWM is linear this implementation gives voltage vector sequence of V_3-V_2-V_1-V_2-V_3. However as M_i decreases the duty cycle of V_2 gets narrower and at the boundary of the voltage linearity range it disappears. Under the voltage linearity range the voltage vector sequence is V_3-V_0-V_1-V_0-V_3 such that instead of V_2, V_0 is utilized. This pattern is different from the defined NSPWM pulse pattern and the utilization of a zero-voltage vector degrades the common mode voltage reduction attribute of NSPWM. In this operation mode V_{no} fluctuates between -V_{dc}/2 and -V_{dc}/6.

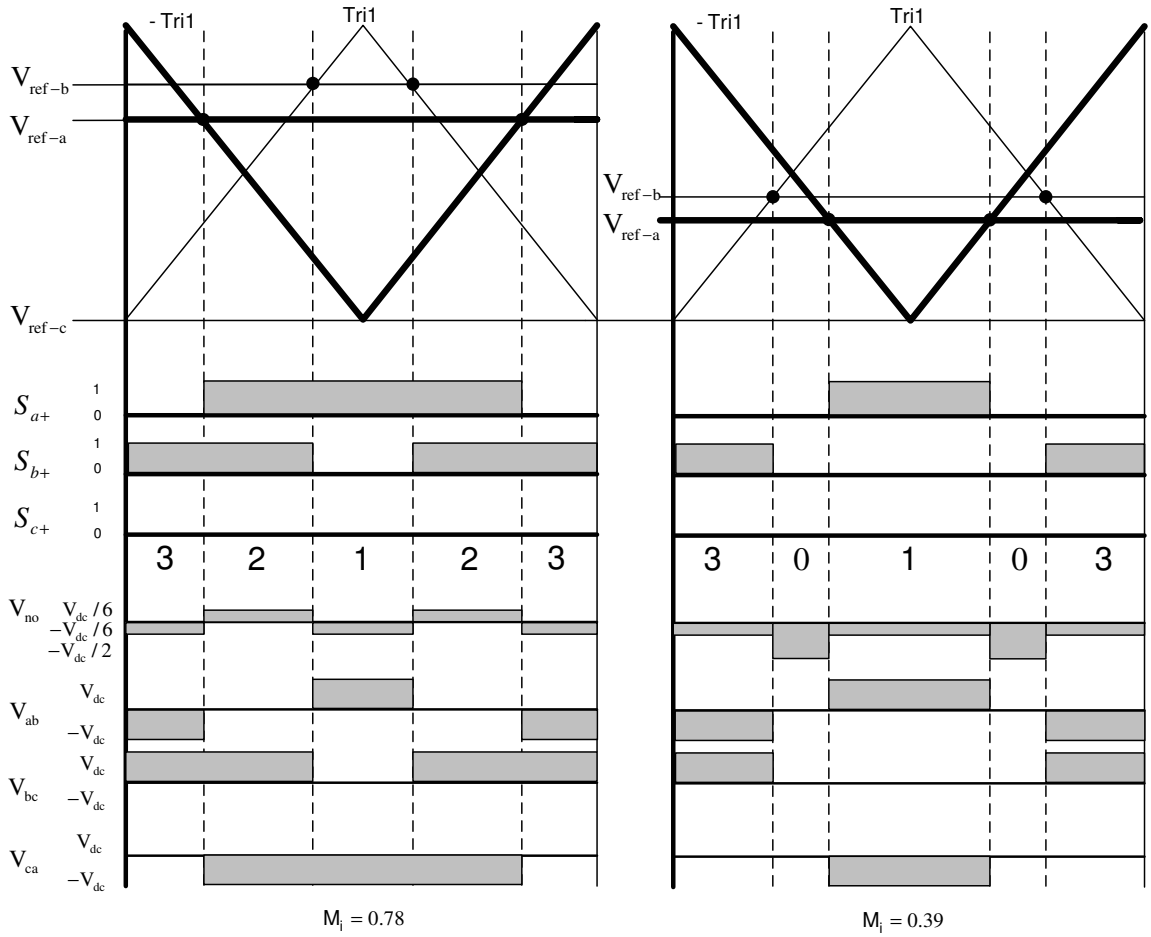


Figure. 2.19 Scalar implementation of NSPWM (region B2).

2.5 Performance Characteristics of PWM Methods

All standard PWM methods and RCMV-PWM methods utilize different voltage vectors with different sequences. They result in equal output voltage on the average, but their microscopic performances are unique.

The CMV characteristics of PWM methods were investigated in the previous sections and the results are tabulated at Table 2.6. It is found that all RCMV-PWM methods reduce the maximum CMV from $V_{dc}/2$ in magnitude to $V_{dc}/6$. The number of CMV changes occurring within a carrier cycle is also different for different PWM methods. In SVPWM and AZSPWM1 CMV changes 6 times; in DPWM1 and NSPWM CMV changes 4 times; in AZSPWM2 CMV changes twice in a carrier cycle; while for RSPWM methods CMV remains constant within a carrier cycle. The fundamental frequency of the resulting CMV is equal to that of the carrier frequency for SVPWM, DPWM1, and AZSPWM2. For AZSPWM1 and NSPWM the fundamental frequency of the resulting CMV is 3 f_s and 2 f_s respectively. For RSPWM1 and RSPWM2 the CMV is constant and for RSPWM3 the fundamental frequency of the resulting CMV is equal to three times of the fundamental frequency (f_e) of the inverter output voltage fundamental component. Given the properties of the CMV waveforms of the inverter, the inverter drive behavior will be experimentally investigated in the following chapters due to the difficulty in theoretically modeling and analyzing the CMV/CMC behavior of the practical system involving parasitic components effective at high frequency.

In addition to the CMV characteristics, other important characteristics of PWM methods must be taken into consideration during evaluation for practical applications. In order to make comparison between PWM methods, other performance attributes of the PWM methods which are inverter voltage linearity range, inverter input and output current waveform quality at a given switching frequency and inverter output line-to-line voltage pulse patterns are investigated in this section.

Table 2.6 CMV characteristics of PWM methods.

PWM Method	|CMV|	Number of dv_{no}/dt transitions per PWM cycle	Base f_{cmv}
SVPWM	$V_{dc}/2$	6	f_s
DPWM1	$V_{dc}/2$	4	f_s
AZSPWM1	$V_{dc}/6$	6	$3 f_s$
AZSPWM2	$V_{dc}/6$	2	f_s
RSPWM1	$V_{dc}/6$	0	NA
RSPWM2	$V_{dc}/6$	0	NA
RSPWM3	$V_{dc}/6$	0	$3 f_e$
NSPWM	$V_{dc}/6$	4	$2 f_s$

2.5.1 Voltage Linearity

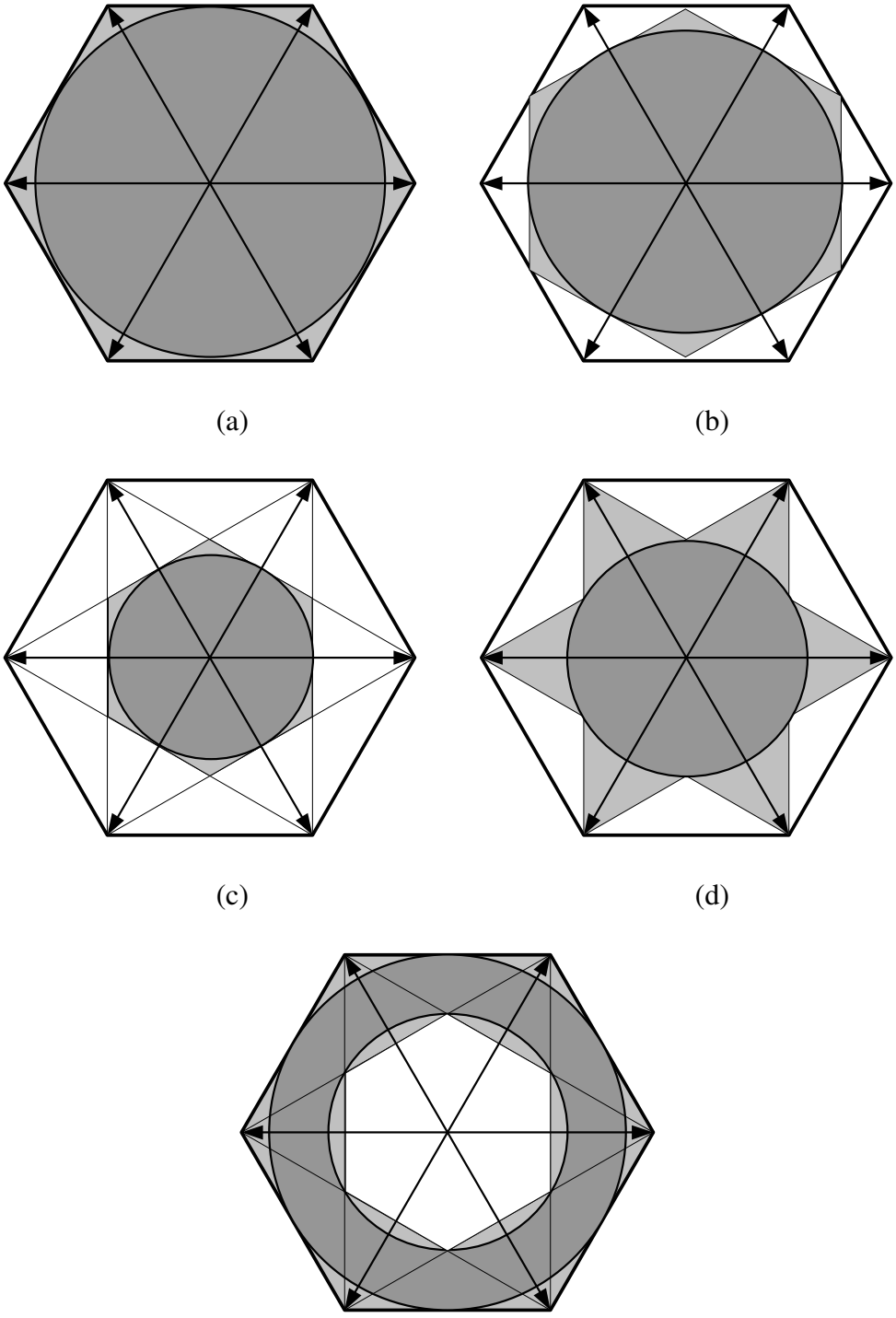
In the scalar PWM implementation, where the reference signal is compared with a triangular carrier signal, there is a linear relation between the reference signal and the output phase voltage. The operation range where this linear relation is satisfied is called voltage linearity region. However this linear relation is violated when the peak value of the reference signal is greater than triangular carrier signal peak value. Hence this region is called non-linear (overmodulation or undermodulation) region. In the non-linear overmodulation region output voltage is always less than the reference value [16].

In the space vector implementation of the PWM methods, volt-second balance equations can only be utilized in the linear region. In the non-linear region this equations do not have a valid solution such that some of the duty cycles of the voltage vectors are calculated as greater than “1” or smaller than “0”.

Since all PWM methods utilize different reference signals, all have different voltage linearity ranges. Voltage linearity range is an important characteristic of the PWM

methods since it is related with the maximum harmonic free output voltage that can be obtained from a VSI. Within the linearity range no low frequency harmonic voltages appear at the inverter output, thus it is preferable to have a wide voltage linearity range.

In Figure 2.20 voltage linearity ranges of various PWM methods are illustrated. In the figure the light shaded regions define the per-carrier-cycle voltage linearity regions and the dark shaded regions define the per-fundamental-cycle linearity regions. SVPWM, DPWM, AZSPWM1 and AZSPWM2 can utilize the full inverter voltage hexagon [5], [8]. Therefore their per-fundamental-cycle linearity range is $0 \leq M_i \leq 0.907$ which is defined by the circle tangent to the inverter voltage hexagon. SPWM provides a narrower per-fundamental-cycle voltage linearity range that is $0 \leq M_i \leq 0.785$ [5]. For RSPWM1 and RSPWM2 the inner triangles define the per-carrier-cycle voltage linearity range which corresponds to the per-fundamental-cycle voltage linearity range of $0 \leq M_i \leq 0.52$ [8]. RSPWM3 can utilize both triangles so its per-carrier-cycle voltage linearity range is the union of the two inner triangles which provides the per-fundamental cycle voltage linearity range of $0 \leq M_i \leq 0.61$ [8]. For NSPWM, upper boundary of voltage linearity region is defined by the inverter hexagon. Unlike all other methods for NSPWM there is also a lower boundary of the voltage linearity region. Inside the unshaded inner hexagon shown in Figure 2.20.e, the volt-second balance equations of NSPWM do not have a valid solution. So for NSPWM, the reference voltage vectors are generated between the inverter voltage hexagon and the inner hexagon. This corresponds to the per-fundamental-cycle voltage linearity range of $0.61 \leq M_i \leq 0.907$ [15].



(a) (b)

(c) (d)

(e)

Figure 2.20 Voltage linearity regions of: (a) SVPWM, DPWM, AZSPWM1 and AZSPWM2, (b) SPWM, (c) RSPWM1 and RSPWM2, (d) RSPWM3 and (e) NSPWM.

2.5.2 Output Current Waveform Quality

The inverter output voltage waveform quality is best studied with the aid of space vectors. A three-phase voltage source inverter can generate eight different voltage vectors (Figure 2.3). Voltage vectors are utilized to generate a reference voltage. The integral of the applied voltage vectors gives the inverter flux (Figure 2.21), which is a virtual quantity and the harmonic over this flux is proportional to the output current ripple.

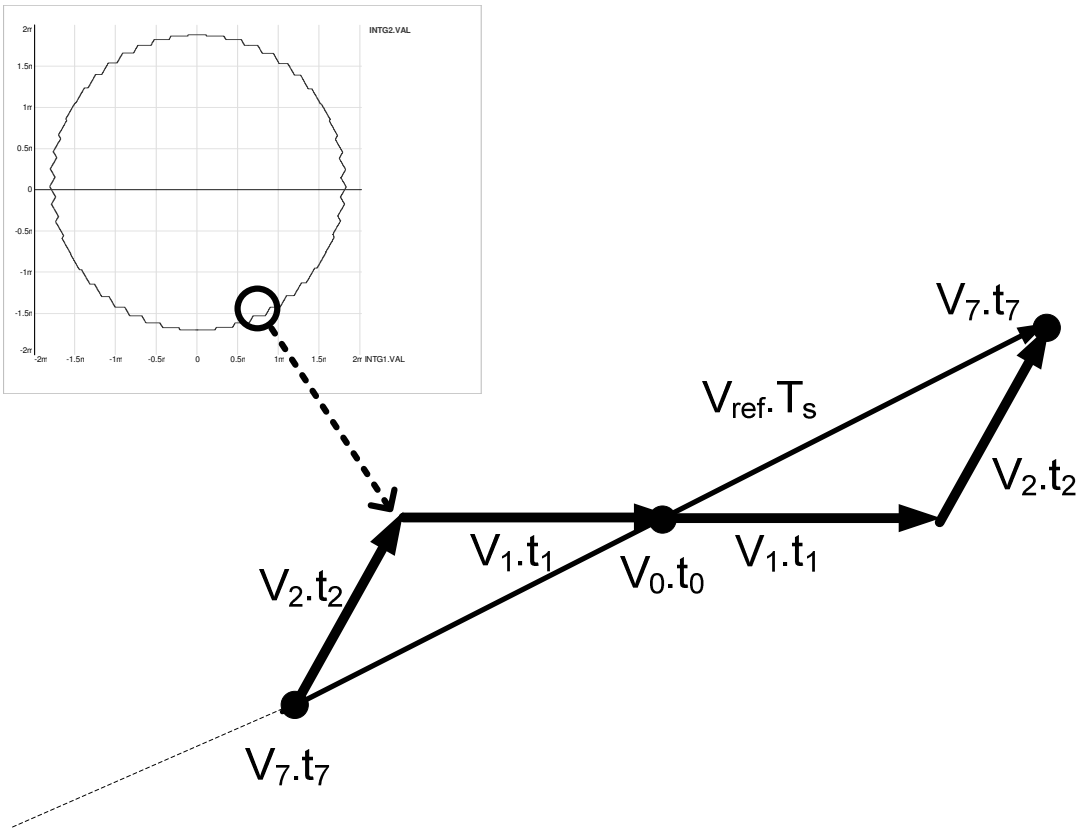


Figure 2.21 The inverter flux as a function of the applied voltage vectors.

The difference between the reference and the output voltage vector is the harmonic voltage vector (Figure 2.22). Since the switching frequency model of motor drives is the motor leakage inductance, the harmonic flux which is the integral of the harmonic voltage vector is proportional to the harmonic current in motor drives [5].

The current ripple has undesirable effects such as torque ripple and harmonic losses. Defined in (2.18), the harmonic flux over an arbitrary cycle (N^{th} cycle), is a measure of the ripple current for each PWM method where V_k is the applied voltage vector and V_{ref} is the reference voltage vector.. Since the fundamental period is much smaller than the PWM period, the reference voltage vector is fixed over a PWM cycle [5].

$$\lambda_h(M_i, \theta, V_{dc}) = \int_{(N-1)T_s}^{NT_s} (V_k - V_{ref})dt \tag{2.18}$$

Normalizing λ_h in the following, the harmonic performance can be comparatively evaluated for various modulation methods.

$$\lambda_{hn} = \frac{\pi}{V_{dc} T_s} \lambda_h \tag{2.19}$$

Since each PWM method differs in the utilization of the voltage vectors and their sequence, the harmonic flux vector of each PWM method is unique. Therefore shape of the flux trajectories of each PWM is also unique. For example, the SVPWM voltage vector sequence in sector A1 is $V_7V_2V_1V_0V_1V_2V_7$ and results in the two-symmetric-triangles harmonic flux trajectory shown in 2.22.a [5] In the same sector, the trajectories of AZSPWM1 are of double-diamond shape (Figure 2.22.b). The AZSPWM2 trajectories resemble double-arrowhead shape; however in Figure 2.22.c in order to illustrate the trajectory clearly only the harmonic flux trajectory at first half of the PWM period is drawn. The harmonic flux trajectory at the second half of the PWM period is the symmetrical of the first one. All of the RSPWM trajectories resemble the butterfly shape (Figure 2.22.d) [8]. Similarly the trajectories of the NSPWM also resemble butterfly shape but their orientation is different than those of RSPWM (Figure 2.22.e) [18].

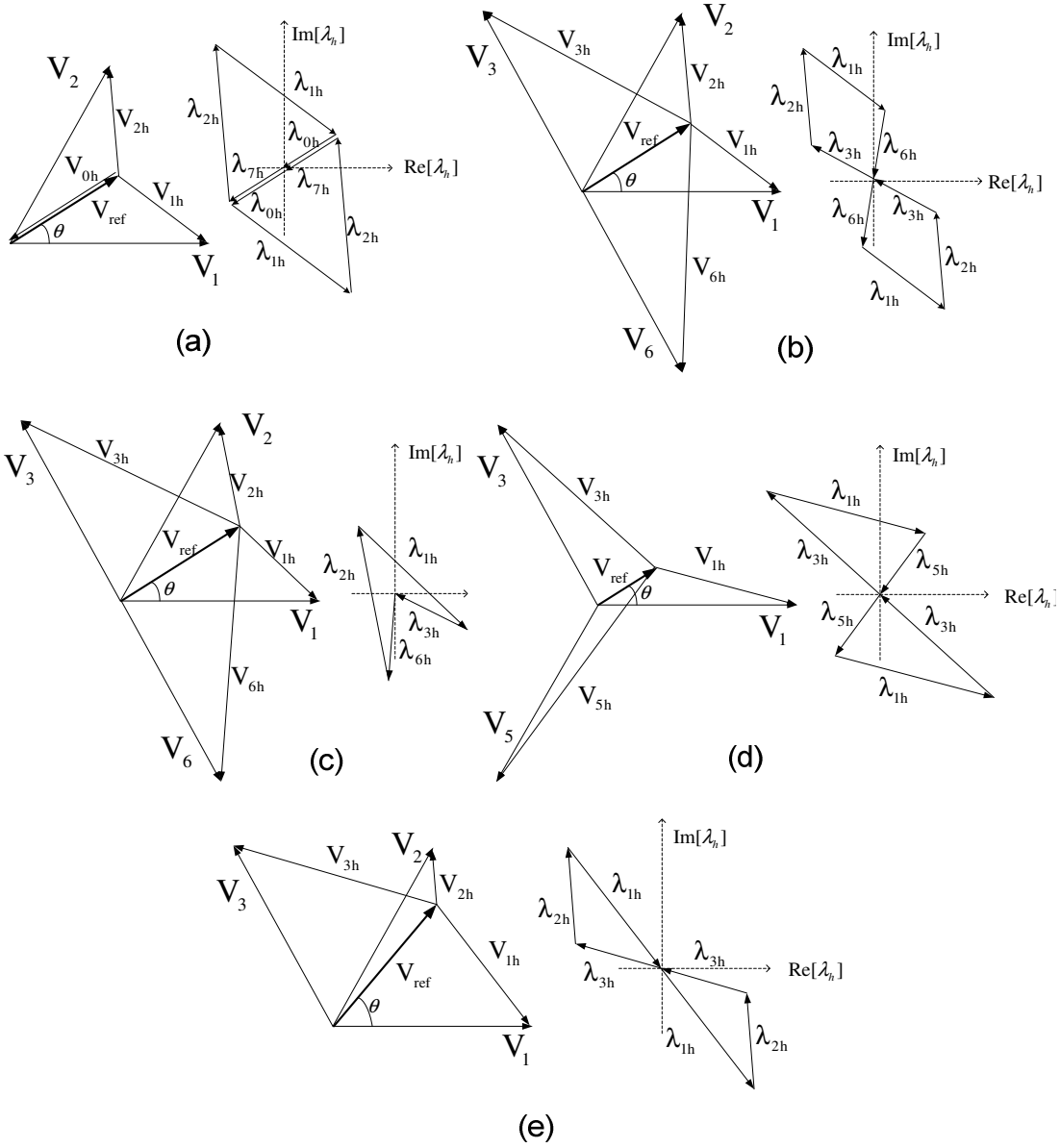


Figure 2.22 Harmonic flux vectors and harmonic flux trajectories of: (a) SVPWM, (b) AZSPWM1, (c) AZSPWM1, (d) RSPWM and (e) NSPWM.

The harmonic flux trajectories of each PWM method vary depending on the angle and the magnitude of the reference voltage vector. The trajectories of the standard PWM methods such as SVPWM and DPWM were reported in [5]. In this thesis, the RCMV-PWM trajectories and their dependency on M_i and θ are evaluated.

Shown in Figure 2.23, the AZSPWM1 trajectories are strongly dependent on θ and M_i. For constant θ, the harmonic flux vector magnitude increases with decreasing M_i, implying large ripple current. For constant M_i, the harmonic flux is minimum at $\theta=0^o$ and $\theta=60^o$ and the harmonic flux increases as θ approaches 30^o. At low M_i, the θ dependency of the harmonic flux trajectories is less significant but at high M_i size of the harmonic flux trajectories are strongly dependent on θ. The harmonic flux trajectories of AZSPWM2 are illustrated at Figure 2.24. In AZSPWM2, just like in AZSPWM1 the harmonic flux trajectories get smaller with increasing M_i. However the θ dependency shows different trends at high and low M_i. At $M_i=0.61$ the harmonic flux trajectories are the smallest at $\theta=30^o$ and get larger significantly as it approaches 0^o and 60^o. On the contrary, at $M_i=0.9$ the harmonic flux trajectories are the largest at $\theta=30^o$ and get smaller as θ approaches 5^o and 55^o. Another characteristic of the harmonic flux trajectories of AZSPWM2 is being center oriented unlike AZSPWM1. The main reason for this is that in AZSPWM2 voltage vectors remote from each other such as V_2 and V_6 are applied on the VSI successively. The harmonic voltage vectors of these voltage vectors result opposite effects on the harmonic flux trajectories.

In RSPWM3, the θ dependency of the harmonic flux trajectories is only investigated at $M_i=0.61$, since above this modulation index level, RSPWM3 looses its voltage linearity. Figure 2.25 illustrates the harmonic flux trajectories of RSPWM3. As the figure illustrates, the size of the harmonic flux trajectories decreases with increasing M_i and with decreasing θ.

The harmonic flux trajectories of NSPWM are illustrated in Figure 2.26. In NSPWM for constant θ, as M_i increases the harmonic flux trajectories get noticeably narrower. However, the θ dependency of the harmonic flux trajectories is not strong. Especially at low M_i the θ dependency is very difficult to observe, so only two extreme cases are illustrated. At $M_i=0.61$, the harmonic flux trajectories at $\theta=30^o$ and $\theta=90^o$ are exactly the same because in both operating points V_2 is not utilized at all and only V_1 and V_3 are utilized. The harmonic voltage vectors resulting from these voltage vectors are exactly opposite to each other, so a 2-dimensional harmonic flux

trajectory observed. As θ approaches 30^o the harmonic flux trajectories become different in shape and resemble a triangle, but the size is still very close to those of trajectories at θ=30^o and θ=90^o. At M_i=0.9 the shapes of harmonic flux trajectories are different for different θ values. However all of them have similar sizes.

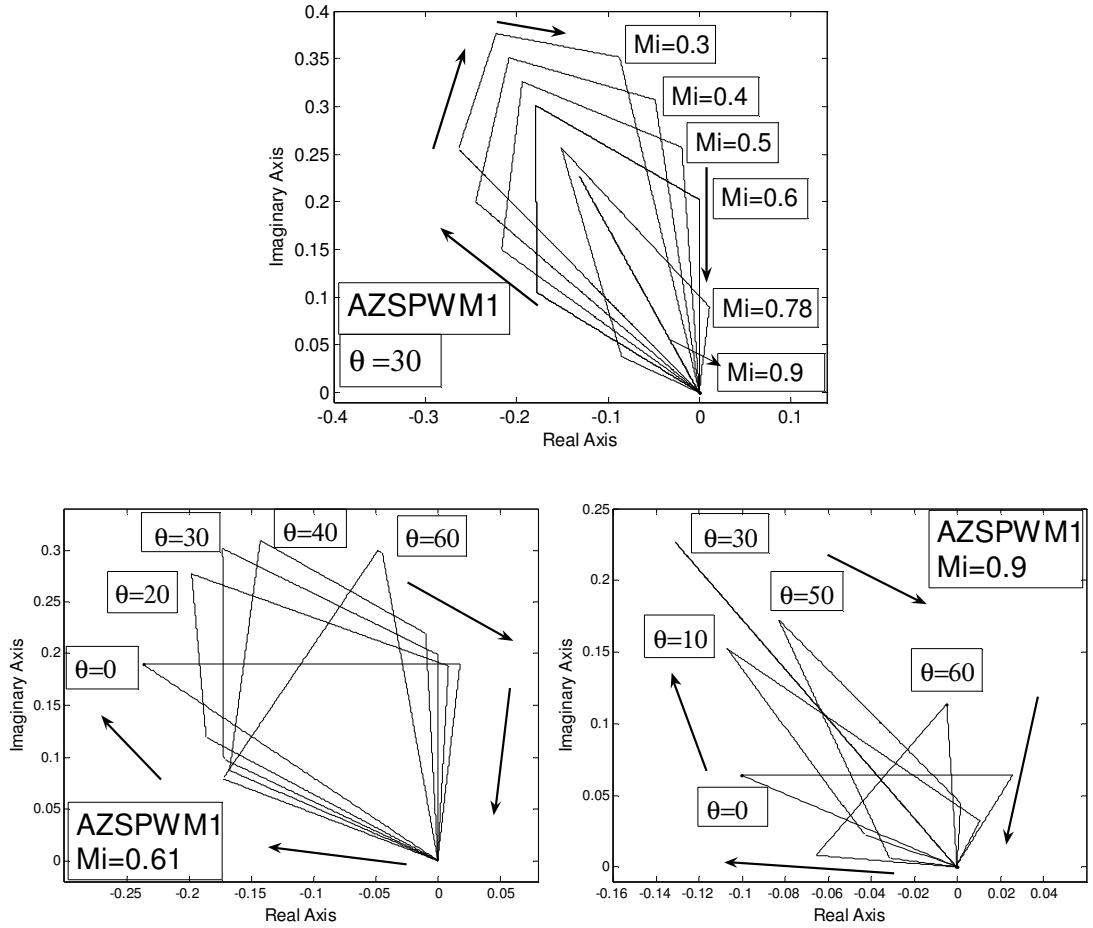


Figure 2.23 Parametric harmonic flux trajectories of AZSPWM1.

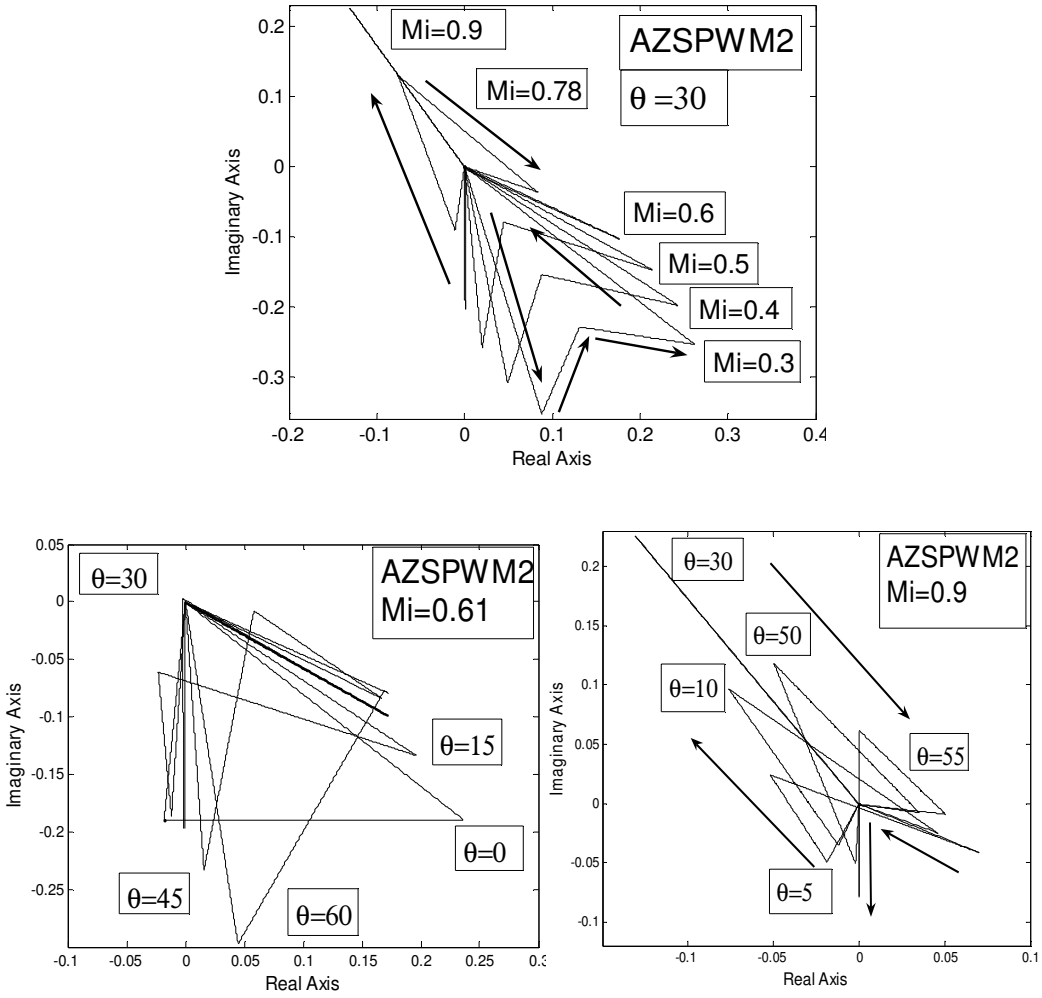


Figure 2.24 Parametric harmonic flux trajectories of AZSPWM2.

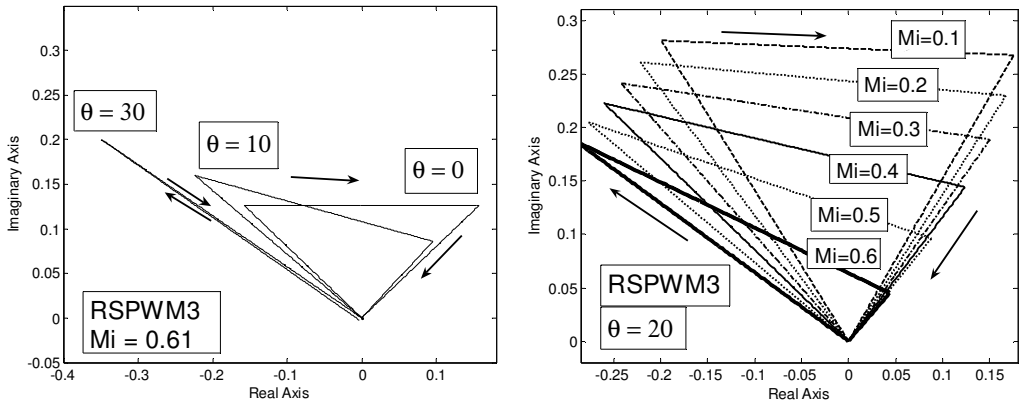


Figure 2.25 Parametric harmonic flux trajectories of RSPWM3.

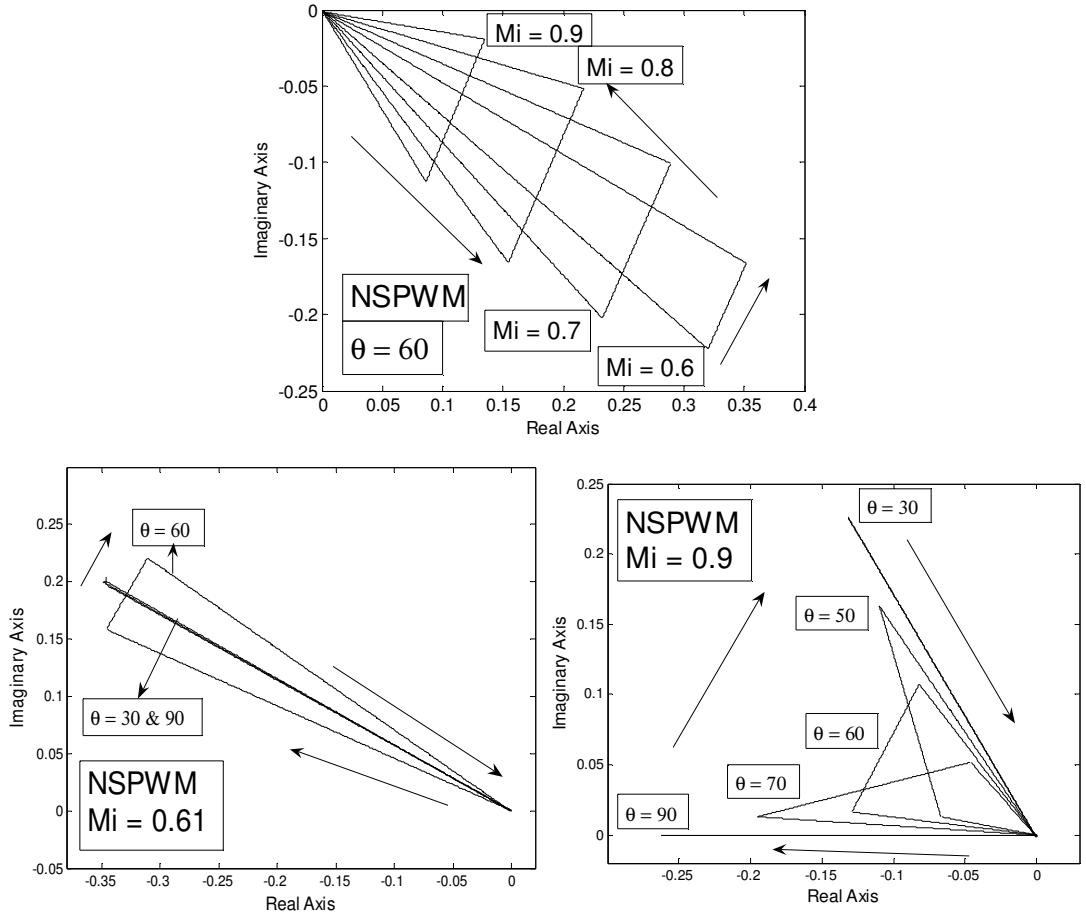


Figure 2.26 Parametric normalized harmonic flux trajectories of NSPWM.

The instantaneous deviation of harmonic flux trajectories from the origin can be seen with the harmonic flux vectors. To show the harmonic content clearly, the magnitudes of the harmonic flux vectors can be illustrated over a half PWM cycle with the time axis normalized to T_s. The area below this harmonic flux curve is directly proportional to the harmonic content of the PWM method [18].

In the following, the harmonic flux vector magnitudes of SVPWM, DPWM1, AZSPWM1, AZSPWM2, RSPWM3 and NSPWM will be discussed in comparison. Harmonic fluxes are studied at M_i=0.61 and at M_i=0.9 for two different θ values, $\theta=30^o$ and $\theta=60^o$. In Figure 2.27, the harmonic flux vector magnitudes over a half PWM cycle are shown. For M_i=0.9 and $\theta=30^o$, all methods utilize only V_1 and V_2 with exactly the same duty cycles. Therefore the shapes and the magnitudes of the

harmonic flux vectors of all methods are exactly the same. As θ approaches 60^o, the harmonic flux trajectories of the PWM methods differ. The magnitudes of the harmonic flux vectors of NSPWM are larger than those of all other PWM methods. The harmonic flux vector magnitudes of AZSPWM1 and AZSPWM2 are symmetrical and equivalent to each other. DPWM1 has slightly less harmonic flux than AZSPWM methods and SVPWM has the least harmonic flux.

At M_i=0.61 and θ=30^o the shapes and the magnitudes of the harmonic flux vectors of NSPWM and RSPWM3 are exactly the same and have similar magnitudes to that of AZSPWM1. The harmonic flux vector magnitudes of these three methods are significantly larger than the other methods. AZSPWM2 and SVPWM have the least harmonic flux and their harmonic content is very close to each other. DPWM1 has lower harmonic content than AZSPWM1 and NSPWM but it is still slightly inferior to AZSPWM2 and SVPWM. At M_i=0.61 and θ=60^o AZSPWM1, AZSPWM2 and NSPWM methods have very large harmonic flux and among the three NSPWM has slightly larger harmonic flux. RSPWM3 and DPWM1 have comparable harmonic flux magnitudes that are much lower than those of other RCMV-PWM methods. For this M_i and θ, SVPWM has the least harmonic content.

The harmonic flux trajectories are not convenient for overall comparison of ripple performance of PWM methods. For this purpose, the below defined integral quantities are employed. The normalized harmonic flux vector RMS value over a PWM cycle (duty cycle δ of 0 to 1) is calculated as follows [5].

$$\lambda_{hn-rms}(M_i,\theta) = {K_f}^2 \sqrt{\int_0^1 {\lambda^2}_{hn}\, d\delta} \qquad (2.20)$$

All PWM methods do not have the same number of commutations per PWM cycle. The ratio of the number of switching per PWM cycle of a PWM method to that of CPWM methods is defined as K_f. A PWM method with less switching per PWM cycle results in less switching losses and it is possible to operate at higher switching frequencies and operating at higher switching frequencies decreases the load current

ripple. In order to make a fair comparison, all methods should be operated at the same number of commutations per fundamental cycle, so the switching (carrier) frequency of each method must be divided by K_f which is shown in Table 2.7. Thus, the harmonics of a PWM method are scaled with the K_f factor and the square-RMS harmonic flux is scaled with K_f^2 [5].

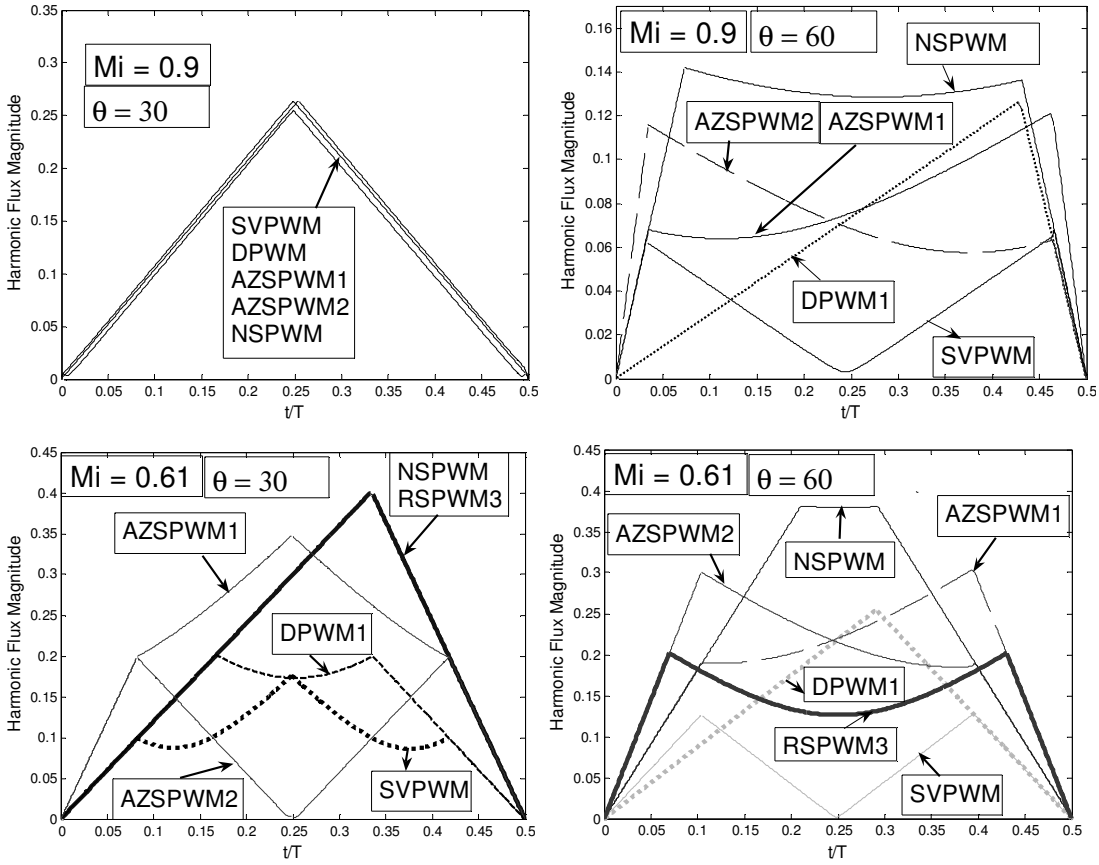


Figure 2.27 Normalized harmonic flux magnitudes of PWM methods.

Table 2.7 The number of commutations per-carrier-cycle and K_f.

	# Commutations	K_f
CPWM & AZSPWM1	6	1
DPWM	4	2/3
NSPWM	4	2/3
RSPWM	8	4/3
AZSPWM2	10	5/3

The RMS harmonic flux over a PWM cycle can be analytically calculated or numerically evaluated via computational software. Due to the complexity of the switch pulse patterns, the calculations of the PWM methods have been carried numerically via MATLAB and for the integration the Euler method is used. Over a PWM cycle, 1000 data points are utilized in order to obtain accurate results. The RMS value of the harmonic flux is calculated for various PWM methods for M_i=0.61 (low modulation) and 0.9 (high modulation). Figure 2.28 and Figure 2.29 illustrate that the square-RMS harmonic flux is strongly dependent on θ. At low modulation (M_i=0.61), CPWM and DPWM methods provide the lowest harmonic flux square-RMS. The RCMV-PWM methods have larger distortion than these methods. The harmonic content of NSPWM is flat and much lower than the other RCMV-PWM methods. The harmonic content of the other methods AZSPWM1, AZSPWM2 and RSPWM3 are space dependent and significantly high.

At high modulation (M_i=0.9), as Figure 2.29 illustrates, DPWM methods provide the lowest harmonic content. Performance of NSPWM is slightly inferior to DPWM but it has significantly less harmonic content than the other PWM methods. AZSPWM1 and SVPWM have comparable harmonic contents, and AZSPWM2 has space dependent and very high harmonic content.

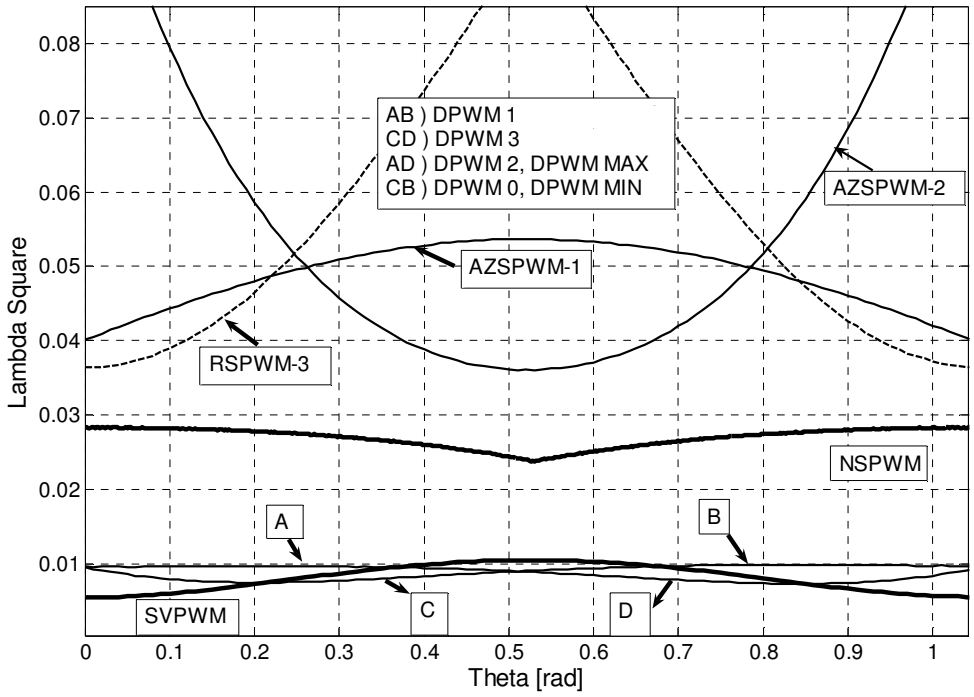


Figure 2.28 $\lambda_s^2=f(\theta)$ spatial variation for $M_i=0.61$.

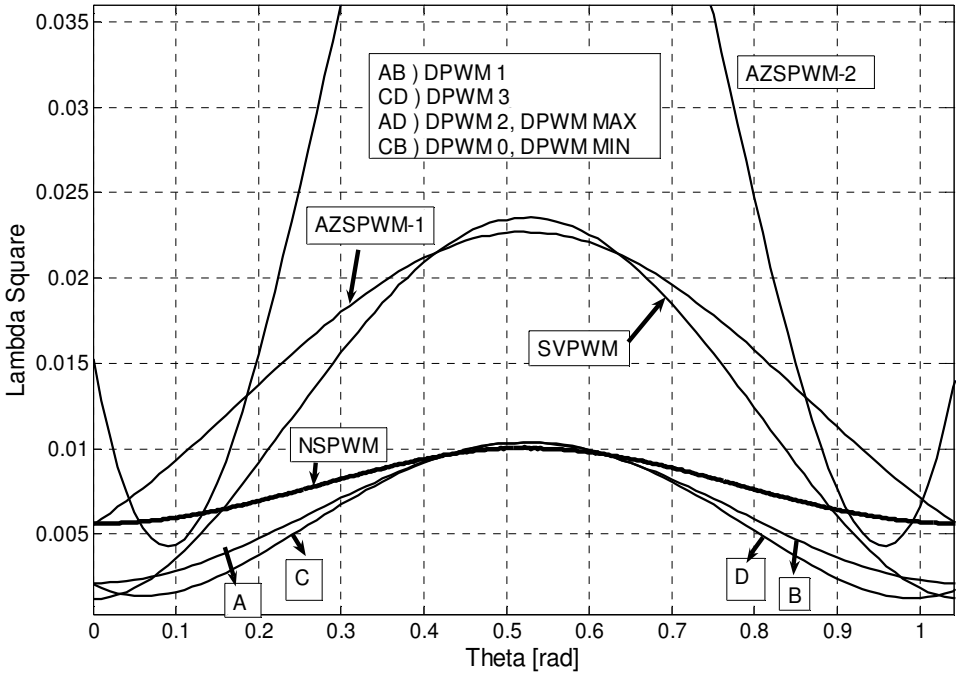


Figure 2.29 $\lambda_s^2=f(\theta)$ spatial variation for $M_i=0.9$.

Taking the average value of the local RMS harmonic flux function over the full fundamental cycle (spanning the whole vector space) and scaling it with $288/\pi^2$, the Harmonic Distortion Factor (HDF) which is a true measure of AC current ripple RMS value, is calculated as follows [5].

$$HDF = f(M_i) = \frac{288}{\pi^2}\frac{1}{2\pi}\int_0^{2\pi} \lambda^2_{hn-rms}\, d\theta \tag{2.21}$$

The HDF function is only M_i dependent and each PWM method has a unique HDF characteristic. It can be calculated analytically or numerically. Due to the complexity of the switch pulse patterns, the calculations of the RCMV-PWM methods are performed numerically via MATLAB. The integral is calculated with the Euler method and the vector space is spanned with 628 data points for accurate results. The sample MATLAB code is provided in Appendix A.

As shown in Figure 2.30, over the wide range of the linear modulation range, the CPWM and DPWM methods provide lower HDF than the RCMV-PWM methods. Near zero M_i, the difference is in orders of magnitude. However, as M_i increases, the differences rapidly decrease. All RSPWM methods loose voltage linearity at about 0.5-0.6 modulation index. At the expiration point of linearity, HDFs of RSPWM methods are still significantly inferior to the standard methods. AZSPWM methods are linear throughout the inverter hexagon. At low M_i the harmonic content of AZSPWM1 is very high and very similar to that of RSPWM3, and the harmonic content of AZSPWM2 is even higher. As M_i increases the HDF performance of AZSPWM methods improves and both methods show similar characteristics. NSPWM is linear in the $0.61<M_i<0.907$ range and its curve is provided for a narrower range than other methods. The starting point of linearity range of NSPWM coincides with the expiration of voltage linearity range of RSPWM3. Similar to the other RCMV-PWM methods the harmonic content of NSPWM decreases with M_i. Throughout its linearity range, NSPWM has the least harmonic distortion among all RCMV-PWM methods. In its lower linear M_i range, NSPWM has higher harmonic content than the conventional PWM methods but in the higher end of the linear

modulation range, NSPWM performs better than CPWM methods and comparably with DPWM methods.

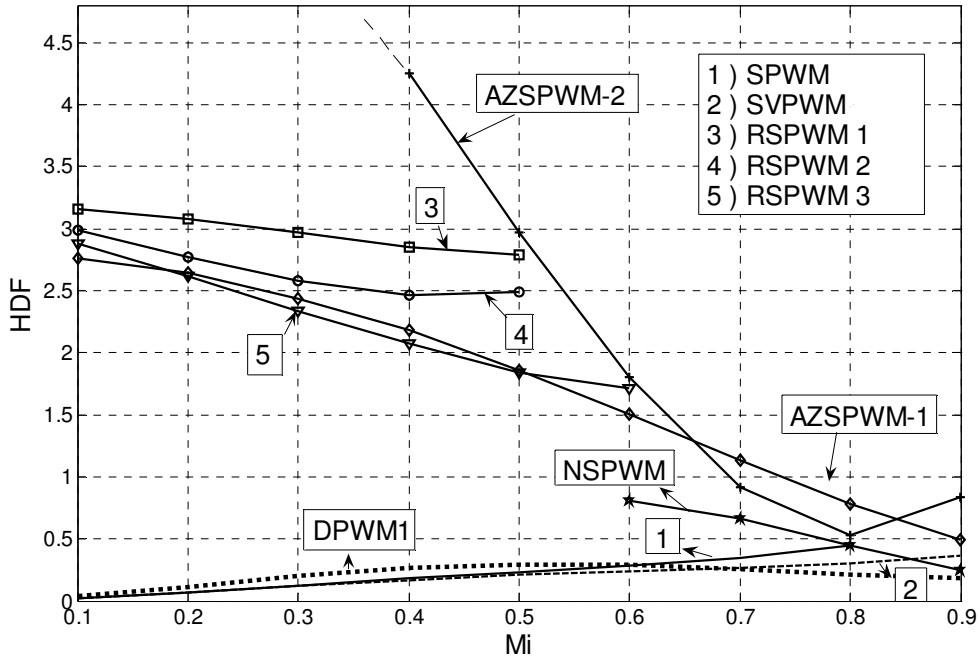


Figure 2.30 HDF=f(M_i) for various PWM methods.

2.5.3 Inverter DC Link Current Ripple

The DC link current of the inverter i_{in} (Figure 1.1), is composed of an average DC value and ripple over it and is important for DC bus capacitor sizing as the capacitor suppresses all the PWM ripple current. The DC link ripple current has limiting effect on the capacitor lifetime, so it should be as small as possible.

Each PWM method has a unique DC link current ripple characteristic. In order to compare the DC link current ripple performance of the PWM methods K_{dc} is defined in (2.22), as the ratio of DC link ripple rms current I_{inhrms} square to output phase current RMS value I_{1rms} square [5]. Smaller K_{dc} implies smaller capacitor requirement and longer capacitor life.

$$K_{dc} = I^2_{inhrms} / I^2_{1rms} \tag{2.22}$$

In (2.22) I_{inhrms} is calculated as (2.23) where (I_{inrms}) is the DC link rms current and (I_{inmean}) is the average DC link current.

$$I^2_{inhrms} = I^2_{inrms} - I^2_{inmean} \tag{2.23}$$

For given M_i and load power factor angleφ, K_{dc} is calculated as a function of θ. For all the methods discussed, (2.22) is analytically calculated. K_{dc} for the standard PWM methods is given in [5]. However K_{dc} of RCMV-PWM methods are different from those of the standard PWM methods and the K_{dc} formulas of RSPWM, AZSPWM and NSPWM are given in (2.24), (2.25), and (2.26) as a function of M_i and load power factor angle φ [8], [18]. Note that K_{dc} of all the RSPWM methods is the same. Likewise, K_{dc} of both AZSPWM methods is the same since K_{dc} is independent of sequence of the voltage vectors utilized.

$$K_{dc}^{RSPWM} = 1 + M_i \frac{6}{\pi^2} \cos 2\varphi - M_i^2 \frac{18}{\pi^2} \cos^2 \varphi \tag{2.24}$$

$$K_{dc}^{AZSPWM} = 1 - \frac{3\sqrt{3}}{2\pi} \cos 2\varphi + M_i \frac{9\sqrt{3}}{\pi^2} \cos 2\varphi - M_i^2 \frac{18}{\pi^2} \cos^2 \varphi \tag{2.25}$$

$$K_{dc}^{NSPWM} = 1 + (M_i \frac{24}{\pi^2} - \frac{3\sqrt{3}}{\pi}) \cos 2\varphi - M_i^2 \frac{18}{\pi^2} \cos^2 \varphi \tag{2.26}$$

Evaluating K_{dc} reveals important attributes of the modulators. In Figure 2.31, K_{dc} curves of various PWM methods are illustrated as a function of M_i with the power factor (PF=cos(φ)) as parameter. The RSPWM and NSPWM methods are analyzed only at their voltage linearity range. At low M_i, AZSPWM and RSPWM methods have several times higher DC link current ripple than the CPWM and DPWM methods. The power factor (PF) dependency of the K_{dc} of the RSPWM is low but the K_{dc} of the AZSPWM is strongly dependent on the PF and AZSPWM methods exhibit

larger ripple at low PF. At higher PF and M_i the DC link current ripple of the AZSPWM methods decreases and becomes comparable to those of the conventional methods due to the expiration of the active zero state duration. Similarly K_{dc} of NSPWM decreases with increasing M_i and PF. For PF=1, NSPWM has lower DC link ripple content than all other PWM methods. For PF of 0.8-0.9, K_{dc} of NSPWM is similar to those of AZSPWM methods and CPWM/DPWM methods. However, for the PF lower than approximately 0.6, K_{dc} of NSPWM is inferior to the other methods.

For practical motor drive applications at full-load the PF is close to unity and the motor runs at the rated current. Although the motor current is large, due to high PF, K_{dc} is small. At no-load, the motor PF is poor but the motor current is quite small compared to rated case. Here, K_{dc} is large but the magnitude of the ripple current remains small compared to that of the rated-load operating condition. Therefore, with NSPWM, the DC bus capacitor can be smaller compared to the conventional PWM methods.

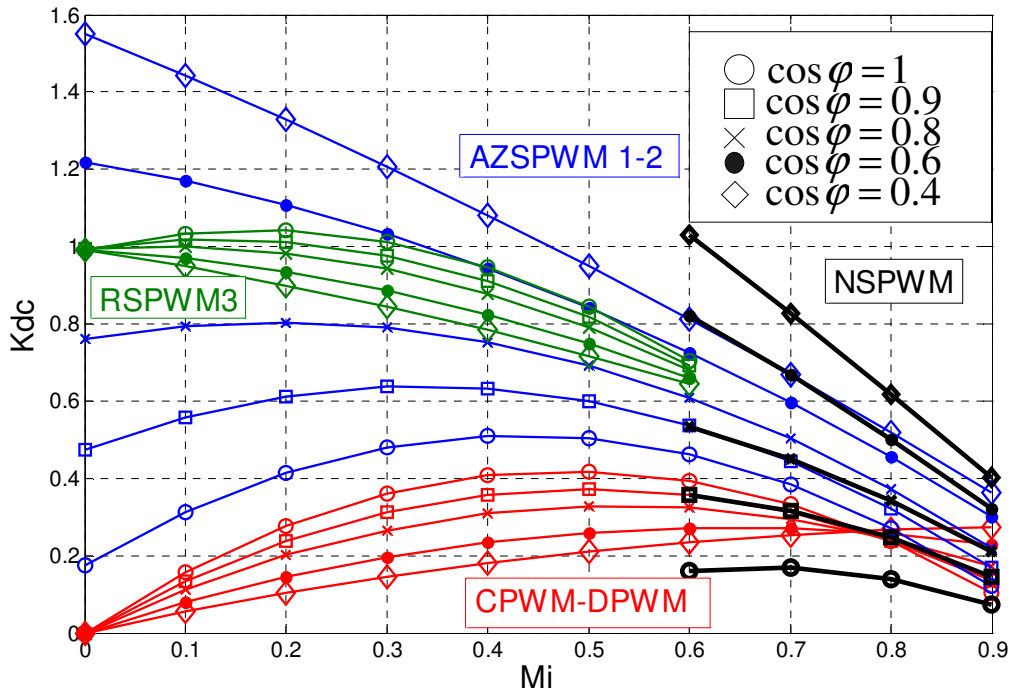


Figure 2.31 $K_{dc}=f(M_i,\cos\varphi)$ for various PWM methods.

2.5.4 Inverter Output Line-to-Line Voltage Characteristics

There are fundamental differences between the pulse patterns of the PWM methods. The line-to-line voltage patterns influence the inverter performance significantly in terms of switching transients and high frequency behavior. The inverter leg upper switch logic, CMV, and line-to-line voltage patterns for SVPWM, DPWM1, AZSPWM1, AZSPWM2, NSPWM, and RSPWM3 are shown in Figure 2.32.

As Figure 2.32 shows, the inverter output line-to-line voltage pulse patterns of CPWM and DPWM methods are unipolar such that the polarity of the line-to-line voltage does not change within a PWM cycle (there is pulse-polarity-consistency). All RCMV-PWM methods have bipolar patterns that generate undesirable effects such as high PWM ripple current and overvoltage transients. In motor drive applications involving long cables, two consecutive voltage pulses with opposite polarity must be separated by a sufficient time interval to damp the switching induced overvoltage due to voltage reflection [6]. When the pulses are close to each other and the polarity of pulses reverses rapidly (with high dv/dt) the switching transients may lead to very large voltage stresses at the load terminals. The high frequency model of an AC motor drive involves inductive and capacitive components. Applying sharp rising/falling voltage pulses results in voltage reflection phenomena which amplifies the motor terminal and front coil voltages to excessive values leading to winding failure. Therefore, methods with bipolar pulse pattern are not favorable unless the pulses are safely distant from each other. The zero-voltage time (t_z) is the time interval between the polarity reversals of the line-to-line voltages. In AZSPWM2 and RSPWM3 instantaneous polarity reversals always occur in every PWM cycle in two different line-to-line voltages. Therefore the zero-voltage time is zero regardless of M_i and θ. This problematic line-to-line output voltage pulse patterns prohibit their practical use. In AZSPWM1 and NSPWM, zero-voltage time intervals are function of M_i and θ and in NSPWM, the zero-voltage time interval between the two bipolar pulses is always greater than the AZSPWM1 case and sufficiently large for most of the NSPWM voltage linearity range. Thus, NSPWM differs in performance compared to other RCMV-PWM methods [15].

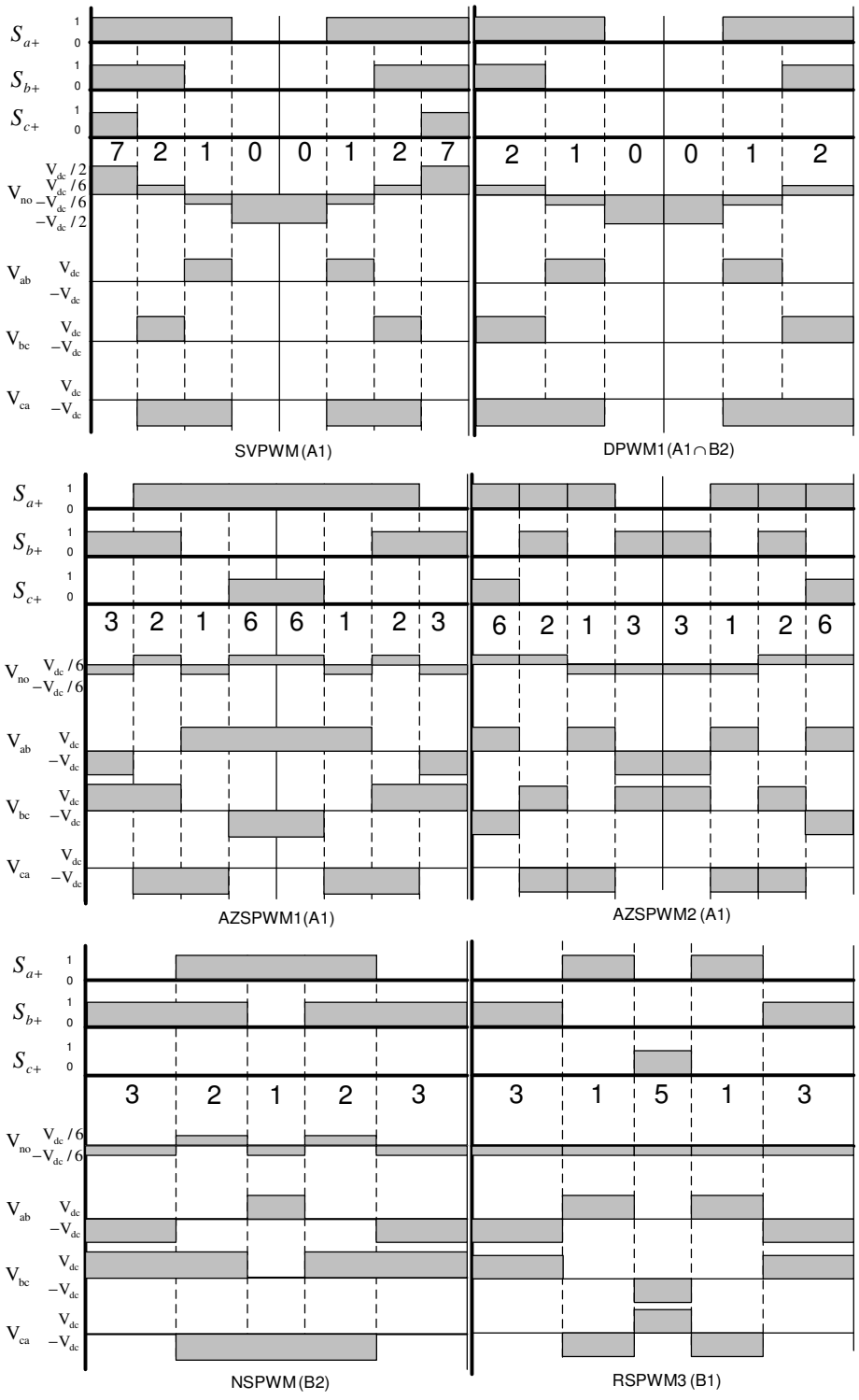


Figure 2.32 PWM Pulse pattern and line to line voltages of SVPWM, DPWM1, AZSPWM1, AZSPWM2, NSPWM and RSPWM3 methods.

For NSPWM, within each 60^o segment, only one line-to-line voltage has bipolar pulses and the duration of this zero-voltage time interval $t_{z\text{-}nspwm}$ can be calculated. For example, for region B2 it is given as in (2.27). For AZSPWM1 for each 60^o segment two line-to-line voltages have bipolar pattern. Therefore, two different zero-voltage time intervals $t_{z\text{-}azspwmx}$ and $t_{z\text{-}azspwmy}$ are defined. For example, for region A1, they are given as in (2.28) and (2.29), respectively. Normalizing the zero-voltage time intervals with the carrier cycle, the duty cycles of the zero-voltage time intervals is found [15].

$$t_{z-nspwm} = \left[-1/2 + (3/\pi)\cdot M_i \cos(60-\theta)\right]T_s \tag{2.27}$$

$$t_{z-azspwmx} = \left[(\sqrt{3}/\pi)\cdot M_i \sin(60-\theta)\right]T_s \tag{2.28}$$

$$t_{z-azspwmy} = \left[(\sqrt{3}/\pi)\cdot M_i \sin(\theta)\right]T_s \tag{2.29}$$

Figure 2.33 illustrates the zero-voltage time duty cycles of NSPWM ($d_{z\text{-}nspwm}$) over a 60^o segment in space with M_i as parameter. At high M_i there is always sufficient amount of zero-voltage time between the voltage pulses that change from $+V_{dc}$ to $-V_{dc}$ and vice versa. However, for lower M_i, the zero-voltage time gradually shrinks and for M_i=0.61 it expires at the boundaries (at 0^o and 60^o). As Figure 2.34 illustrates, for AZSPWM1 similar to NSPWM, zero-voltage time duty cycles ($d_{z\text{-}azspwmx}$ and $d_{z\text{-}azspwmy}$) get smaller with decreasing M_i. However, in this case the space (θ) dependency is stronger than M_i dependency. Regardless the value of M_i, $d_{z\text{-}azspwmx}$ expires at 0^o and $d_{z\text{-}azspwmy}$ expires at 60^o.

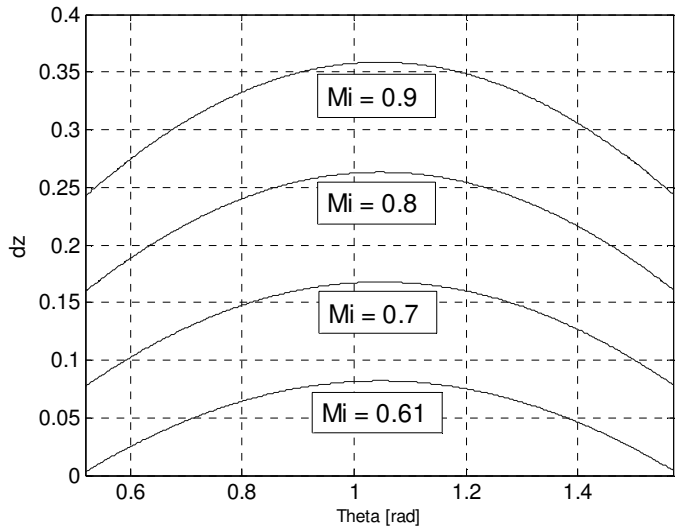


Figure 2.33 NSPWM Zero voltage time duty cycle d_{zNSPWM} for various M_i for region B2.

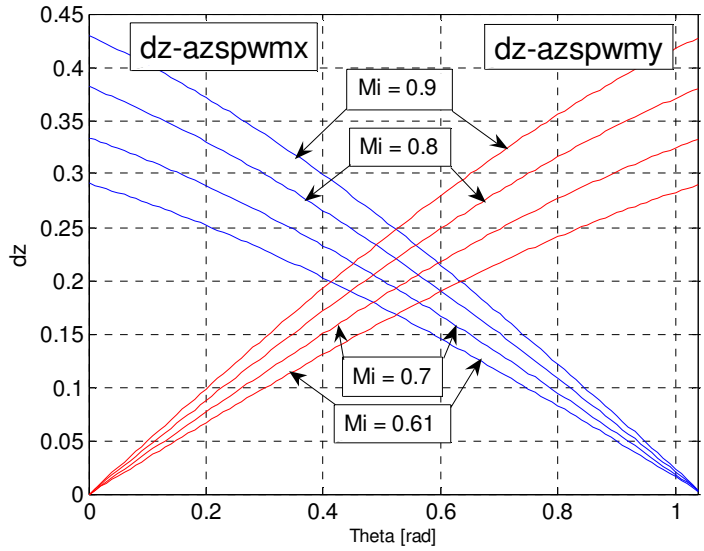


Figure 2.34 AZSPWM1 Zero voltage time duty cycles $d_{z\text{-}azspwmx}$ and $d_{z\text{-}azspwmy}$ for various M_i for region A1.

In Figure 2.35, duty cycle of the zero-voltage time interval (d_z) variation with respect to θ over a half fundamental cycle (d_z is periodic at π) for the inverter output line-to-line voltage V_{ab} is illustrated for both NSPWM and AZSPWM1. Both unipolar

(light) and bipolar (bold) voltage sections are considered. As the figure illustrates, for NSPWM the line-to-line voltage is bipolar for a total of 2x60°, while for AZSPWM1 the total is 2x120°. Also the figure indicates that the unipolar line-to-line voltage pulses of NSPWM are more distant from each other than those of AZSPWM1 [15].

The narrowest zero-voltage time intervals of bipolar pulses are most problematic in the application as they result in the largest overvoltage stresses. The narrowest d_z can be calculated from (2.27), (2.28), and (2.29) and are shown in Figure 2.36 with respect to M_i. For AZSPWM1 d_{zmin}=0 regardless M_i. For NSPWM the relation is linear with M_i. For example, for M_i=0.65 the duty cycle is 3%, corresponding to a sufficiently long time interval for the voltage pulses to settle. Thus, overvoltages are avoided. Given a minimum d_z constraint, the applicable M_i range of NSPWM can be found from the figure [15].

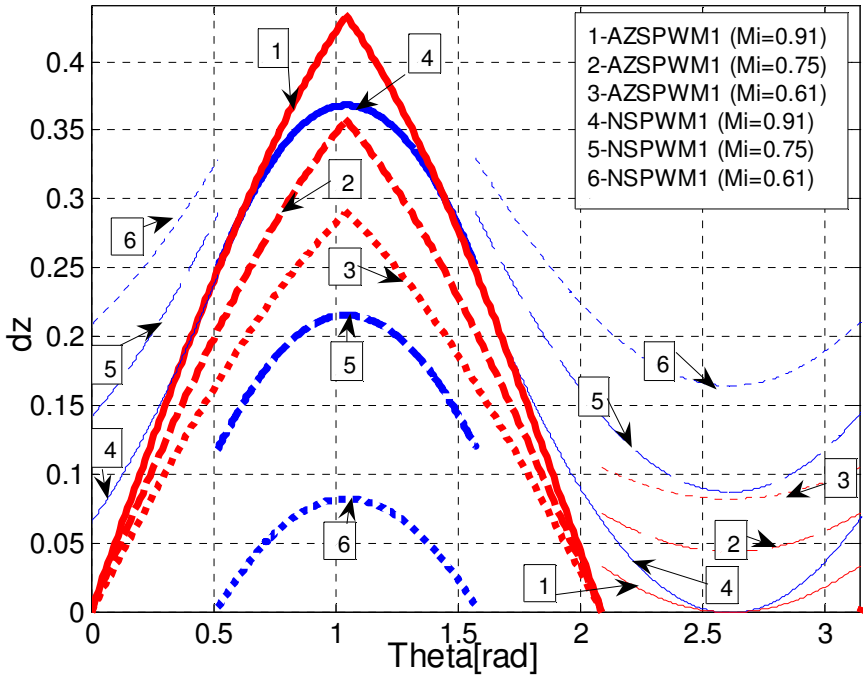


Figure 2.35 Variation of zero-voltage time interval duty cycle of the line-to-line voltages with respect to M_i and θ (Blue: NSPWM, Red: AZSPWM1).

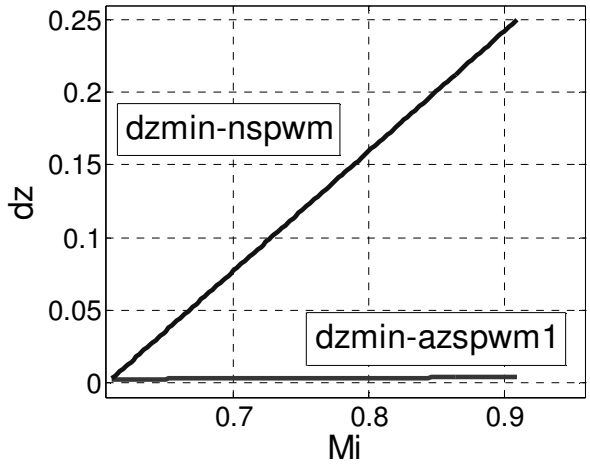


Figure 2.36 Minimum zero-voltage time duty cycles of NSPWM and AZSPWM1.

2.6 Combined Algorithm of PWM Methods

Theoretical and analytical performance analyses of PWM methods reveal that each PWM method has different performance attributes and none of them is the best overall PWM method. Standard PWM methods have less current ripple in AC and DC side of the inverter however they result in high CMV. NSPWM is satisfactory according to its harmonic content characteristics and results in low CMV but its voltage linearity range is narrow. AZSPWM1 has voltage linearity range of $0<M_i<0.91$ and results in low CMV but its overall performance characteristics are inferior. Therefore a decision flowchart of overall combined algorithm is proposed as illustrated in Figure 2.37. As seen in the figure if low CMV is required, NSPWM is utilized at high M_i and AZSPWM1 is utilized at low M_i and the transition decision is based on the fundamental component voltage magnitude value (effectively M_{icr} value). For example, $M_{icr}=0.61$ utilizes NSPWM outside the inner circle of Figure 2.20.e and inside the inner circle, AZSPWM1 is utilized. In this case at steady-state only one method is utilized per fundamental cycle. Similarly if there is no CMV restriction DPWM methods should be utilized at high M_i and SVPWM is utilized at low M_i [18]. In this algorithm, the transition between the methods is problem free as at the beginning of every PWM cycle the harmonic currents are reset.

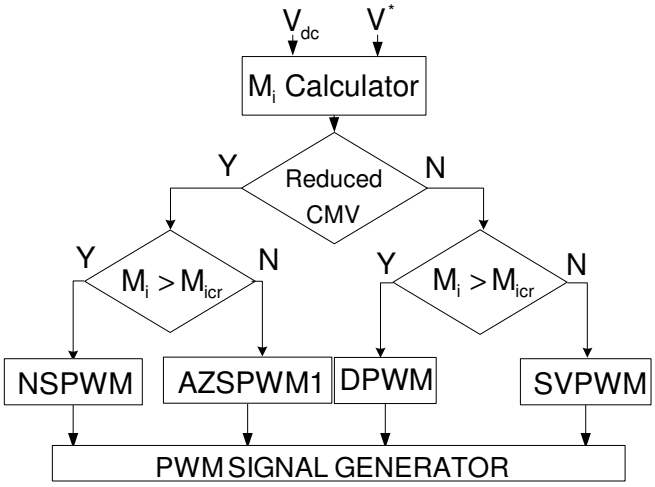


Figure 2.37 Decision flowchart of the combined modulation algorithm.

Also the decision can be based on the vector space region definition. In this case, inside the white region of Figure 2.20.e AZSPWM1 and outside it NSPWM is utilized such that at steady-state for $0.52<M_i<0.61$ NSPWM and AZSPWM1 alternate six times per fundamental cycle. For $M_i<0.52$ AZSPWM1 and for $M_i>0.61$ NSPWM are utilized.

2.7 Summary

In this chapter various PWM methods are reviewed and several new PWM methods developed and their performance attributes which are the voltage linearity range, output current harmonics (HDF), DC link current harmonics (K_{dc}), the output line-to-line voltage pulse pattern and the zero-voltage time (t_z) between polarity reversals at the output line-to-line voltage are investigated. The evaluation of the theoretical analysis of the performance attributes of the PWM methods is summarized and tabulated in Table 2.8. The table indicates that RCMV-PWM methods increase the harmonic content on both the AC and DC side of the inverter. However these harmonic contents are less at high M_i and PF. Of the RCMV-PWM methods only the NSPWM exhibits comparable HDF and K_{dc} performance to the standard methods at high M_i. Unlike other RCMV-PWM methods NSPWM does not result in practical

constraints such as requiring simultaneous switchings and having problematic output line-to-line voltage pulse pattern. The only drawback of the NSPWM is providing a narrower voltage linearity range such that it can not be utilized at low M_i. At low M_i AZSPWM1 is the best PWM method among the remaining RCMV-PWM methods. Therefore a combined algorithm is proposed for optimum performance, such that at low M_i AZSPWM1 and at high M_i NSPWM is utilized [18]. According to the proposed algorithm, if CMV performance is important, then the reduced CMV path is selected. Otherwise the conventional PWM methods are selected in the algorithm.

In the following chapter computer simulations will be provided in order to illustrate PWM performance attributes analyzed in this chapter.

Table 2.8 Performance attributes comparison of PWM methods (NA: not applicable).

	SVPWM	DPWM	AZSPWM1	AZSPWM2	RSPWM	NSPWM
CMV (v_{no})	High	High	Low	Low	Low	Low
Voltage Linearity Range	0-0.91	0-0.91	0-0.91	0-0.91	0-0.52 or 0-0.60	0.61-0.91
HDF (M_i>0.61)	Low	Low	High	High	NA	Moderate
HDF (M_i<0.61)	Low	Low	Very High	Extremely High	Very High	NA
Switching # per T_s	6	4	6	10	8	4
K_{dc} (M_i>0.61)& High PF	Low	Low	Low		NA	Lowest
K_{dc} (M_i>0.61)& Low PF	Low	Low	Moderate		NA	High
K_{dc} (M_i<0.61)& High PF	Low	Low	Moderate		High	NA
K_{dc} (M_i<0.61)& Low PF	Low	Low	Very High		High	NA
V_{ll} Pulse Pattern	Unipolar	Unipolar	2-Phase Bipolar	2-Phase Bipolar	3-Phase Bipolar	1-Phase Bipolar
Zero Voltage Time	NA	NA	Sometimes Problematic	Always Problematic	Always Problematic	Always Sufficient
Simultaneous Switching Requirement	No	No	No	Yes	Yes	No

CHAPTER 3

INPUT AND OUTPUT CURRENT RIPPLE PERFORMANCE ANALYSIS OF PWM METHODS BY MEANS OF COMPUTER SIMULATIONS

3.1 Introduction

In this chapter performance attributes of the standard PWM methods and the RCMV-PWM methods are investigated by means of computer simulations. First the simulation model of a VSI, feeding a three-phase AC induction motor is constructed. The equivalent parameters of the AC induction motor are obtained and the control of the VSI is programmed according to various PWM methods. The AC induction motor is operated at various loading levels and various speeds. Since the scope of this thesis involves the steady state performance of the PWM-based VSIs, the transient behavior of the AC motor is ignored and only the steady-state performance attributes are investigated. Important PWM methods which are NSPWM, DPWM1, SVPWM, AZSPWM1, AZSPWM2 and RSPWM3 are simulated first at M_i=0.61 and then at M_i=0.9 as representatives of low and high modulation index operating points, respectively. During the simulations important performance attributes of the PWM methods are emphasized which are the VSI output current ripple performance, the DC link current ripple performance, and the common mode voltage characteristics. Of these characteristics the VSI output current and the CMV are investigated under only no-load condition whereas the DC link current ripple is investigated under both no-load and rated-load conditions. In order to illustrate the feasibility of the combined algorithm of NSPWM and AZSPWM1 which was described in the previous chapter, the control algorithm of the simulation model is programmed and the simulations are conducted at M_i=0.57 where at steady-state each method becomes

active over a segment of the space and transition between the two methods occurs periodically. Finally the overall performance evaluation of the PWM methods is provided including the tabulated simulation results of the measured K_{dc} and peak-to-peak load current ripple. The measured quantities are compared with each other and the theoretically (analytically) calculated K_{dc} and HDF values.

3.2 Adjustable Speed Drive Simulation Model

In order to verify the theoretical results and to illustrate the PWM-based VSI performance attributes, computer simulations are conducted utilizing the Ansoft Simplorer simulation program [19]. The program is a graphic window based power electronic circuit simulator. In this simulation program in the schematic window, the power electronic circuit is constructed by picking, placing, and connecting the circuit components and the control blocks. Control of the power circuit is performed by programming control and/or equation blocks accordingly. After the circuit schematic is created and the simulation parameters are entered, simulations can be conducted. Selected waveforms such as voltage and current waveforms are illustrated by the graphic view window. The conducted simulation results are evaluated by the analysis-tools of the day-postprocessor window.

In the computer simulations, during the solution of equations, trapezoidal integration method is utilized. During steady-state performance analysis simulations of PWM-based VSIs, very fast control of any close loop operation is not required and therefore minimum simulation step size is selected as 1 μs (1/100 of the switching period) which is small enough to minimize the computational errors.

In practical ASDs, DC voltage is provided by rectifying the AC grid voltage by diode rectifiers and feeding DC-link capacitors with this rectified voltage. However this operation results in voltage fluctuations on the DC-bus when a current is drawn from the DC-bus by the VSI. In order to keep the output voltage at a constant fundamental rms value, modulation index (M_i) which corresponds to the DC-bus voltage

utilization level should be modified accordingly (DC-bus voltage disturbance rejection controller is applied). Whereas in these simulations, the performance attributes of the PWM methods need to be investigated at a definite M_i value. Therefore in the computer simulations AC/DC conversion of ASD is ignored and the VSI is fed by a constant DC voltage source of 500 V. In Figure 3.1 the simulation circuit diagram of the VSI is given.

In simulations during construction of the VSI, "system level" semiconductor components (IGBT and diodes) are utilized. Detailed device level models of these semiconductor components are avoided for the sake of simplicity since utilization of the detailed or simplified model equivalent parameters do not affect the investigated PWM performance attributes but increase the simulation run time substantially.

During the simulations, the three-phase induction motor model of the simplorer program is utilized. A 4-kW, 380-V, 4-pole, 1440 rpm induction motor is driven by a VSI and the motor parameters are calculated from a commercial motor with same ratings by the locked rotor and the no load tests. The calculated parameters are tabulated in Table 3.1.

Table 3.1 Induction motor T equivalent circuit parameters.

Stator Resistance	1.76 Ω
Stator Inductance	7 mH
Rotor Resistance (stator referred)	0.55 Ω
Rotor Inductance (stator referred)	7 mH
Magnetizing Inductance	165 mH

In the simulations of this chapter, only the PWM frequency range behavior is of interest. Frequencies involving several hundred kilohertz and above, where the motor capacitive parasitic circuit components and their effects begin to appear are not considered in the simulation. Modeling the motor and inverter high frequency

behavior is an involved task that is beyond the scope of this thesis. The motor behavior in this frequency range, which includes the common mode current, voltage behavior, is only investigated experimentally in Chapter 5. Thus, as far as the high frequency behavior, in this chapter only the common mode voltages could be investigated and the models are based on the fundamental equivalent circuit of the motor and inverter (which do not include the parasitic capacitances of the motor and inverter drive).

In the motor model of the Simplorer program the star point of the windings in not reachable. Thus, the CMV can not be directly observed in the simulations. Therefore, a virtual star point is created by a star connected resistor network in front of the motor. For this purpose ideal resistors with very high resistance values (1 MΩ) are utilized. The CMV is measured as the potential difference between the virtual star point and the midpoint of the DC-bus.

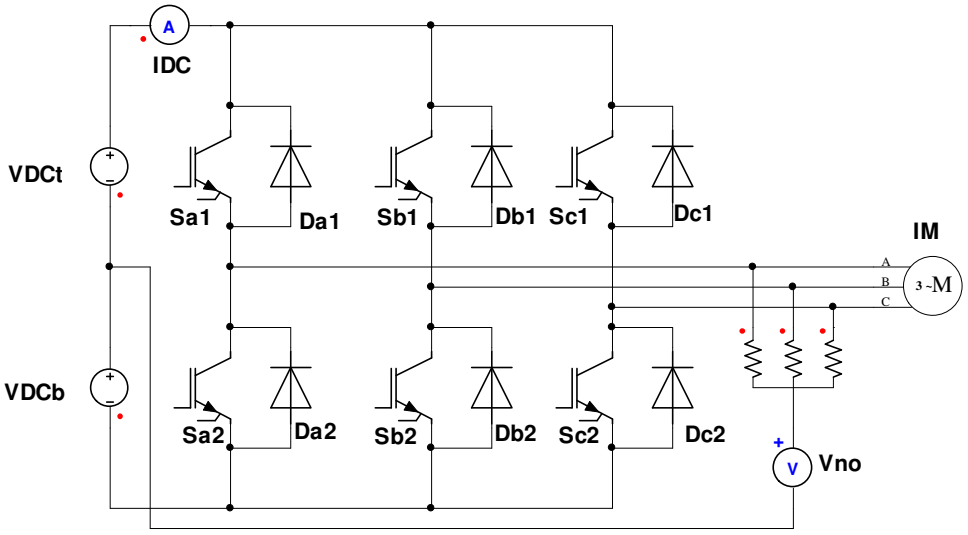


Figure 3.1 Three-phase ASD simulation model.

3.3 Simulation Results

In the simulations, the motor is driven by open-loop control and the constant V/f control algorithm is employed (176.7 V_{rms}/50 Hz). Various PWM methods are utilized to drive AC motor. In the simulations, the carrier frequency is 6.6 kHz for SVPWM and AZSPWM1, 10 kHz for NSPWM and DPWM1, 5 kHz for RSPWM3, and 4 kHz for AZSPWM2 ($f_{s\text{-}ave}$=6.6 kHz). This is done to obtain equal average switching frequency in all methods and a fair comparison can be provided among all methods. All methods are simulated at two different M_i values which are M_i=0.61 (137.6 V_{rms}/38.8 Hz) and M_i=0.9 (201.4 V_{rms}/57.3 Hz) corresponding to low and high modulation index values respectively. In all the simulations the DC bus voltage is fixed at 500V.

In the simulations, the load is modeled as fan type load such that the load torque is assumed to be proportional with the square of the motor speed. In the simulations two different loading conditions are tested at each modulation index, resulting in two different load power factors. For this purpose two different load torque profiles which simulate the operations under no-load and under rated-load are created and entered as simulation parameter. The load torque profiles are shown in Figure 3.2. Under no-load operation, the load torque is adjusted to be 1.3 Nm at the rated speed (1440 rpm) corresponding to the load power of 200W, simulating the friction and windage losses. Under rated-load operation, the load torque is adjusted to be 26.5 Nm at rated speed (1440 rpm) corresponding to the rated power of 4 kW. As Figure 3.2 illustrates, for both loading conditions the load torque increases with the motor speed and they are equal to the adjusted torque level at the rated speed (1440 rpm). Hence the load torque is less than the adjusted value for speeds less than the rated speed and it is higher for speeds higher than the rated speed.

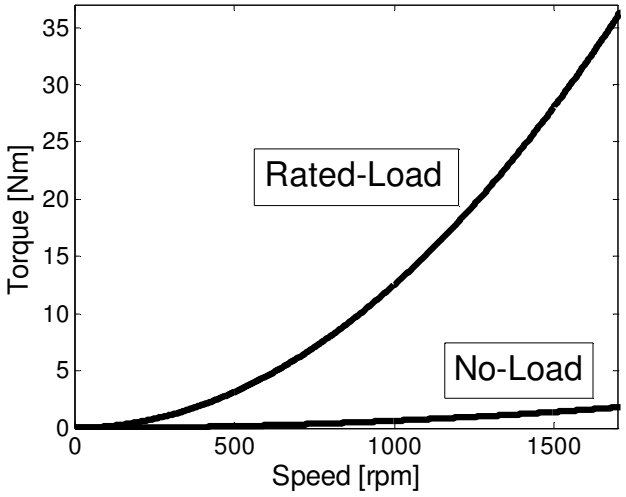


Figure 3.2 The fan load torque – speed curve for no-load and rated-load operations.

3.3.1 Simulation Results at $M_i = 0.61$

In this section simulation results at M_i=0.61 which correspond to the output phase voltage of 137.6 V_{rms}/38.8 Hz are provided. Various simulation results such as the modulation reference signals, load currents (output phase currents), DC link currents, common mode voltage, and inverter flux trajectories are illustrated.

In Figure 3.3, the modulation signals of all three-phases are illustrated for the NSPWM method. The modulation signals are symmetric for all phases and 120^o distant from each other. Since steady-state operation is considered, the symmetric characteristics of the modulation signals are valid for all of the modulation methods and for all modulation index values. Therefore, in the following illustrations the modulation signal of only one phase is shown. Also throughout the simulations in this thesis, the modulation signals are scaled such that they are normalized to unity magnitude with "1" corresponding to 250 V and "-1" corresponding to -250 V. Figure 3.3 also illustrates the discontinuous character of NSPWM, such that at each 60^o segment, one of the phases is locked and not switched at all. This is a desirable characteristic since it reduces the switching losses. The modulation signals are reference for the inverter output voltage and in open-loop operation, they are applied

as exactly same for no load and full load cases. In Figure 3.4 the three-phase load currents of NSPWM are illustrated under no-load. Similar to the modulation signals, the load currents are also symmetric for all phases and 120^o distant from each other. For the same reason, in the following illustrations the phase current of only one phase will be shown. In Figure 3.5 CMV of NSPWM is illustrated over a fundamental cycle such that it is reduced and it alternates between -83V and 83V ($-V_{dc}/6$ and $V_{dc}/6$). In Figure 3.6 the DC link current is illustrated over a fundamental cycle under no-load. There is very high ripple over an average DC value and the waveform of the DC link current is repeating at every 60^o. In Figure 3.7, expanded 60^o waveform of the DC link current is illustrated where the shapes of the DC link current pulses are observed more clearly. The instantaneous values of the DC link current pulses are very different from their average value. Since the DC link current waveform is repeating at every 60^o, and the 60^o expanded waveform is much more detailed, from now on only 60^o expanded simulation results will be provided for the other modulation methods and operating conditions considered. In Figure 3.8 the load current of one phase and the corresponding modulation signal are illustrated under no-load case. In this figure, and also hereby, when a figure involves multiple waveforms with different scales, the scales will be indicated in the figure caption with a scale multiplier such as 2x which implies the measured signal is multiplied with 2 and plotted (therefore, the actual signal can be obtained by dividing the observed signal by 2). The harmonic ripple over the phase current is high and space dependent such that it is very low when the corresponding phase is locked and significantly higher elsewhere. Also since the motor operates at no-load, the power factor (PF) is very low. Hence, the reference voltage and the output current are nearly 90^o distant from each other. Therefore, semiconductor switches of the corresponding phases are locked when the current flowing through them is relatively low and the reduction of the switching losses is less significant at low PF applications for NSPWM. In Figure 3.9 the inverter flux over a fundamental cycle and its 60^o zoom-in view are illustrated. As seen from the figure, the inverter flux is circular as expected and a little harmonic flux is observed over it. Since the load current ripple is a function of the harmonic flux over the inverter flux, the current ripple and the harmonic flux analysis of the modulation methods are correlated.

In Figure 3.10 the phase current of one phase and the corresponding modulation signal are illustrated under rated-load. In this case the PF is higher such that the reference voltage and the phase current are closer to each other (with nearly 30^o phase angle). Therefore the effect of the reduction of the switching losses is increased since the semiconductor switches of the corresponding phases are locked when the current flowing through them is higher. Also load current ripple is less significant in the loaded case. In fact the harmonic flux content is not a function of the PF hence the amount of ripple current is same for loaded or unloaded cases. However, in the loaded case the fundamental component of the output current is higher and the current ripple is less significant over the fundamental component. Therefore, for other PWM methods output current ripple simulation results will not be provided for the loaded case and will be provided only for the no-load case in order to illustrate the ripple current clearly. In Figure 3.11 the DC link current simulation result is provided under rated-load case. In the loaded case DC link current ripple is still high but it is less significant with respect to the output current and K_{dc} is lower. For rated-load case, the inverter flux is not illustrated since it is only function of the applied voltage and therefore the inverter flux is expected to be exactly same as the no-load case.

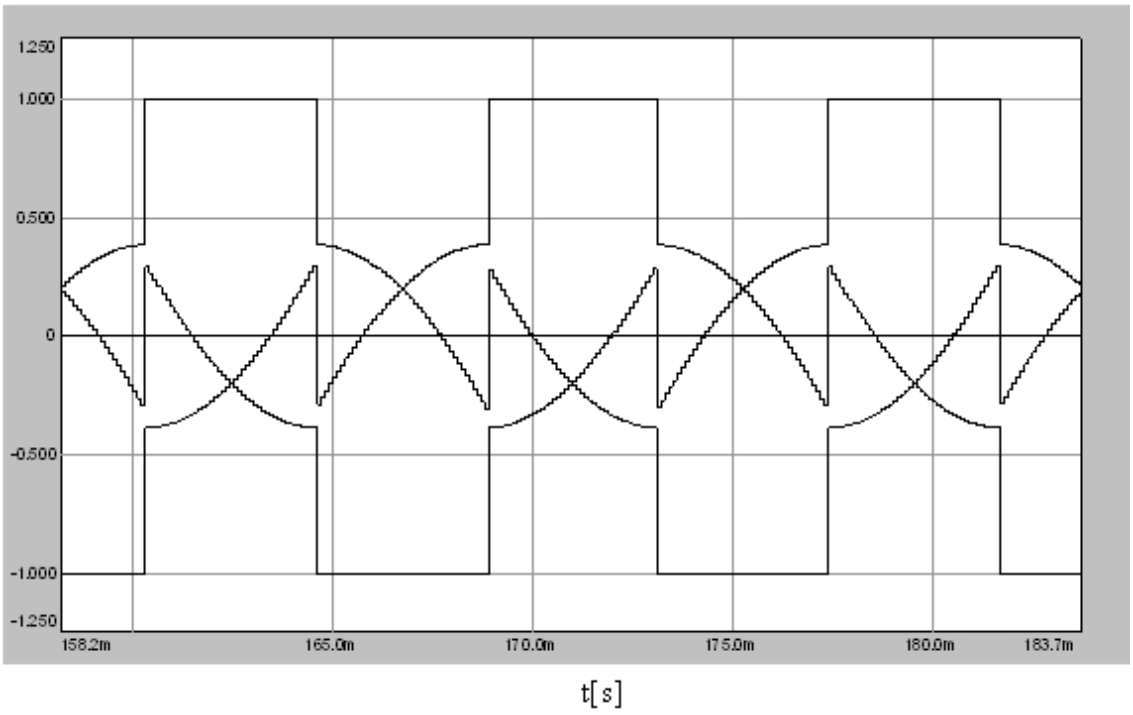


Figure 3.3 Modulation signals of all three-phases of NSPWM (M_i=0.61) under no-load.

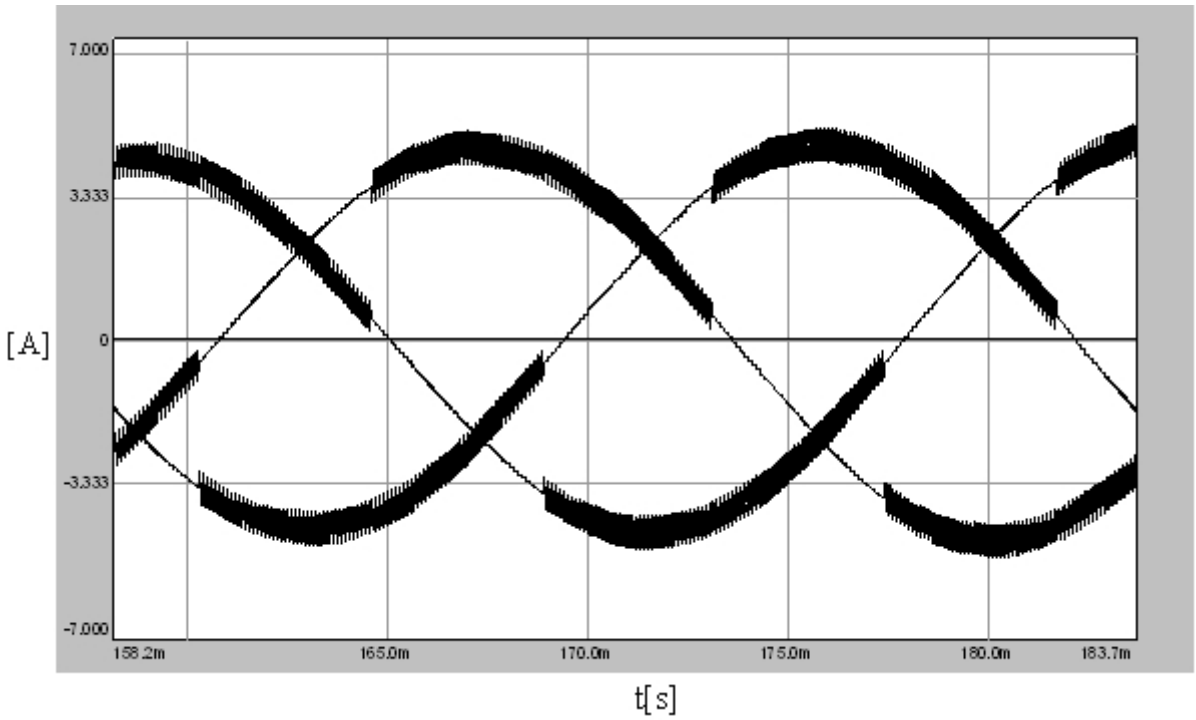


Figure 3.4 Load currents of all three-phases of NSPWM (M_i=0.61) under no-load.

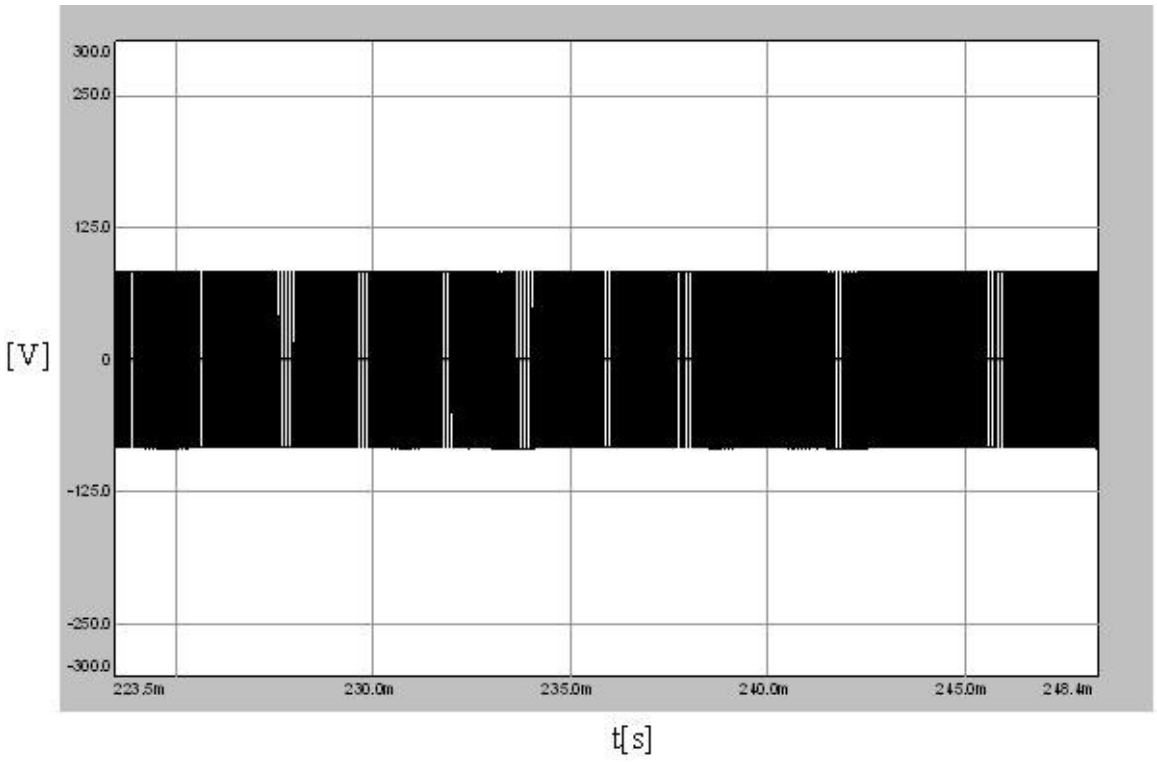


Figure 3.5 CMV of NSPWM (M_i=0.61) over a fundamental cycle under no-load.

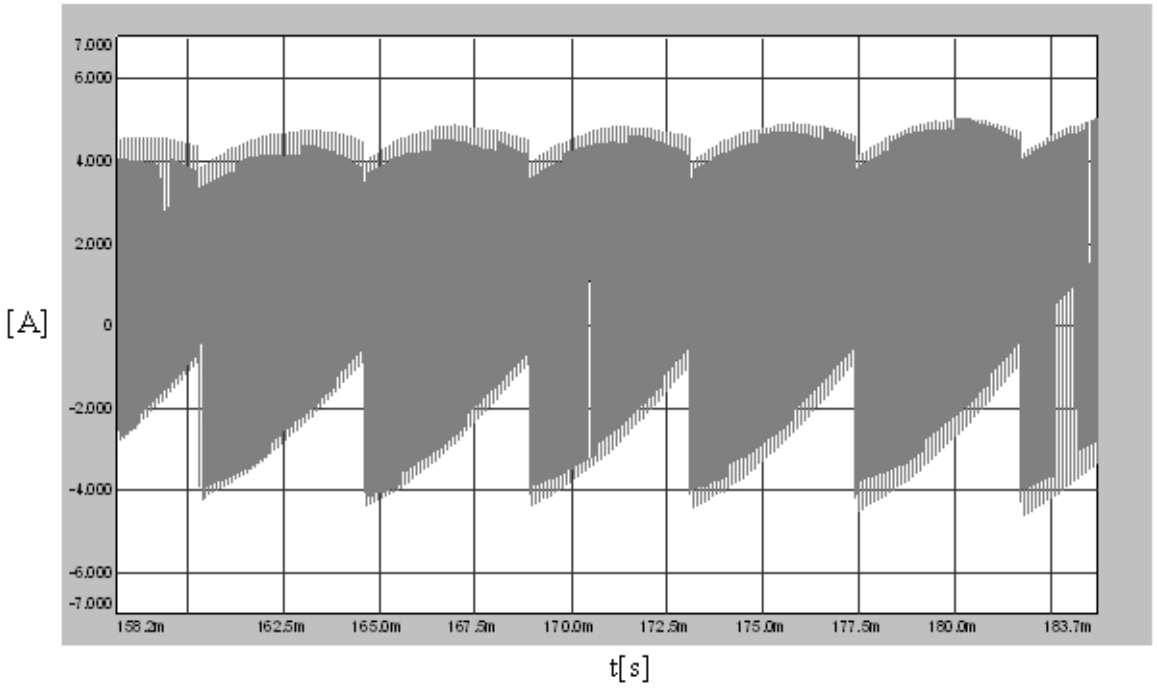


Figure 3.6 The DC link current of NSPWM (M_i=0.61) under no-load.

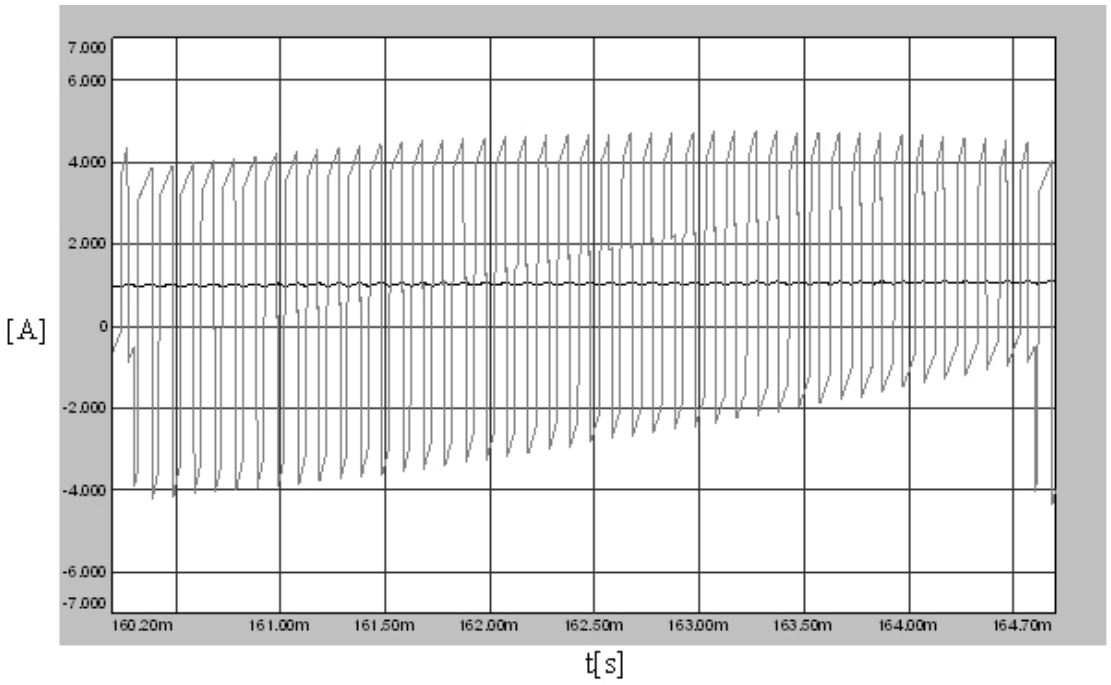


Figure 3.7 Expanded view of the DC link current of NSPWM (M_i=0.61) under no-load and its average value.

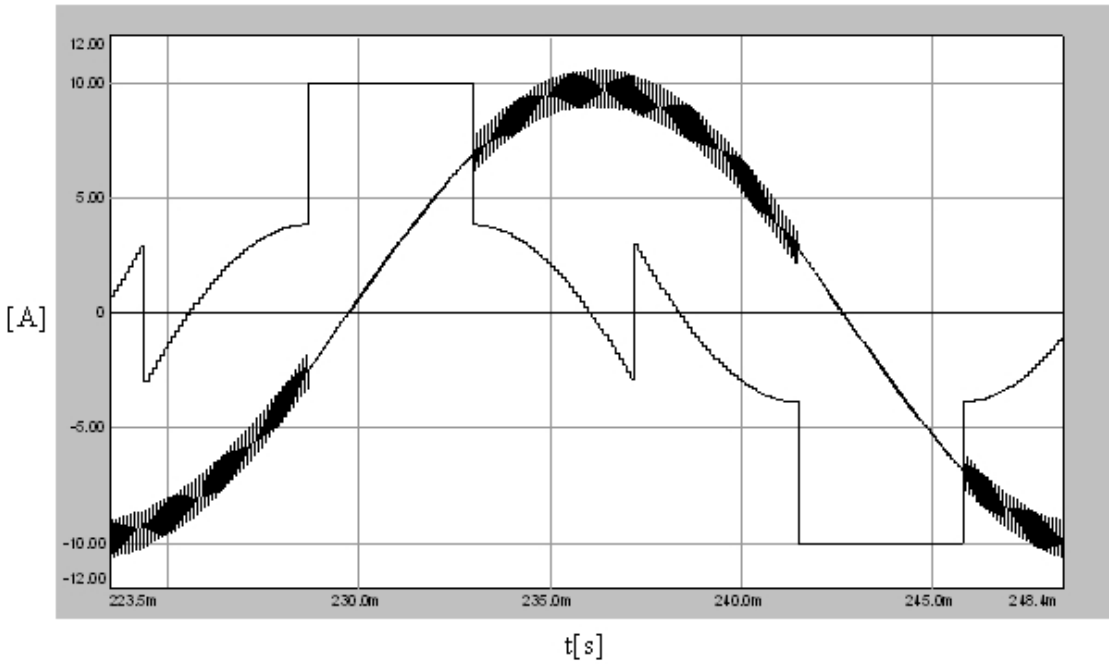
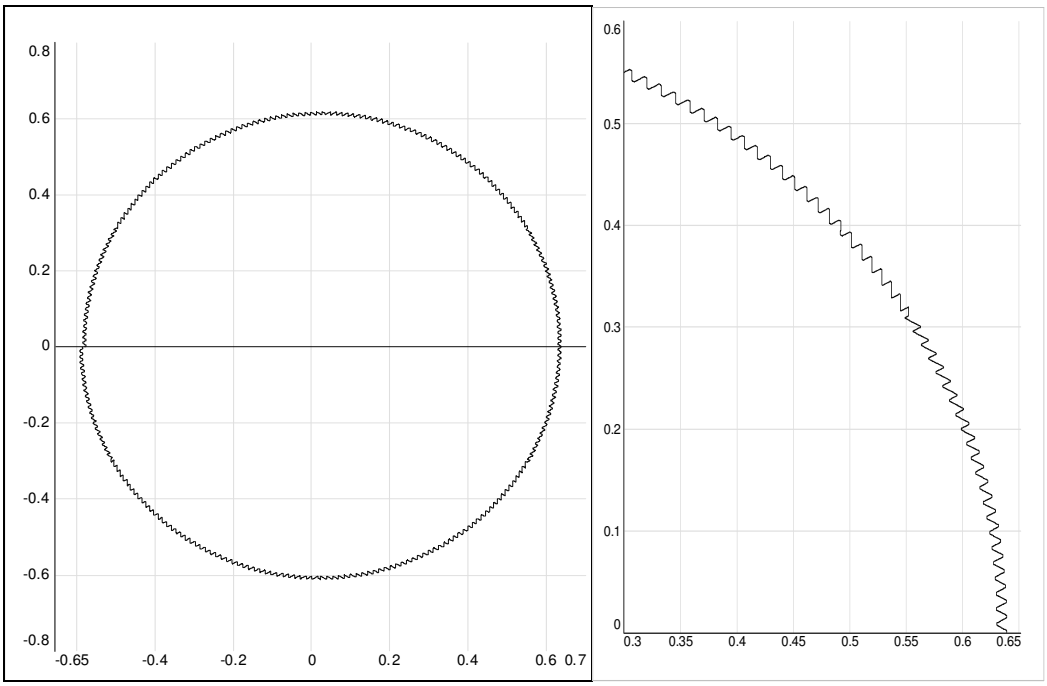


Figure 3.8 Load current (scale: x2) and the modulation signal (scale: x10) of NSPWM (M_i=0.61) for one phase under no-load.



(a) (b)

Figure 3.9 The inverter flux of NSPWM (M_i=0.61) under no-load (a) and the zoom-in view over a 60^o interval (b).

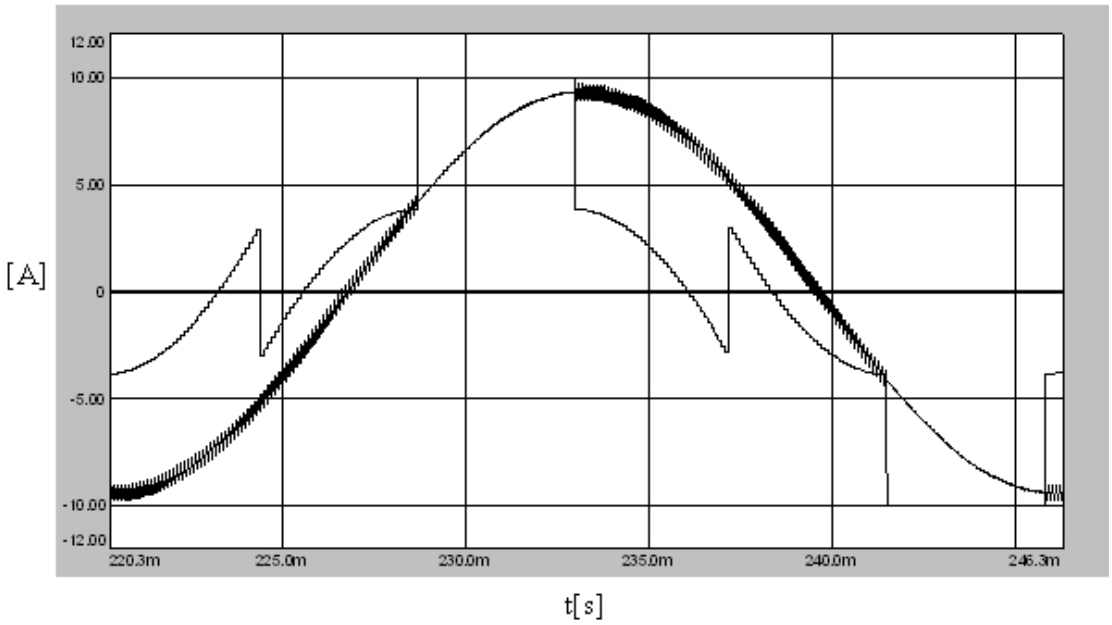


Figure 3.10 One phase load current and the modulation signal (scale: x10) of NSPWM (M_i=0.61) under rated-load.

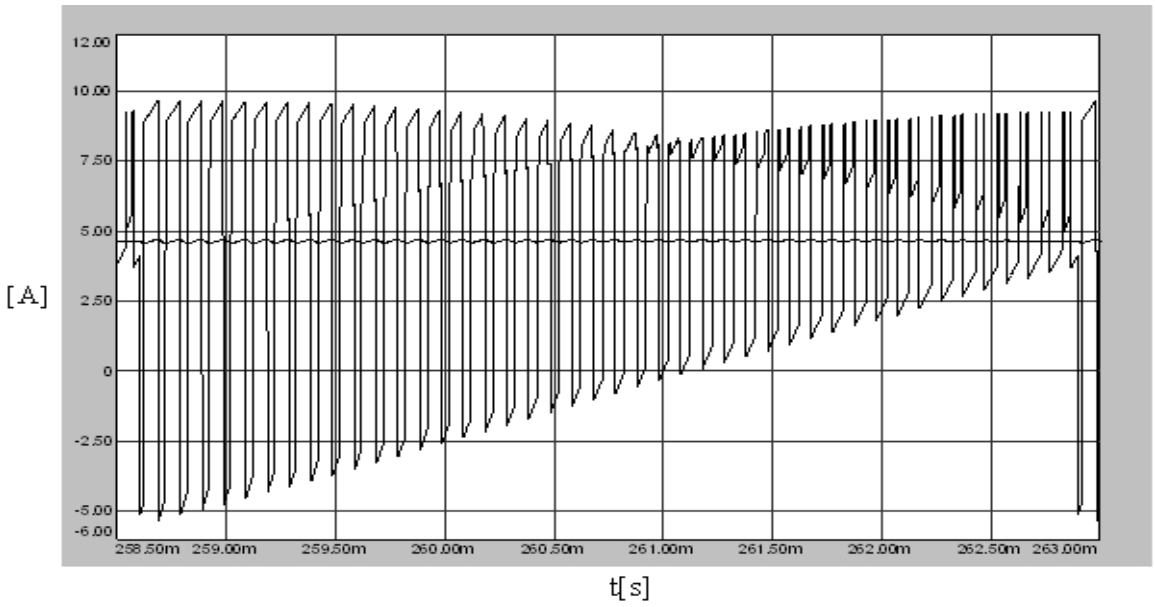


Figure 3.11 The DC link current of NSPWM (M_i=0.61) under rated-load and its average value.

In Figure 3.12 the load current of one phase and the corresponding modulation signal are illustrated for DPWM1 under no-load case. The modulation signal of DPWM1 is just same as that of NSPWM. Therefore the reduction of the switching losses of DPWM1 is very similar to that of NSPWM such that when a phase is locked, switching losses are eliminated and this reduction is more effective as the power factor approaches unity. However the load current ripple characteristics are very different from those of NSPWM. The load current ripple is less in DPWM1 compared to NSPWM and less space dependent such that the variation of the magnitude of the current ripple is nearly uniform over a fundamental cycle. In DPWM1, the ripple slightly increases in the nonswitching segments, while in NSPWM the opposite is true and the ripple difference is substantial between the switching and nonswitching segments. In Figure 3.13 the inverter flux of DPWM1 over a fundamental cycle and its 60^o zoom-in view are illustrated. Over the inverter flux very little harmonic flux is occurred which is very difficult to observe. In Figure 3.14 CMV of DPWM1 is illustrated such that it is high and alternates between -250V and 83V ($-V_{dc}/2$ and $V_{dc}/6$) or between -83V and 250V ($-V_{dc}/6$ and $V_{dc}/2$) depending

on the 60^o region. In Figures 3.15 and 3.16, the DC link current simulation results of DPWM1 are provided for no-load and rated-load cases respectively. Under no-load, the DC link current ripple is very low and the DC link current pulses are very close to their average value. In the loaded case, the DC link harmonic content increases compared to the unloaded case but it is still tolerably small.

In Figure 3.17 the waveforms of NSPWM and DPWM1 are compared to clearly illustrate the differences and similarities of these two methods. While the clamped $2x60^o$ segments of NSPWM create the least ripple in the associated phase, in DPWM1 this phase carries the largest ripple current. By observing the switch logic signals globally it is not possible to distinguish these two methods from each other. However zooming into the PWM waveforms and observing the switch states and associated voltage vector states it can be distinguished whether NSPWM or DPWM1 is utilized. In Figure 3.18, the voltage space vectors and harmonic voltage vectors of DPWM1 and NSPWM are illustrated. This figure explains the different characteristics of the harmonic ripple of the clamped phase in NSPWM and DPWM1. At the region $0^o<\theta<30^o$ for both NSPWM and DPWM1, phase-a is the clamped phase. For DPWM1 V_{0h} is the most effective harmonic voltage vector and it is nearly parallel to the voltage vector of phase-a hence it results in high current ripple on phase-a. On the contrary, for NSPWM V_{1h} and V_{6h} are the effective harmonic voltage vectors and both of them are nearly perpendicular to voltage vector of phase-a. Since the components of the effective harmonic voltage vectors along the phase-a vector are small; they result in very little ripple current on the clamped phase. Thus, there results significant difference in the ripple current waveforms in these methods.

In Figure 3.19 the load current of one phase and the corresponding modulation signal are illustrated for SVPWM at no-load. Unlike NSPWM and DPWM1, SVPWM is a continuous PWM method such that none of the phases is locked at any instant. Therefore utilizing SVPWM has no contribution to the switching loss reduction. The load current ripple characteristics are similar to those of DPWM1 such that it is space independent and the magnitude of the load current ripple is close to that of DPWM1

due to the fact that SVPWM utilizes a lower carrier frequency than the DPWM1 carrier frequency for equal average switching frequency. In Figure 3.20 the inverter flux over a fundamental cycle and its 60^o zoom-in view are illustrated. Similar to that of DPWM1 the harmonic flux occurs over the inverter flux is very little and very difficult to observe. In Figure 3.21 CMV of SVPWM is illustrated such that it is high and alternates between -250V and 250V ($-V_{dc}/2$ and $V_{dc}/2$). In Figures 3.22 and 3.23 the DC link current simulation results of SVPWM are provided for no-load and rated-load cases respectively. For both loaded and unloaded cases the DC link current characteristics of SVPWM are nearly same as those of DPWM1 since both utilize the same voltage vectors and only the partitioning of the zero voltage vectors are different. The shapes of the DC link current pulses are slightly different (pulses are position shifted) but the magnitude of the harmonic rms current is same as that of DPWM1 and it is low for both loaded and unloaded case.

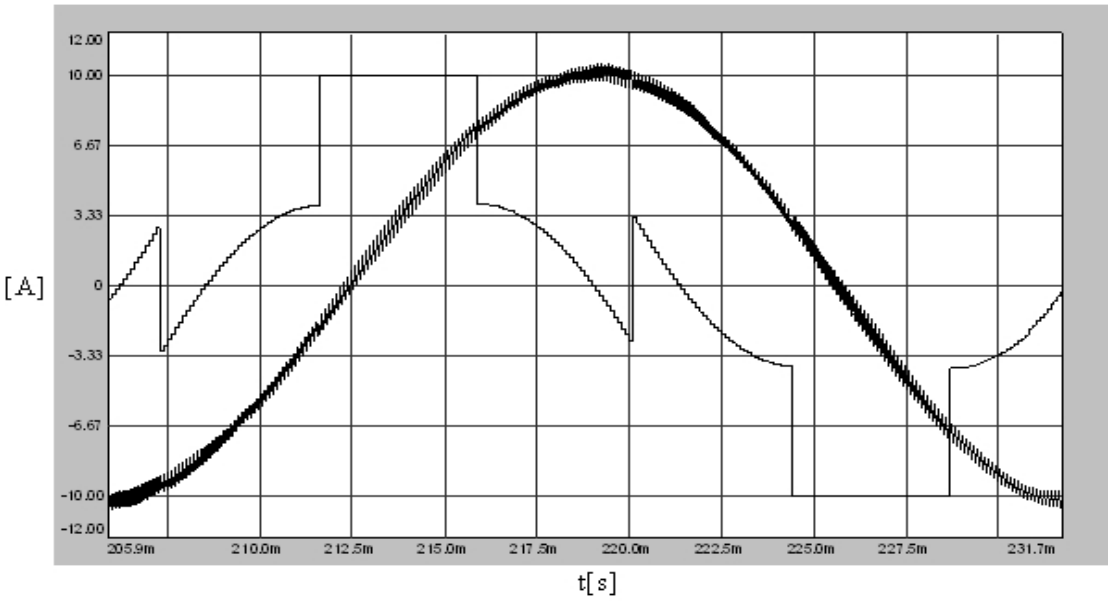
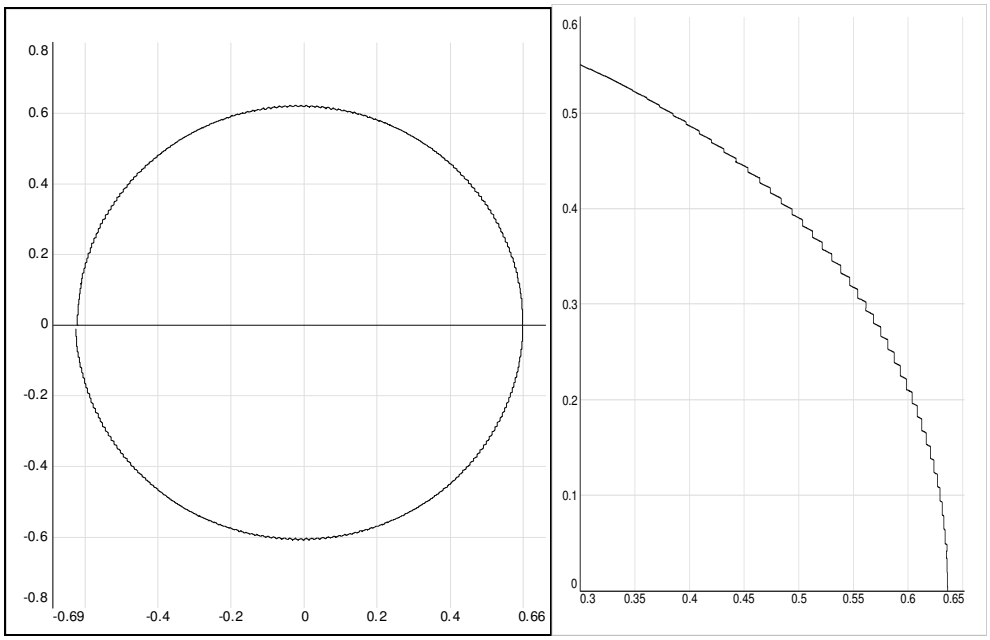


Figure 3.12 One phase load current (scale: x2) and the modulation signal (scale: x10) of DPWM1 (M_i=0.61) under no-load.



(a) (b)

Figure 3.13 Inverter flux of DPWM1 (M_i=0.61) under no-load (a) and the zoom-in view over a 60^o interval (b).

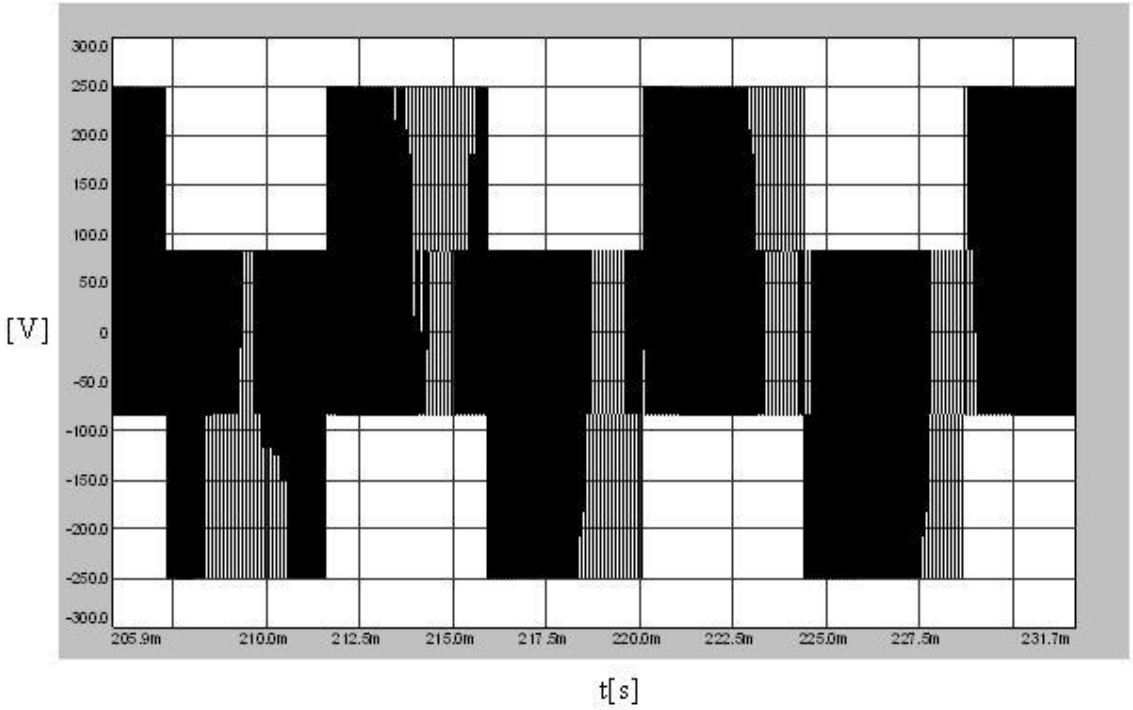


Figure 3.14 CMV of DPWM1 (M_i=0.61) over a fundamental cycle under no-load.

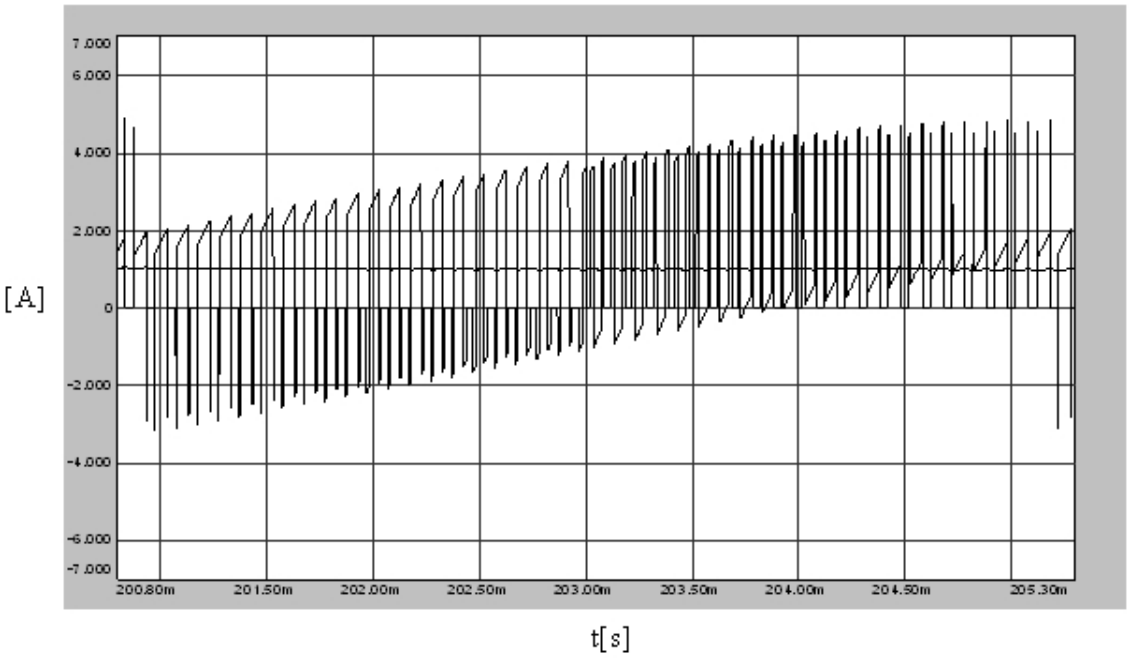


Figure 3.15 The DC link current of DPWM1 (M_i=0.61) under no-load and its average value.

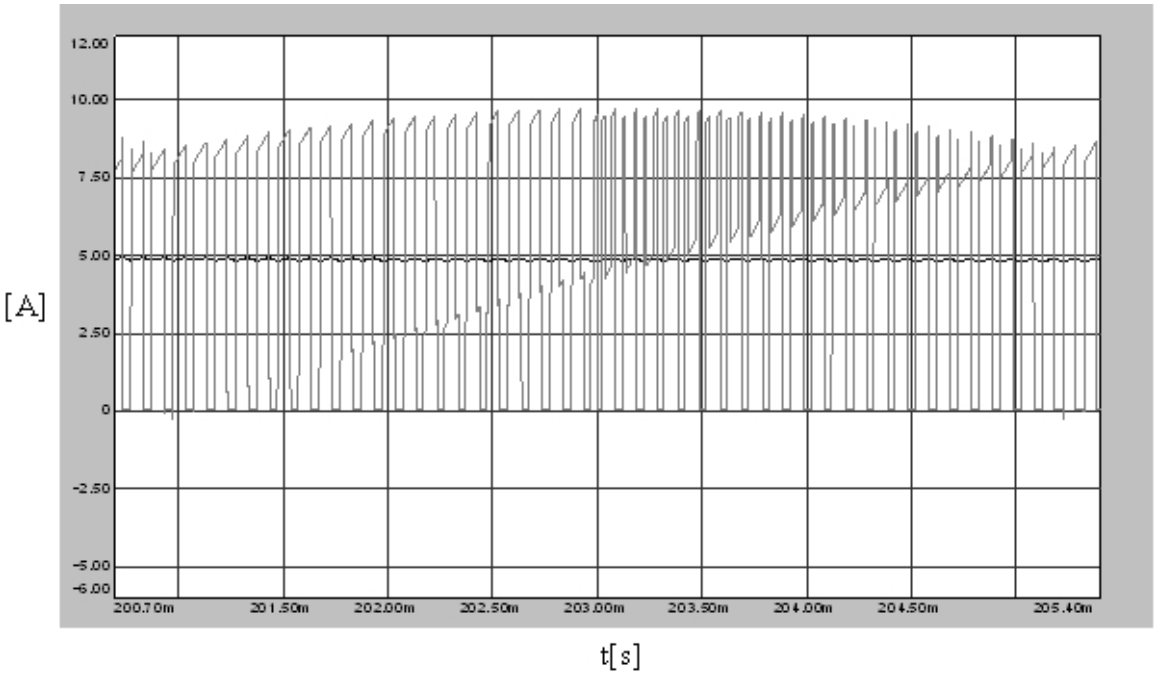


Figure 3.16 The DC link current of DPWM1 (M_i=0.61) under rated-load and its average value.

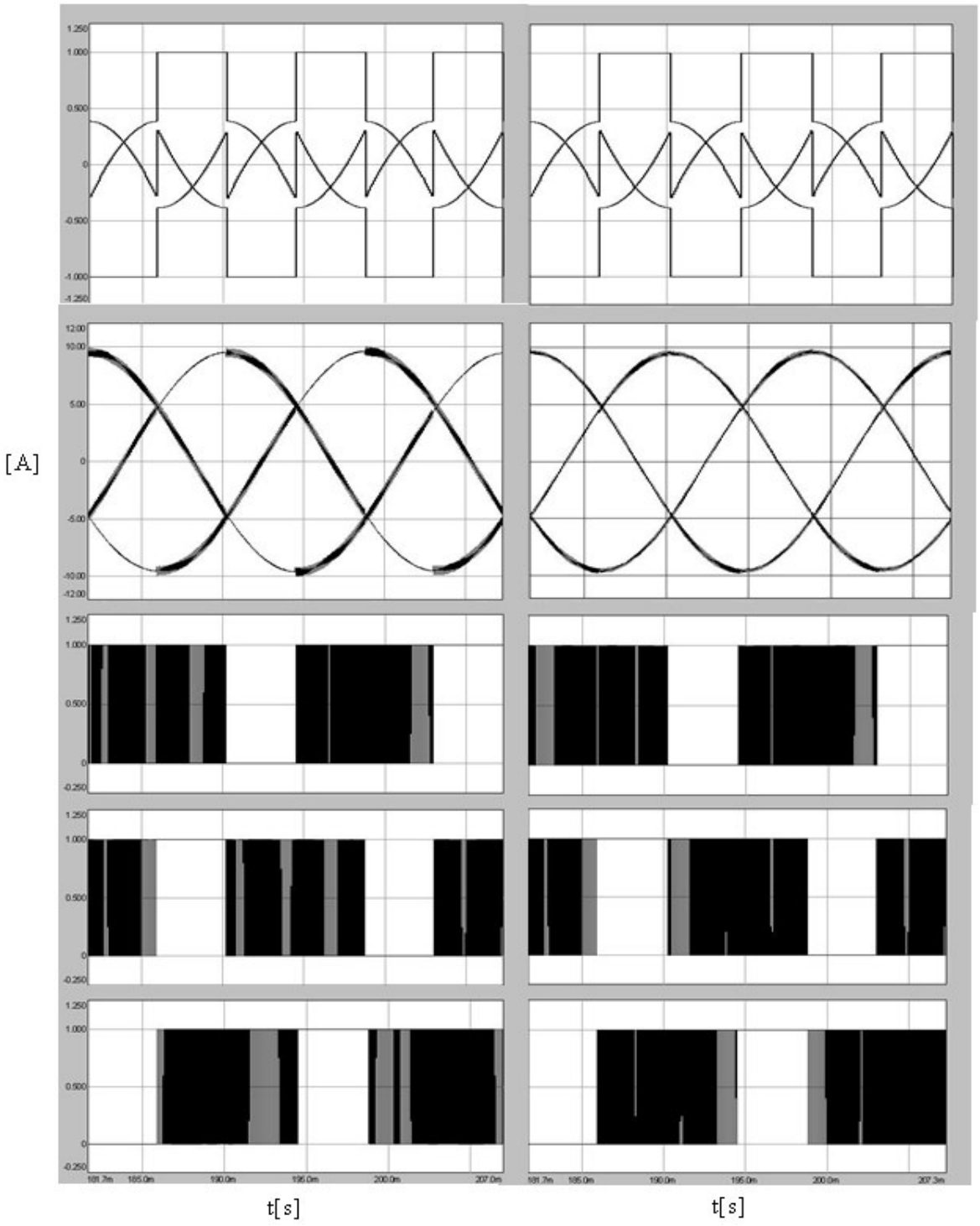
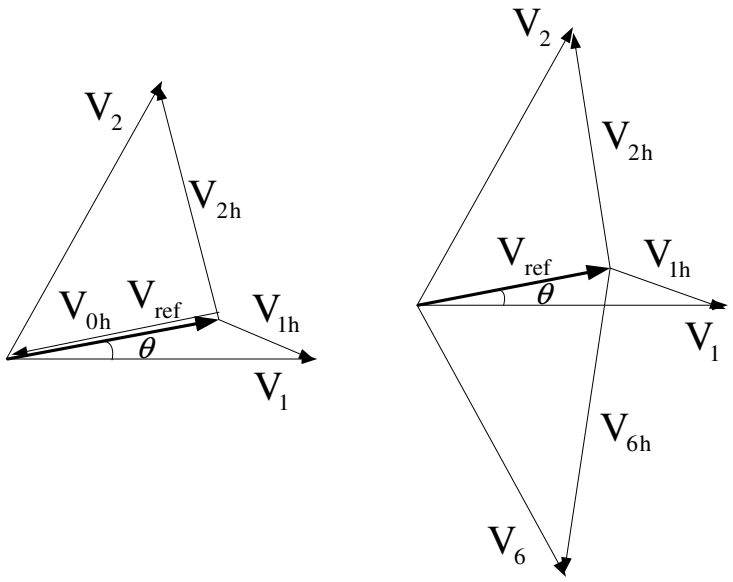


Figure 3.17 The modulation signals (top), phase currents (center), and switch logic signals (bottom) of NSPWM (left) and DPWM1 (right) at M_i=0.61 under rated-load.



(a) (b)

Figure 3.18 Voltage space vectors and harmonic voltage vectors of (a) DPWM1 (b) NSPWM for $0^o<\theta<30^o$.

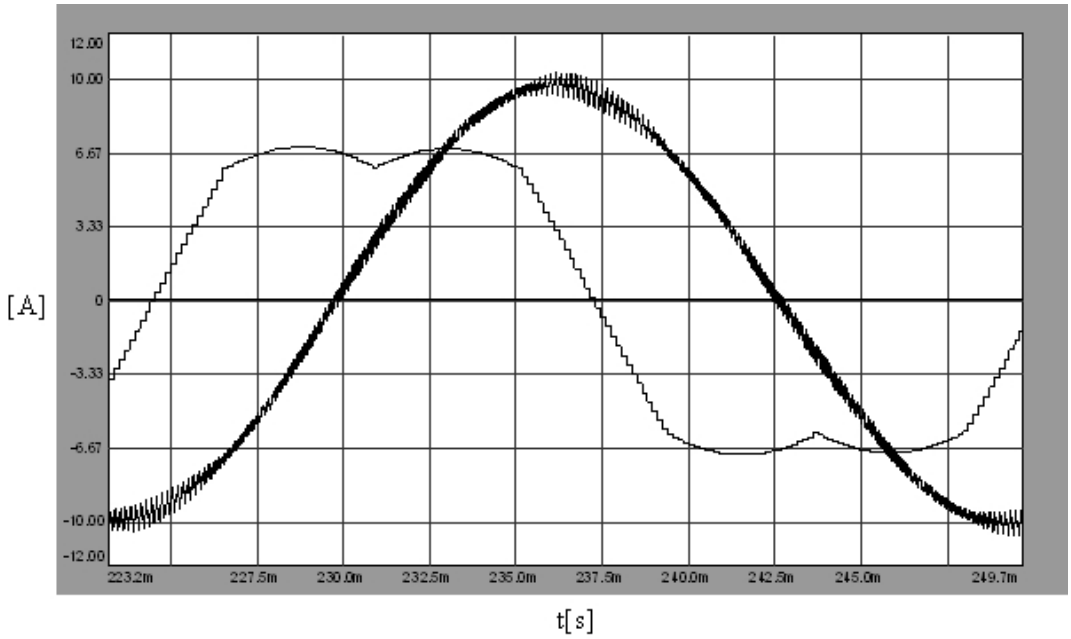
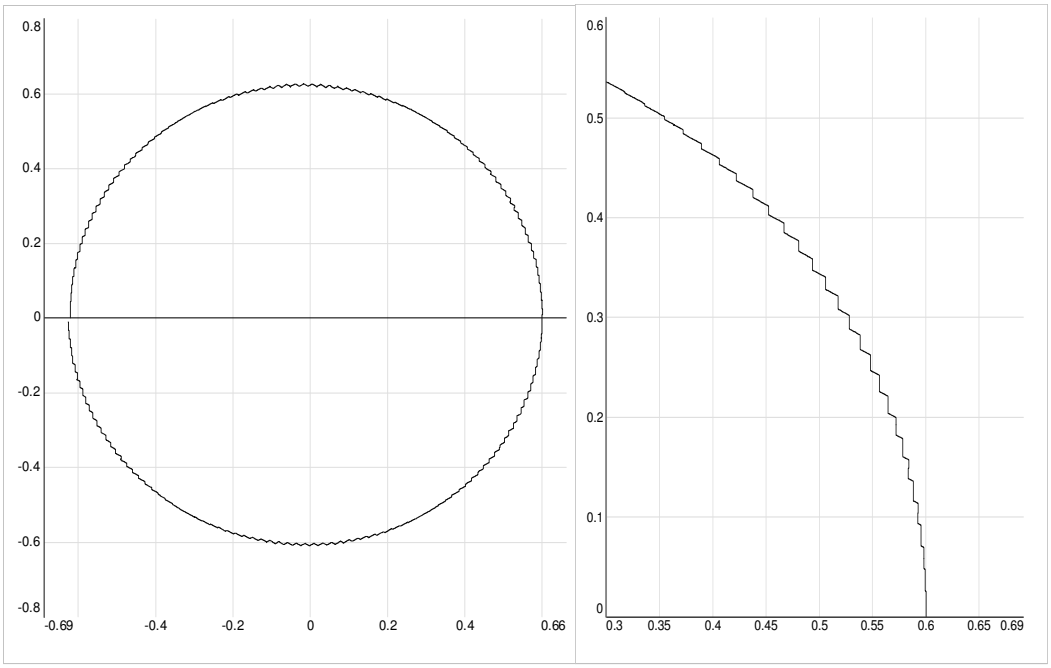


Figure 3.19 One phase load current (scale: x2) and the modulation signal (scale: x10) of SVPWM (M_i=0.61) under no-load.



(a) (b)

Figure 3.20 Inverter flux of SVPWM (M_i=0.61) under no-load (a) and the zoom-in view over a 60^o interval (b).

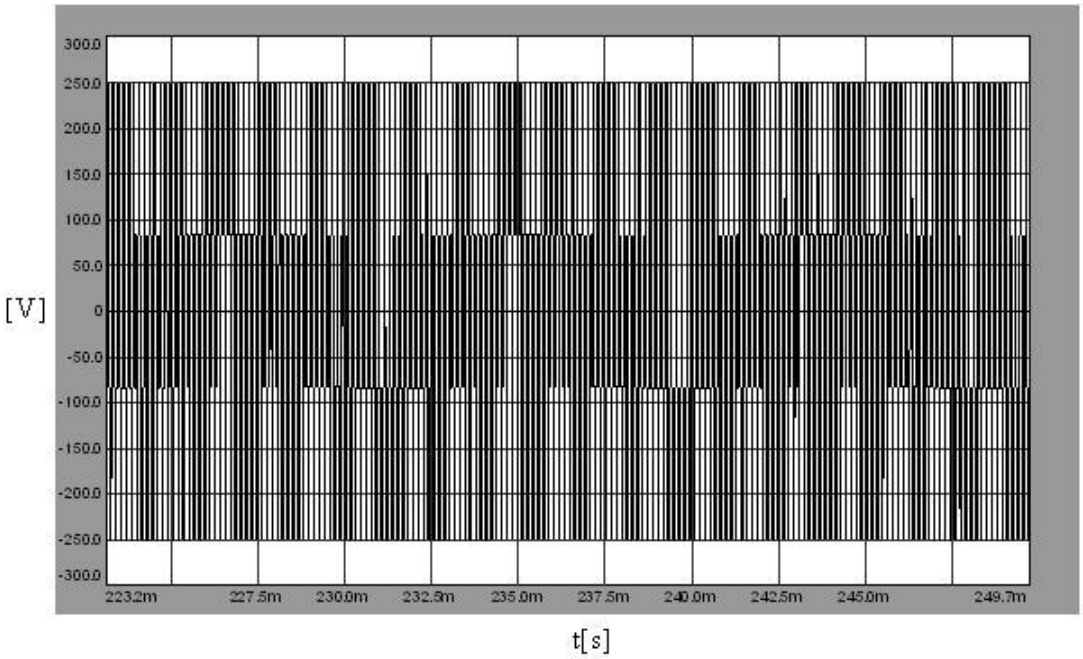


Figure 3.21 CMV of SVPWM (M_i=0.61) over a fundamental cycle under no-load.

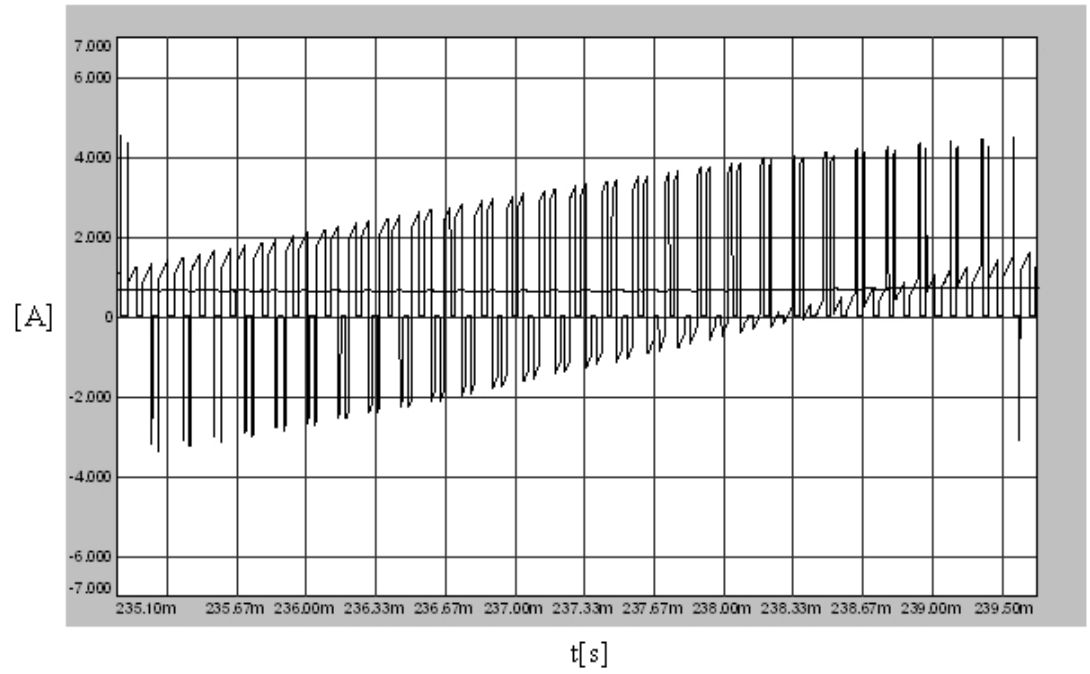


Figure 3.22 The DC link current of SVPWM (M_i=0.61) under no-load and its average value.

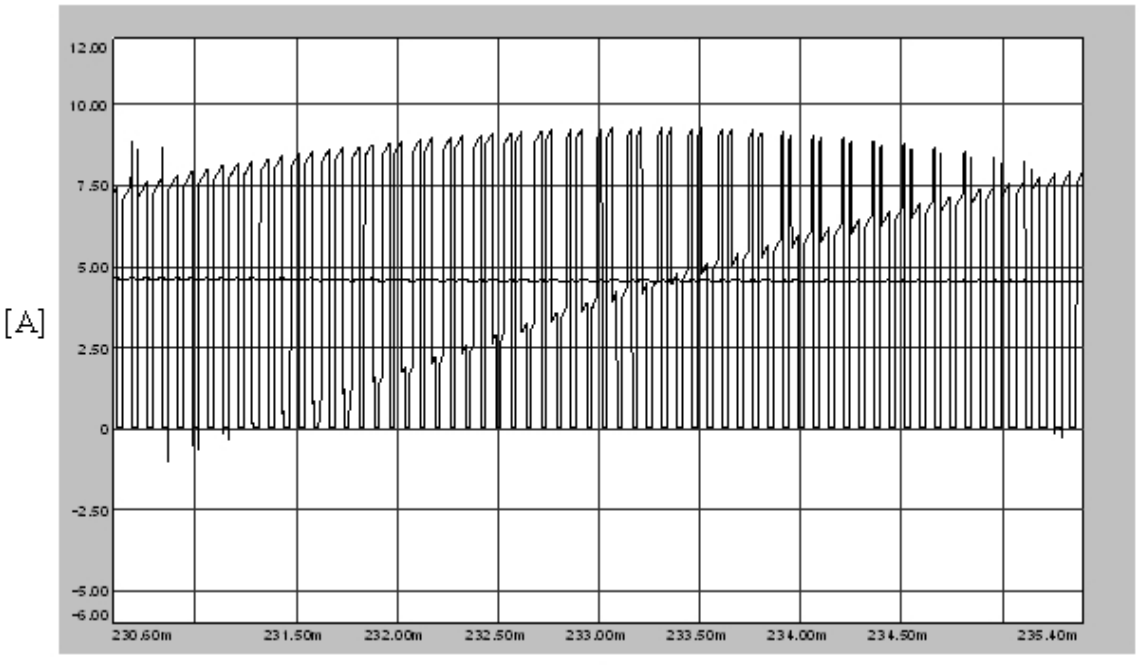


Figure 3.23 The DC link current of SVPWM (M_i=0.61) under rated-load and its average value.

In Figure 3.24 the load current of one phase and the corresponding modulation signal are illustrated for AZSPWM1 at no-load. The modulation signal of AZSPWM1 is just same as that of SVPWM. However the load current ripple characteristics are very different from those of SVPWM. The load current ripple of AZSPWM1 is very high compared to NSPWM and standard PWM methods. In Figure 3.25 the inverter flux over a fundamental cycle and its 60^o zoom-in view are illustrated. For AZSPWM1 the harmonic flux over the inverter flux is noticeably high. In Figure 3.26 CMV of AZSPWM1 is illustrated over a fundamental cycle such that CMV is reduced and alternates between -83V and 83V ($-V_{dc}/6$ and $V_{dc}/6$).

In Figures 3.27 and 3.28 the DC link current simulation results of AZSPWM1 are provided for no-load and rated-load cases respectively. At no-load, the DC link current ripple is very high due to the fact that the method always uses active states and loads the DC bus. However the rms DC-link current ripple is particularly low. Under rated-load case the DC link current ripple is still high but the DC link current pulses are closer to their average value and the K_{dc} is lower than the no-load case.

In Figure 3.29 the load current of one phase and the corresponding modulation signal are illustrated for AZSPWM2 at no-load. The modulation signal of AZSPWM2 is same as that of AZSPWM1 since both utilize the same voltage vectors. However due to the differences in the sequences of the voltage vectors, their load current ripple characteristics are different and ripple over the load current of AZSPWM2 is slightly higher. In Figure 3.30 the inverter flux over a fundamental cycle and its 60^o zoom-in view are illustrated. For AZSPWM2 the harmonic flux over the inverter flux is high and has sharp edges due to the sequence of the applied voltage vectors such that distant voltage vectors are applied successively. In Figure 3.31 the CMV of AZSPWM2 is illustrated over a fundamental period such that it is similar to that of AZSPWM1 as it is reduced and alternates between -83V and 83V ($-V_{dc}/6$ and $V_{dc}/6$).

In Figures 3.32 and 3.33, the DC link current simulation results of AZSPWM2 are provided for no-load and rated-load cases respectively. For both no-load and rated-load cases the DC link current characteristics of AZSPWM2 are nearly same as that

of AZSPWM1 since both utilize the same voltage vectors. The shapes of the DC link current pulses are slightly different (their positions are different) but the peak-to-peak and rms DC link ripple current is same as that of AZSPWM1. For both methods the peak-to-peak DC link current ripple is high for both loaded and unloaded cases but the rms of the harmonic ripple is relatively lower especially in the loaded case.

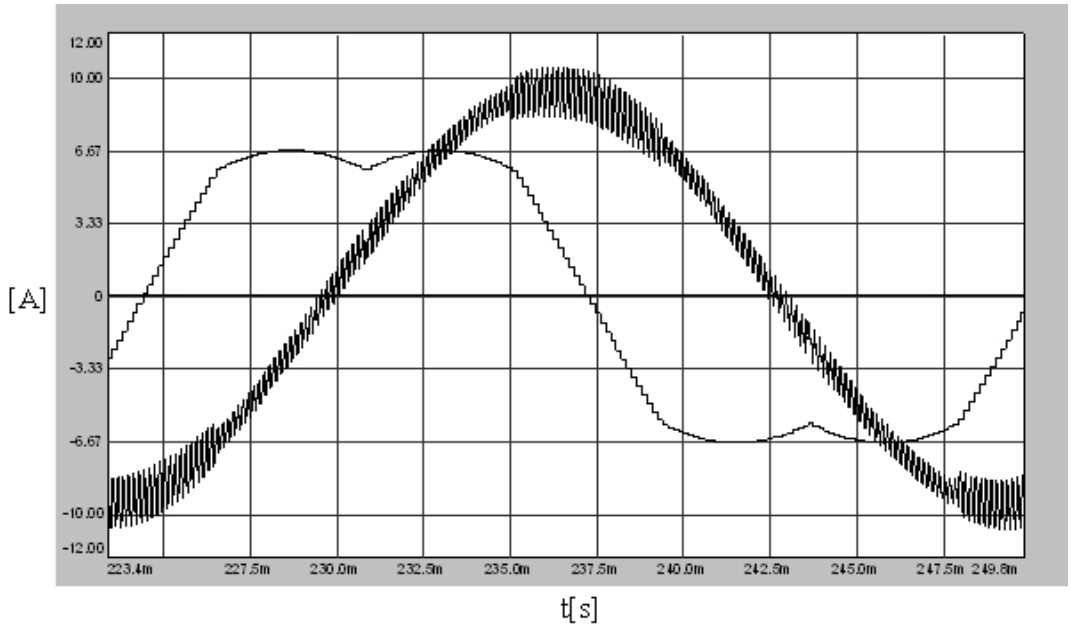
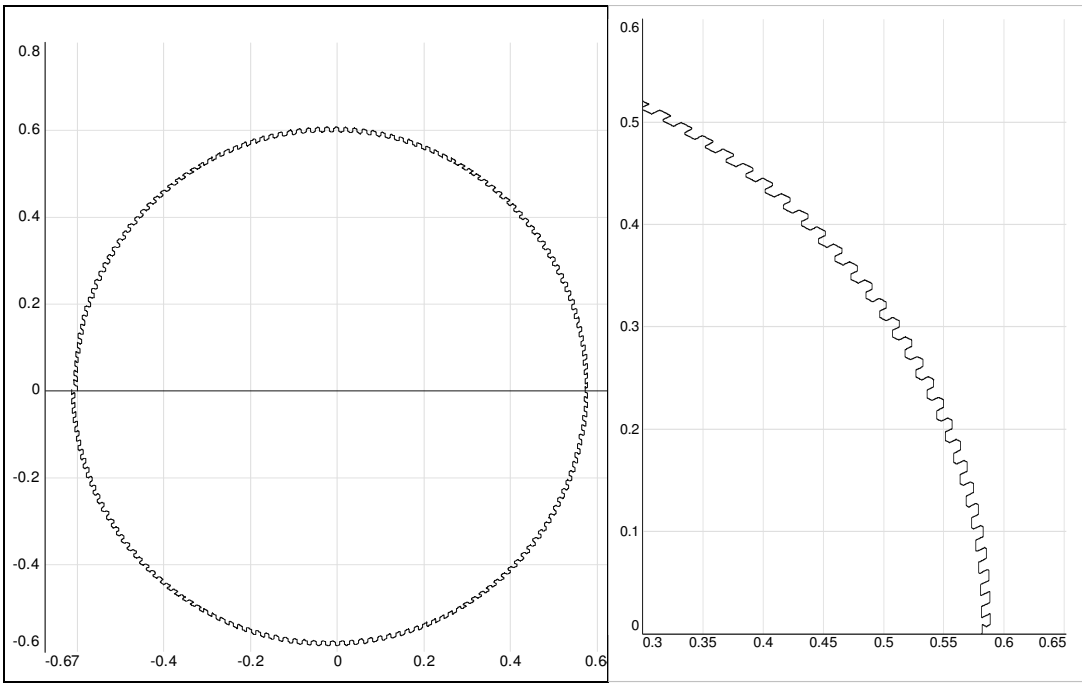


Figure 3.24 One phase load current (scale: x2) and the modulation signal (scale: x10) of AZSPWM1 (M_i=0.61) under no-load.



(a) (b)

Figure 3.25 Inverter flux of AZSPWM1 (M_i=0.61) under no-load (a) and the zoom-in view over a 60^o interval (b).

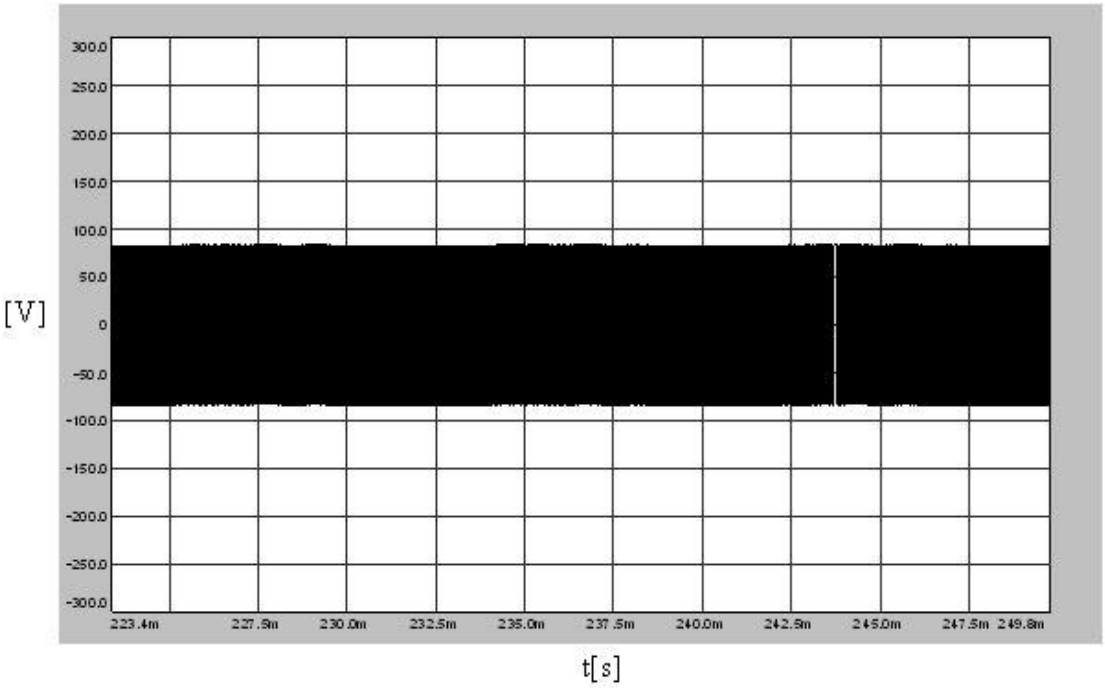


Figure 3.26 CMV of AZSPWM1 (M_i=0.61) over a fundamental cycle under no-load.

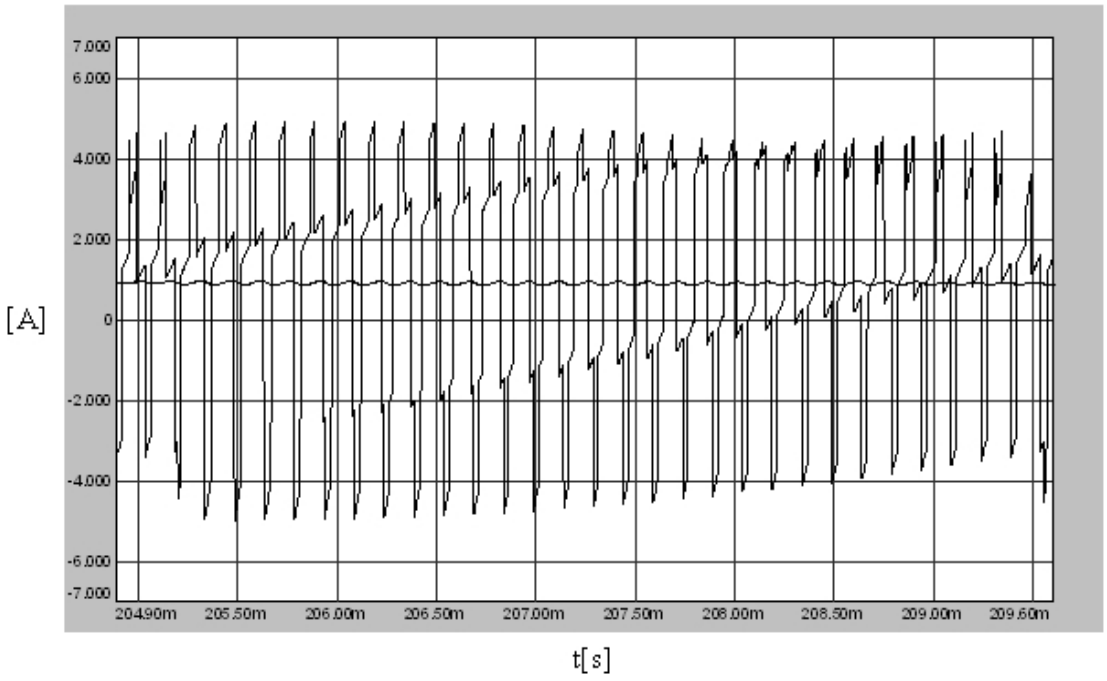


Figure 3.27 The DC link current of AZSPWM1 (M_i=0.61) under no-load and its average value.

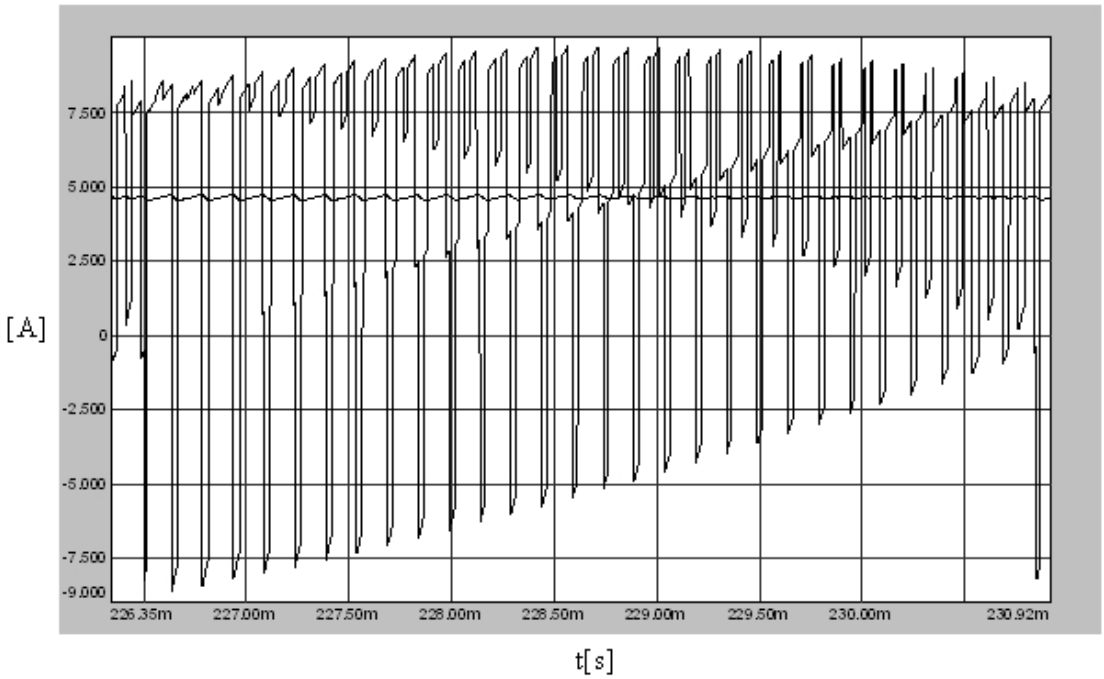


Figure 3.28 The DC link current of AZSPWM1 (M_i=0.61) under rated-load and its average value.

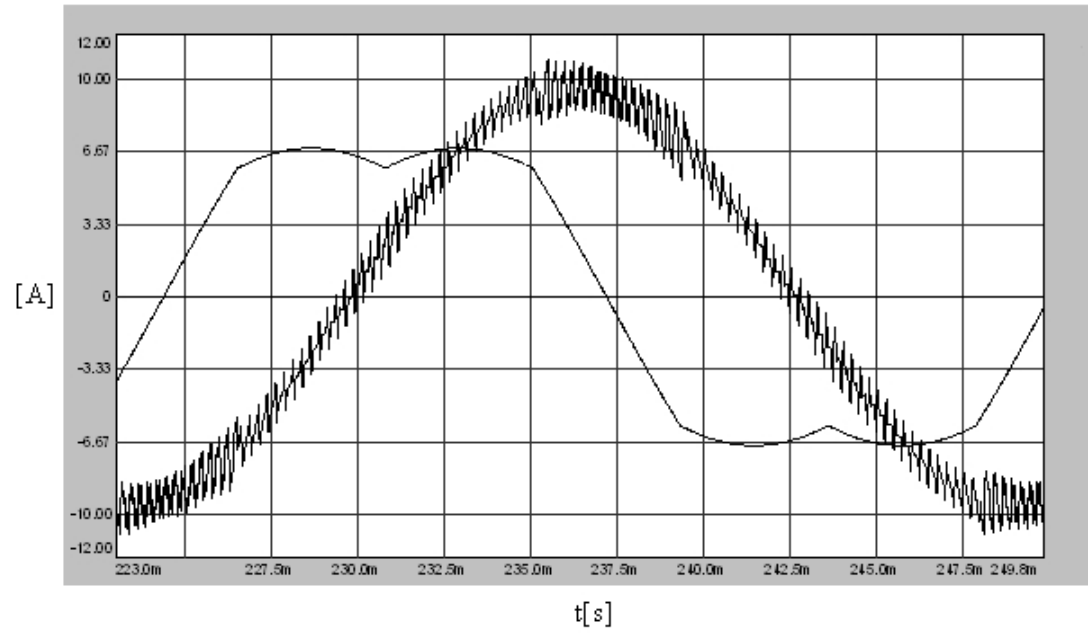
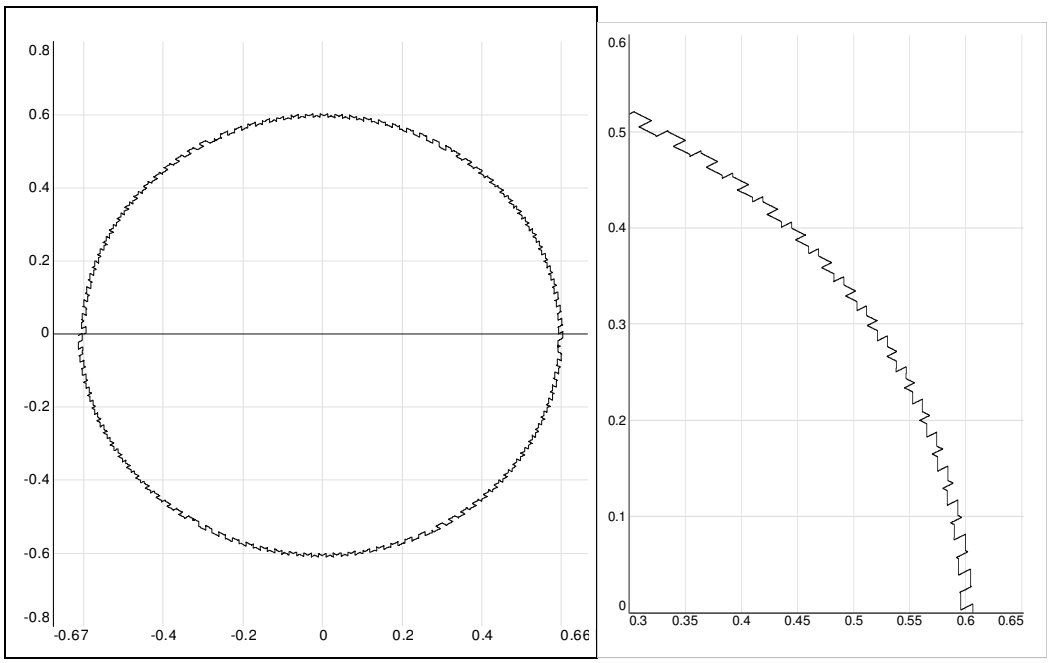


Figure 3.29 One phase load current (scale: x2) and the modulation signal (scale: x10) of AZSPWM2 (M_i=0.61) under no-load.



(a) (b)

Figure 3.30 Inverter flux of AZSPWM2 (M_i=0.61) under no-load (a) and the zoom-in view over a 60^o interval (b).

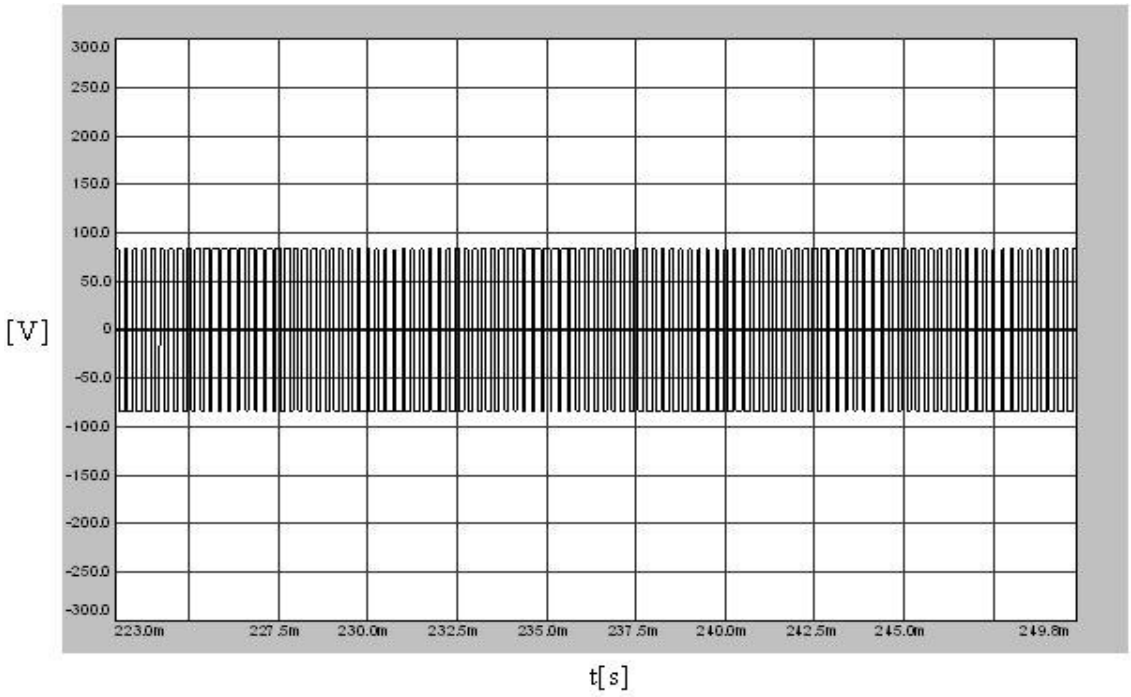


Figure 3.31 CMV of AZSPWM2 (M_i=0.61) over a fundamental cycle under no-load.

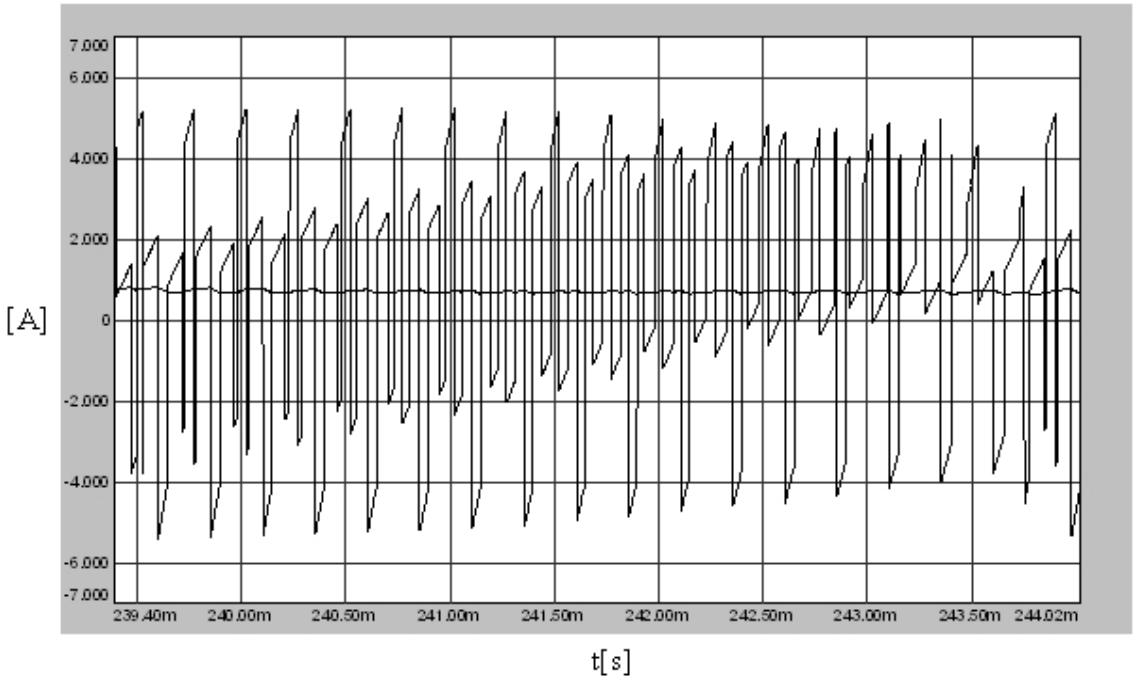


Figure 3.32 The DC link current of AZSPWM2 (M_i=0.61) under no-load and its average value.

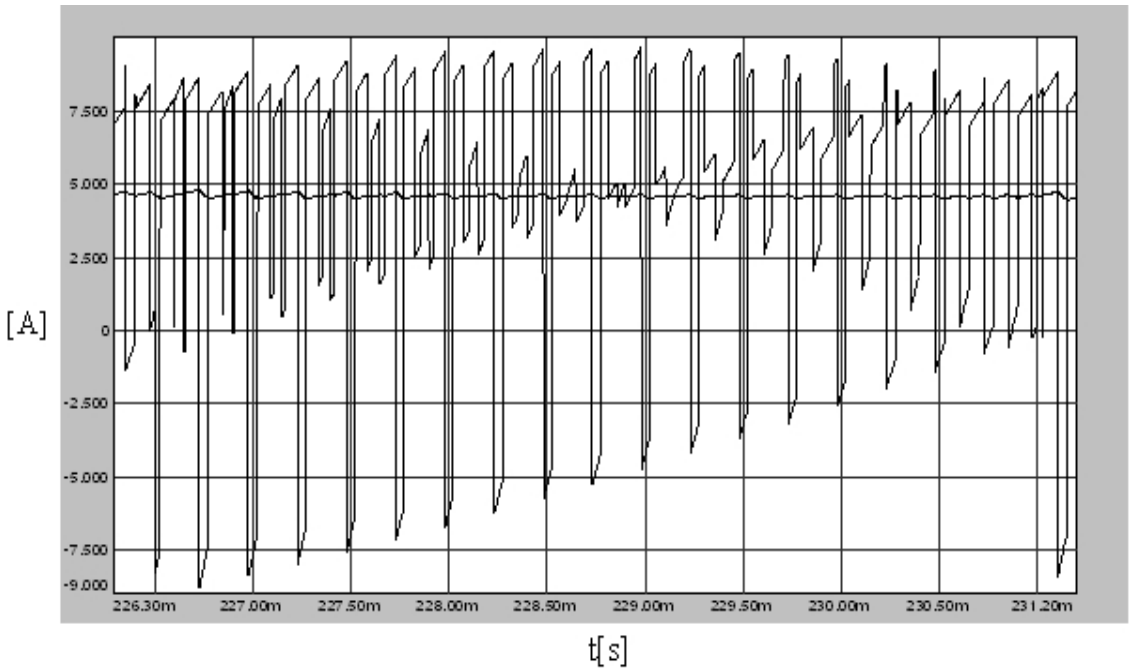


Figure 3.33 The DC link current of AZSPWM2 (M_i=0.61) under rated-load and its average value.

In Figure 3.34 the load current of one phase is illustrated for RSPWM3 under no-load. The modulation signal of RSPWM3 is not illustrated since in generation of RSPWM3 pulse pattern, scalar implementation is not applied and inverter switch states are decided by direct voltage vector implementation. The load current ripple of RSPWM3 is space dependent such that the magnitude of the ripple over the load current increases and decreases within a fundamental period and it is very high in most of the fundamental cycle. In Figure 3.35 the inverter flux over a fundamental cycle and its 60^o zoom-in view are illustrated. For RSPWM3 the harmonic flux over the inverter flux is high and has sharp edges due to the sequence of the applied voltage vectors such that distant voltage vectors are applied successively. In Figure 3.36 CMV of RSPWM3 is illustrated over a fundamental cycle such that it is reduced and fixed at either -83V or 83V ($-V_{dc}/6$ or $V_{dc}/6$) according to 60^o segments. This low CMV could be obtained in the simulation due to the use of system level switches in the inverter and the lack of the inverter deadtimes which is not implemented in the simulation. In the practical application, as shown in [20] the method does not work due to the finite deadtime and also the unequal switch transient characteristics. Thus,

the CMV waveforms of RSPWM3 are the best that can be obtained and not what expected in the practical application. In Figures 3.37 and 3.38 the DC link current simulation results of RSPWM3 are provided for no-load and rated-load cases respectively. For both no-load and rated-load cases the DC link current ripples are high and the DC link current pulses are distant from the average value, resulting in high K_{dc}.

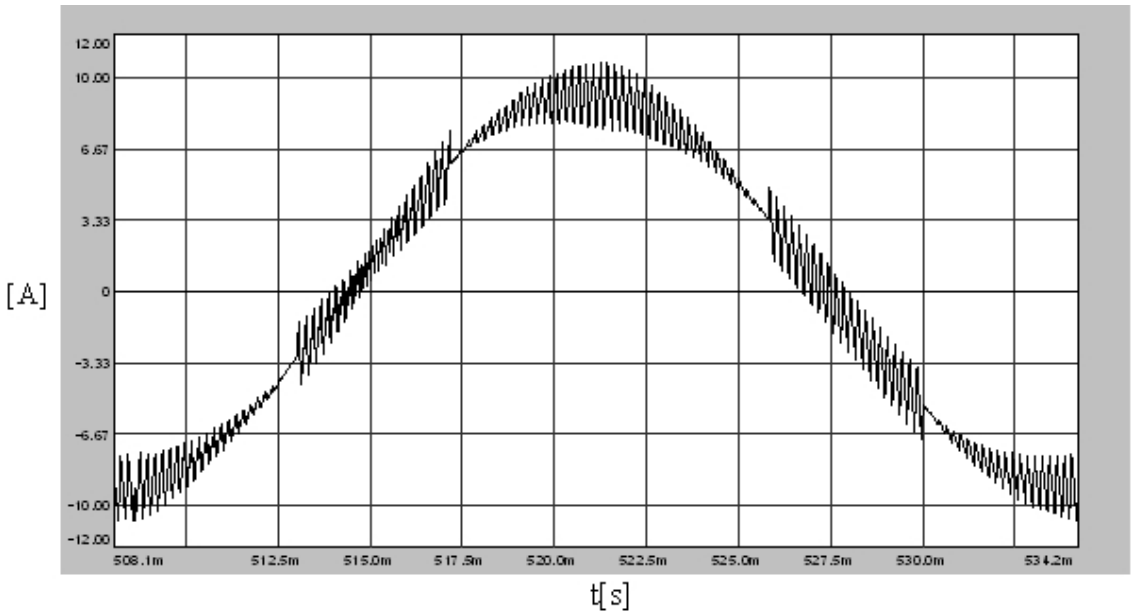
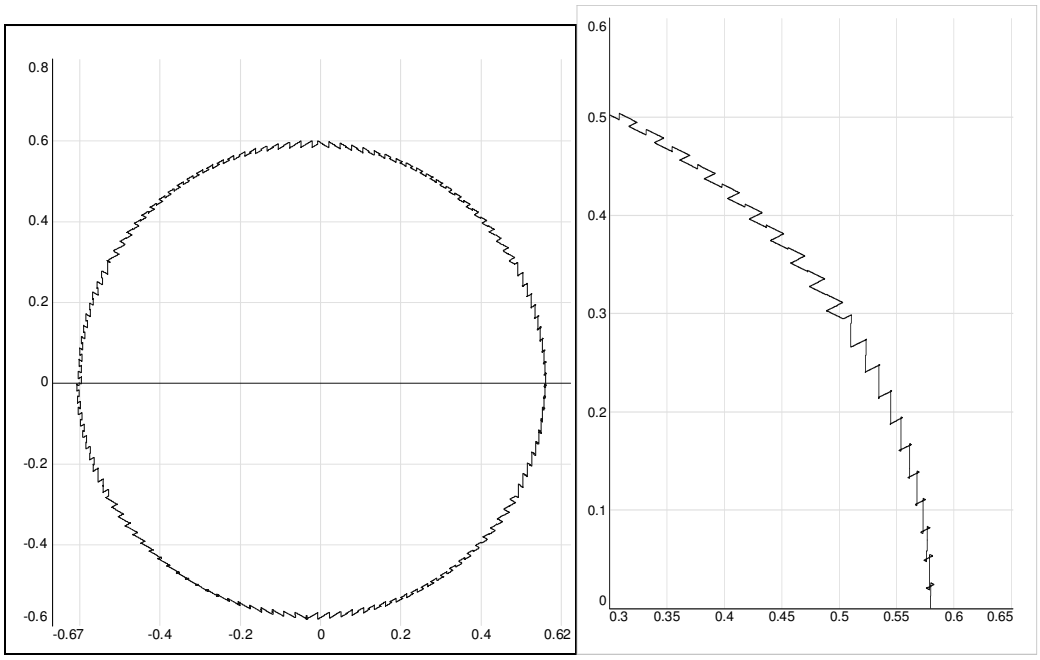


Figure 3.34 One phase load current (scale: x2) of RSPWM3 (M_i=0.61) under no-load.



(a) (b)

Figure 3.35 Inverter flux of RSPWM3 (M_i=0.61) under no-load (a) and the zoom-in view over a 60^o interval (b).

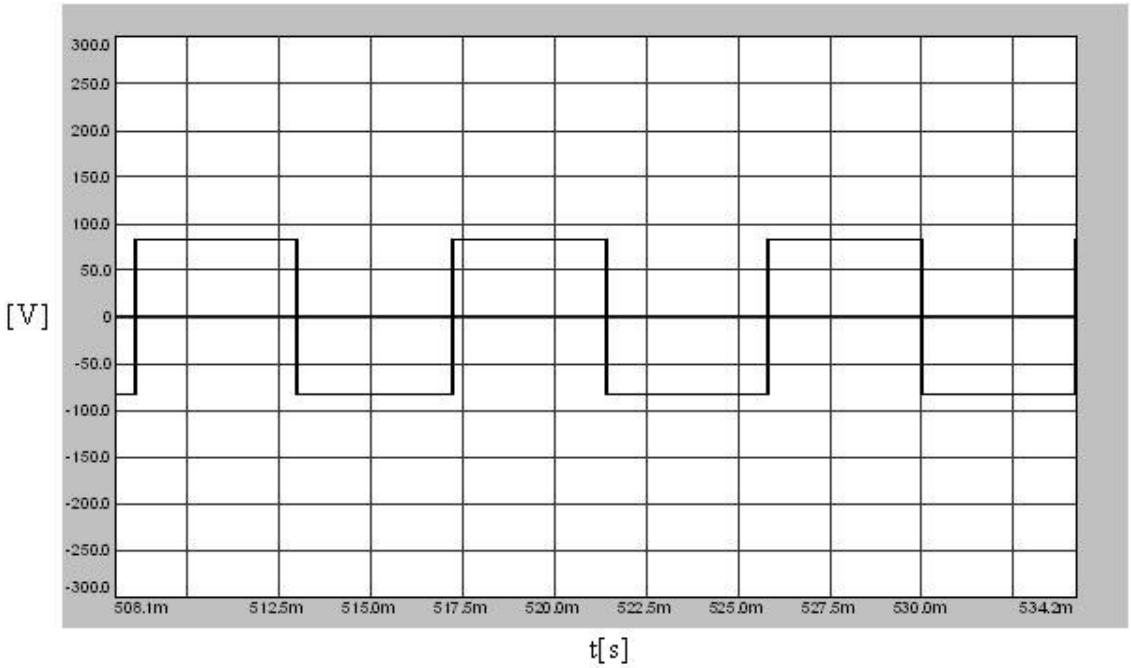


Figure 3.36 CMV of RSPWM3 (M_i=0.61) over a fundamental cycle under no-load.

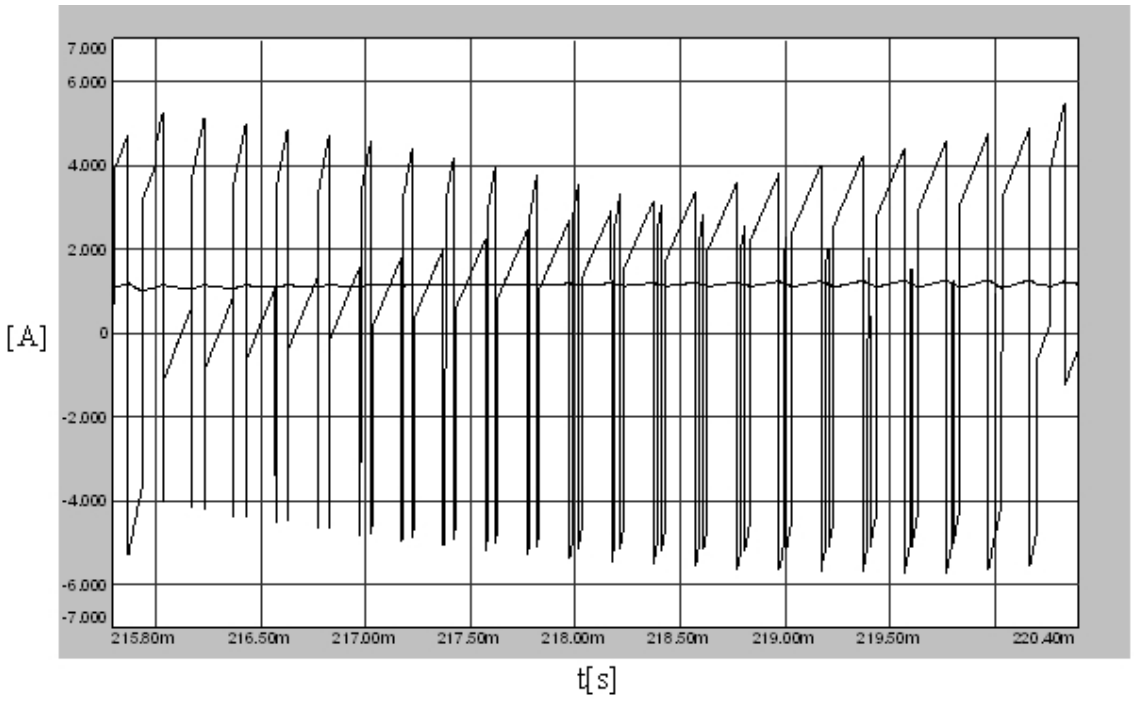


Figure 3.37 The DC link current of RSPWM3 (M_i=0.61) under no-load and its average value.

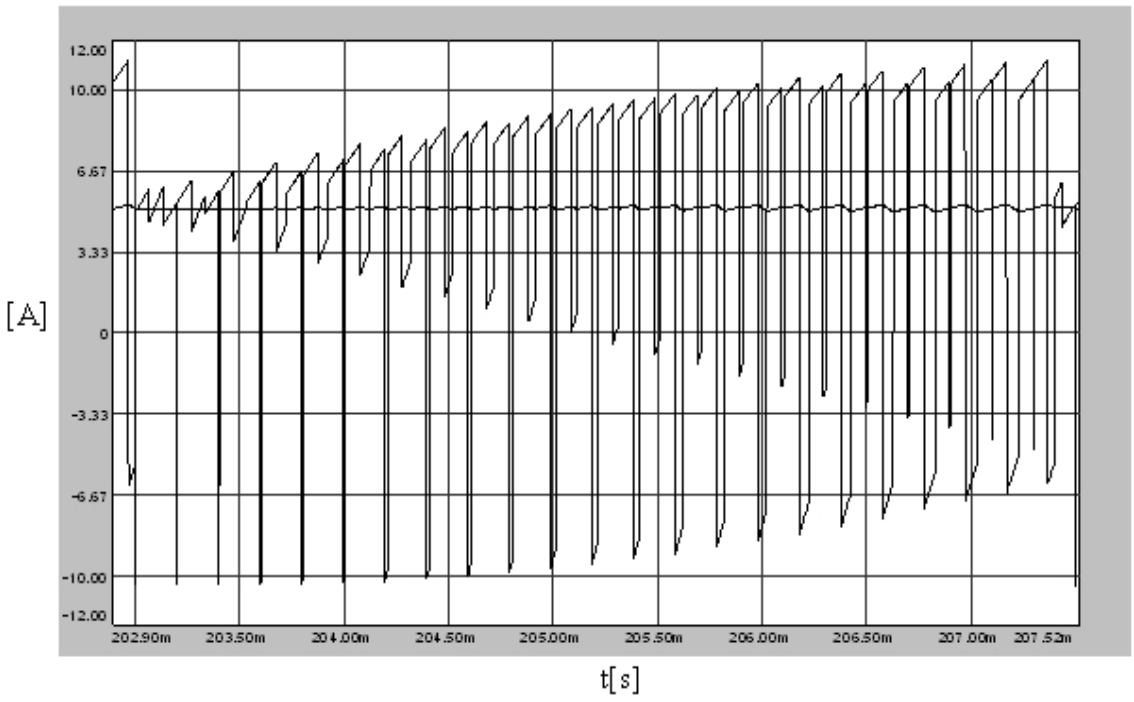


Figure 3.38 The DC link current of RSPWM3 (M_i=0.61) under rated-load and its average value.

3.3.2 Simulation Results at $M_i = 0.9$

In this section the simulation results obtained at M_i=0.9 which correspond to the output phase voltage of 201.4 V_{rms}/57.3 Hz are provided. The simulation results of the modulation signals and the load currents are illustrated under no-load operation and the DC link currents are illustrated for both no-load and rated-load cases for all PWM methods except RSPWM3 (since the voltage linearity range of this method expires at M_i=0.61). CMV simulations are not included since they are just same as at M_i=0.61. Inverter flux simulations are also not included since at high M_i all PWM methods exhibit very low harmonic flux and the magnitude of the harmonic flux over the inverter flux is not easily observable.

In Figure 3.39 the load current of one phase and the corresponding modulation signal are illustrated for NSPWM for M_i=0.9. At high M_i the load current ripple is significantly lower than that at the low M_i case. Also the space dependency is also less such that the difference between the magnitudes of the current ripples when the phase is locked or continuous are not as significant as at the low M_i case.

In Figures 3.40 and 3.41 the DC link current simulation results are provided for no-load and rated-load cases respectively. For both loaded and unloaded cases the DC link current ripple is lower than those at the low M_i case and the DC link current pulses are closer to their average value. Especially under rated-load, although the current ripple is particularly high, wide DC link current pulses are very close to the average value of DC link current and only very narrow and less significant current pulses are distant from the average value. Therefore under rated-load case K_{dc} is very low.

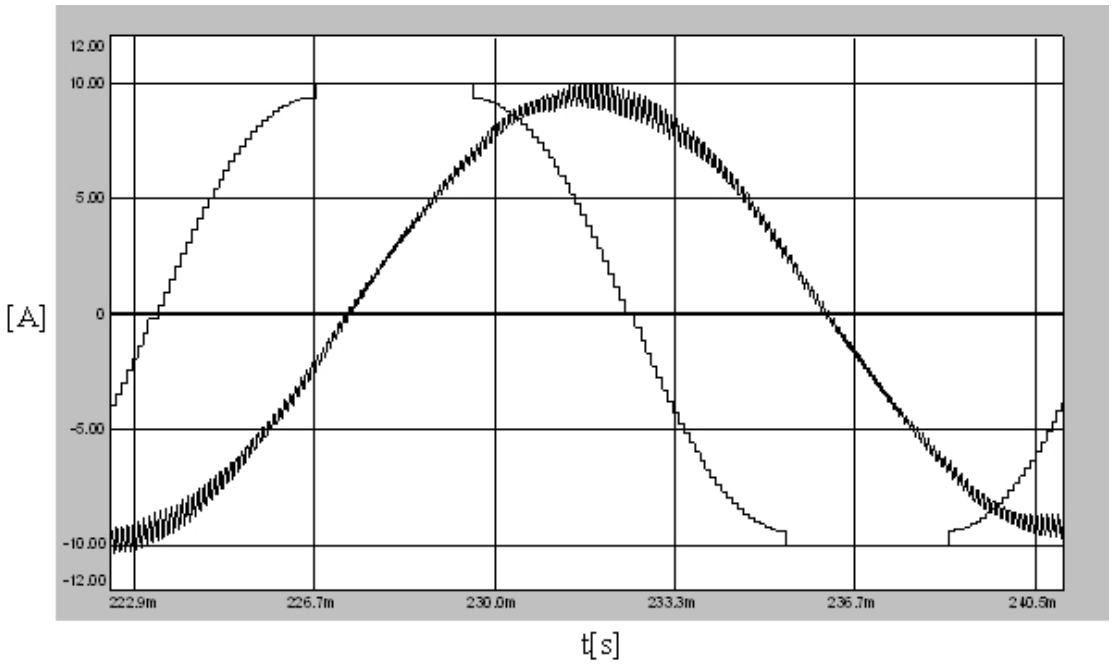


Figure 3.39 One phase load current (scale: x2) and the modulation signal (scale: x10) of NSPWM (M_i=0.9) under no-load.

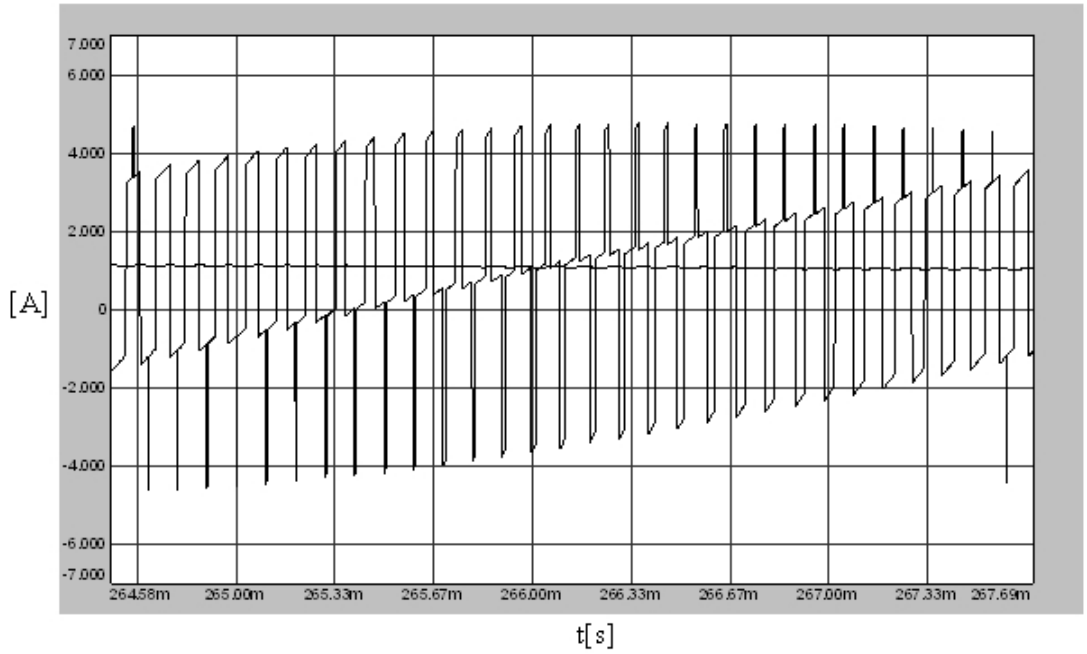


Figure 3.40 The DC link current of NSPWM (M_i=0.9) over a fundamental cycle under no-load and its average value.

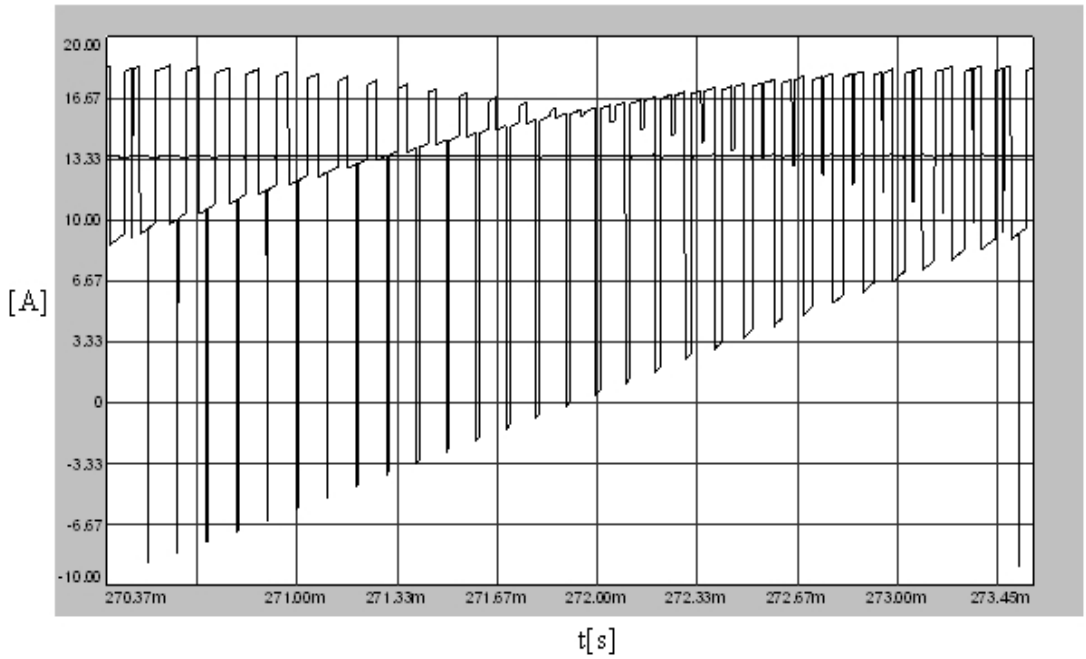


Figure 3.41 The DC link current of NSPWM (M_i=0.9) over a fundamental cycle under rated-load and its average value.

In Figure 3.42 the load current of one phase and the corresponding modulation signal are illustrated for DPWM1 at no-load. Similar to NSPWM, the load current ripple characteristics are improved with increasing M_i and load current ripple content is very low. Comparatively it is lower than that of NSPWM and other PWM methods.

In Figures 3.43 and 3.44 the DC link current simulation results are provided for no-load and rated-load cases respectively for DPWM1. At no-load the DC link current ripple is low and nearly same as those at M_i=0.61 case, however at the loaded case the DC link current ripple performance improves with increasing M_i significantly and the DC link current pulses are very close to their average value.

In Figure 3.45 the load current of one phase and the corresponding modulation signal are illustrated for SVPWM at no-load. The load current ripple characteristics are similar to those at low M_i case for SVPWM and the magnitude of the ripple over the load current is low. However load current ripple performance of SVPWM is inferior to NSPWM and DPWM1.

In Figures 3.46 and 3.47 the DC link current simulation results are provided for no-load and rated-load cases. Just like at low M_i case, under both no-load and rated-load operations the DC link current ripple characteristic of SVPWM are same as that of DPWM1 since both utilize the same voltage vectors and only the shape of the DC link current pulses are slightly different.

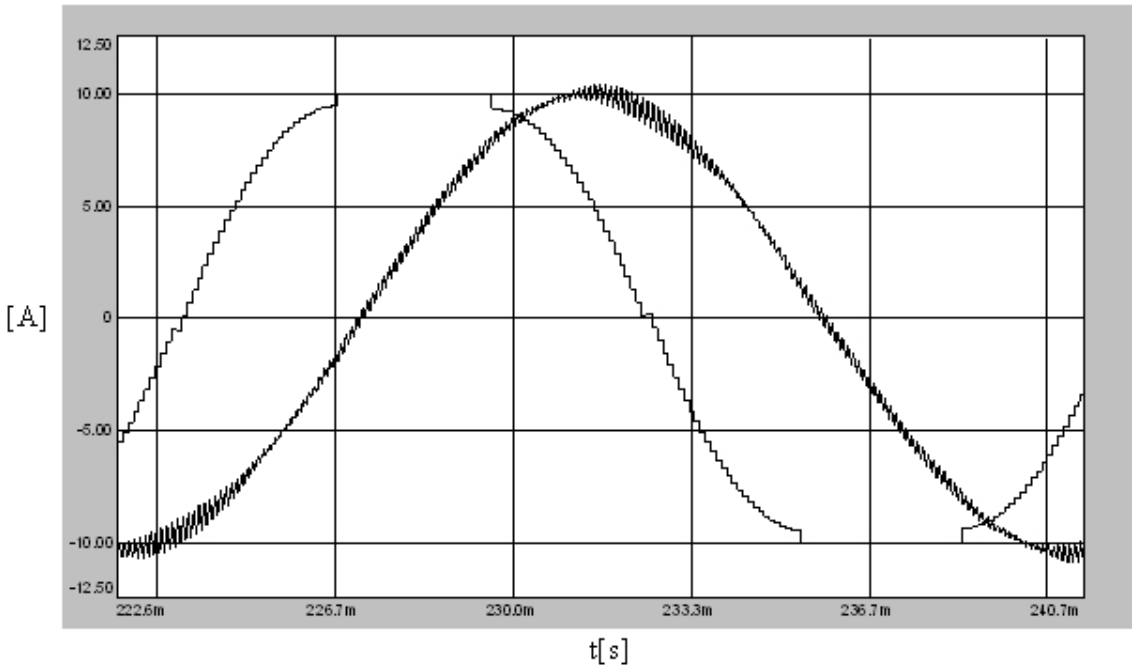


Figure 3.42 One phase load current (scale: x2) and the modulation signal (scale: x10) of DPWM1 (M_i=0.9) under no-load.

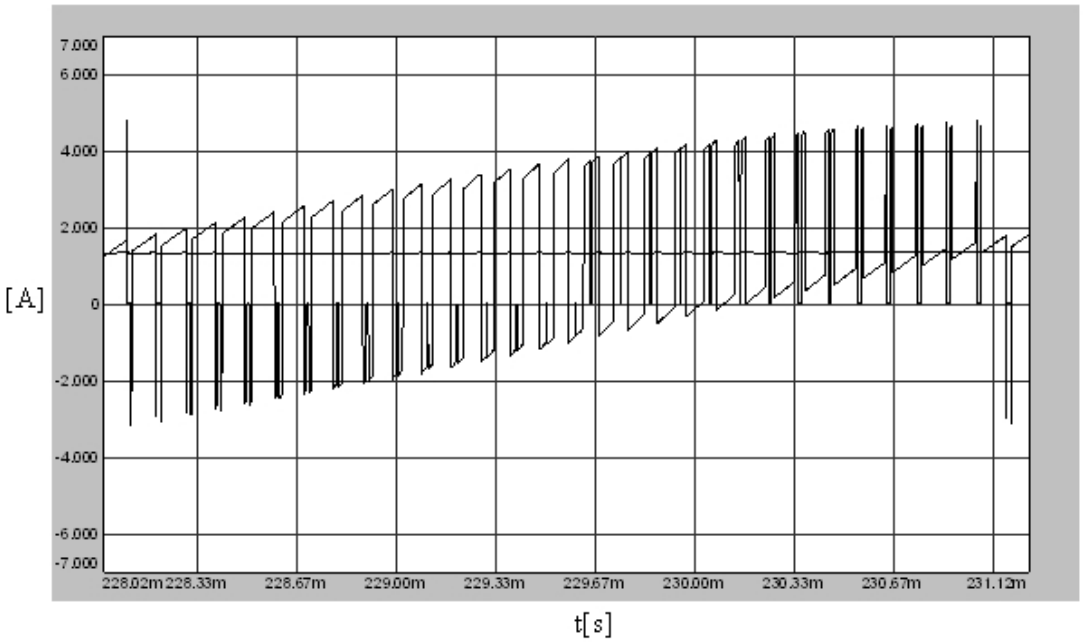


Figure 3.43 The DC link current of DPWM1 (M_i=0.9) under no-load and its average value.

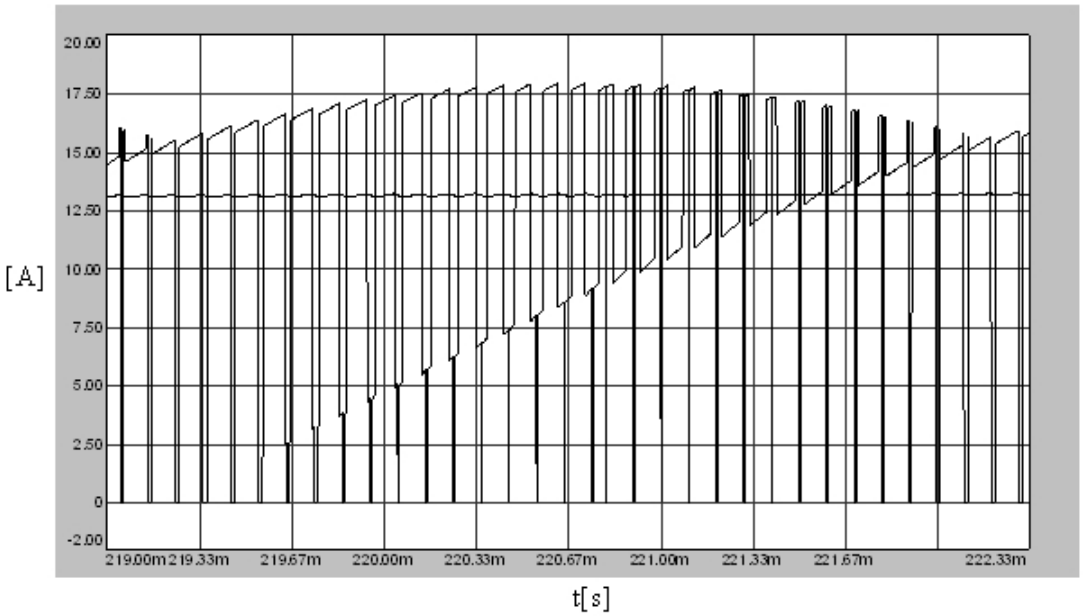


Figure 3.44 The DC link current of DPWM1 (M_i=0.9) under rated-load and its average value.

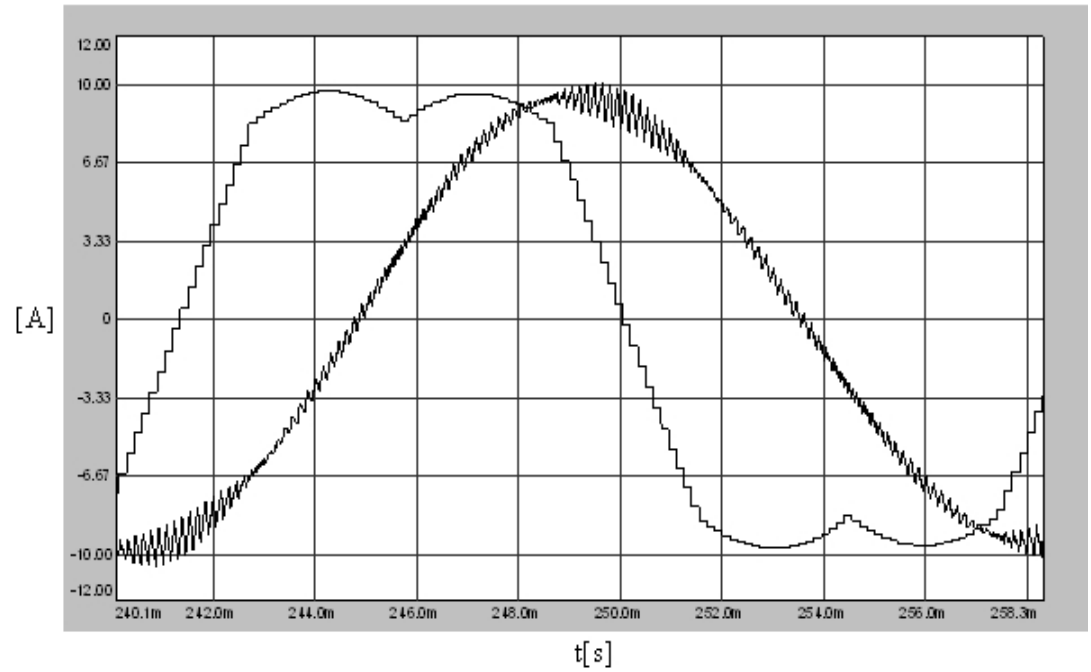


Figure 3.45 One phase load current (scale: x2) and the modulation signal (scale: x10) of SVPWM (M_i=0.9) under no-load.

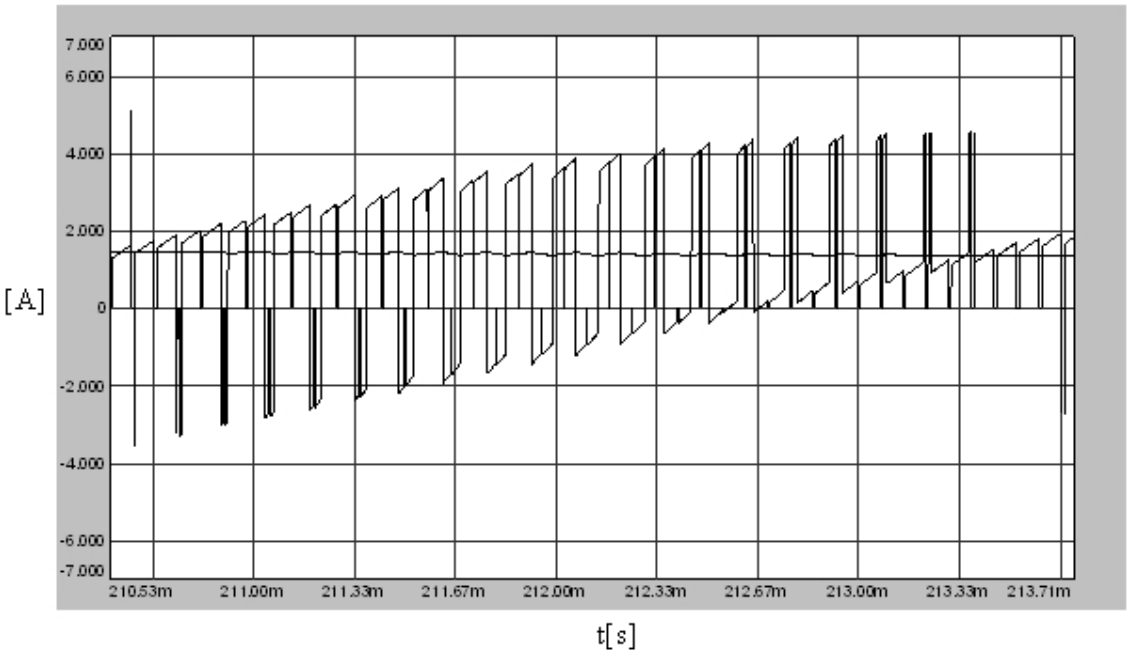


Figure 3.46 The DC link current of SVPWM (M_i=0.9) under no-load and its average value.

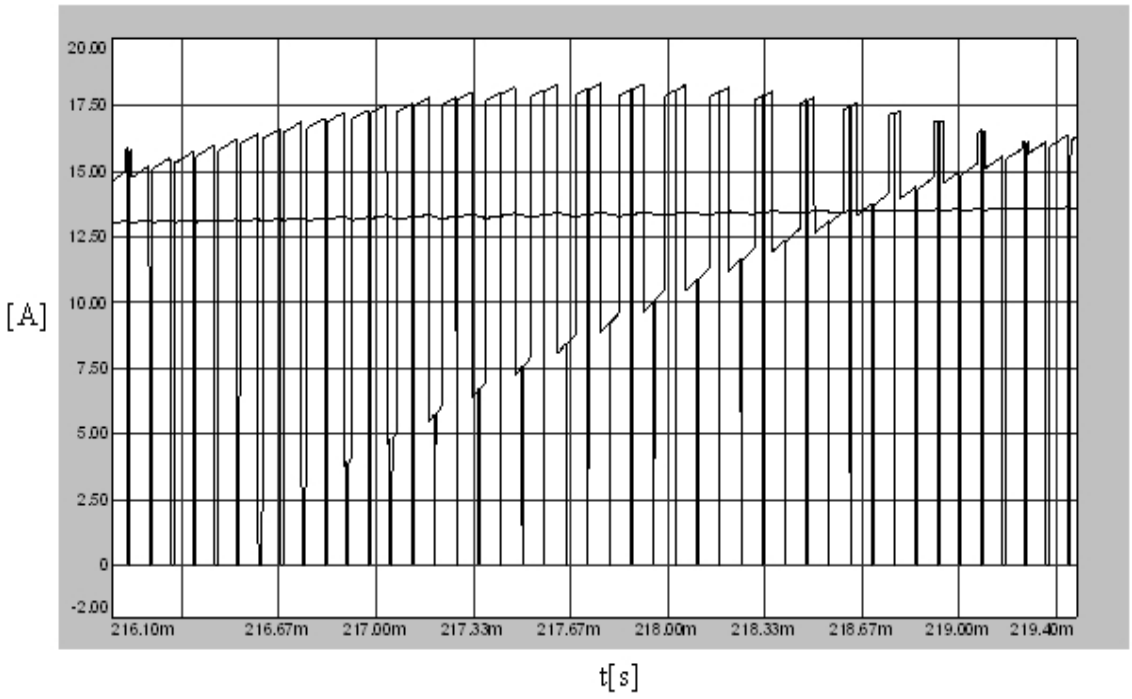


Figure 3.47 The DC link current of SVPWM (M_i=0.9) under full-load and its average value.

In Figure 3.48 load current of one phase and the corresponding modulation signal are illustrated for AZSPWM1 at no-load. Similar to those of other PWM methods the load current ripple characteristic of AZSPWM1 is improved with increasing M_i. However the harmonic ripple content is still higher than those of standard PWM methods and NSPWM.

In Figures 3.49 and 3.50 the DC link current simulation results are provided for no-load and rated-load cases respectively for AZSPWM1. For both no-load and rated-load cases the magnitudes of the DC link current ripples are higher than those of standard methods. However unlike at low M_i case, DC link current pulses which are relatively wide are very close to the DC link current average value and only very narrow and less significant current pulses are distant from the average value. Therefore K_{dc} is low for M_i=0.9 and even lower for the high power factor operations.

In Figure 3.51 load current of one phase and the corresponding modulation signal are illustrated for AZSPWM2 at no-load. The load current ripple of AZSPWM2 is reduced with increasing M_i but it is still higher than those of other methods discussed.

In Figures 3.52 and 3.53 the DC link current simulation results are provided for AZSPWM2 for no-load and rated-load cases respectively. Just like at low M_i case for both no-load and rated-load cases the DC link current characteristics of AZSPWM2 are nearly same as AZSPWM1 since both utilize the same voltage vectors and only the shape of the DC link current pulses are slightly different.

RSPWM3 method is not simulated for M_i=0.9 case since its voltage linearity range expires at this point.

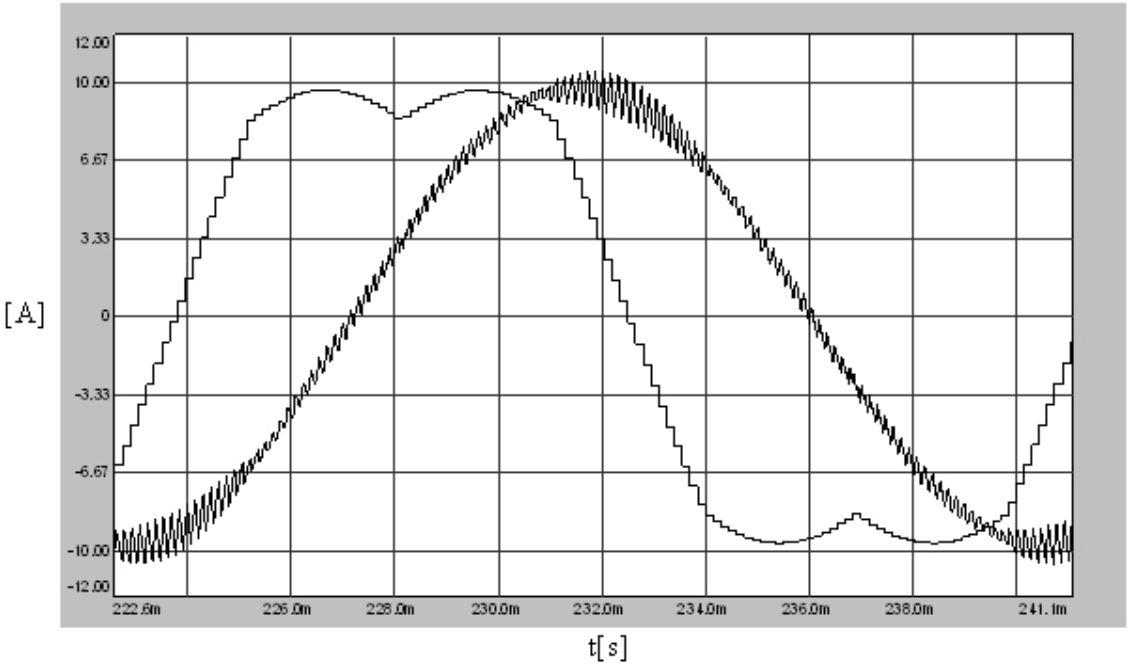


Figure 3.48 One phase load current (scale: x2) and the modulation signal (scale: x10) of AZSPWM1 (M_i=0.9) under no-load.

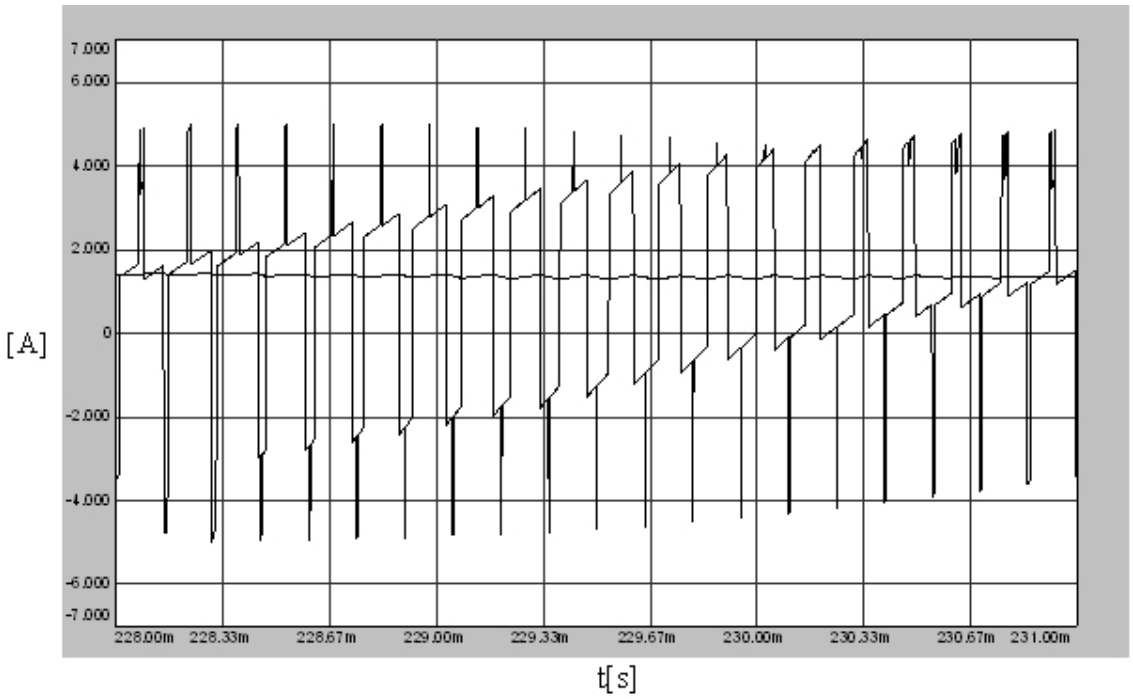


Figure 3.49 The DC link current of AZSPWM1 (M_i=0.9) under no-load and its average value.

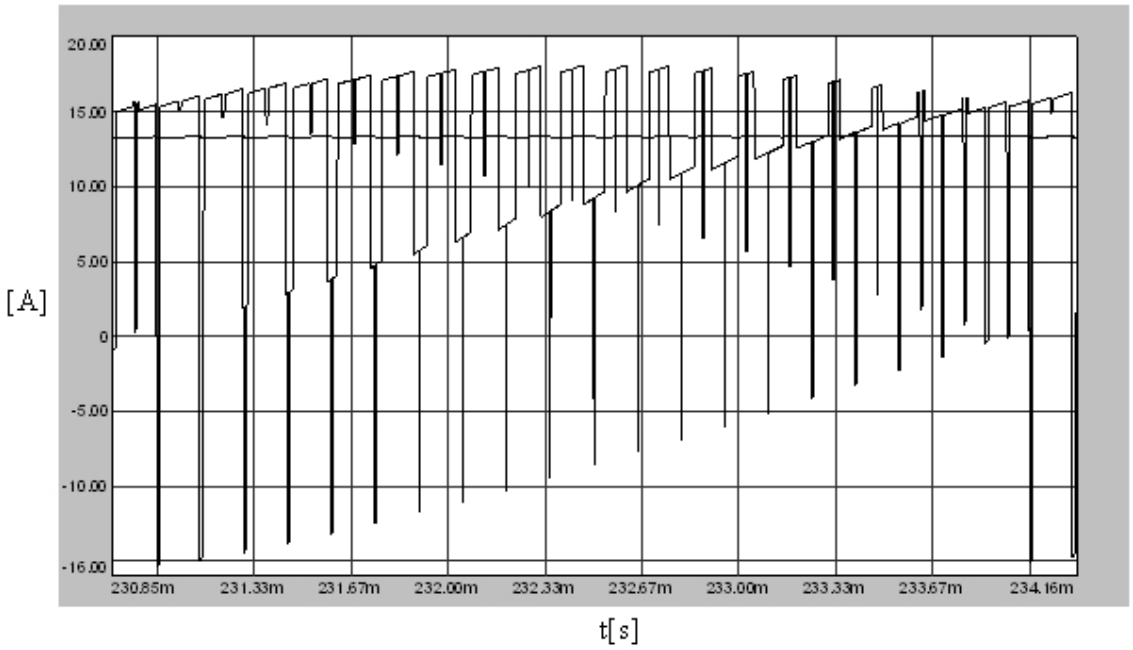


Figure 3.50 The DC link current of AZSPWM1 (M_i=0.9) under rated-load and its average value.

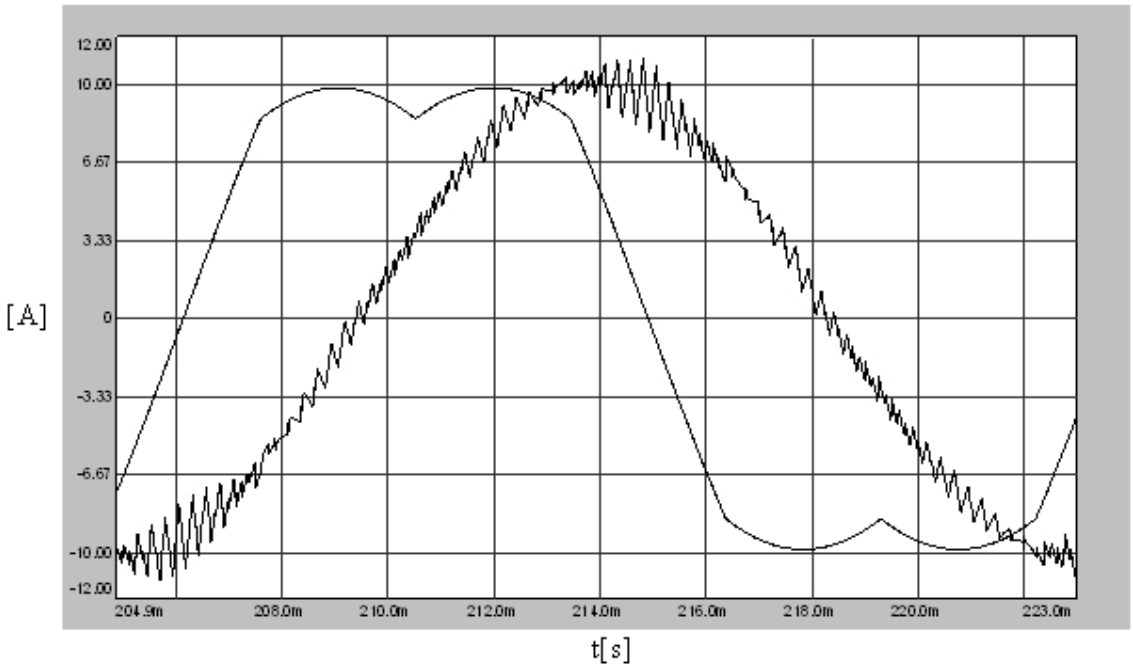


Figure 3.51 One phase load current (scale: x2) and the modulation signal (scale: x10) of AZSPWM2 (M_i=0.9) under no-load.

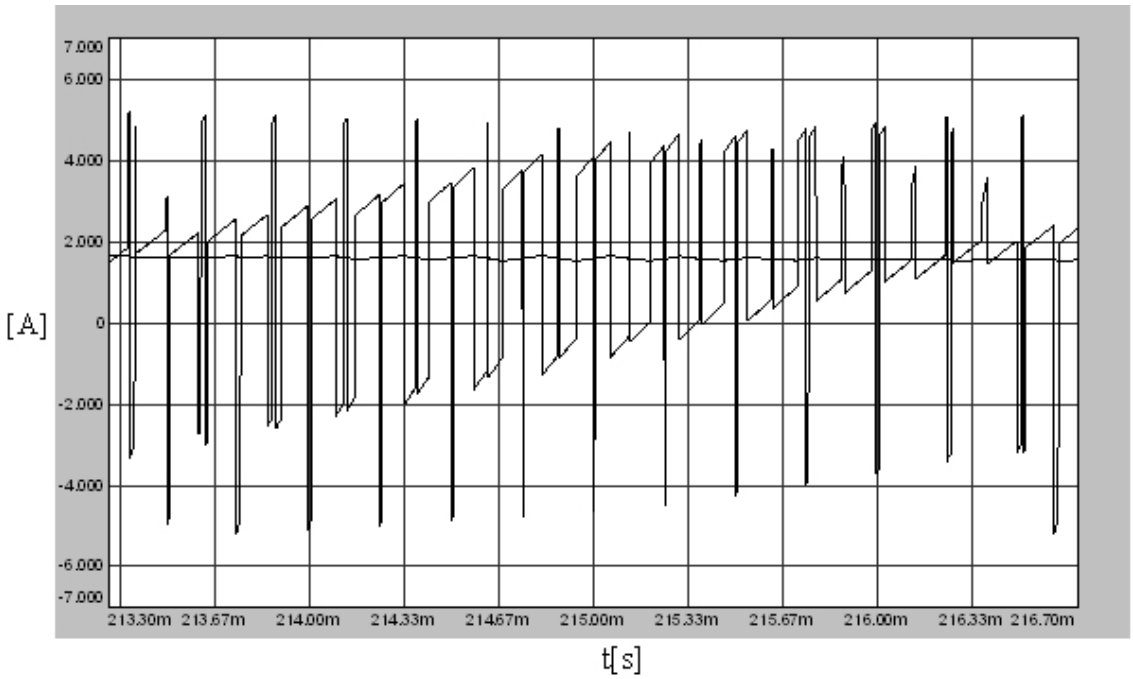


Figure 3.52 The DC link current of AZSPWM2 (M_i=0.9) under no-load and its average value.

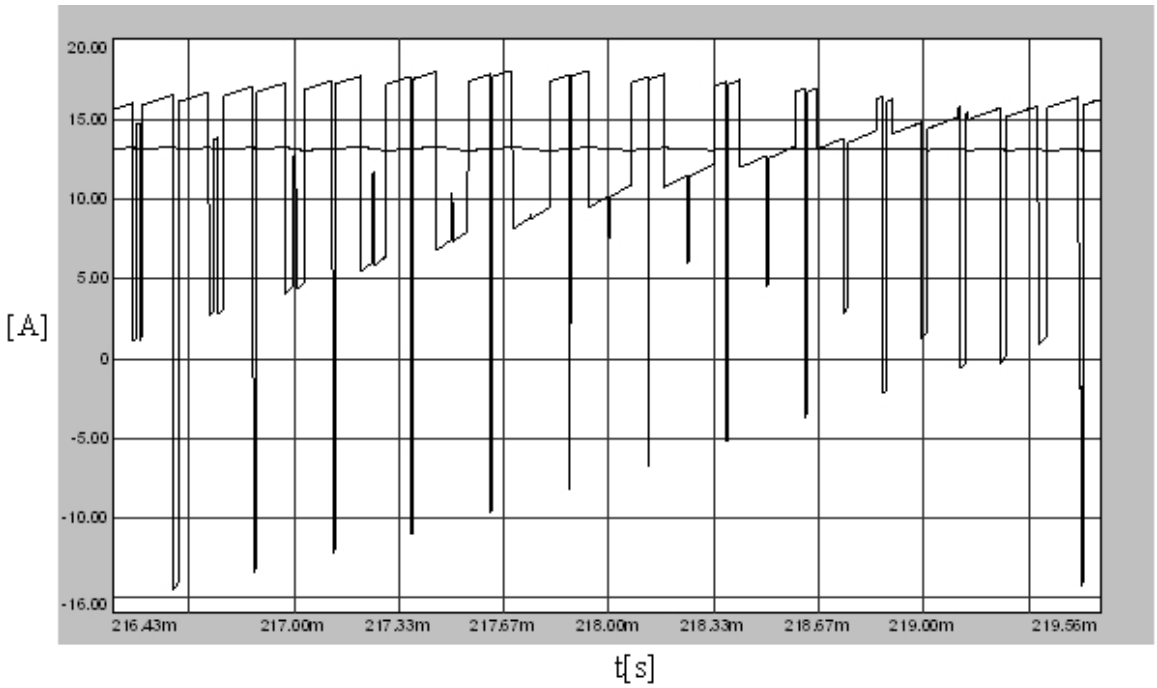


Figure 3.53 The DC link current of AZSPWM2 (M_i=0.9) under rated-load and its average value.

3.4 Simulations of the Combined Algorithm

The performance analysis and the simulation results reveal the superior characteristics of NSPWM within all other RCMV-PWM methods. However it is impossible to utilize NSPWM under its voltage linearity range as an RCMV-PWM method. In order to reduce the CMV inside the voltage nonlinear region of NSPWM which is illustrated as unshaded hexagon in Figure 2.20.e, another RCMV-PWM method should be utilized. Of the remaining RCMV-PWM methods AZSPWM1 is superior to other methods and as Figure 2.37 illustrates AZSPWM1 is selected for combined algorithm to utilize at low M_i together with NSPWM which is utilized at high M_i to reduce the CMV.

In order to illustrate the transitions at the instants of entering from one modulation method to other modulation method, computer simulations are conducted. The control algorithm is selected such that AZSPWM1 is utilized inside the unshaded

hexagon shown in Figure 2.20.e, which corresponds to the voltage non-linear region of NSPWM, and NSPWM is utilized elsewhere. The ASD is operated at M_i=0.58 (f_s=37 Hz) under no-load and rated-load operations. At the adjusted M_i the reference voltage vector enters and exits the voltage linearity region of NSPWM several times in a fundamental cycle (six times). This allows examine the transitions from one method to other at a steady-state operating speed of the motor. From here the dynamic transitions can also be predicted. If these transitions create no disturbances in the motor current/torque/speed, then other transitions also should exhibits the same behavior.

In Figure 3.54 load current of one phase and the corresponding modulation signal are illustrated for NSPWM at M_i=0.58. Similarly in Figure 3.55 the waveforms of the same quantities of AZSPWM1 are illustrated at same M_i. As explained in the section 2.4.3, by utilizing the scalar implementation of NSPWM under the voltage linearity region, the obtained voltage vectors and their sequence are different than those of the defined NSPWM pulse pattern. Therefore at this modulation index NSPWM can not be utilized as an RCMV-PWM method since zero-voltage vectors are generated resulting in high CMV. However, at this M_i value the method provides linearity and allows normal operation of the motor as can be observed from the current waveform. However the ripple is relatively high. On the other hand, only in a specific segment the method operates in the RCMV region of NSPWM where the CMV is reduced as targeted. Outside this range/segment, the method is not favorable. Therefore AZSPWM1 should be utilized in the combined algorithm wherever NSPWM can not be utilized as an RCMV-PWM method (in its non-linear region).

In Figure 3.56 the resulted reference signals of all three phases of the combined PWM algorithm is illustrated such that the applied reference signal is same as that of AZSPWM1 when AZSPWM1 is utilized and is same as that of NSPWM when NSPWM is utilized. In Figure 3.57 CMV of the combined algorithm is illustrated over a fundamental cycle such that it is reduced and it alternates between -83V and 83V ($-V_{dc}/6$ and $V_{dc}/6$). In Figure 3.58 load current of one phase and the corresponding modulation signal of the combined algorithm is illustrated for no-load

operation. The ripple over the load current shows the characteristics of the applied PWM method at that instant. Although there is a ripple over the load current, transitions from one method to another do not result in dynamics. This is due to the fact that every PWM period the ripple flux is reset and no transients remain. In Figure 3.59 the inverter flux over a fundamental cycle and its 60^o zoom-in view are illustrated such that the inverter flux is continuous during the transitions from one method to other. In Figure 3.60 load current of one phase and the corresponding modulation signal of the combined algorithm is illustrated for rated-load operation. Similar to the no-load operation during the transition instants unwanted dynamics are not resulted and transitions are achieved smoothly. Simulation results verify the feasibility of utilizing the combined PWM algorithm such that the algorithm does not result in any problems since the fundamental component of the reference signals are same and continuous.

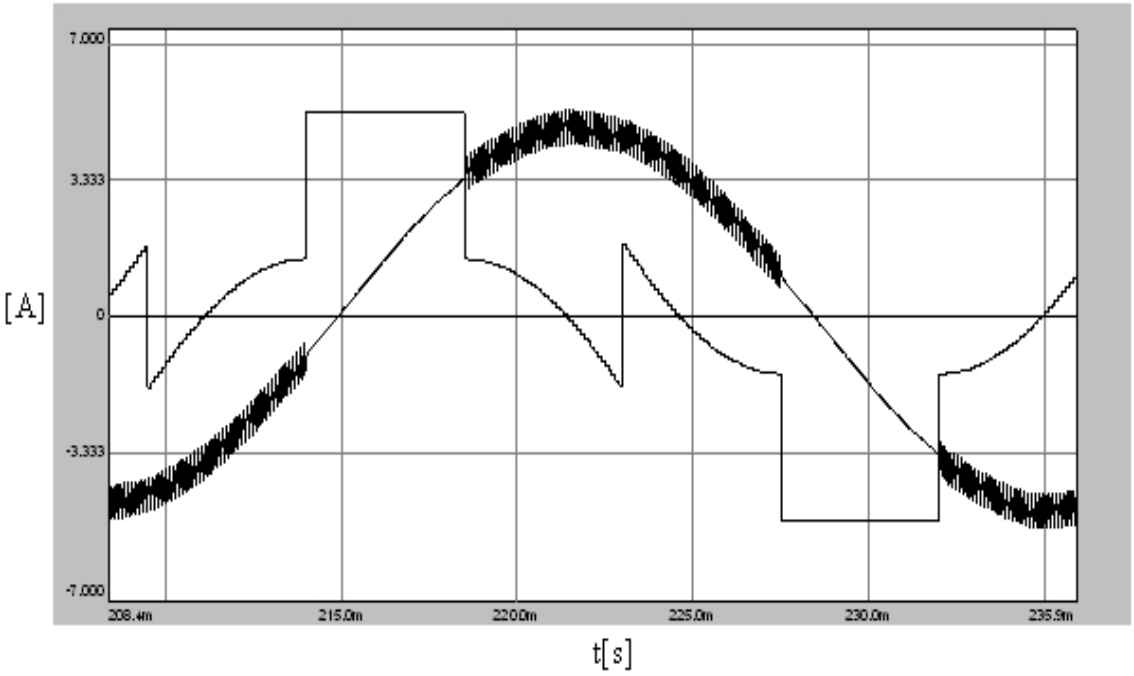


Figure 3.54 One phase load current and the modulation signal (scale: x5) of NSPWM (M_i=0.58) under no-load.

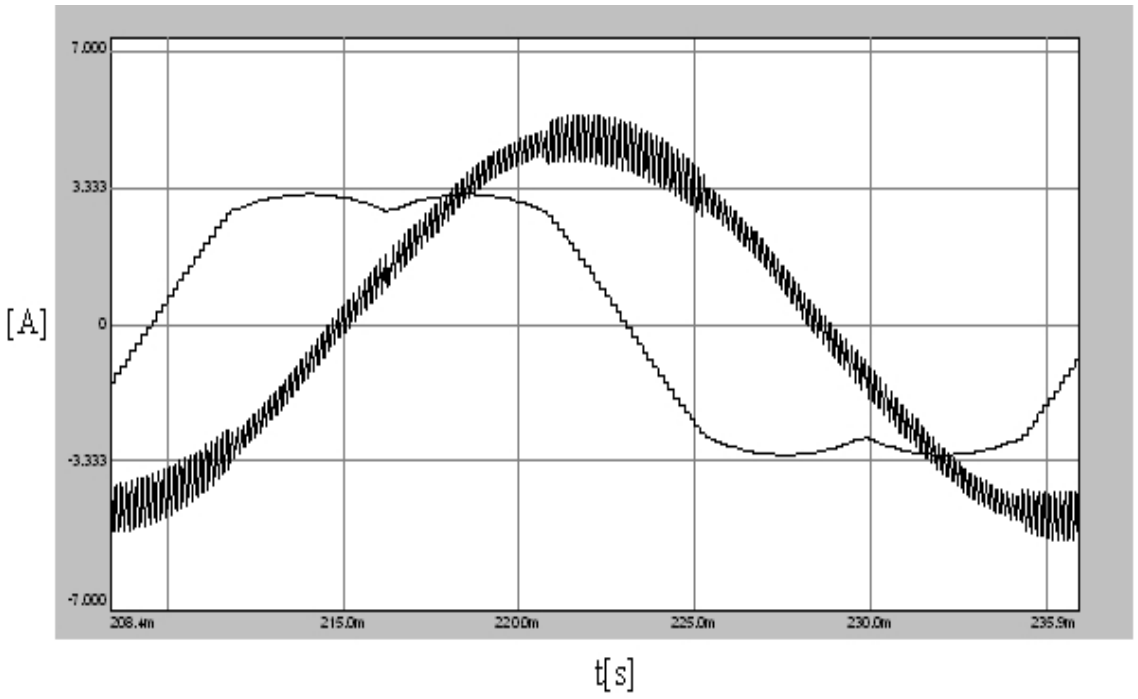


Figure 3.55 One phase load current and the modulation signal (scale: x5) of AZSPWM1 (M_i=0.58) under no-load.

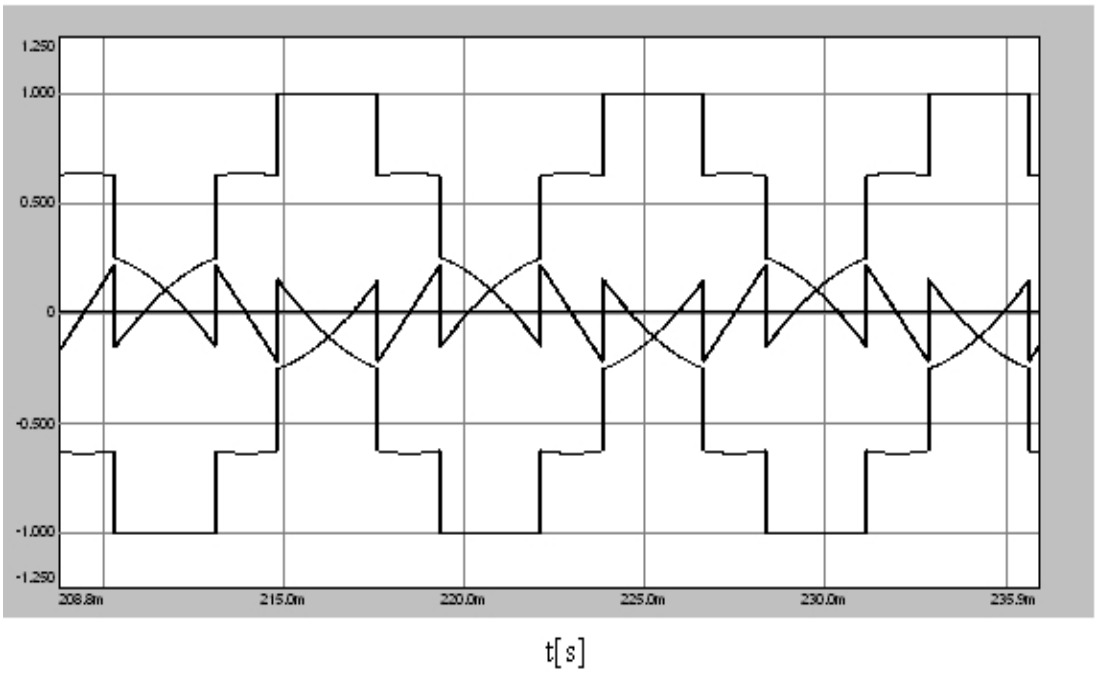


Figure 3.56 The modulation signal of all three phases for the combined algorithm (M_i=0.58).

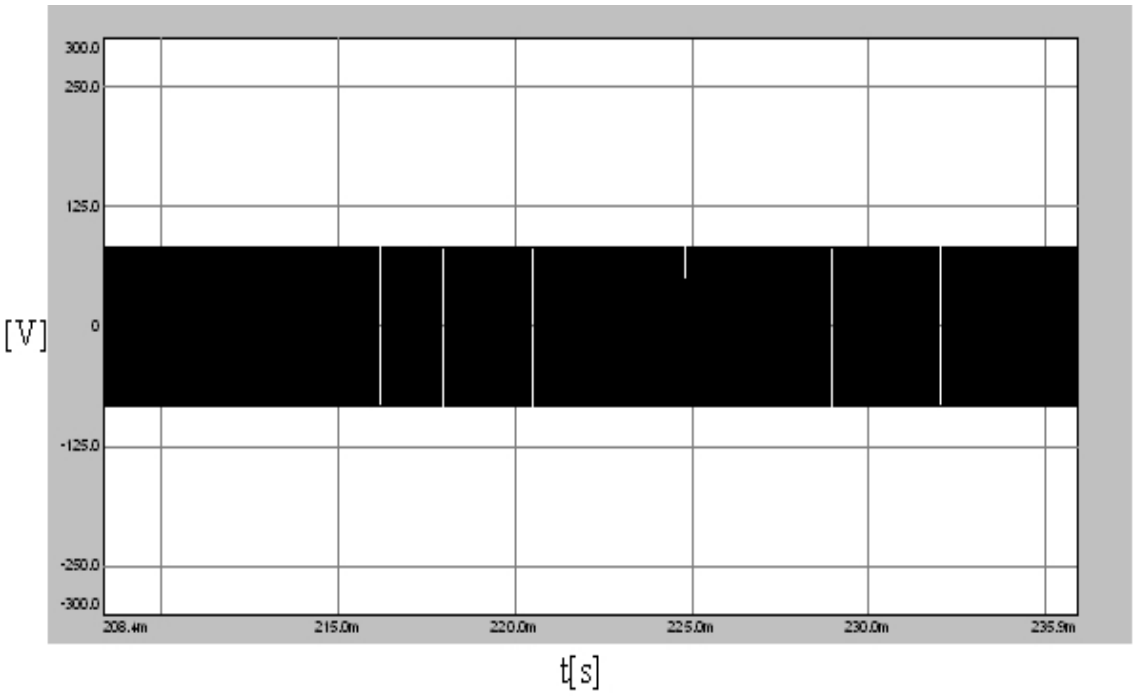


Figure 3.57 CMV of the combined algorithm (M_i=0.58) over a fundamental cycle under no-load.

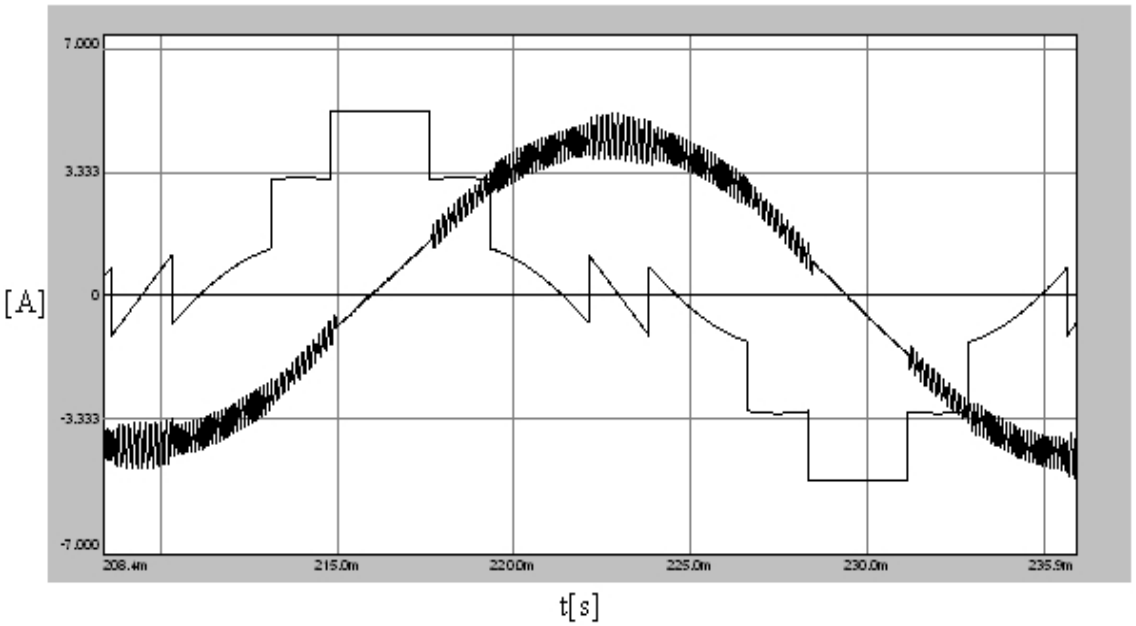
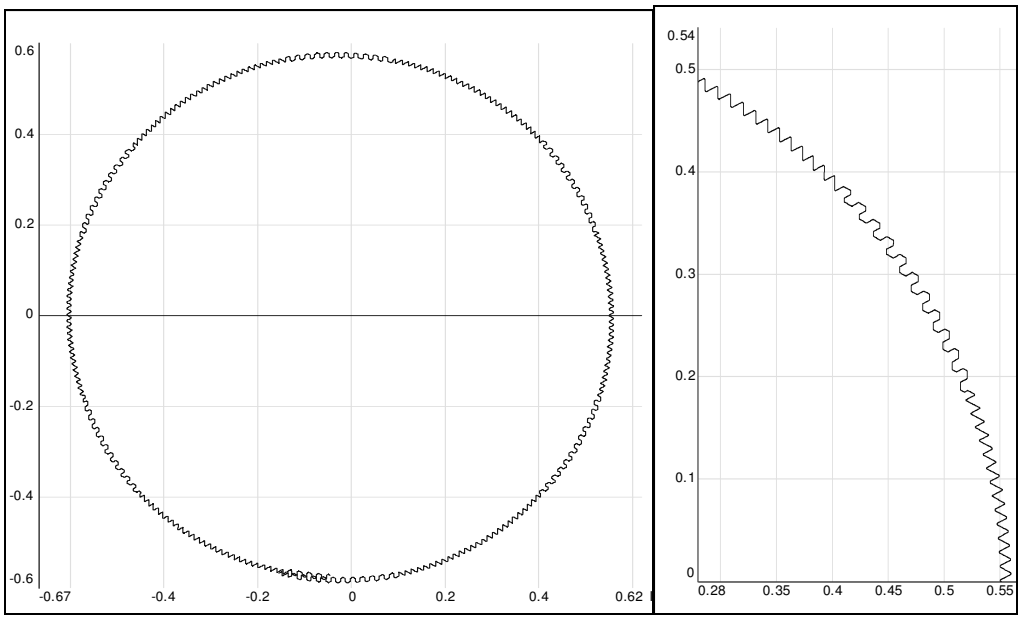


Figure 3.58 One phase load current and the modulation signal (scale: x5) of the combined algorithm (M_i=0.58) under no-load.



(a) (b)

Figure 3.59 Inverter flux of the combined algorithm (M_i=0.58) under no-load (a) and the zoom-in view over a 60^o interval (b).

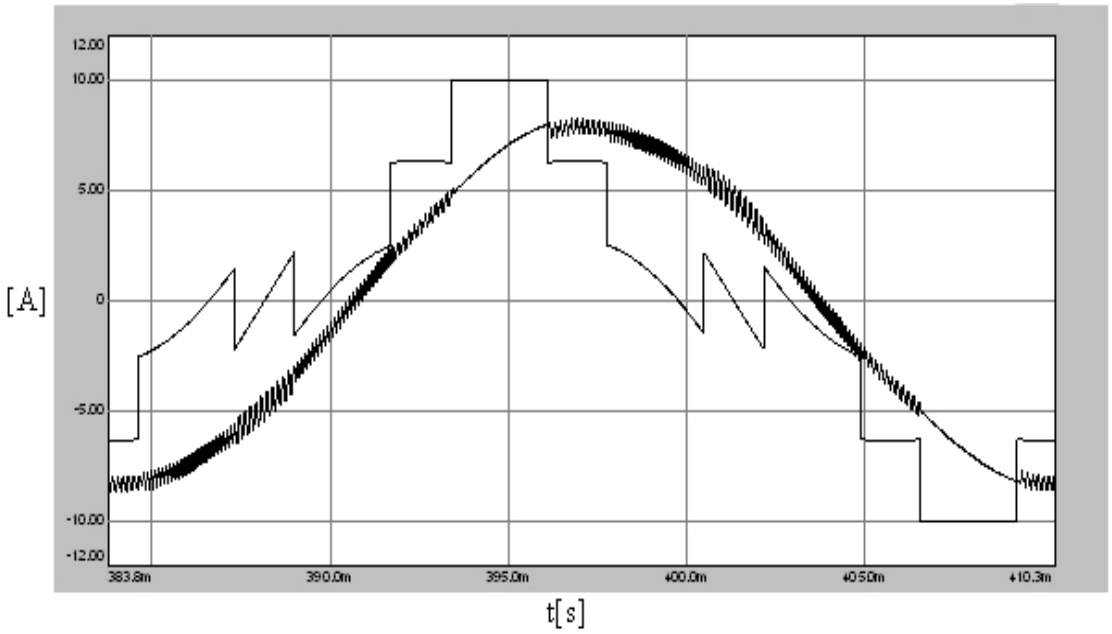


Figure 3.60 One phase load current and the modulation signal (scale: x10) of the combined algorithm (M_i=0.58) under rated-load.

3.5 Summary

In this chapter important PWM attributes of the PWM methods which are the inverter load current, the common mode voltage, and the DC link current harmonic content are investigated for various PWM methods by means of computer simulations. The load current waveforms are simulated for two different modulation indices under no-load operation and the highest measured peak-to-peak current ripples are tabulated in Table 3.2. For both modulation indices, load current rms value is approximately 3.4 A for all PWM methods. In the same table expected HDF values which are calculated in Chapter 2 are also tabulated for comparison. As expected there are no direct proportion between the HDF and the largest ripple magnitude, however it is observed that generally the PWM methods with higher HDF have higher load current ripple. At M_i = 0.61 the load current ripple of SVPWM and DPWM1 are significantly lower than those of the RCMV-PWM methods. Of the RCMV-PWM methods, NSPWM has the least load current ripple where AZSPWM1, AZSPWM2, and RSPWM3 methods exhibit very high load current ripple. At M_i = 0.9 the load current ripples of NSPWM and DPWM1 are close to each other and lower than all other methods. The load current ripple of SVPWM and AZSPWM1 are close to each other and practically low, whereas AZSPWM2 has very high load current ripple.

Table 3.2 Magnitudes of largest peak-to-peak current ripples and HDF of PWM methods

	Largest peak-to-peak current ripple (I_{1rms}=3.4 A)		**HDF**	
	M_i=0.61	**M_i=0.9**	**M_i=0.61**	**M_i=0.9**
NSPWM	0.84 A	0.62 A	0.81	0.25
SVPWM	0.60 A	0.85 A	0.24	0.36
DPWM1	0.59 A	0.61 A	0.29	0.18
AZSPWM1	1.20 A	0.96 A	1.50	0.48
AZSPWM2	1.58 A	1.50 A	1.79	0.82
RSPWM3	1.61 A	NA	1.70	NA

CMV simulation results illustrates that NSPWM, AZSPWM1, AZSPWM2, and RSPWM3 have CMV of maximum magnitude of 83V (V_{dc}/6) which is the 1/3 of those of the DPWM1 and SVPWM. Therefore simulation results illustrate the low CMV characteristics of the RCMV-PWM methods.

The DC link current waveforms are simulated for two different modulation indices for both no-load and rated-load cases. K_{dc} is obtained from simulated DC link current for each PWM method and are tabulated in Table 3.3. Similarly in the same table expected K_{dc} values which are calculated in Chapter 2 are also tabulated for comparison. It is observed that the simulated and calculated K_{dc} values are very close to each other. As expected, simulated K_{dc} values of SVPWM and DPWM1 are practically equal to each other for all operating points. Similarly both AZSPWM1 and AZSPWM2 have also practically equal simulated K_{dc} values for all operating points.

At M_i=0.61 at no-load, the harmonic contents of the DC link currents of the standard PWM methods are several times lower than those of the RCMV-PWM methods. Of the RCMV-PWM methods, RSPWM3 has the least DC link harmonic current where NSPWM and both AZSPWM methods have very high DC link current harmonic

content. Under rated-load operation the differences between K_{dc} of standard and RCMV-PWM methods decrease. Standard PWM methods still have relatively low DC link current harmonics. The performance characteristics of the RCMW-PWM methods except RSPWM3 are improved and especially NSPWM exhibits low DC link current ripple which is close and slightly inferior to the standard PWM methods.

At M_i=0.9 under no-load operation, K_{dc} of standard PWM methods are low and superior to the RCMV-PWM methods. AZSPWM methods have slightly less DC link current ripple than NSPWM method. Under rated-load operation (at high PF) all PWM methods have very low K_{dc} measurements which are very close to each other where AZSPWM methods have slightly higher DC link current harmonic content than the standard PWM methods and NSPWM method.

As a result it can be summarized that at high M_i the NSPWM method exhibits satisfactory PWM characteristics. At low M_i, due to its poor CMV performance NSPWM is not favorable and there AZSPWM1 which has satisfactory PWM ripple performance and low CMV is preferable. Thus, the study favors the combination of the two methods.

In this chapter the combined algorithm of NSPWM and AZSPWM1 is simulated and the results show that implementation of this algorithm is possible without resulting in any problems.

In the next chapter practical investigations of the results of CMV; and the CMC resulting mechanisms are studied. Practical CMV/CMC mitigation methods will be investigated in detail.

Table 3.3 Calculated K_{dc} values compared to the simulation results.

	M_i=0.61				**M_i=0.9**			
	No-Load		**Rated-Load**		**No-Load**		**Rated-Load**	
	Simulation	Calculated	Simulation	Calculated	Simulation	Calculated	Simulation	Calculated
NSPWM	1.09	1.13	0.46	0.47	0.49	0.45	0.17	0.16
SVPWM	0.24	0.22	0.34	0.33	0.32	0.30	0.17	0.15
DPWM1	0.24	0.22	0.35	0.33	0.32	0.30	0.17	0.15
AZSPWM1	0.84	0.85	0.59	0.58	0.42	0.40	0.20	0.19
AZSPWM2	0.80	0.85	0.55	0.58	0.39	0.40	0.21	0.19
RSPWM3	0.63	0.63	0.75	0.68	NA	NA	NA	NA

CHAPTER 4

COMMON MODE VOLTAGE AND COMMON MODE CURRENT

4.1 Introduction

The common mode voltage of a three-phase inverter drive (V_{no}) is defined in Chapter 1.2 and expressed as (1.1). Although the values that the CMV takes at different inverter topologies are different, formula (1.1) is valid for all two-level or higher-level voltage source inverters. The inverter switch states, output phase voltages, and corresponding V_{no} which is calculated as (1.1) are tabulated for a two-level VSI in Table 4.1.

Table 4.1 Two-level VSI switch states and CMV.

S_{a+} S_{b+} S_{c+}	V_{ao}	V_{bo}	V_{co}	V_{no}
0 0 0	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$
1 0 0	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
1 1 0	$V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/6$
0 1 0	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/6$
0 1 1	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/6$
0 0 1	$-V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	$-V_{dc}/6$
1 0 1	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/2$	$V_{dc}/6$
1 1 1	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$

In two-level three-phase VSIs for all inverter switch states the CMV has high magnitude and its magnitude is changed at each switching instant. Due to the high dv/dt and magnitude of the CMV, leakage currents (CMCs) flow from the motor to the ground and through other CMC paths [21], [22] such as from the transmission

cables to the ground. The CMC results in fluting bearing failures, EMI and nuisance trips in the system [7].

In this chapter the generation of CMV at different inverter topologies is discussed. The CMC and the bearing currents which are the main undesired effects of CMV are studied. Types of the CMCs and the bearing currents and their generating mechanisms are discussed by investigating the equivalent high frequency model of the induction motor and the drive. Factors affecting the CMC and CMV and the CMV/CMC mitigation methods are reviewed.

4.2 CMV in Different Inverter Topologies

There are various types of VSIs available and they are utilized at different applications. All VSI types have different CMV attributes. The two-level three-phase voltage source inverter is the most common inverter type utilized at the low voltage applications (DC-bus voltage of 500-600V). However as the DC-bus voltage level is increased, the two-level VSI is not preferred since high blocking voltage (V_{dc}) is required over the switches. Also the change of the VSI output voltage during the switching instants is high ($V_{dc}/2$) in the two-level inverter. Therefore, in the higher DC-bus voltage level applications than 500-600V, often three or higher-level VSIs are utilized since they result in less voltage stress over the semiconductor switches. In Figure 4.1 the Neutral Point Clamped (NPC) three-level VSI is illustrated [23].

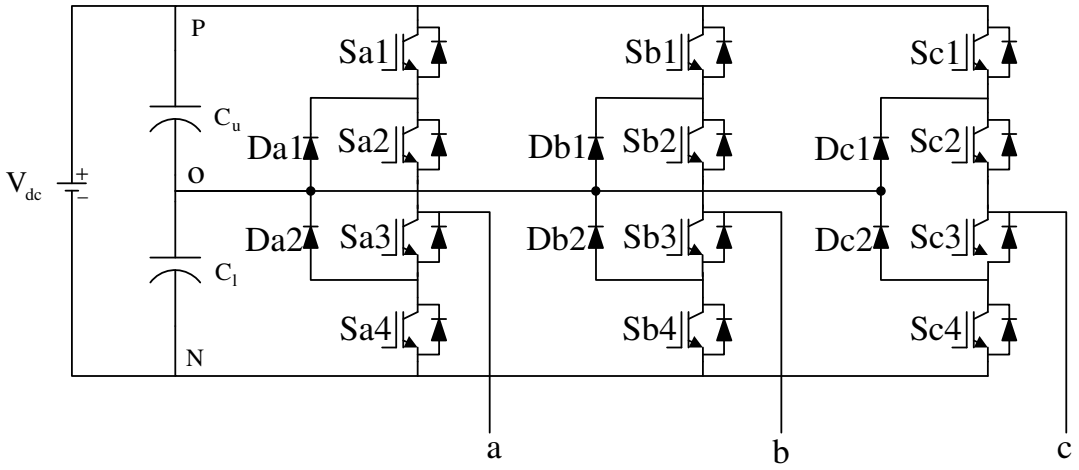


Figure 4.1 The three-level neutral point clamped VSI topology.

In the NPC three-level VSI, CMV is as defined in (1.1) just like the two-level VSI. However in the NPC three-level inverter, output phase voltage can take three different voltage values according to the switch states. The output phase voltage is $+V_{dc}/2$, 0, or $-V_{dc}/2$ when the top, middle or bottom two switches of the corresponding phase are on-state respectively [24]. As a result, in the NPC three-level VSI, CMV magnitude can be $V_{dc}/2$, $V_{dc}/3$, $V_{dc}/6$ or 0 according to the switch states and the change of the CMV at each switching instant is $V_{dc}/6$ which is the half of that of the two-level inverter [24]. In the higher DC-bus voltage operations, higher-level VSIs are utilized and the change of the output phase voltage and hence that of CMV are further reduced. The CMV values defined here are topologic properties of the three-level inverters and some of these CMV voltage levels may not be generated at different PWM methods. By utilizing these PWM methods CMV can be reduced in NPC three-level VSIs [25], [26], [27].

The most common PWM method utilized in the NPC three-level VSI is the Nearest Triangle Vector (NTV) PWM method. In this method each 60^o sector of the voltage vector space is divided into four triangles (Figure 4.2) and the voltage vectors pointing the edges of the triangle in which the reference voltage vector is inside are utilized. The switch state and CMV pulse pattern of the NTV PWM method are illustrated in Figure 4.3 for four different triangles of region A1 [24]. As the figure

illustrates, only in triangle T_1 the magnitude of CMV reaches $V_{dc}/2$, and in other three triangles (T_2, T_3 and T_4) the magnitude of the CMV is limited at $V_{dc}/3$. Note that V_{ref} is inside T_1 only when M_i is low; at high M_i values V_{ref} enters only T_2, T_3, and T_4. Therefore CMV of the three-level VSIs is low at the operations at high M_i when NTV PWM method is utilized. Additionally CMV can take "0" value at some switch states resulting lower CMV rms value (e.g., while utilizing the zero voltage vector generated via utilizing the middle two switches of all phases), and the rate of change of the CMV is lower than the two-level VSI case resulting less CMC. Therefore CMV/CMC performance of the three-level VSI is better than that of the two-level VSI. However due to the control complexity and cost, three-level VSI is not utilized at low DC-bus voltage applications to reduce the CMV/CMC.

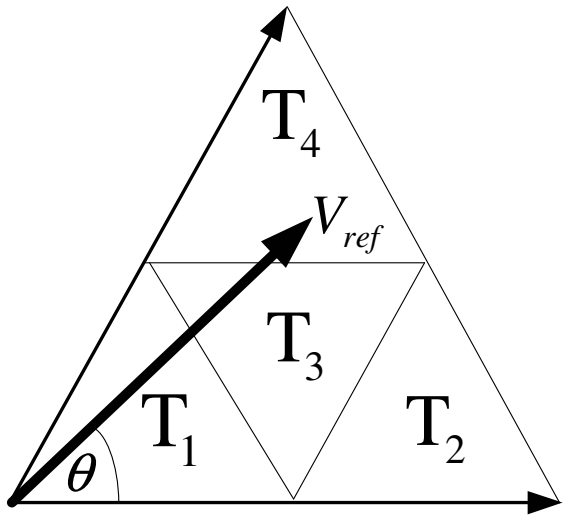


Figure 4.2 Triangular region definitions for sector A1.

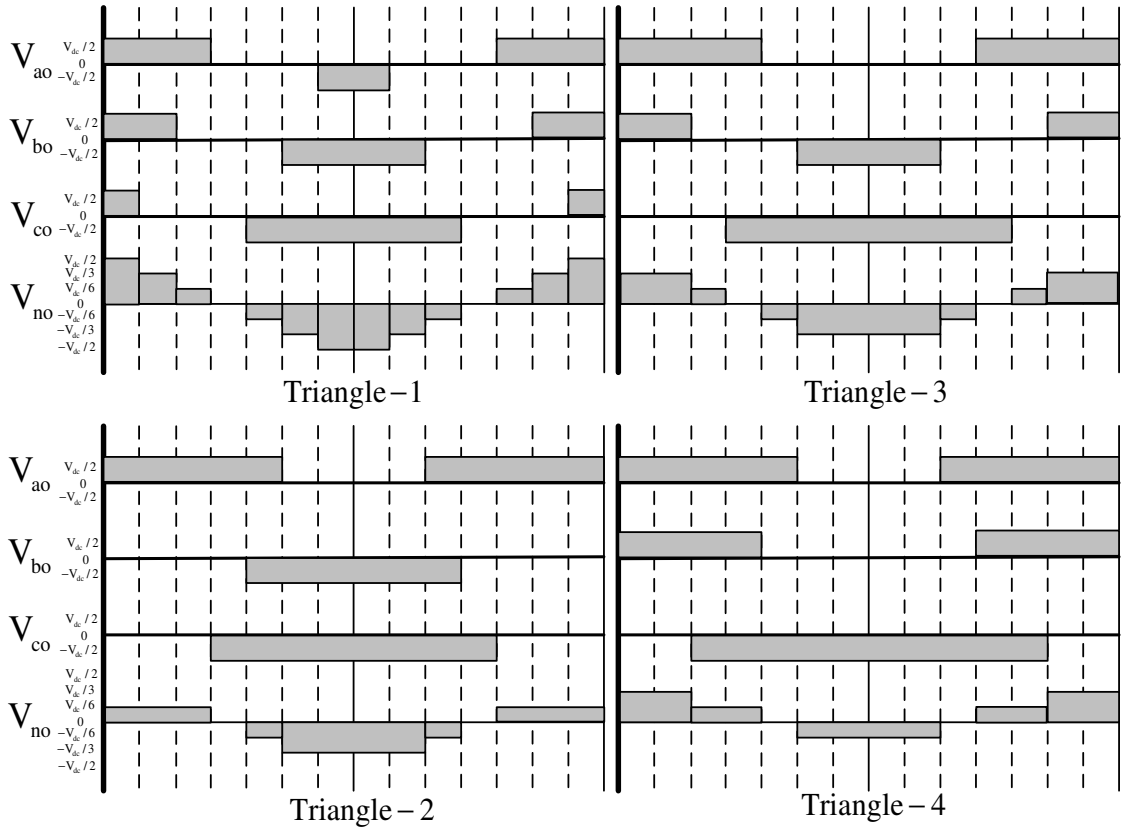


Figure 4.3 The NPC three-level inverter phase-to-midpoint output voltages and CMV pulse patterns for NTV-PWM.

4.3 Common Mode Current Generating Mechanisms and The Bearing Currents

In order to investigate the CMC generating mechanisms and the CMC paths, the common mode equivalent circuit of a three-phase induction motor should be studied. In order to model the high frequency behavior of the induction motor, including its stray components, significant amount of literature has been published [9], [10], [14], [28], [29], [30]. In Figure 4.4 the detailed common mode high frequency equivalent circuit of the VSI – cable- induction motor system is illustrated [9], [14]. As seen from the figure there are capacitive paths existing between the motor windings and the ground which are effective especially at high frequencies (higher than the carrier frequency and extending to the rise and fall rate of the current during switching which corresponds to MHz range). In the circuit the resistance of the cable and the

inductance of the motor windings can be neglected in the CM equivalent circuit. In Figure 4.5 the simplified common mode high frequency equivalent circuit of the VSI - cable - induction motor system is illustrated [28] such that the system is represented as an RLC resonant circuit where the capacitive current paths are represented as a single equivalent capacitance (C_{eq}) in which the CMC pass through.

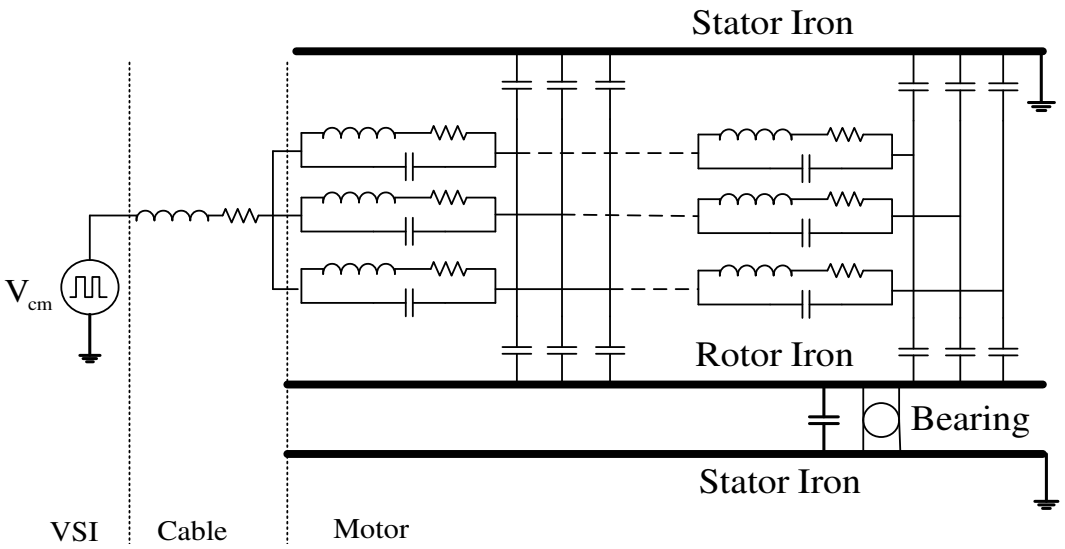


Figure 4.4 Detailed common mode high frequency equivalent circuit of a three-phase AC induction motor.

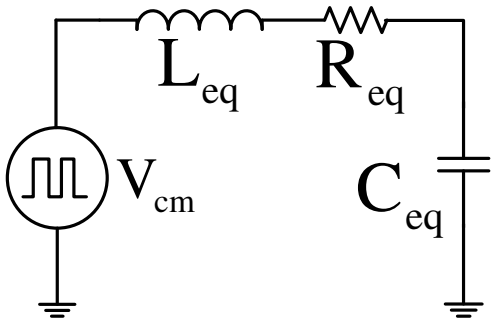


Figure 4.5 Simplified common mode high frequency equivalent circuit of three-phase AC induction motor drive system.

In Figure 4.6 the equivalent stray capacitances between the stator winding, rotor, and motor frame are illustrated separately [10]. Of these capacitances, C_{wf} which is the equivalent capacitance between motor windings and motor frame is significantly higher than other capacitances. Therefore the motor common mode equivalent capacitance (C_{eq}) can be assumed as equal to the C_{wf}. C_{wr} is the capacitance between the stator windings and rotor, C_{rf} is the capacitance between the rotor and motor frame (excluding bearing capacitance) and C_b is the bearing capacitance. Since there are two bearings in each motor C_b is multiplied by 2 in the equivalent model [10], [31].

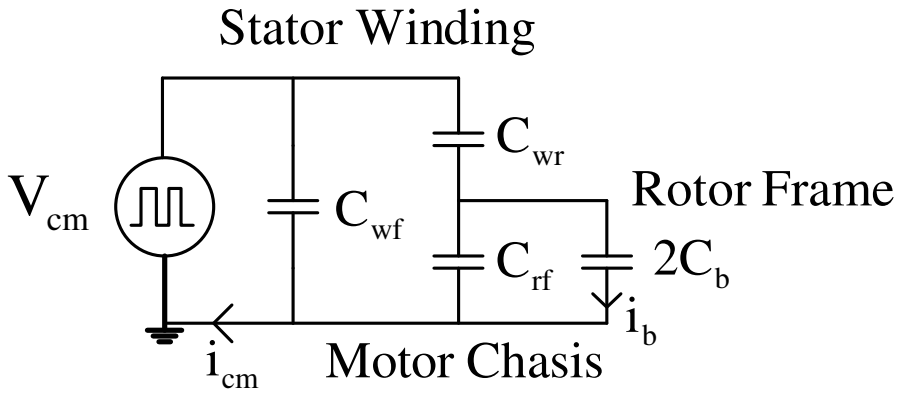


Figure 4.6 Equivalent capacitances between stator winding, rotor frame, and motor chassis.

In the above figure i_{cm} is the overall leakage current flowing from the motor frame to the ground (CMC) and i_b is the bearing current. In practice bearing currents compose a very little fraction of the overall leakage currents [10]; however they are very catastrophic since they result in bearing failures. Therefore, in this section bearing currents are investigated in detail.

There are various types of bearing currents according to their generating mechanism. [32]. The inverter-induced bearing currents are classified in Figure 4.7 according to their causes. The CMV results in capacitive bearing currents, Electric Discharge

Machine (EDM) bearing currents, and leakage currents. For the generation of EDM bearing currents, the magnitude of the CMV is effective while for the generation of capacitive bearing currents and leakage currents both the magnitude and dv/dt of the CMV are effective. The leakage ground currents result in rotor ground currents and High Frequency (HF) shaft voltage which is the source of the HF circulating bearing currents [32]. Of these types of bearing currents, the capacitive bearing currents are small in magnitude and harmless. The rotor ground currents may be harmful, but they occur only in operation where the rotor is grounded (via the mechanical load) [32]. Therefore, the EDM and the HF circulating bearing currents are most important and discussed in the following.

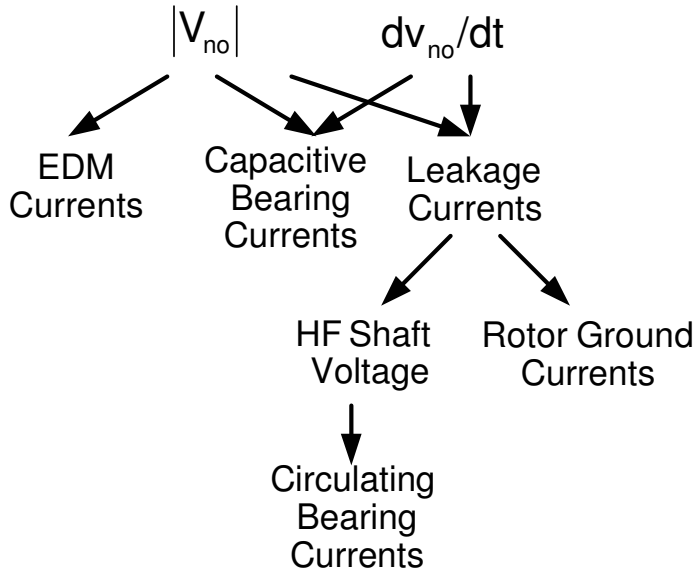


Figure 4.7 Cause-and-effect chains of inverter-induced bearing currents [32].

EDM bearing currents are result in due to the voltage built up over the bearing (bearing voltage or shaft voltage). The ratio of the bearing voltage to V_{cm} (Bearing Voltage Ratio (BVR)) is dependent on the motor common mode equivalent capacitance values and is defined in [10] as follows.

$$BVR = \frac{C_{wr}}{C_{wr} + C_{rf} + 2C_b} \tag{4.1}$$

In practice $C_{rf} >> C_{wr}$ therefore BVR is generally in the range of 2%-10% [10]. Since the grease film thickness is a fraction of μm, discharges frequently occur when the bearing build up voltage reaches several volts. When a discharge occurs, a sharp current pulse is generated and the bearing voltage suddenly collapses to zero [7]. During the breakdown instant a steep fall or rise is observed on the CMV waveform. The magnitude of the breakdown current is dependent on the bearing voltage before the discharge. In low quality bearings with rough surfaces, discharges commonly occur, however since discharges occur at relatively low built up bearing voltages, the magnitudes of the bearing current impulses are relatively lower [10]. Similarly EDM bearing currents are less significant at very low motor speed (< 100 rpm) operations since at low speed, metallic contact is occurred inside the bearing, preventing bearing voltage to build up [10]. The motor size dependency of the EDM bearing currents is low. Therefore on small size motors (few kW and below) the EDM bearing currents are high and effective with respect to the motor size. In the small size motors nearly all bearing currents are EDM type bearing currents since HF circulating bearing currents are effective only at very high power motors (100 kW and above) [10]. As the size of the motor increases, the contribution of the EDM bearing currents decreases.

Due to the leakage currents flowing from the motor windings to the ground, the currents which are measured at two opposite ends of a phase winding coil are not equal. These unbalanced currents result in a net flux inside the motor and HF circulating currents are induced due to the net flux [33]. These currents flow inside the motor and through the bearings and have negative effects on them. HF circulating bearing currents are dominant at low speed operations and especially at the large size motors [10].

As well as the magnitudes of the bearing currents, the densities (J_b) of the bearing currents are also important and they scale the danger of bearing failure [10]. As the

motor size increases the bearing currents also increase, however if the increment of the bearing current is less than the increment of the bearing surface; the bearing failures occur less likely. In small size motors (less than few kW) EDM type bearing currents are dominant and results in very high bearing currents with respect to the size of the motor (hence high current density (J_b)). In small size motors, as the motor size and power increase, the bearing currents also increase but the increment is very limited since the dependency of the EDM bearing currents to the motor size is low. Therefore J_b decreases with increasing motor size until the HF circulating bearing currents become dominant. Therefore in motors between 10kW and 100kW, J_b is relatively low since neither EDM nor HF circulating bearing currents are dominant [10]. Above 100kW HF circulating bearing currents are dominant and their magnitudes increase dramatically with motor size hence J_b increases [10].

4.4 Factors Affecting CMCs

The magnitudes of CMCs which are resulted by CMVs are dependent on many factors such as motor type, size, structure, and grounding. In large motors the equivalent capacitance between the phase windings and chassis is greater than those at the smaller motors. This results in larger CMC in larger motors [34]. Also the existence of a path for leakage currents is also effective on the flow of CMC. If the high frequency equivalent impedances of these paths are high, CMC is reduced. For example, in ceramic isolated bearings CMC is smaller. In some types of permanent magnet motors which have wider airgap CMC is less. For the same DC-bus voltage level, higher-level inverters result in less CMC on the motor. However low or high, CMC is always generated in every application where the modern drives are utilized, and they result in negative effects. Especially for VSI type drives applications where the DC bus voltage, switching speed and frequency are high; CMC can be catastrophic and must be suppressed for the system performance in many applications.

4.5 Common Mode Voltage and Current Mitigation Methods

CMV and CMC can be reduced by various methods. One of them is based on the principle of modifying the inverter topology and utilizing a three or more leveled voltage source inverter instead of utilizing a standard two-level inverter. However this approach increases the drive cost significantly and therefore it is not preferred except at the high power and voltage applications. Instead of this, passive and active CMV/CMC filtering methods are utilized in which filters are inserted between the inverter and the motor without changing the drive topology. In the passive filters only passive components and their combinations are utilized [9], [11], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45]. In active filters semiconductor switches are utilized as well as passive components [12], [46], [47], [48]. Another approach that reduces CMV/CMC is utilizing PWM rectifiers and arranging the pulse pattern of the PWM rectifier and inverter accordingly. CMV/CMC can also be reduced by modifying the PWM pulse pattern of the VSI. In this section various important mitigation methods will be studied in detail.

4.5.1 Common Mode Inductor (CMI)

The simplest passive filtering method involves adding a series common mode inductor (also known as common mode choke) between the inverter output and the motor (Figure 4.8) [9], [38], [43]. In a common mode inductor, windings of all three phases are wounded over a ferrite toroid core such that they generate a flux in the same direction. In Figure 4.9 a CMI is shown. Since the sum of the balanced three-phase currents is zero, normal mode currents (the motor currents identified by the motor fundamental equivalent circuit) do not result a net flux in the core and therefore the normal mode inductance of the CMI is very low (negligible), however common mode currents result a net flux and therefore the common mode inductance is very high and impedes against CMC. Although ferrite cores utilized in the typical applications loose their magnetic permeability (μ) at high frequencies, cores which are utilized in CMC inductors should maintain their permeability at high frequencies

(at the frequencies related with the switching frequency and its multiples corresponding to tens of kHz, and at the frequencies related with the semiconductor turn-on and turn-off speeds of MHz range) in order to suppress CMC effectively. Alternatively, recently magnetic cores made from nanocrystalline material have been developed which can operate at higher flux density and provide performance in smaller size than ferrites [43].

The main effect of the CMI on the system is acting as an additional inductor in the common mode equivalent circuit [9]. The inductance value of the common mode inductor is calculated in (4.2) where A_c and l_c are the cross sectional area and the circumferential length of the toroid core respectively and N is the number of turns at each phase [49].

$$L = \frac{N^2 \mu A_c}{l_c} \tag{4.2}$$

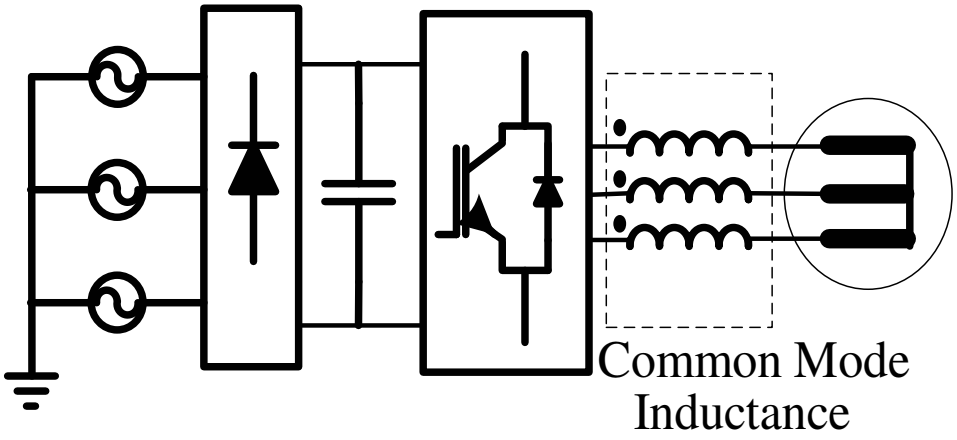


Figure 4.8 The utilization of CMI in a motor drive.

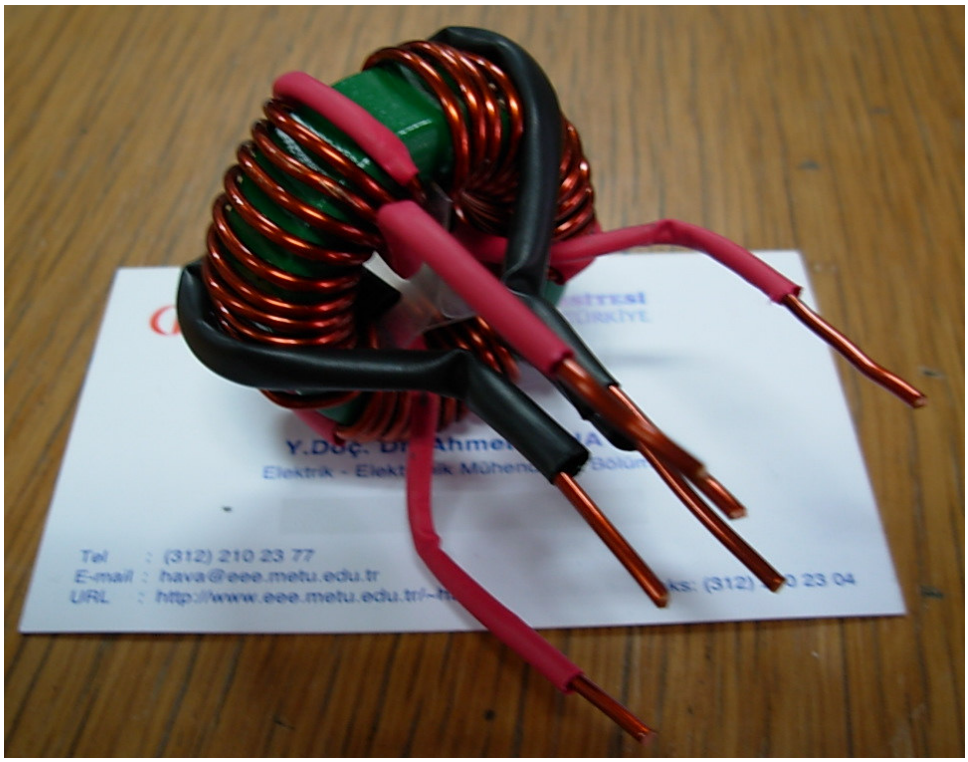


Figure 4.9 A three-phase CMI.

From the inductance formula it can be noticed that keeping the core size constant (hence keeping A_c and l_c constant) the inductance can be increased by increasing the turn number and/or utilizing a toroid with a higher μ. However the magnetic saturation of the toroid cores should also be considered in the design of the common mode inductors. The magnetic flux formula in a common mode inductor is given in (4.3) assuming the magnetic core is not saturated (B-H relation is linear).

$$B = \frac{LI_{cm}}{NA_c} \tag{4.3}$$

The ferrite toroids utilized in the common mode inductors reach magnetic saturation at approximately 0.4 T. If the core enters magnetic saturation (4.3) is no more valid since the B = μH linear relation is violated and the effective inductance of the CM inductor is less than its nominal value. Therefore, increasing the inductance value by only increasing N and μ while keeping the toroid size constant is not practical and

increasing the size of the toroid (hence the size of the common mode inductor) is unavoidable to achieve high inductance values for the performance of the common mode inductor.

Common mode inductors have very high impedance at frequencies related with the dv/dt of the semiconductor switches (typically MHz range). Therefore common mode inductors successfully suppress the high frequency peak notches on CMC. The common mode inductors are designed as typically with a few mH value and the equivalent common mode capacitances of motors at several kW power ratings are in the order of few nF. Therefore these components have a resonant frequency at tens of kHz and oscillatory common mode currents flow at the resonant frequency range when the common mode inductor is added. The peak value of the CMC when the CM inductor is added is several times less than the case when the CM inductor is not added. However due to the oscillation, CM inductors can not reduce the rms of the CMC significantly unless the toroid core is lossy.

The CM equivalence of a CM inductor is composed of an inductance parallel to a resistance. In CM inductors which are made of low loss toroid cores, the shunt resistance is very high and can be assumed open circuit. However in lossy toroids the shunt resistance is relatively lower and the series equivalent of the CM inductor is an inductance series to a resistance. Therefore lossy toroids increase the resistance as well as the inductance in the common mode equivalent circuit and help the oscillation to damp faster, resulting in less rms CMC. The ratio of the reduction of peak CMC is proportional with the square root of the increment on the series inductance of the common mode equivalent circuit after CM inductor is added. Similarly the ratio of the reduction of rms CMC is proportional with the square root of the increment on the series resistance of the common mode equivalent circuit after CM inductor is added [9].

In summary, CM inductors are bulky and poor at decreasing the CMV at the motor end and the rms of the CMC. However they are simple, cheap, and they successfully suppress the peak CMC which is very harmful for the motor bearings. Therefore

CMC inductances are widely utilized in the motor drives and various power electronic devices.

4.5.2 Common Mode Transformer (CMT)

Another passive mitigation method of reducing CMC is utilizing a common mode transformer (CMT) which is more effective compared to the CMI. Common mode transformers are connected between the inverter drive and the motor terminals (Figure 4.10) like the CMIs. The difference between the CMTs and the CMIs is consisting a secondary winding on the toroidal core which is terminated by a damping resistor (Figure 4.11) [9], [36], [40].

Similar to the common mode inductors, only CMC results a magnetic flux inside the toroid core and this flux induces voltage and current in the secondary winding. Due to the damping resistor, high frequency resonance magnitudes are suppressed and low rms CMC results.

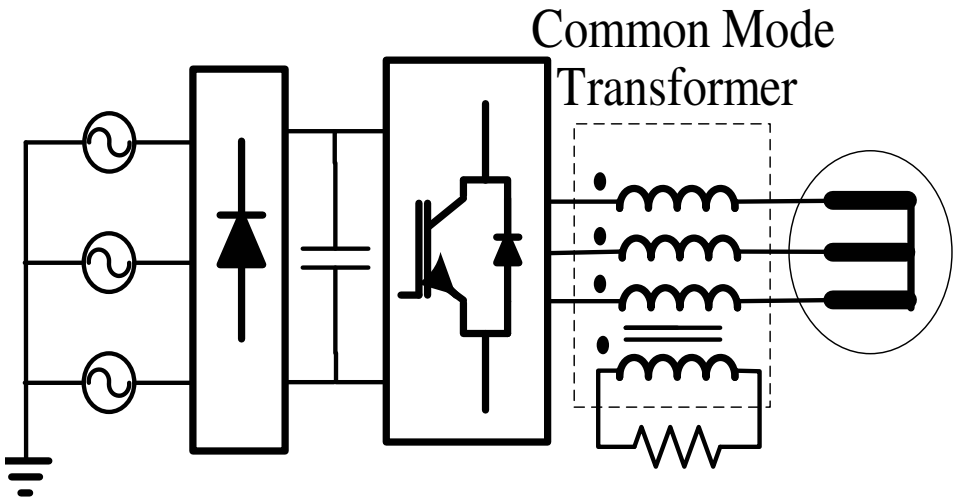


Figure 4.10 The utilization of a CMT in a motor drive.

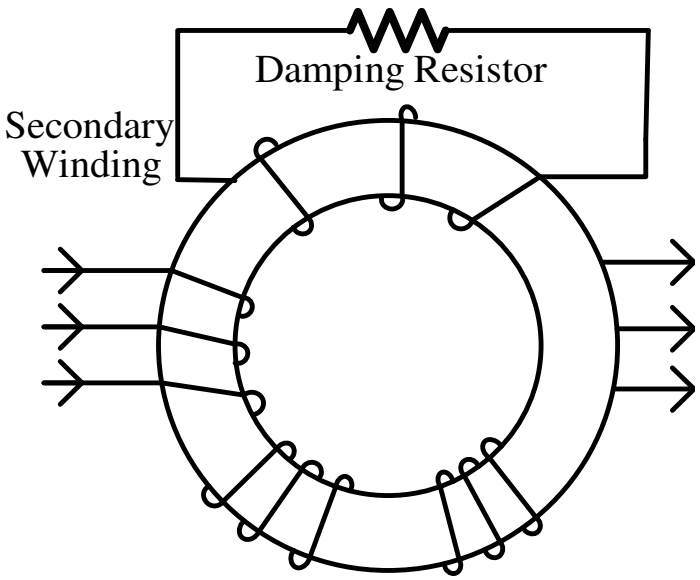
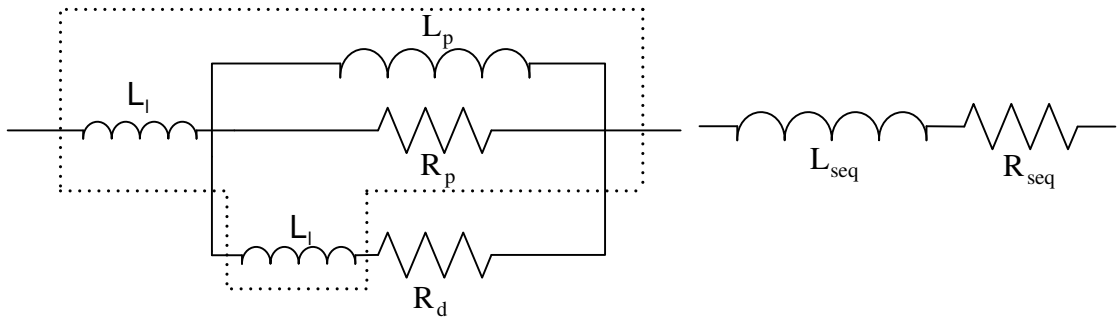


Figure 4.11 Common mode transformer.

The simplified equivalent circuit of a CMT is given in Figure 4.12. Here L_p and R_p are the parallel magnetizing inductance and the parallel core loss resistance of the magnetizing branch of the transformer, L_l is the leakage inductances which is practically low and may be neglected. R_d is the additional secondary damping resistor. When the secondary side is open circuited ($R_d = \infty$) equivalent circuit of the CMT is same as that of the CMI. The equivalent circuit of the CMT can also be modeled as a series RL circuit (Figure 4.12.b). The additional secondary damping resistor increases the shunt conductance of the parallel equivalent circuit and hence increases the resistance of the series RL equivalent of the CMT. The series equivalent resistor (R_{seq}) helps damping the oscillation on the CMC. Therefore by utilizing a CMT both the peak and rms values of CMC are reduced [9].



(a) (b)

Figure 4.12 Simplified common mode equivalent circuit of the CMT (a) parallel equivalent, (b) series equivalent.

Selection of the damping resistor is important in the design as the performance of the transformer degrades with the deviation of the parallel equivalent resistance (R_p // R_d) from the optimal value. Optimum parallel equivalent resistor (R_{peq}) should be calculated as (4.4) where C is the equivalent CM stray capacitance of the motor between the phase windings and the ground [9].

$$R_{peq} = \frac{1}{2}\sqrt{\frac{L_p}{C}} \tag{4.4}$$

If the core loss resistance of the transformer is neglected, the damping resistor R_d can be selected as R_{peq} as calculated in (4.4). However due to the existence of the core loss resistance, R_d should be selected slightly higher than R_{peq}.

For better performance, R_d should be increased. However in order not to violate the relation defined in (4.4) L_p should also be increased accordingly since the C is constant for each motor. Although there is no practical limitation for increasing R_d, there are practical limitations for increasing L_p such as size and cost. For a successful operation, CMT should also be designed such that the magnetic core shall not enter magnetic saturation. Therefore magnetic structure design is an important point in the CMT design, such that it's magnetizing inductance should be as high as possible

without entering saturation. The maximum magnetizing inductance should be designed for no magnetic saturation and is calculated in the following.

$$L_{max} = \frac{B_{max} N_{max} A_c}{I_{cm}} \tag{4.5}$$

For a selected magnetic core size, the toroid cross section (A) and the maximum number of turns (N_{max}) which are defined by the geometric limitations are constant. Similarly for a definite motor drive application, the peak I_{cm} can be estimated, and for all ferrite cores B_{max} is approximately 0.4 T. Therefore a CMT with magnetizing inductance higher that L_{max} can not be designed from a definite magnetic core size by increasing μ. However magnetic cores such as nanocyristaline cores with higher B_{max} value can be utilized to achieve higher L_{max} values by utilizing higher μ [43].

In CMIs where lossy toroids (with low equivalent core loss resistance) are utilized, coupling a secondary coil and adding a secondary damping resistor do not increase the filter performance significantly since the equivalent core loss resistor is already close to the optimal value of equivalent shunt resistor of the CMT. Further decreasing the resistance does not increase the performance. Therefore, coupling a secondary coil increases the performance especially at CMIs with low-loss toroid cores. With low loss toroid ferrite cores, with a proper design a CMT provides same CMC suppression by a smaller magnetic structure size (approximately 1/3 ratio) than a CM inductor [9].

In some applications where CMT are utilized, a damping resistor may not be connected to the secondary winding. Instead, a CMV compensating voltage may be applied from the secondary winding by utilizing passive components only, in order to resist the CMC flow within primary windings [41], [44].

4.5.3 RLC Type Passive CM Filter

Another approach of mitigating the CMC flow through the motor is providing a shortcut for the CMC to close its path through the inverter rather than the motor. For this purpose the RLC filtering circuit shown in Figure 4.13 can be utilized [11]. In the circuit, L, C and R components act as standard output filters and increase the quality of the voltage waveform at the output of the motor. In PWM based motor drive applications when no normal mode filter is utilized, the line-to-line voltages on the motor terminals have pulsating waveforms. By utilizing the normal mode filter components the line-to-line voltages on the motor terminals become sinusoidal [11]. Since the line-to-line voltages are free of sharp edges, relatively low CMC is generated at the motor side. The filter consists of a common mode inductance L_c that further reduces CMC. In this filtering topology, the common mode inductor is designed just same as described in the previous sections. Additionally the star point of the R-C network acts as a virtual star point of the motor since its potential is equal to the potential of the star point of the motor. R_c and C_c shorten the path of CMC and let CMC flow through the filter instead of the motor [11]. For the success of the method, C_c should be much larger than the common mode equivalent capacitance of the motor (approximately 100 times). By utilizing this filtering method the generated CMC is significantly reduced and since nearly all generated CMC flows through the filter, very little leakage current flows through the motor. Since both the CMV and CMC at the motor are eliminated, the motor bearings are protected by this method. Other than the defined topology there are many other variations of RLC type filters are developed [35], [37], [39], [42], [45] based on similar operating principles.

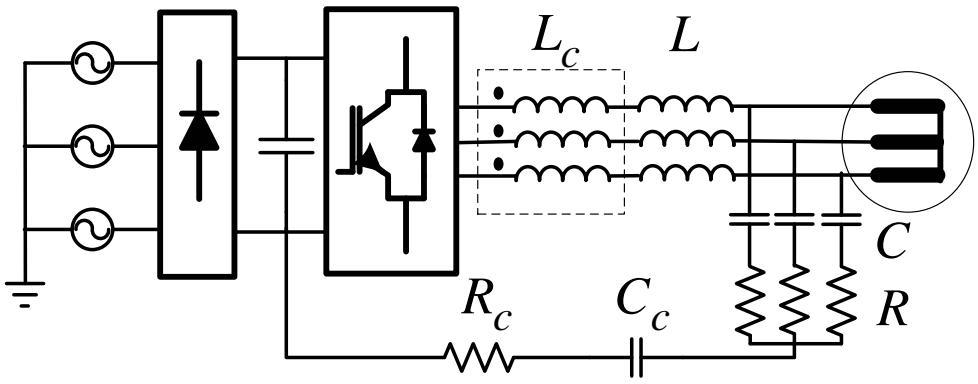


Figure 4.13 Utilization of RLC type passive CMC filter in a motor drive.

4.5.4 Active Common Mode Filter

Other than the passive filtering methods explained in the previous sections, in order to suppress the CMC active filters are also utilized which are consist of semiconductor switches as well as passive components [12], [46], [47], [48]. In Figure 4.14 the circuit topology of an active filtering method is illustrated. The filter is composed of a voltage detector with three capacitors, a common mode transformer and a push-pull emitter follower. The C_1 capacitors utilized in the voltage detector are small, and they indicate the information of CMV. If C_1 capacitors are selected too large they draw current from the system and if they are selected too small they can not map the CMV accurately [46]. The mapped voltage is applied to the CMT secondary winding after buffering by the emitter-follower.

The CMT utilized in this method is same as explained in previous sections, except an emitter follower is connected to the secondary winding of the CMT instead of a damping resistor. This active filter is developed with the same principle with the passive filters investigated in [41] and [44] such that, the inverse voltage of the inverter generated CMV is applied to the secondary winding of the CMT added between the inverter and the motor. The only difference is instead of passive components a push-pull emitter follower is utilized [12], [46], [47]. The magnitude of the applied voltage is equal to the voltage detected by the C_1 capacitors and

dependent on the switch states of Tr_1 and Tr_2. If the applied voltage to the secondary winding of the CMT is at the opposite polarity and at a similar magnitude with the CMV, then the effect of the CMV over the motor is reduced and therefore CMC is suppressed. For this purpose winding ratios of the transformer should be selected properly.

In this topology, the active filter acts as a controlled voltage source [12]. Since the current is drawn from the midpoint of the C_0 capacitors, the potential of this midpoint can fluctuate (may not be 0). In order to keep this fluctuation less than 1-2% C_0 capacitors should be selected large enough. In practice by utilizing this type of active filters CMV and CMC are reduced. However the method is problematic due to complexity and reliability. Similarly, the transistors Tr_1 and Tr_2 should be selected with sufficient voltage blocking capability. Therefore power transistors must be utilized in these filters which will increase the cost of the filter significantly.

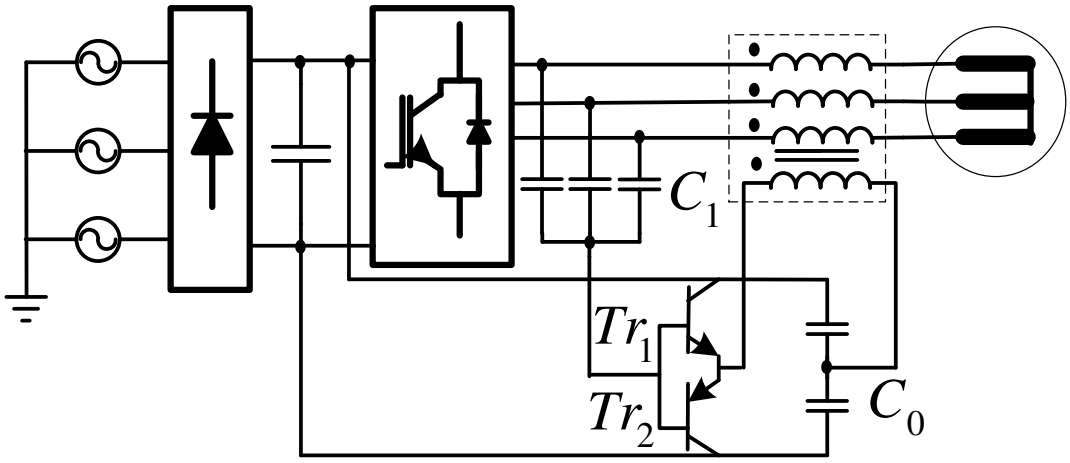


Figure 4.14 Motor drive diagram with active CMC filter.

4.5.5 Utilizing PWM Rectifier

Another approach of reducing CMV and its effects is utilizing a PWM rectifier instead of a standard diode rectifier as illustrated in Figure 4.15; and programming

the pulse pattern of the PWM rectifier and PWM inverter accordingly [50], [51], [52]. In a VSI fed by diode rectifiers, the V_{og} potential is small and has only low frequency components (Does not have rectangular pulsating waveform). Therefore only V_{no} determines the CMV. However when a PWM rectifier is utilized V_{og} potential also has pulsating waveform which is dependent on the rectifier switch states. Therefore V_{ng} potential which results CMC is dependent on both V_{no} and V_{og} ($V_{ng} = V_{no} + V_{og}$).

In order to reduce the CMV and CMC, the pulse patterns of the inverter and the rectifier are arranged such that V_{og} and V_{no} potentials have opposite polarity with magnitudes equal or close to each other [50]. In this circumstance the potential between the motor star point and the ground (V_{ng}) is $\pm V_{dc}/3$ or 0. Therefore both CMV and CMC are reduced. However the PWM rectifier is economical only at minority of the operations such as the regenerative load operations and at operations requiring high power quality. Therefore reducing CMV/CMC by utilizing PWM rectifier is not widely utilized. Also according to the operating point especially at low output voltage operations, CMV can be $\pm 2V_{dc}/3$ [50]. This is higher than $\pm V_{dc}/2$ which is the peak value of CMV when a diode rectifier is utilized. This high CMV is harmful for the motor and therefore this approach is not utilized alone and utilization of the additional filters is unavoidable.

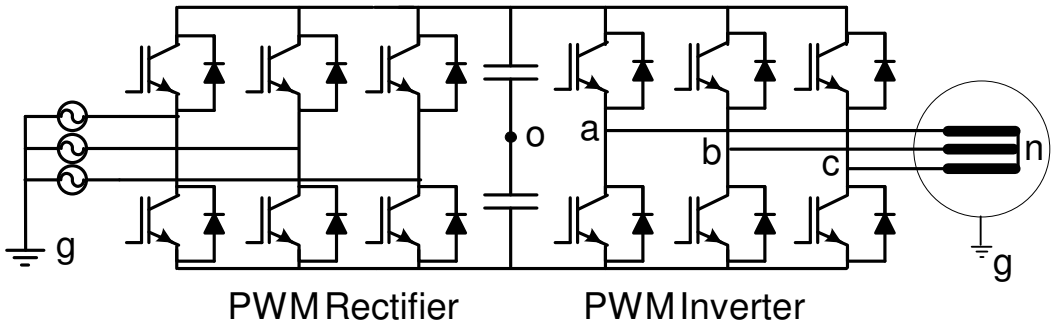


Figure 4.15 A motor drive with PWM rectifier and inverter.

4.6 CMV/CMC Reduction By Means of PWM Pulse Pattern Modification

In the Chapter 2, when investigating various PWM methods it was shown that all PWM methods have unique performance attributes. The PWM pulse patterns of these methods are different hence they have different CMV characteristics. In the traditional PWM methods (such as SVPWM and DPWM) the peak CMV is $V_{dc}/2$ while in the RCMV-PWM methods the peak CMV is limited to $V_{dc}/6$ which is much less than those of standard methods. The reduction of the CMV results in suppression of the CMC. However during the switching instants change of the CMV is $V_{dc}/3$ for all PWM methods in the two-level VSI. Therefore, by PWM pulse pattern modification, CMC can not be suppressed completely. The PWM pulse pattern modification can be applied by software modification only. Hence, the hardware remains the same resulting in no additional cost. If the PWM performance attributes of the RCMV-PWM methods (such as harmonic ripple performance) are satisfactory, these methods can be utilized in CMV/CMC reduction. Utilization of the RCMV-PWM methods together with additional filters provides supreme CMV/CMC reduction performance.

4.7 Summary

In this chapter, the CMC generation mechanisms are investigated and passive and active CMV/CMC mitigation methods are reviewed. It is concluded that the passive CMC mitigation methods reduce the CMC but they make the system bulky. Similarly the active CMC mitigation methods can be utilized to mitigate CMV/CMC but they are expensive and make the system complex. For achieving better performance, larger passive filters or more complex active methods need to be utilized.

In two-level inverter drives CMV/CMC can be reduced from the source and the requirement to the additional filters is decreased by selecting a proper PWM pulse pattern (utilizing RCMV-PWM methods). These PWM methods are preferred especially when the switching ripple, switching loss and voltage linearity region

performances of them are satisfactory. Utilizing RCMV-PWM methods has no additional cost and CMV/CMC reduction is achieved by means of software only. As explained in Chapter 2, CMV can be reduced from $V_{dc}/2$ to $V_{dc}/6$ in magnitude by utilizing the RCMV-PWM methods such as NSPWM. In RCMV-PWM methods CMV is reduced but its dv/dt is not changed ($\Delta V=V_{dc}/3$). Therefore suppression on the CMC is not as effective as the reduction on the CMV. Therefore utilizing only RCMV-PWM methods is not preferred in CMV/CMC mitigation. However utilizing RCMV-PWM methods do not have any cost and they reduce the requirement for additional filters. Therefore optimum performance is achieved when RCMV-PWM methods are utilized together with additional filters. Similarly by modifying PWM pulse patterns, CMV/CMC can be reduced in three or more leveled inverters just like in two-level inverter applications.

In the following chapter the laboratory experimental results will be provided. In the experiments PWM methods will be implemented and their CMV/CMC characteristics will be investigated with/without passive filters. Additionally the line-to-line voltage waveforms will be investigated at the motor terminals for PWM methods at long cable applications.

CHAPTER 5

EXPERIMENTAL WORK

5.1. Introduction

In this chapter, the CMV and CMC performances of the PWM methods discussed in the previous chapters are investigated by means of laboratory experiments. The effects of utilizing RCMV-PWM methods and the effects of passive common mode filters on the CMV and CMC performances are studied. Also the CMV/CMC characteristics of a commercial two-level inverter and a three-level inverter are investigated and the measurements are compared with each other and with the measurements of the prototype two-level VSI built in this thesis.

During the CMV/CMC experiments, an induction motor is operated at no-load at various speed levels. Since this thesis focuses on the steady-state CMV and CMC performances of the PWM-VSIs, the transient operations of the motor are ignored and only the steady-state performance attributes are investigated.

In addition to the CMV and CMC performances of the PWM methods, the line-to-line voltage waveforms of the PWM methods are investigated for long-cable applications where the motor and inverter are distant from each other. This study is necessary as some reduced CMV methods exhibit bipolar line-to-line voltage pulses and result in overvoltage problems (voltage reflection). Therefore, during the long-cable tests, voltage overshoots over the motor terminal line-to-line voltage waveforms are investigated. First the voltage reflection problem of AZSPWM1 is

shown, then a modification algorithm for AZSPWM1 is proposed to reduce the peak overshoots observed at the line-to-line voltage waveforms on the motor terminals.

Finally a combined algorithm of NSPWM and the modified form of AZSPWM1 is implemented such that NSPWM is utilized when the reference voltage is inside the voltage linearity region of NSPWM and the modified AZSPWM1 method is utilized when the reference voltage is in the under-modulation region of NSPWM.

5.2. Adjustable Speed Drive System Hardware

For the purpose of conducting the laboratory experiments, a two-level three-phase voltage source inverter to drive a three-phase 4-kW, 380-V, 4-pole, 1440-min^{-1} induction motor, was built at METU, Electrical and Electronics Engineering Department, in the Electrical Machines and Power Electronics Laboratory. The inverter was built in collaboration with Mr. Ömer Göksu, another MSc thesis student, who also utilizes this inverter hardware for his thesis research on motor speed control. The experimental system diagram is illustrated in Figure 5.1. The AC line voltage is fed to the drive through a three-phase variable transformer in order to control the DC-link voltage of the inverter and also avoid inrush currents (there is no pre-charge circuit in the drive). After the variable transformer, a Y/Y connected isolation transformer is utilized to galvanically isolate the drive system from the AC grid. Between the isolation transformer and the rectifier a three-phase circuit breaker is connected for system protection. This circuit-breaker also allows interrupting the input voltage of the rectifier manually. In the experimental set-up, the three-phase AC input voltage is rectified by a Semikron SKD30/12 diode bridge rectifier which has a voltage rating of 1200 V and a current rating of 30 A. Between the rectifier and the DC link, a 20 A semiconductor fuse is inserted for system protection. The rectified DC voltage is filtered via two series connected 2200 μF electrolytic capacitors, with 450 V voltage rating. In order to discharge the DC-link capacitors when system is shut down, and also to provide voltage balancing among the series

connected capacitors, a 30 kΩ discharging resistor with 10W power ratings is connected in parallel to each capacitor.

The VSI is built from three Semikron SKM75GB123D dual-pack IGBT modules. The voltage and the current ratings of the IGBT modules are 1200 V and 75 A respectively. The current rating is selected far higher then the rated current of the system and the motor, in order to minimize the risk of burn out of the IGBT switches. Semikron Skyper 32 Pro gate-drive modules are utilized to drive the IGBT switches. These gate drive modules have internal overcurrent protection such that they generate a fault signal when the collector-emitter voltage (V_{CE}) of the IGBT is too high in conduction state (In IGBT switches when a high current is flowing, the V_{CE} of the corresponding switch rises, so called the desaturation or desat condition). Another feature of these gate drives is the insertion of a dead-time of 3.3 μs. The gate resistor value is 22 Ω which corresponds to approximate rise and fall times of 200 ns (Figure 1.3). In order to measure the output phase currents for an additional overcurrent protection and for the determination of the load current polarity for the dead-time compensation, LEM LA25 P/SP1 current transducers are utilized. In the experimental set-up, for the control of the overall system and for the generation of the required PWM pulse patterns, the eZdsp F2808 starter kit is utilized which includes a Texas Instruments TMS320F2808 fixed-point DSP and peripheral units such as A/D converters [53].

Between the DSP and the gate drives, a signal conditioning card is connected for overcurrent protection and level shifting of DSP logic signals. The card disables (turns off) the system by applying “0” logic to all top and bottom switches of the inverter legs when an error signal occurs. The error signal may occur either at the overcurrent protection board or at the gate drives. Input signals of gate drives require logic signals of 0V as low and +15V as high signal. For this purpose this card converts 0/+3.3 V digital logic signals of the DSP to 0/+15V in order to make the signals compatible with the gate drive.

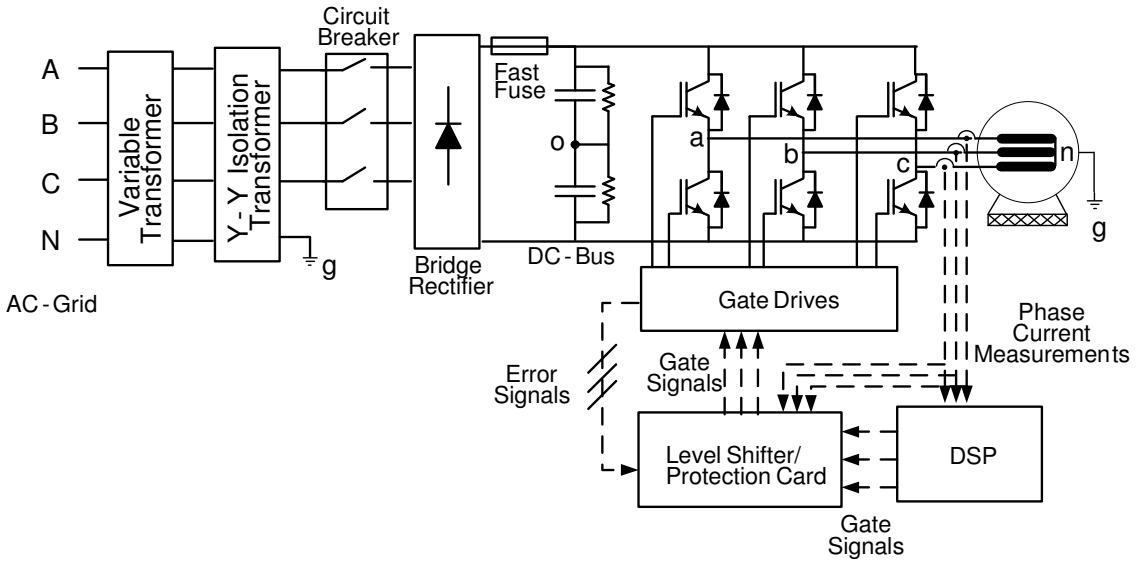


Figure 5.1 Experimental inverter drive system hardware and the control diagram.

For the measurement of the leakage current, the experimental set-up illustrated in Figure 5.2 is constructed. The induction motor is placed on an insulating plate. Between the AC line and the diode rectifier an isolation transformer is connected to isolate the system from the AC line. The star point of the primary side of the isolation transformer is connected to the neutral of the AC line and the star point of the secondary side of the isolation transformer is connected to the frame (chassis) of the induction motor. The induction motor frame, the isolation transformer, etc. are all electrically floating with respect to the transformer primary star point (true earth/ground) via the laboratory wooden floors isolation. The motor is placed on an additional wooden frame to insure galvanic isolation from the ground. The motor chassis and the isolation transformer secondary winding star point are connected via a copper wire to form the motor leakage current circulation path. The leakage current from the motor star point to the transformer secondary star point is measured through this wire by a high bandwidth current transducer and is considered as the CMC. In Figure 5.3 the photograph of the constructed experimental set-up is illustrated. The common mode voltage is also measured between the stator star point and the inverter DC bus center point (common connection point of the two DC bus capacitors). The common mode voltage is measured via a high bandwidth differential voltage probe.

During the long cable tests a 70 m cable is inserted between the drive and the motor and the line-to-line voltage is measured at the motor terminals via a high voltage differential voltage probe.

During the experiments, measurements are conducted with a 500 MHz, 4-channel oscilloscope, LeCroy Waverunner 6050A. The current measurements including phase current and CMC are conducted with LeCroy CP150, 150 A, 10 MHz current transducer, the CMV measurements are conducted with LeCroy ADP305, 1000 V, 25 MHz differential voltage probe. During the long cable tests for the measurement of the line-to-line voltage waveforms Pintek DP-100, 6500 V 100 MHz differential voltage probe is utilized.

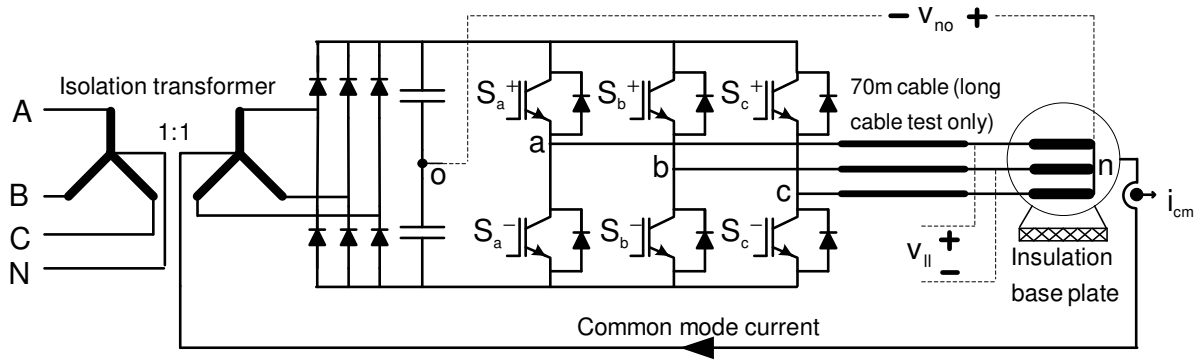


Figure 5.2 The CMV/CMC measurement set-up in the three-phase induction motor drive system.

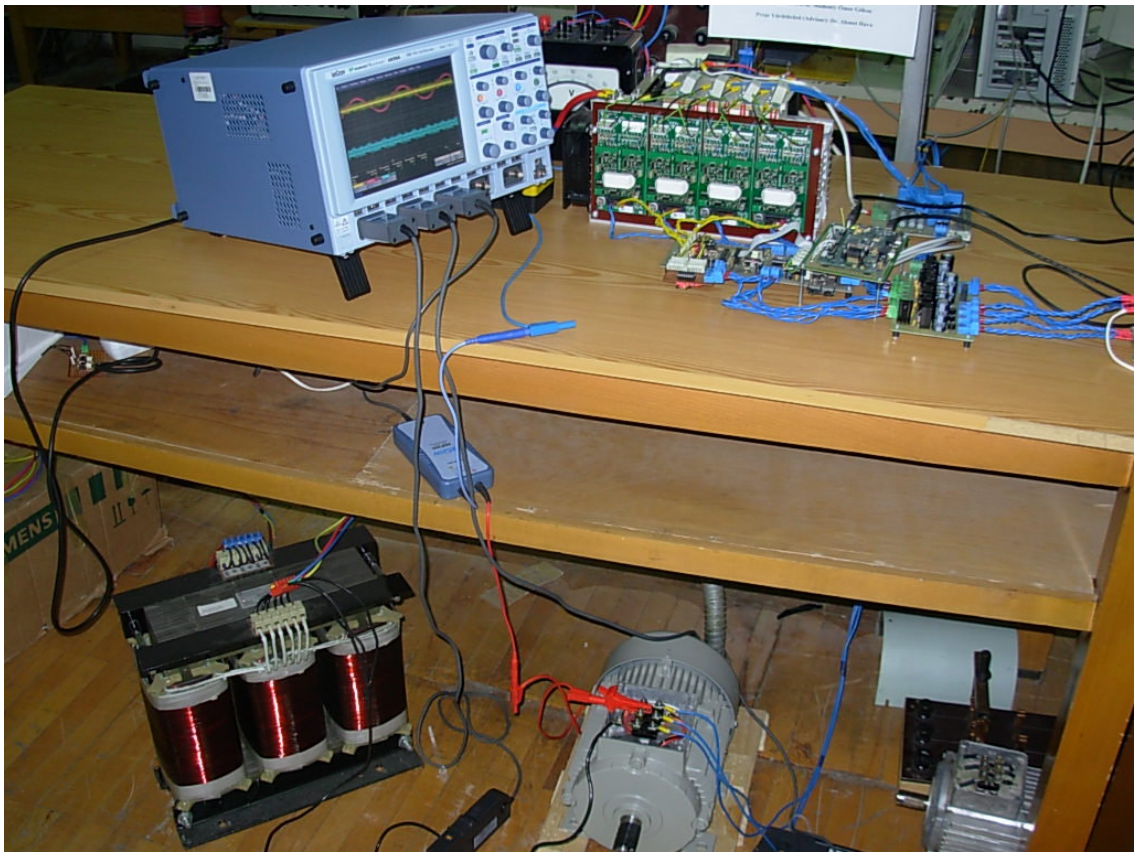


Figure 5.3 Laboratory experimental set-up.

5.3. PWM Signal Generation

In the experimental set-up the PWM signals are generated by the PWM unit of the Texas Instruments TMS320F2808 fixed-point DSP chip [54] which has a on chip digital hardware PWM module with flexible programmability. During this process instead of the direct voltage vector PWM implementation, the scalar PWM implementation approach which was explained in Chapter 2.2 is utilized such that the PWM pulses are generated by comparing a reference signal with a triangular carrier signal. The PWM signals are generated by the enhanced PWM (EPWM) unit of the DSP [54]. The EPWM unit includes an internal counter which corresponds to the triangular carrier signal for comparison with the reference. The carrier signal counts up and down; and when the carrier signal reaches zero (underflow) or the full value (period) an interrupt is given. When the interrupt is given, the duty cycles of the phase switch signals are calculated. The analog phase current measurements by the

LEM LA25 P/SP1 current transducers are converted to digital signals by the A/D converter of the eZdsp F2808 starter kit. With the phase current measurements the polarity information of the phase currents are obtained and these polarity informations are considered in the compensation of the effects of the dead-time. According to the polarities of the phase currents the calculated duty cycles of the phase switch signals are modified. After the calculation of the duty signals of the phase switch signals, the comparator registers of the EPWM are set accordingly to give the defined pulse pattern of the selected PWM method.

The EPWM unit has two different comparator registers (COMPA and COMPB) per phase. In this application the switching rule is defined as the PWM signal of the upper switch of an inverter phase is at logic level "1" when the counter value is between the loaded values of COMPA and COMPB comparator registers (Figure 5.4). The COMPA has always a greater value than the COMPB and the differences between these comparator registers define the duty cycle of the corresponding phase. For the above defined switching rule, during the rising edge of the triangular counter, the upper switch of an inverter phase turns on when "Counter = COMPB" and turns off when "Counter = COMPA"; similarly during the falling edge of the triangular counter, the upper switch of an inverter phase turns-on when "Counter = COMPA" and turns-off when "Counter = COMPB". The lower switches of each phase operate at the complementary manner with the upper switch. For each inverter phase there are different comparator registers. The above defined switching rule is valid for all PWM methods but for SVPWM and DPWM1, COMPB is always set to zero, therefore during implementation of these methods only COMPA decides the turn-on and turn-off instants of the switches. However, in order to generate the PWM pulse pattern of NSPWM and AZSPWM1, both of the comparator registers (COMPA and COMPB) are required (Figure 5.4).

For example to generate the required pulse pattern of NSPWM defined in Figure 2.18 for region B1, the duty cycles of the phase switch signals (d_a,d_b,d_c) are calculated. The comparator registers (COMPA and COMPB) of each phase are set

such that; for phase-a COMPA= d_a, COMPB = 0; for phase-b COMPA= 1, COMPB = 1-d_b; for phase-c COMPA= 0, COMPB = 0.

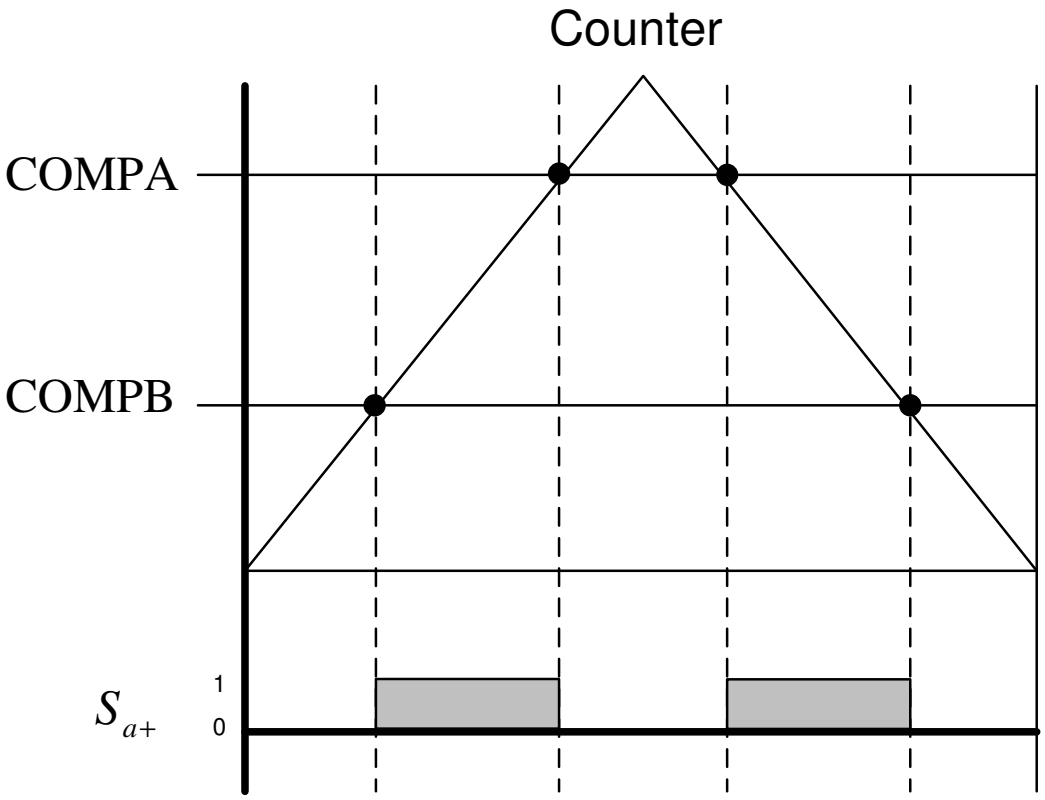


Figure 5.4 Generation of the PWM pulses by the PWM unit of the TMS320F2808 DSP utilizing the EPWM unit with two comparator registers COMPA and COMPB.

5.4 CMV/CMC Experimental Results without Passive Filters

To investigate the effects of utilizing different PWM methods on CMV and CMC, laboratory experiments are conducted. The induction motor is directly connected to the VSI output terminals via a short cable (less than 2m) and no filter is inserted between the motor and the VSI. The inverter is operated in the constant V/f mode (176.7V_{rms}/50Hz) and the induction motor is operated at no-load. With this constant V/f ratio, the motor is underfluxed implying no magnetic saturation for the given operating conditions. Common mode current and voltage characteristics of four different PWM methods DPWM1, NSPWM, SVPWM, and AZSPWM1 are

investigated. SVPWM and AZSPWM1 are tested at 6.66 kHz and DPWM1 and NSPWM are tested at 10 kHz switching frequencies, yielding equal number of average switchings per fundamental cycle. DC bus is fixed at 500 V by means of the variable transformer.

Operations at M_i=0.8 and M_i=0.61 are considered. During the selection of these operating points, the voltage linearity ranges of the PWM methods are taken into consideration. Although the theoretical upper voltage linearity ranges of the selected PWM methods correspond to M_i=0.907, in practice due to the existence of dead-time the voltage linearity ranges of PWM methods (especially of continuous PWM methods) expire at a lower M_i [16]. Here, the SVPWM and AZSPWM1 for the given carrier frequency of 6.6 kHz and deadtime of 3.3 μs begin to loose linearity at approximately 0.8 modulation index. Therefore, this method places the constraint for the maximum M_i range and M_i=0.8 is selected for high M_i operation where all tested PWM methods remain linear. As low M_i operation M_i=0.61 is selected which corresponds to the lower voltage linearity range of NSPWM.

In the experiments, the modulation signals of the considered PWM methods could be observed at the oscilloscope screen. The PMA2 software of LeCroy Waverunner 6050A oscilloscope calculates and plots the time distances between the PWM logic signals of the DSP or output voltages and as this corresponds to the switch duty cycles that are proportional to the modulation signals with a scale factor. Thus, the oscillograms include modulation signals identifying the method employed in the drive.

5.4.1 CMV/CMC Experimental Results without Passive Filters at M_i=0.8

During these experiments the VSI output voltage is set to be 180.3 V_{rms}/51 Hz and the results are recorded at steady-state. Experimental results of phase current, CMC, CMV, and the modulation signal for DPWM1, NSPWM, SVPWM, and AZSPWM1 are illustrated at Figures 5.5, 5.6, 5.7, and 5.8 respectively.

The phase current waveforms are sinusoidal and the PWM current ripple is low and comparable in all the methods as predicted in the simulations. The CMV comparison indicates that both DPWM1 and SVPWM have high CMV compared to others. NSPWM and AZSPWM1 have similar CMV values. During the experiments peak CMV measurements are approximately 450 V for conventional PWM methods and approximately 200 V for RCMV-PWM methods. These values are higher than the theoretically expected CMV values which are 250 V ($V_{dc}/2$) for conventional PWM methods and 83 V ($V_{dc}/6$) for RCMV-PWM methods. The reason of this mismatch is the non-zero CMC flowing in the laboratory experiments. Note that in (1.1) the CMV formula assumes that the motor stator winding star point is insulated from the ground and no current flows. Hence $i_{cm} = i_a + i_b + i_c = 0$. However, in practice the motor-inverter based system model involves parasitic components and as the CMC flows through the motor through the parasitic component impedances the CMV becomes higher than the theoretically expected value under zero leakage current condition. This voltage rise is due to the LC resonance of the parasitic components increasing the CMV higher than the open circuit case.

Comparing the CMC characteristics, the differences are not as emphasized as the CMV characteristic, because dv/dt is the same regardless the PWM method (800 V/μs for the laboratory inverter as illustrated in Figure 1.3). The switching instants result in sharp edge voltage pulses that cause high frequency currents flowing through the capacitive paths and these current pulses have high magnitude in all methods. However, differences are still notable in terms of rms and peak CMC values and the CMC values of SVPWM and DPWM1 are higher than those of NSPWM and AZSPWM1. The CMC peak and RMS measurements will be provided later in the comparative results section.

Figures 5.9, 5.10, 5.11, and 5.12 illustrate the microscopic (over the PWM cycles) view of the CMV/CMC waveforms. Since the PWM pulse pattern varies over a fundamental cycle, the PWM characteristics are θ dependent. As a result, the CMV/CMC characteristics also vary in space. When comparing the CMV/CMC

characteristics, the worst CMV/CMC points are selected for each method and shown in these oscillograms. It can be seen that the CMV values of DPWM1 and SVPWM are quite larger than those of NSPWM and AZSPWM1. The CMV waveforms are not rectangular but involve oscillations. Because of the existence of the parasitic components and the CMC discussed above the CMV deviates from the rectangular shape. The microscopic CMV's of NSPWM and AZSPWM1 are almost identical. These similarities are explained by Table 2.6. Both methods have peak CMV of $V_{dc}/6$. The CMV of NSPWM changes 4 times and that of AZSPWM1 changes 6 times over their carrier cycles. However NSPWM is operated at 10 kHz switching frequency and AZSPWM1 is operated at 6.6 kHz switching frequency resulting in same number of CMV changes over a constant time period. Similarly the fundamental frequency of the CMVs of NSPWM and AZSPWM1 are equal in this example such that both of them are equal to 20 kHz (2x10kHz for NSPWM and 3x6.6kHz for AZSPWM1). Due to these similarities the CMV waveforms of NSPWM and AZSPWM1 are almost identical. The microscopic CMC's of the discussed methods also indicate that NSPWM and AZSPWM1 are better. The CMC waveforms consist of low frequency oscillations and sharp spikes. While the low frequency oscillations are due to the CMV magnitude, the spikes are mainly due to the high dv/dt during switching. While in NSPWM and AZSPWM1 the CMC's have smaller magnitude oscillations, SVPWM and DPWM1 exhibit CMC's with larger magnitude oscillations. Also the spikes of NSPWM and AZSPWM1 are smaller in magnitude than those of the SVPWM and DPWM1 methods.

In summary, for the considered operating point, the RCMV-PWM methods and in particular NSPWM significantly reduce the CMV and partially reduce the CMC. The peak value of CMC is more noticeably reduced than its RMS value.

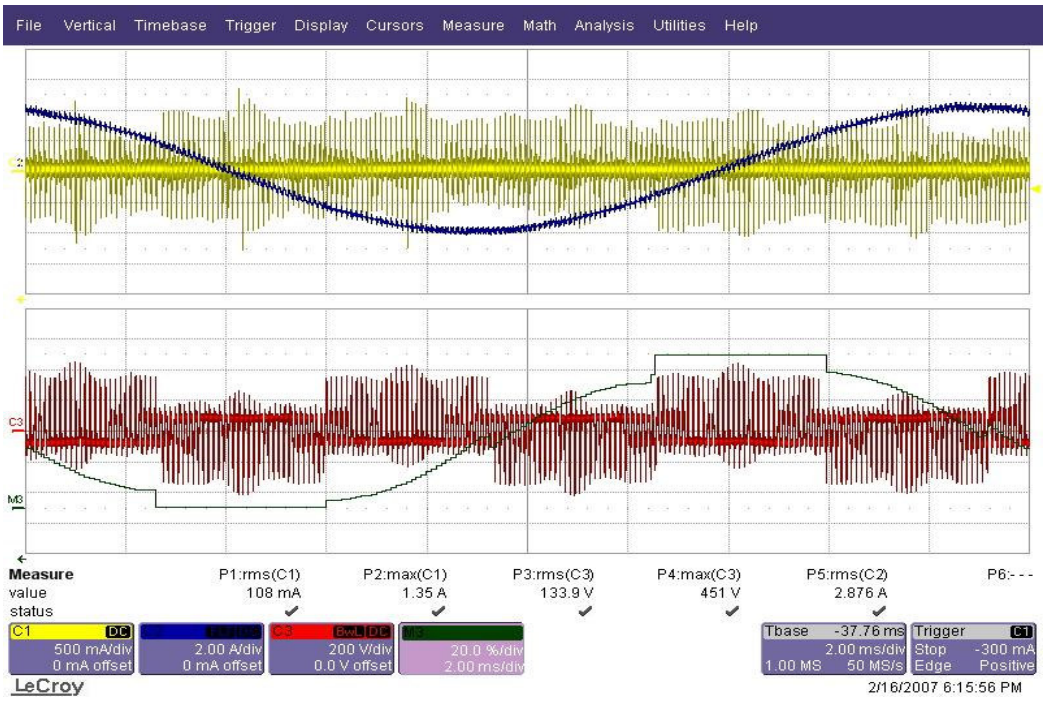


Figure 5.5 Phase current (blue), CMC (yellow), CMV (red), and modulation signal (green) waveforms for DPWM1 (M_i=0.8 and f_s=10 kHz).

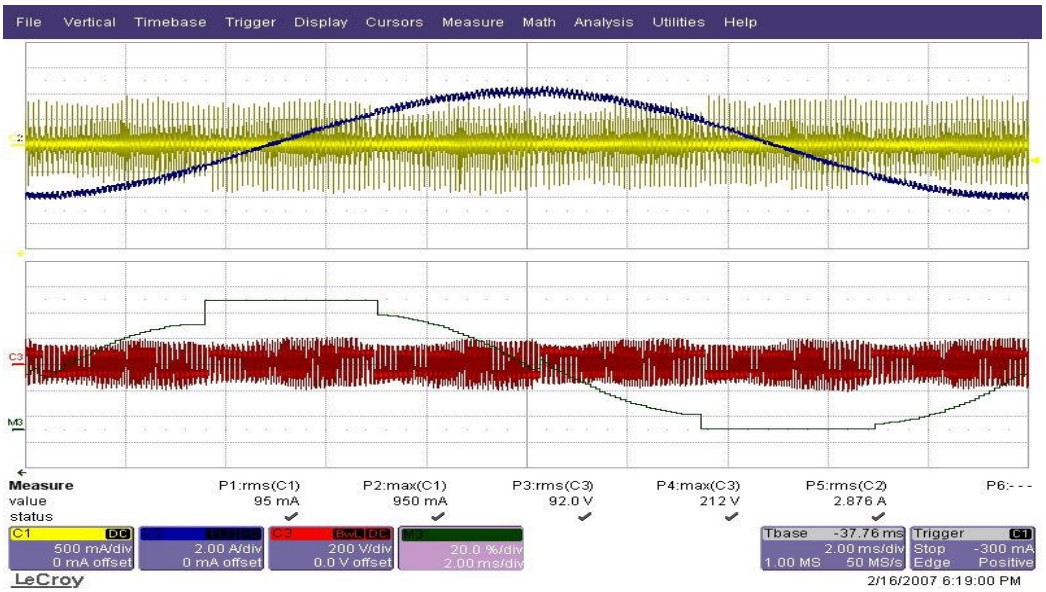


Figure 5.6 Phase current (blue), CMC (yellow), CMV (red), and modulation signal (green) waveforms for NSPWM (M_i=0.8 and f_s=10 kHz).

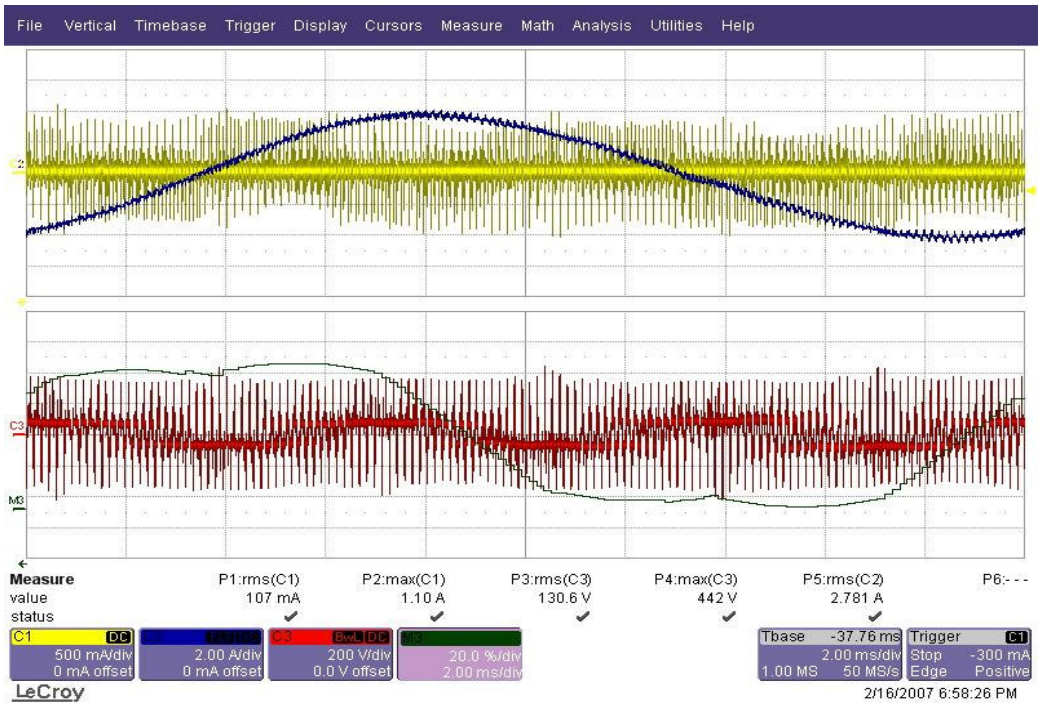


Figure 5.7 Phase current (blue), CMC (yellow), CMV (red), and modulation signal (green) waveforms for SVPWM(M_i=0.8 and f_s=6.6 kHz).

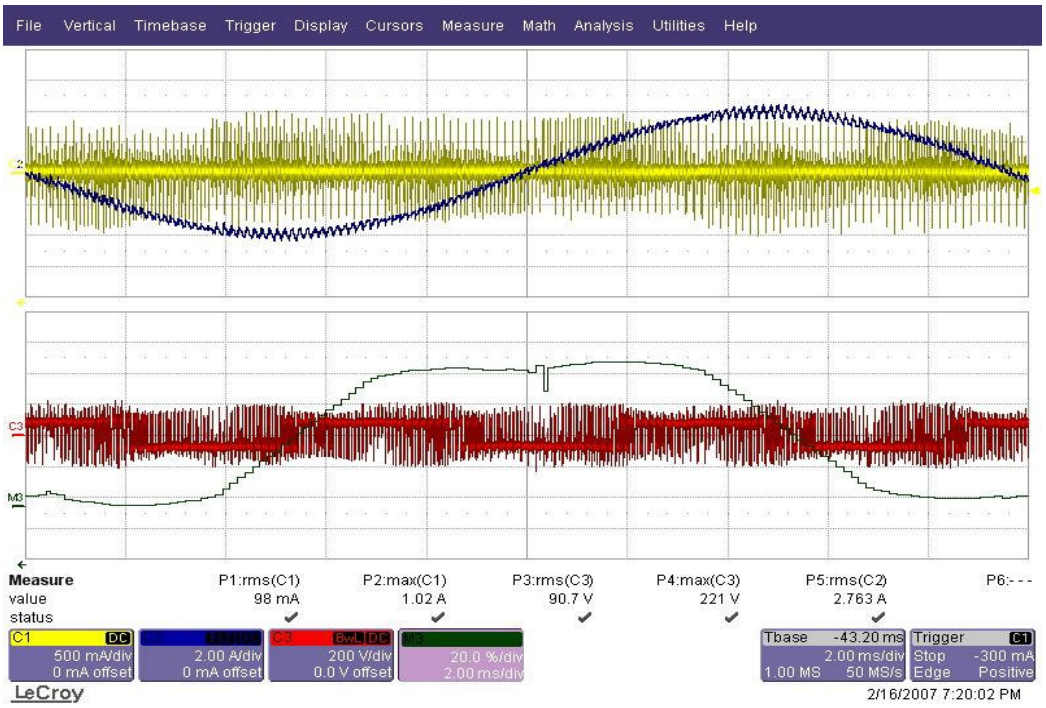


Figure 5.8 Phase current (blue), CMC (yellow), CMV (red), and modulation signal (green) waveforms for AZSPWM1(M_i=0.8 and f_s=6.6 kHz).

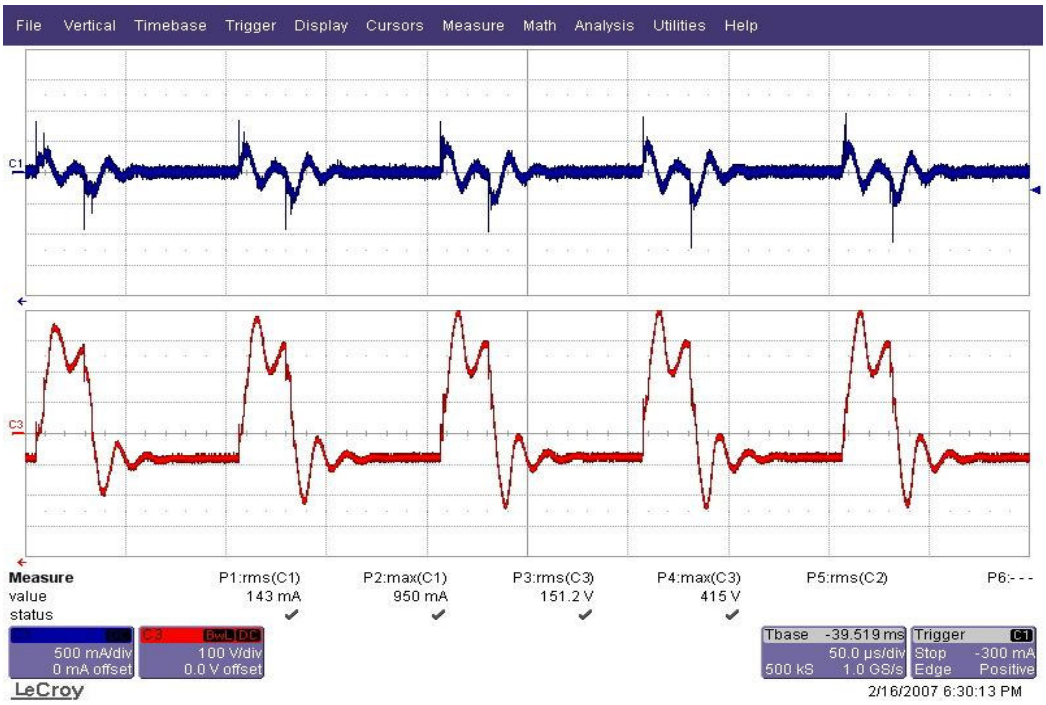


Figure 5.9 DPWM1 zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8.

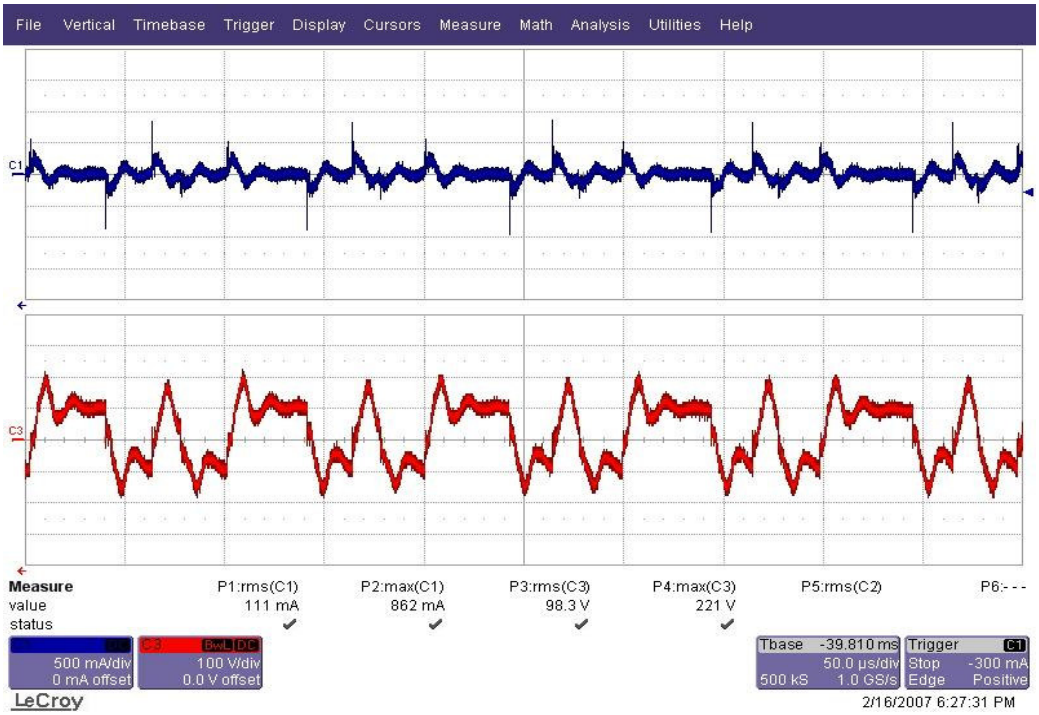


Figure 5.10 NSPWM zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8.

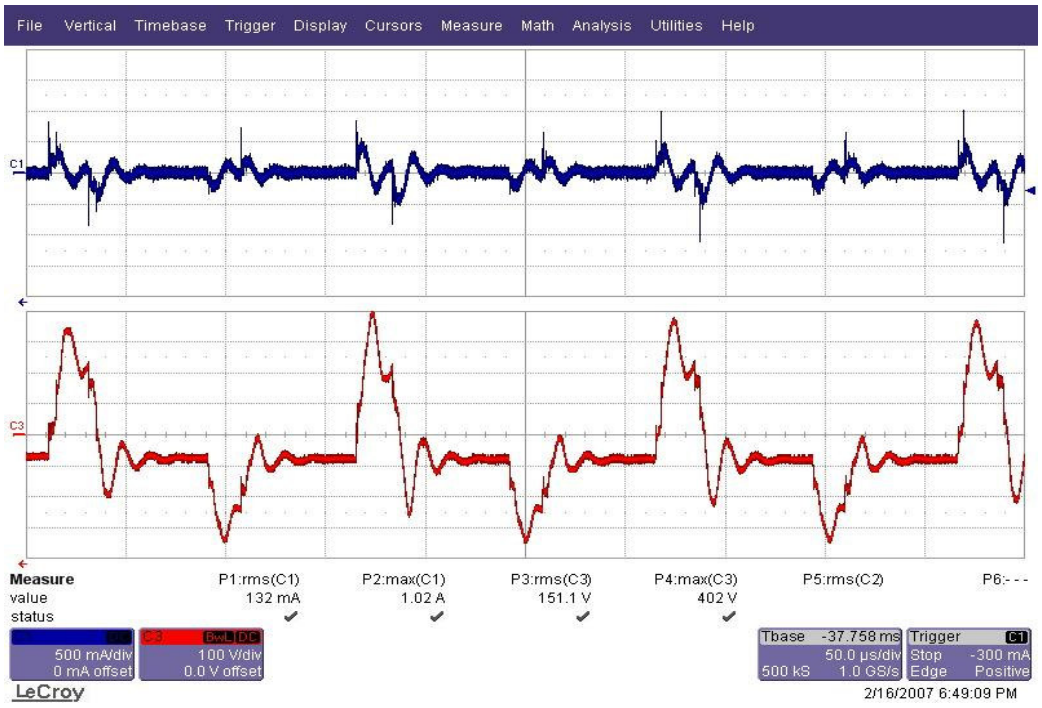


Figure 5.11 SVPWM zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8.

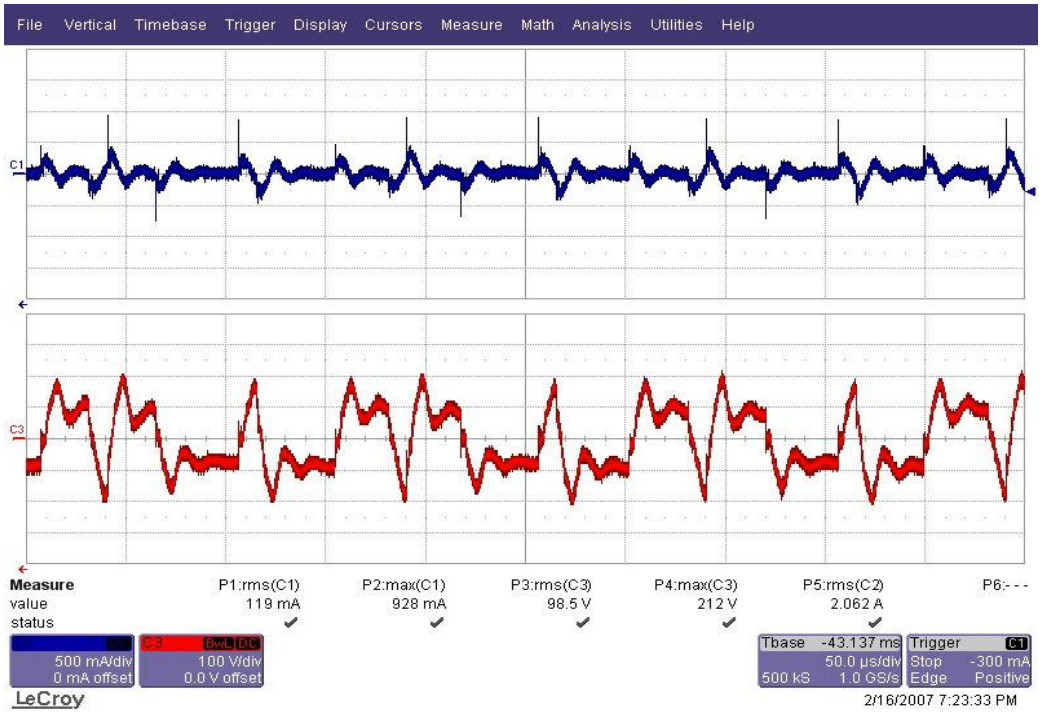


Figure 5.12 AZSPWM1 zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8.

5.4.2 CMV/CMC Experimental Results without Passive Filters at M_i=0.61

In this section the experimental results obtained at M_i=0.61 which correspond to output voltage of 137.6 V_{rms}/38.8 Hz are provided. The experimental results of phase current, CMC, and CMV for DPWM1, NSPWM, SVPWM, and AZSPWM1 are illustrated in Figures 5.13, 5.14, 5.15, and 5.16 respectively.

The phase current waveforms are sinusoidal but the PWM current ripple is not same for all the methods unlike the high modulation index case. The current ripples of NSPWM and AZSPWM1 are noticeably higher. The CMV performances of the PWM methods are similar to their performance at M_i=0.8 but the CMV rms values of DPWM1 and SVPWM slightly increase with decreasing M_i since the duty cycles of the zero-voltage vectors increase. Therefore the difference between the CMVs of the RCMV-PWM methods and those of the standard PWM methods become more significant. Also the CMC performances of the PWM methods are similar to their performance at high M_i and CMCs of the RCMV-PWM methods are slightly less than those of the standard PWM methods. However, the differences are still notable in terms of peak CMC values.

Figures 5.17, 5.18, 5.19, and 5.20 illustrate the microscopic view of the CMV/CMC waveforms. The microscopic views at the worst CMV/CMC points reveal that the magnitude and shape of the CMV and CMC are also not affected significantly with the modulation index variation. It can be seen that the CMVs of DPWM1 and SVPWM are quite larger than those of NSPWM and AZSPWM1. NSPWM and AZSPWM1 have nearly the same CMV. Similarly the CMC waveforms of PWM methods are similar to waveforms obtained at high M_i. The magnitudes of the CMC current spikes and the magnitudes of the oscillations of the CMC are slightly smaller at NSPWM and AZSPWM1 compared to SVPWM and DPWM1.

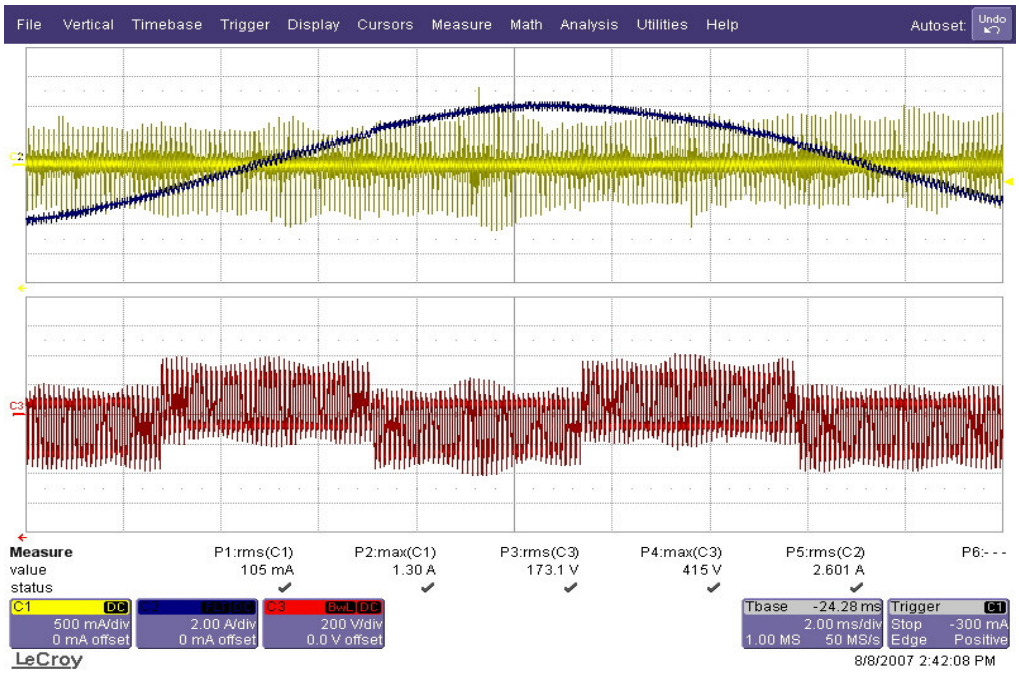


Figure 5.13 Phase current (blue), CMC (yellow), and CMV (red) waveforms for DPWM1 (M_i=0.61 and f_s=10 kHz).

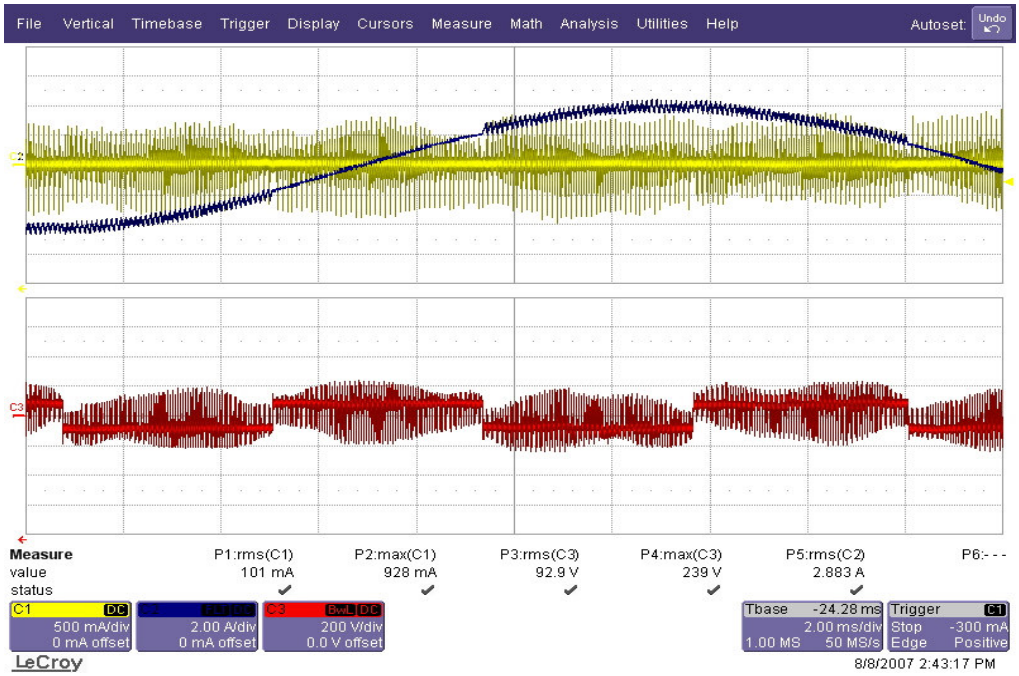


Figure 5.14 Phase current (blue), CMC (yellow), and CMV (red) waveforms for NSPWM (M_i=0.61 and f_s=10 kHz).

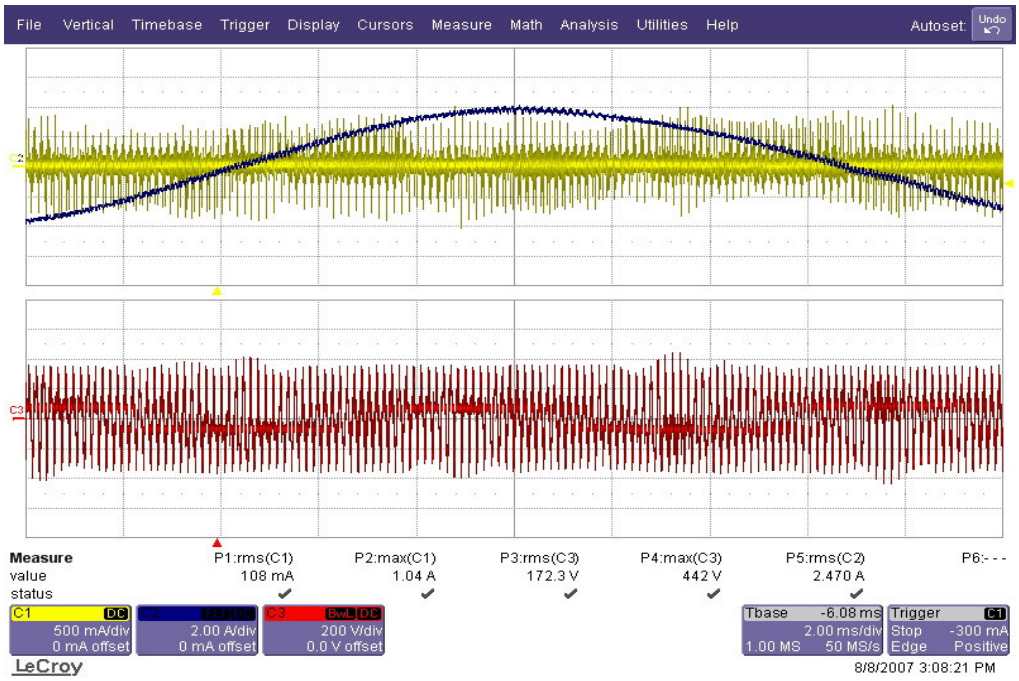


Figure 5.15 Phase current (blue), CMC (yellow), and CMV (red) waveforms for SVPWM (M_i=0.61 and f_s=6.6 kHz).

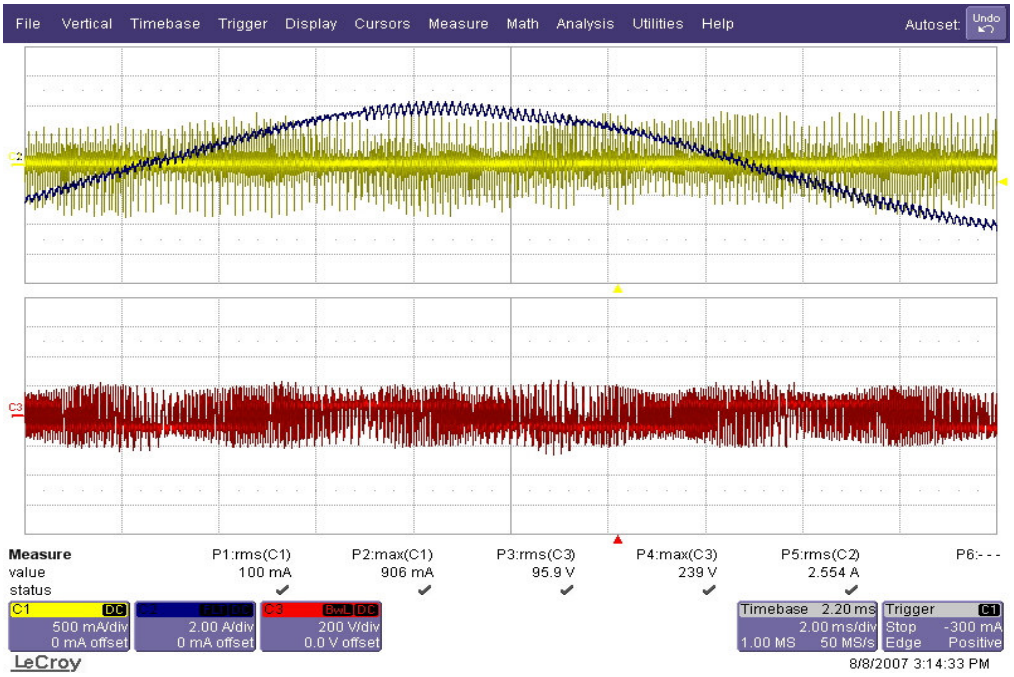


Figure 5.16 Phase current (blue), CMC (yellow), and CMV (red) waveforms for AZSPWM1 (M_i=0.61 and f_s=6.6 kHz).

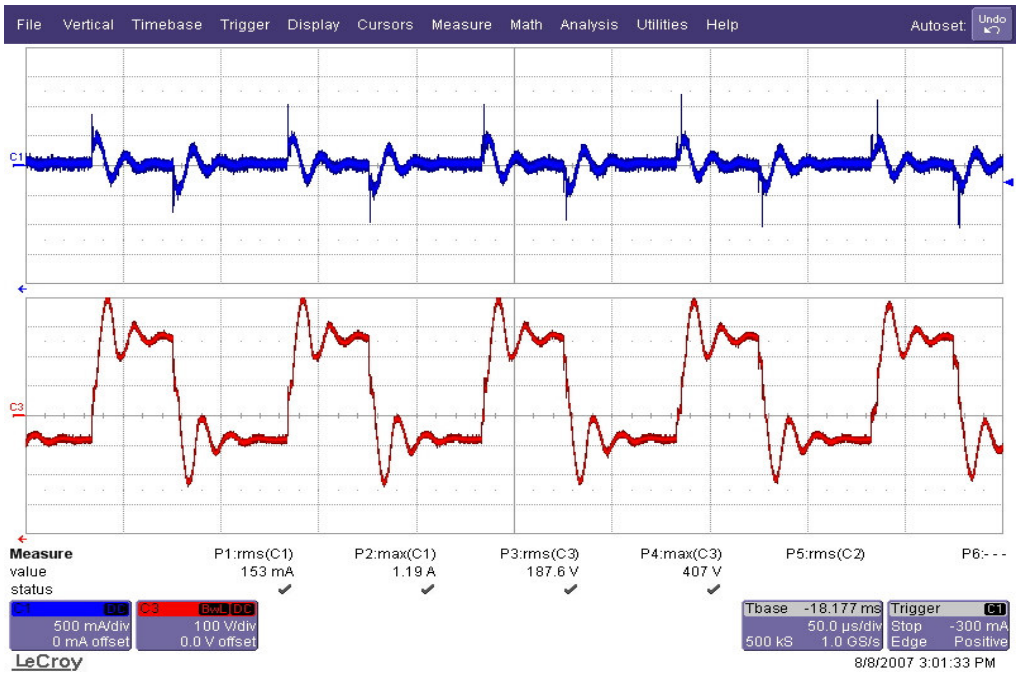


Figure 5.17 DPWM1 zoom in CMC (blue) and CMV (red) waveforms for M_i=0.61.

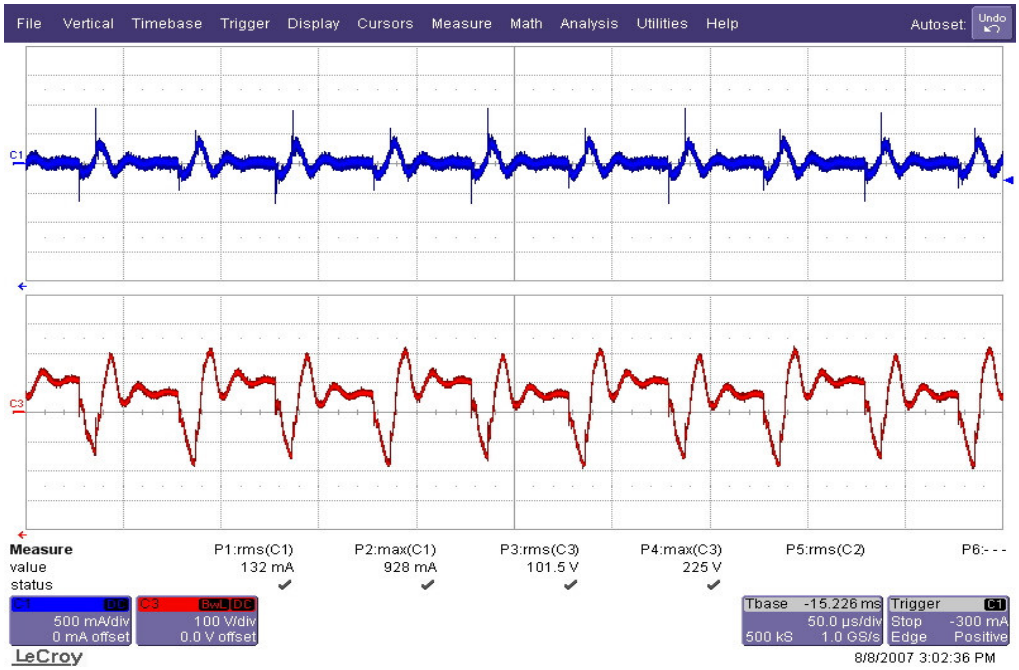


Figure 5.18 NSPWM zoom in CMC (blue) and CMV (red) waveforms for M_i=0.61.

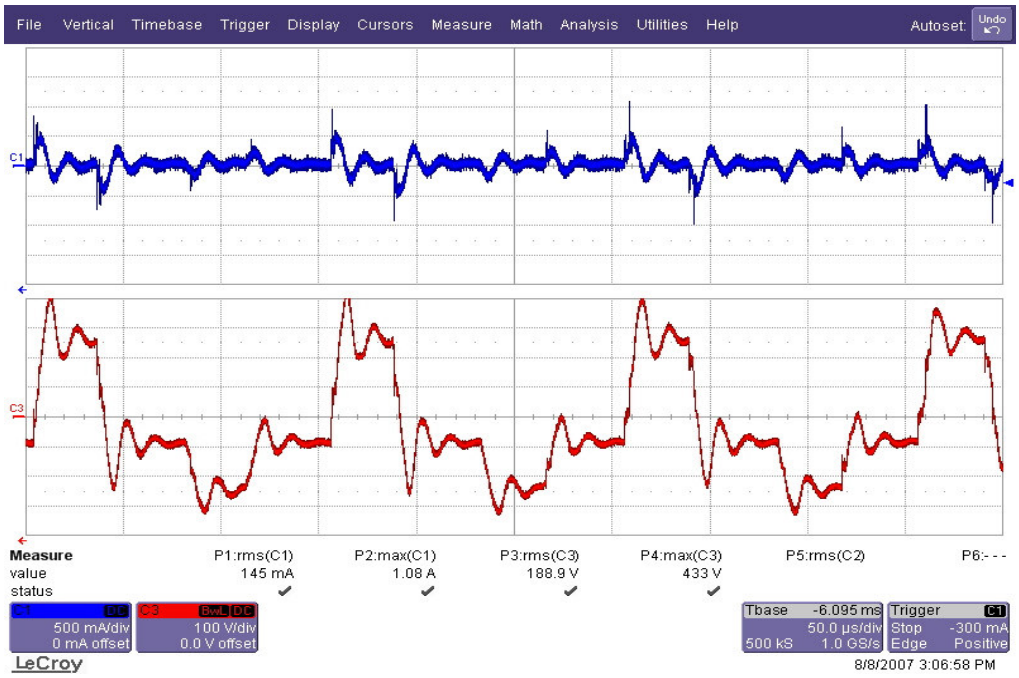


Figure 5.19 SVPWM zoom in CMC (blue) and CMV (red) waveforms for M_i=0.61.

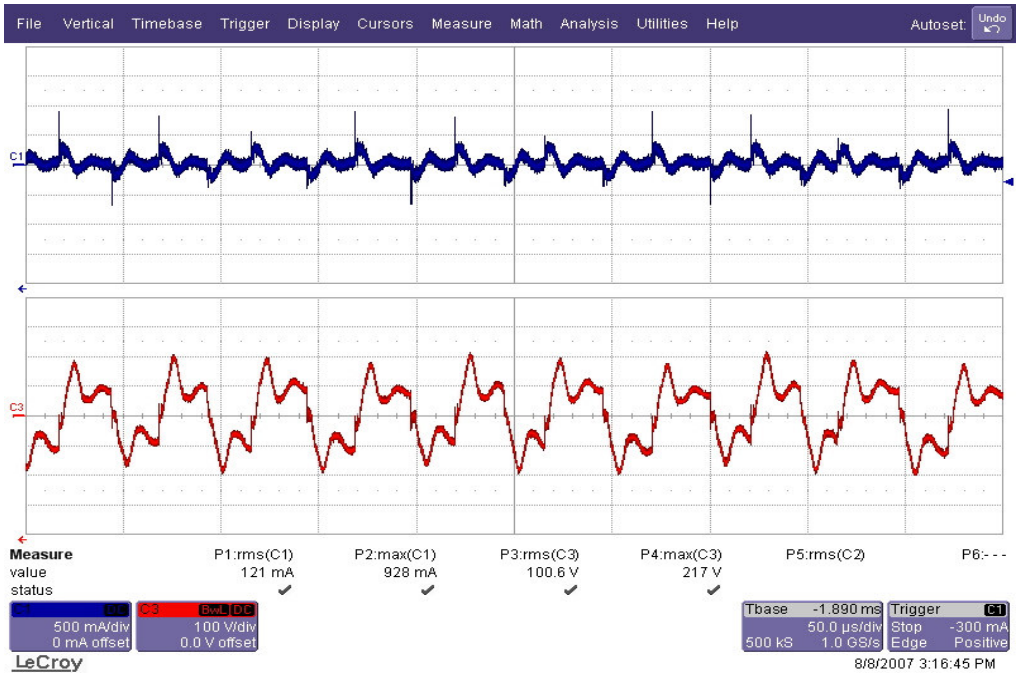


Figure 5.20 AZSPWM1 zoom in CMC (blue) and CMV (red) waveforms for M_i=0.61.

5.4.3 CMV/CMC Performance Evaluation without Passive Filters

To summarize the CMV/CMC characteristics of the PWM methods, comparison tables are provided in this section. The experimental peak and rms CMV measurements of the PWM methods at M_i=0.8 and M_i=0.61 are tabulated in Table 5.1 and Table 5.2 respectively. The tables indicate that the peak and rms CMV measurements at M_i=0.61 and M_i=0.8 are quite similar for all PWM methods. The peak and rms CMV measurements of NSPWM and AZSPWM1 are very close to each other for both operating points. Similarly the peak and rms CMV measurements of SVPWM and DPWM1 are very close to each other and significantly higher than those of RCMV-PWM methods. The differences are more significant in the peak CMV measurements. Peak CMV of standard PWM methods are almost twice the values of those of RCMV-PWM methods.

Table 5.1 Experimental Peak CMV measurements.

	CMV(V) (M_i=0.8)	CMV(V) (M_i=0.61)
DPWM	451	415
NSPWM	212	239
SVPWM	442	442
AZSPWM1	221	239

Table 5.2 Experimental RMS CMV measurements.

	CMV(V) (M_i=0.8)	CMV(V) (M_i=0.61)
DPWM	133	173
NSPWM	92	92
SVPWM	130	172
AZSPWM1	90	95

The experimental peak and rms CMC measurements of the PWM methods are tabulated in Table 5.3 and Table 5.4 respectively. Similar to the CMV measurements, the CMC measurements of all PWM methods also are not affected by M_i such that the CMC measurements at M_i=0.8 and M_i=0.61 are similar and slightly less in the RCMV-PWM methods. Note that the peak currents are about 1A in magnitude and not negligible compared to the motor no-load phase current which is 4A. Thus, the effect of CMC on the motor performance and the effect of the drive generated EMI on the environment can not be understated.

Table 5.3 Experimental Peak CMC measurements.

	i_{cm} (A) (M_i=0.8)	i_{cm} (A) (M_i=0.61)
DPWM	1.35	1.3
NSPWM	0.95	0.928
SVPWM	1.1	1.04
AZSPWM1	1.02	0.906

Table 5.4 Experimental RMS CMC measurements.

	i_{cm} (mA) (M_i=0.8)	i_{cm} (mA) (M_i=0.61)
DPWM	108	105
NSPWM	95	101
SVPWM	107	108
AZSPWM1	98	100

5.5 CMV/CMC Experimental Results with Common Mode Inductors

The experimental results which were provided in the previous section show that all PWM methods have high CMC when no CMV/CMC filter is inserted. RCMV-PWM methods decrease CMC partially but the performance increment is not sufficient in some applications. Therefore utilization of passive filters in such applications is

mandatory. In this section CMV/CMC performances of PWM methods are investigated when common mode inductors are connected between the VSI output terminals and the induction motor terminals. For this purpose three different CMIs are designed and tested (Figure 5.21). Of these CMIs, CMI-1 is the blue one (on the left), CMI-2 is the green one (in the middle) and CMI-3 is the grey and large one (on the right) seen in the Figure 5.21. All three inductors utilize different ferrite cores with different characteristics and their equivalent common mode inductance values are different. The characteristics of the CMIs and the magnetic cores utilized in these CMIs are tabulated in Table 5.5 and Table 5.6 respectively. CMI-1 and CMI-2 are very close to each other in size and CMI-3 is much larger than the other two; while CMI-2 has a core higher magnetic permeability than the others. Since each CMI utilizes different magnetic core with different magnetic material, their magnetic characteristics are unique. The Acme A121 magnetic material utilized in CMI-2 saturates at lower magnetic flux density compared to others and its performance significantly degrades with increasing temperature. However it has lower resistivity resulting in higher core losses than the other cores (it is more lossy). The characteristics of Epcos T-65 and Cosmo CF-195 which are utilized in CMI-1 and CMI-3 respectively are similar to each other with the same magnetic permeability. However Epcos T-65 has slightly higher magnetic saturation flux density while it is less lossy compared to Cosmo CF-195. The variation of magnetic permeabilities of these cores with respect to the frequency is illustrated at Figure 5.22. It is observed that magnetic permeabilities of all three cores remain at approximately at their initial value (magnetic permeability at low frequency) at least up to 100 kHz which is a higher value that the frequency of the CMV of the PWM methods and the LC resonant frequency of the CM equivalent components of the system. Therefore all of these magnetic cores can be utilized for the suppression of the CMC at the inverter driven induction motors. The peak current is at very high frequency (in the MHz range) and all the cores considered are sufficient in suppressing the peak. The cores should be designed according to the B_{sat} value of the core such that the peak current does not saturate the core significantly. In the design, the core count and number of turns were determined accordingly.

Note in Table 5.5 the differential mode inductance of the CMI's is given for the purpose of later studies involving parasitics (long cable etc.). The differential mode inductance is measured as the inductance between two CMI input terminals while the output is short-circuited for these two phases.

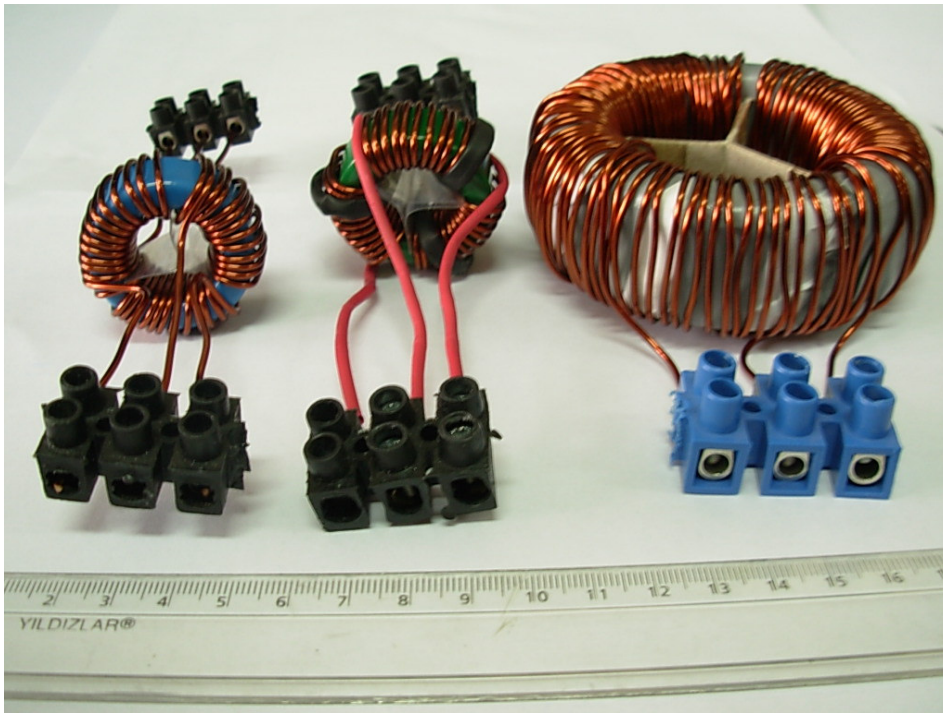


Figure 5.21 CMIs built and utilized in the experiments.

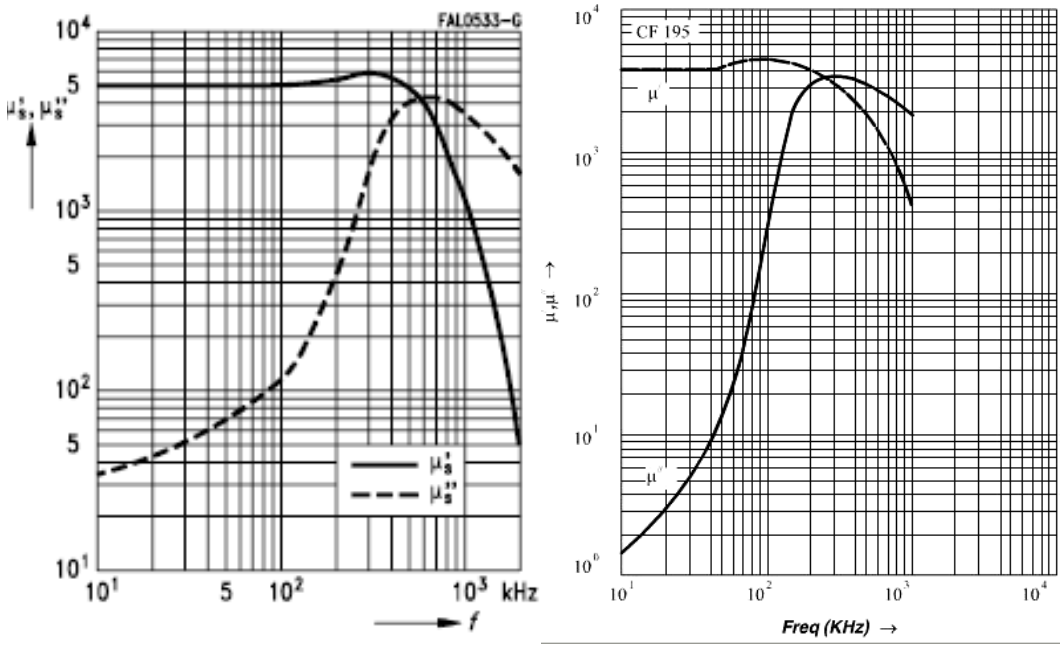
Table 5.5 Design parameters of the utilized CMIs.

	CMI-1	CMI-2	CMI-3
Equivalent CM inductance - L_{eq} (mH)	0.8	2.2	9.8
Equivalent DM inductance - L_{eq} (μH)	13	13	160
Number of turns - N	12	12	30
Relative permeability - μ_r	5000	12000	5000
Outer diameter (mm)	36	36	86
Inner diameter (mm)	22.5	23	62
Height (mm)	16	15	30

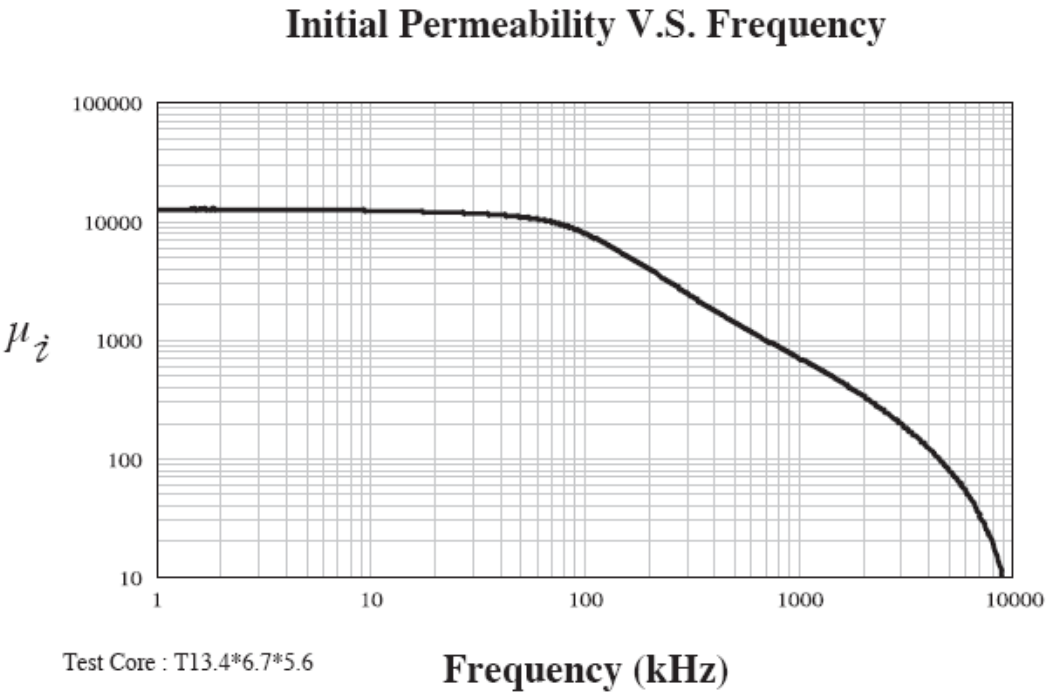
Table 5.6 Properties of the magnetic materials of the utilized toroidal cores.

	CMI-1	CMI-2	CMI-3
Magnetic core manufacturer	Epcos	Acme	Cosmo
Relative permeability - μ_r	5000	12000	5000
Saturation magnetic flux density B_{sat} (mT) (T=25^{o}C)	460	360	400
Saturation magnetic flux density B_{sat} (mT) (T=100^{o}C)	320	180	260
Loss factor - tan δ/μ_i (10^{-6}) (f=10kHz)	<1.5	<10	<5
Loss factor - tan δ/μ_i (10^{-6}) (f=100kHz)	<25	<60	<60
Curie temperature (^{o}C)	>160	>110	>120
Resistivity - ρ (Ωm)	0.3	0.12	0.2

The experimental results show that with the inclusion of the CMIs; CMC suppression performance increases. CMI-3, which is a significantly larger (and thus much more expensive) than CMI-2, exhibits limited performance improvement over CMI-2. Additionally the core of CMI-2 has more lossy characteristics (lower core resistance). Comparable in size to CMI-2, CMI-1 performs noticeably less than CMI-1. Therefore good CMC performance is achieved by utilizing CMI-2 and the experimental waveforms of only CMI-2 are provided in this thesis while experimental measurements taken during the experiments are provided in the comparison table (to be shown shortly) for all CM filters. Since the CMV/CMC do not change significantly with M_i, from now on only operation at one M_i point will be considered for CMV/CMC studies.



(a) (b)



(c)

Figure 5.22 Initial permeability vs. frequency curves for a) Epcos T-65 (CMI-1); b) Cosmo CF195 (CMI-3); c) Acme A121 (CMI-2).

5.5.1 CMV/CMC Experimental Results with CMI-2

For M_i=0.8, the experimental results of the phase current, CMC, and CMV for DPWM1, NSPWM, SVPWM, and AZSPWM1 are illustrated in Figures 5.23, 5.24, 5.25, and 5.26 respectively. The experimental results show that the CMI does not affect the phase currents since its normal mode inductance is negligible and it only affects the CMC. Experimental results show that the peak values of CMC for all PWM methods are significantly reduced by adding CMI. Similarly due to the lossy characteristic of the core of this inductor, the rms value of CMC is also reduced. Although the CMC is reduced in all PWM methods, each PWM method has still different CMC measurement results. NSPWM and AZSPWM1 have lower CMC than DPWM1 and SVPWM and the difference is more obvious than the case when no CMI is added. Additionally RCMV-PWM methods have significantly lower CMV than standard PWM methods. Microscopic investigations reveal that shapes of the waveforms of CMV and CMC of PWM methods are also changed. Figures 5.27, 5.28, 5.29, and 5.30 illustrate the microscopic view of the CMV/CMC waveforms. The shapes of the CMV and CMC waveforms of the PWM methods are also changed. After CMI is inserted, the current spikes over the CMC are not observed. This is the main reason of the decrease of the peak values of the CMC, since the peak current spikes determine the peak CMC when CMI is not added. In addition to eliminating the peak currents; due to the lossy nature of the core of the inductor, oscillations on the CMC are damped faster than the case where other CMIs are utilized is utilized. This damping reduces the rms CMC. The CMV of the RCMV-PWM methods are still smaller than those of SVPWM and DPWM1 and their shapes are smoother the case where no CMI is utilized.

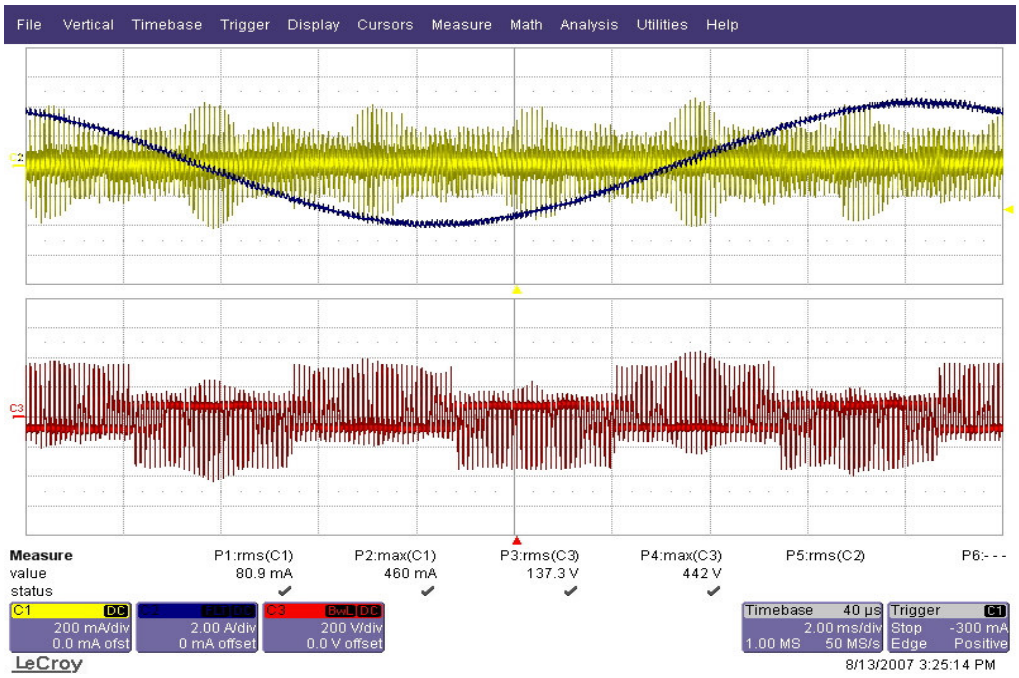


Figure 5.23 Phase current (blue), CMC (yellow), and CMV (red) waveforms for DPWM1 (M_i=0.8 and f_s=10 kHz) with CMI-2.

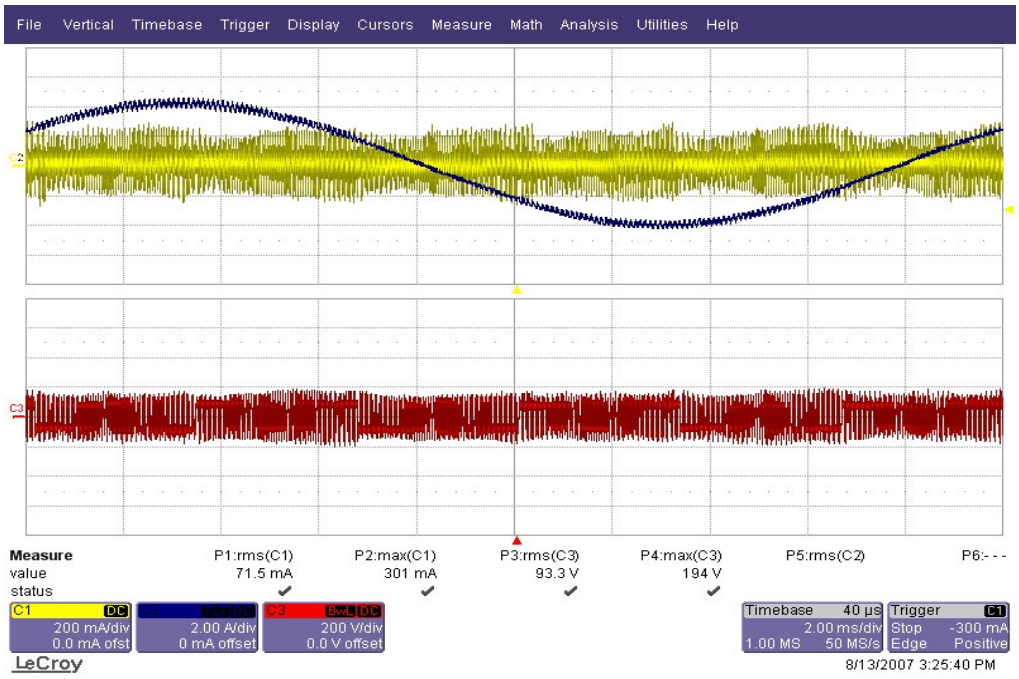


Figure 5.24 Phase current (blue), CMC (yellow), and CMV (red) waveforms for NSPWM (M_i=0.8 and f_s=10 kHz) with CMI-2.

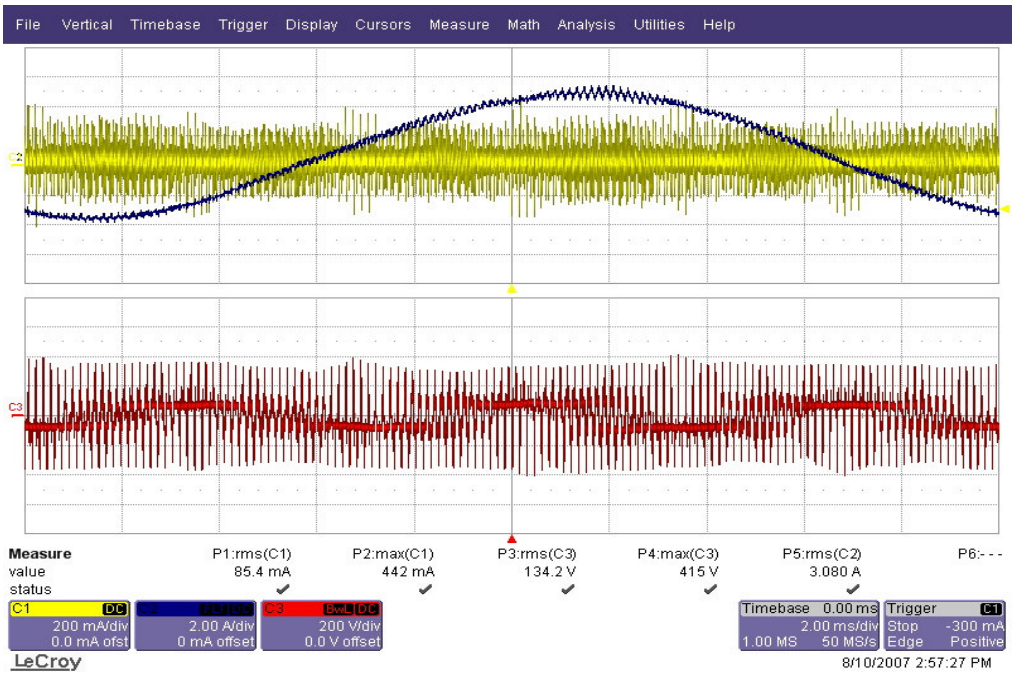


Figure 5.25 Phase current (blue), CMC (yellow), and CMV (red) waveforms for SVPWM (M_i=0.8 and f_s=6.6 kHz) with CMI-2.

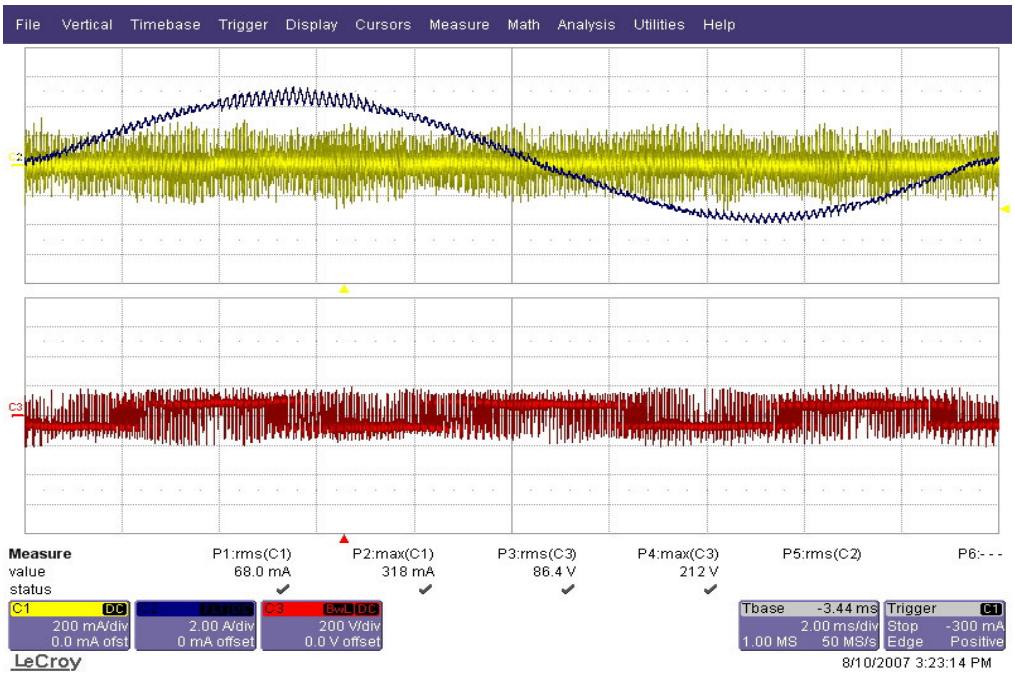


Figure 5.26 Phase current (blue), CMC (yellow), and CMV (red) waveforms for AZSPWM1 (M_i=0.8 and f_s=6.6 kHz) with CMI-2.

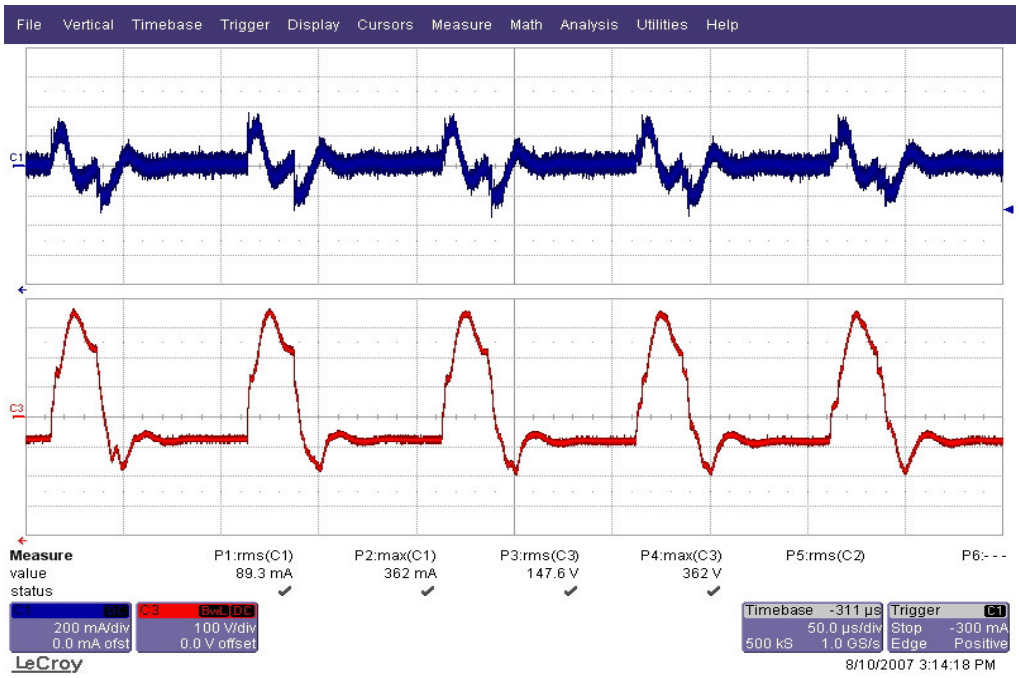


Figure 5.27 DPWM1 zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8 with CMI-2.

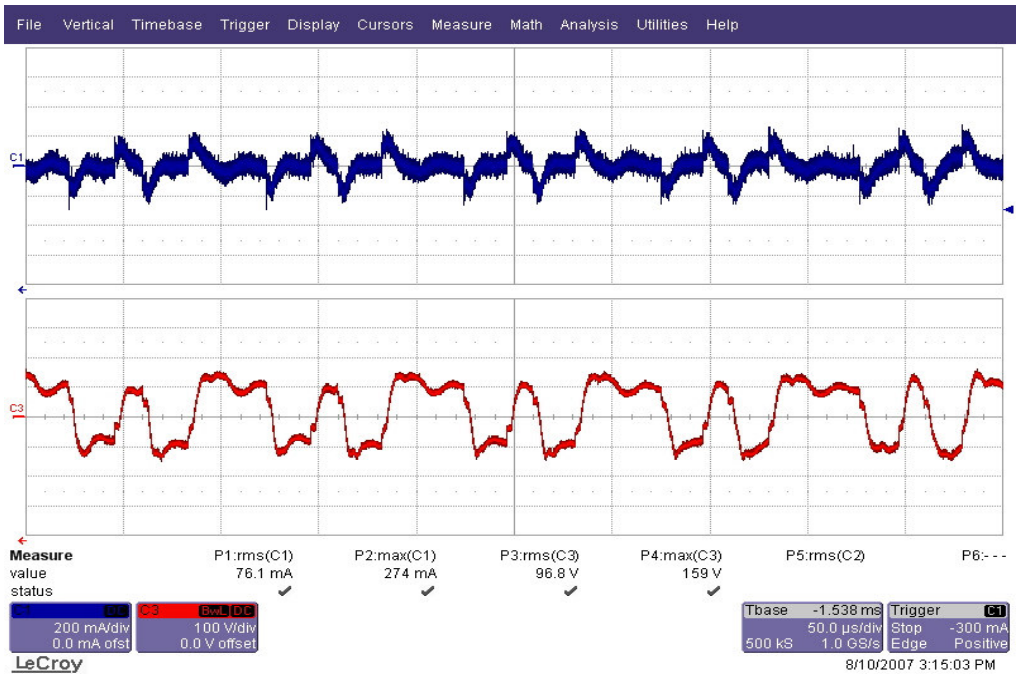


Figure 5.28 NSPWM zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8 with CMI-2.

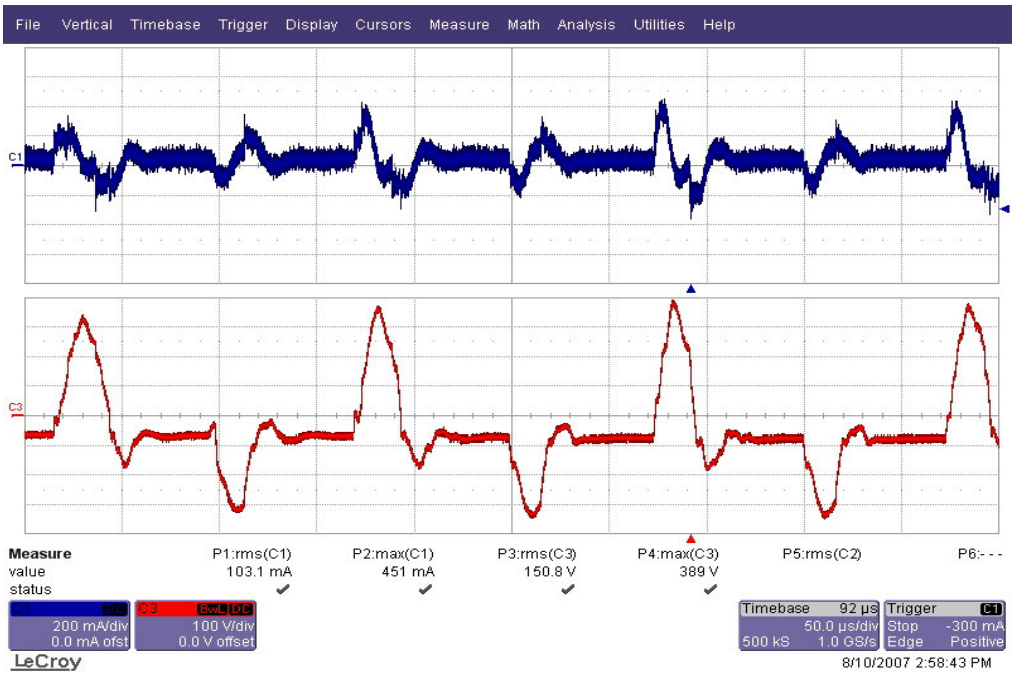


Fig 5.29 SVPWM zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8 with CMI-2.

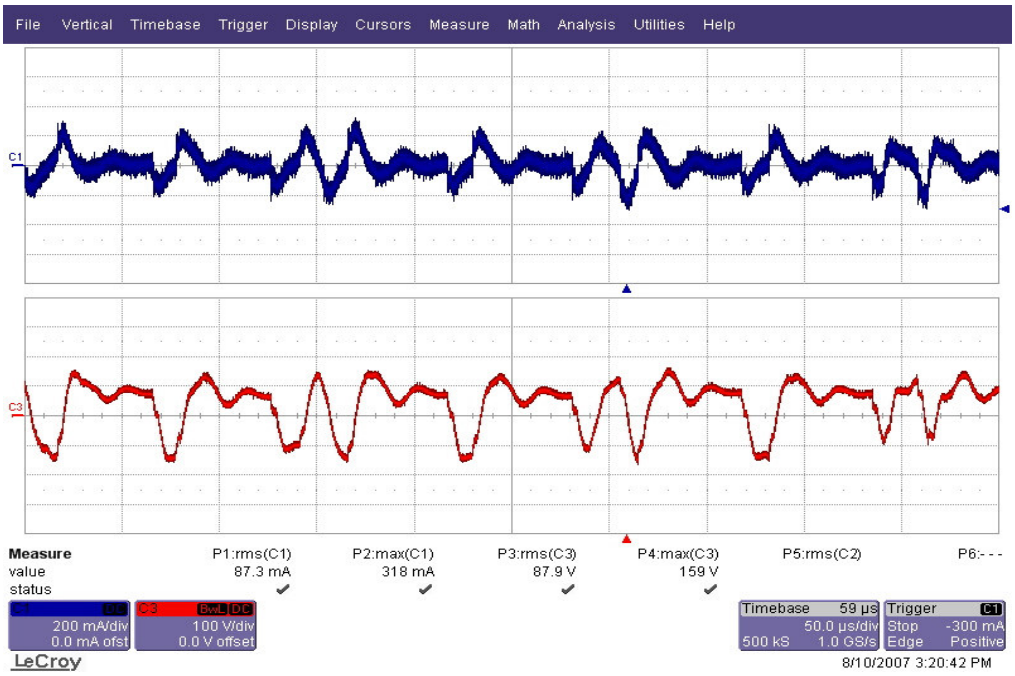


Fig 5.30 AZSPWM1 zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8 with CMI-2.

5.5.2 CMV/CMC Experimental Results with Common Mode Transformer

In the previous sections, CMC reduction performance of the CMI was experimentally investigated and the results were illustrated. The CMIs reduce the CMC but they result in oscillations on CMC waveforms. In order to damp these oscillations CM transformers (CMT) may be utilized. Therefore, in order to investigate the effects of the CMTs over the CMC, a CMT is manufactured by modifying the CMI-3 structure. A secondary winding of 3 turns is wound on the CMI-3 core and a damping resistor of 35 Ω value is connected to the secondary winding. Experimental trials show that this damping resistance value provides optimum performance in the prototype CMT.

The experimental results of phase current, CMC, and CMV for DPWM1, NSPWM, SVPWM, and AZSPWM1 are illustrated at Figures 5.31, 5.32, 5.33, and 5.34 respectively when the CMT is utilized. The experimental results show that the rms values of the CMCs are reduced by connecting the secondary winding for all PWM methods. AZSPWM1 and NSPWM methods have less CMC than standard PWM methods while AZSPWM1 is superior. Inserting CMT does not affect the CMV similar to the CMIs and RCMV-PWM methods have significantly lower CMV than standard PWM methods.

Figures 5.35, 5.36, 5.37, and 5.38 illustrate the microscopic view of the CMV/CMC waveforms for the CMT case. The microscopic investigations illustrate the shapes of the CMV and CMC waveforms. After the secondary winding and the damping resistor are added, the oscillations on the CMC waveforms are damped faster for all PWM methods resulting in less rms CMC. The shapes of the CMV waveforms are very smooth and the high frequency components of the CMV waveform are eliminated remaining only the fundamental component of the CMV (the CMV base frequency) and its low order harmonics.

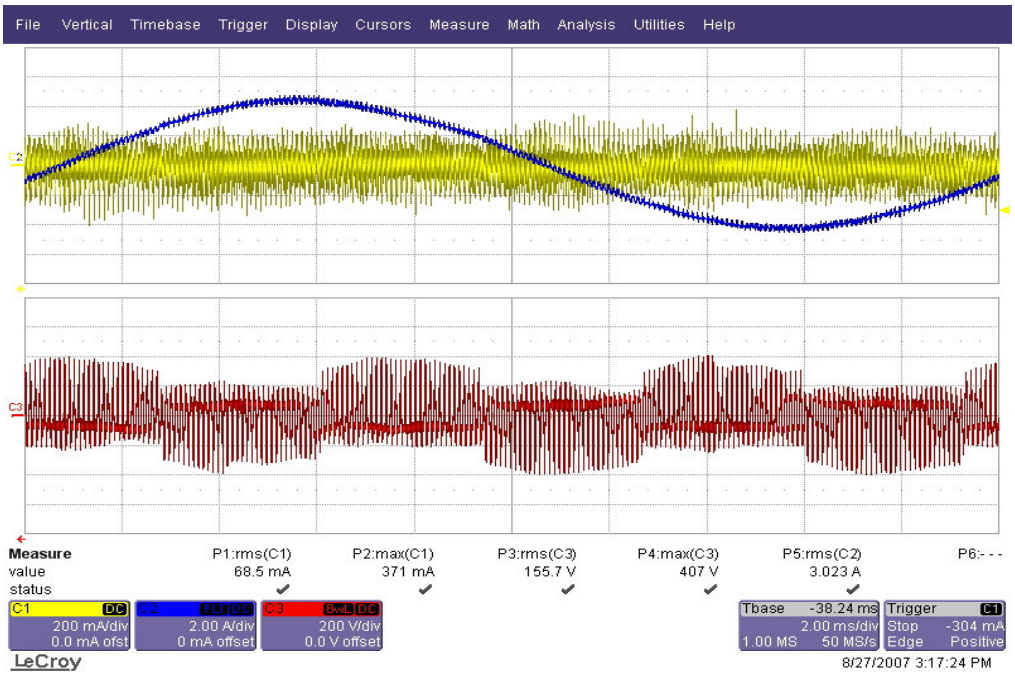


Figure 5.31 Phase current (blue), CMC (yellow), and CMV (red) waveforms for DPWM1 (M_i=0.8 and f_s=10 kHz) with CMT.

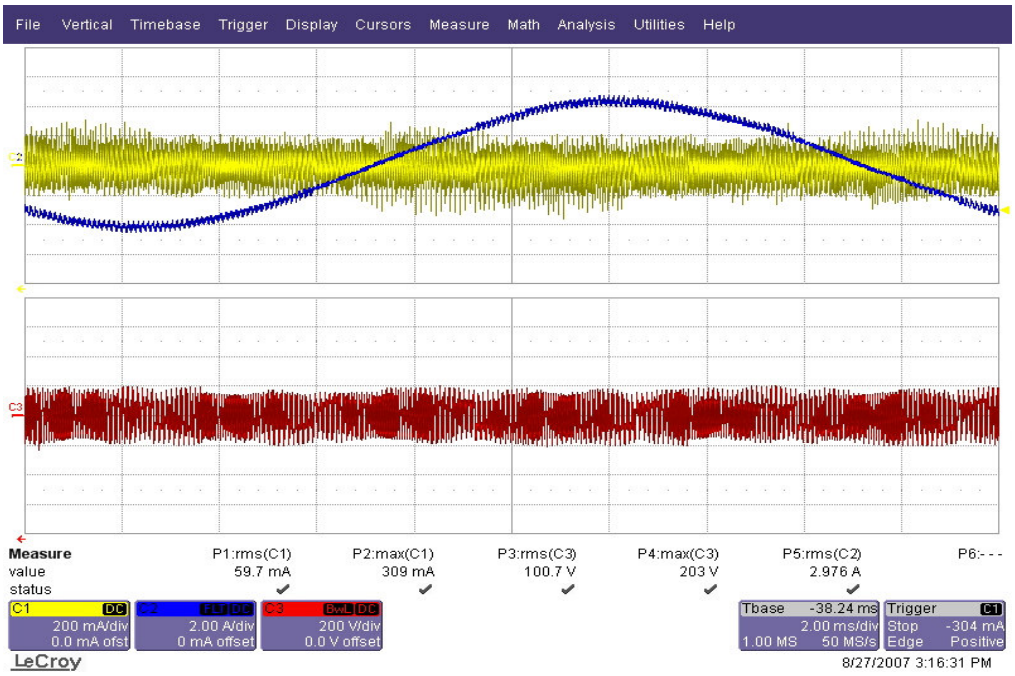


Figure 5.32 Phase current (blue), CMC (yellow), and CMV (red) waveforms for NSPWM (M_i=0.8 and f_s=10 kHz) with CMT.

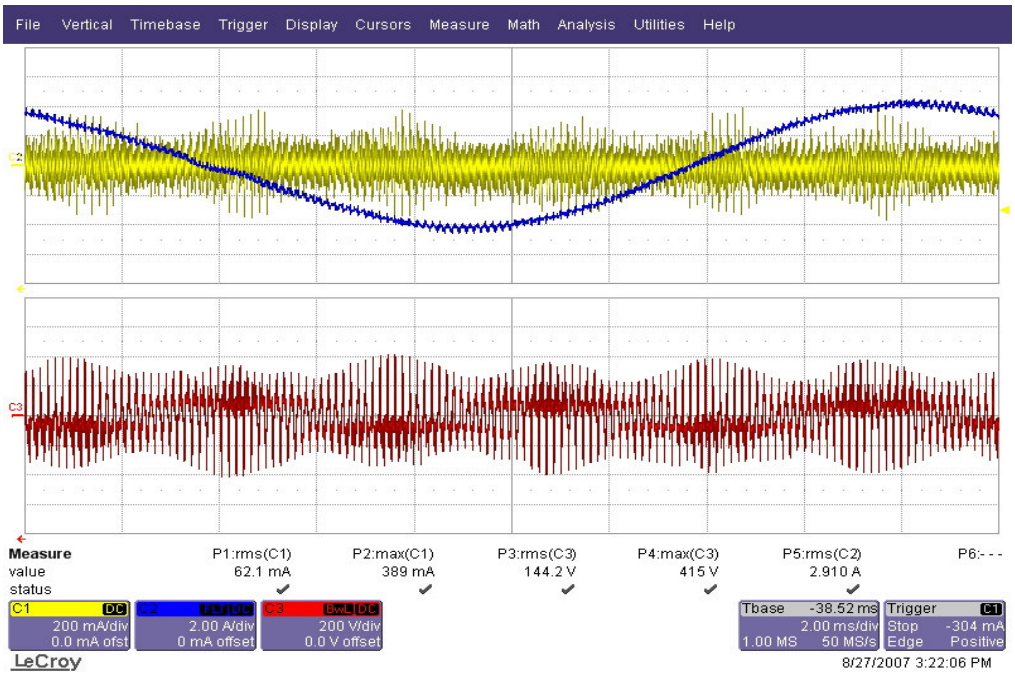


Figure 5.33 Phase current (blue), CMC (yellow), and CMV (red) waveforms for SVPWM (M_i=0.8 and f_s=6.6 kHz) with CMT.

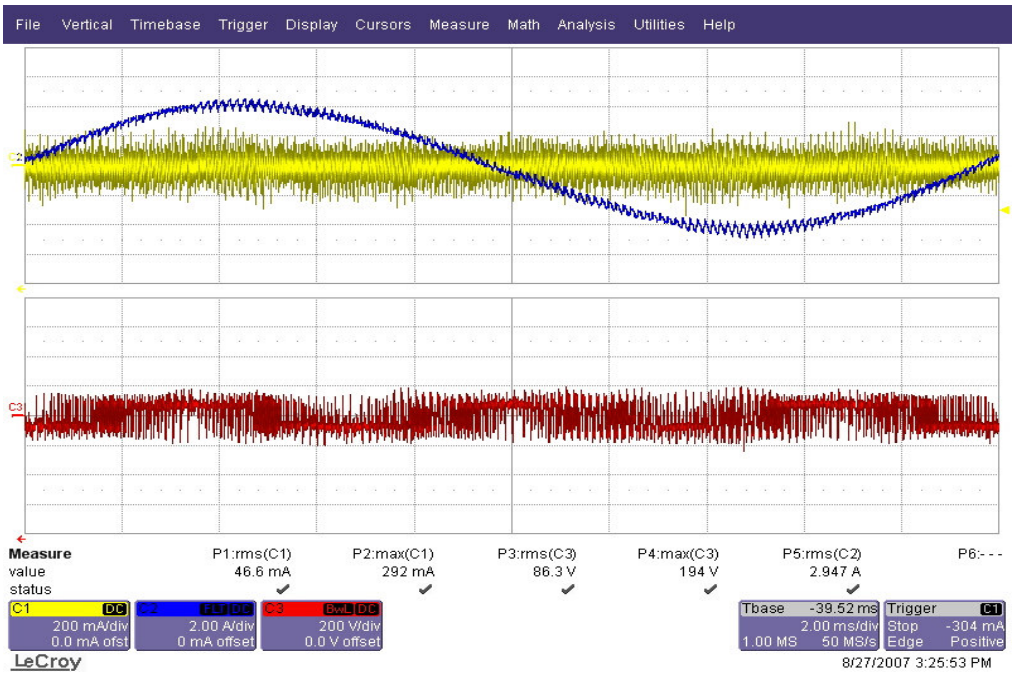


Figure 5.34 Phase current (blue), CMC (yellow), and CMV (red) waveforms for AZSPWM1 (M_i=0.8 and f_s=6.6 kHz) with CMT.

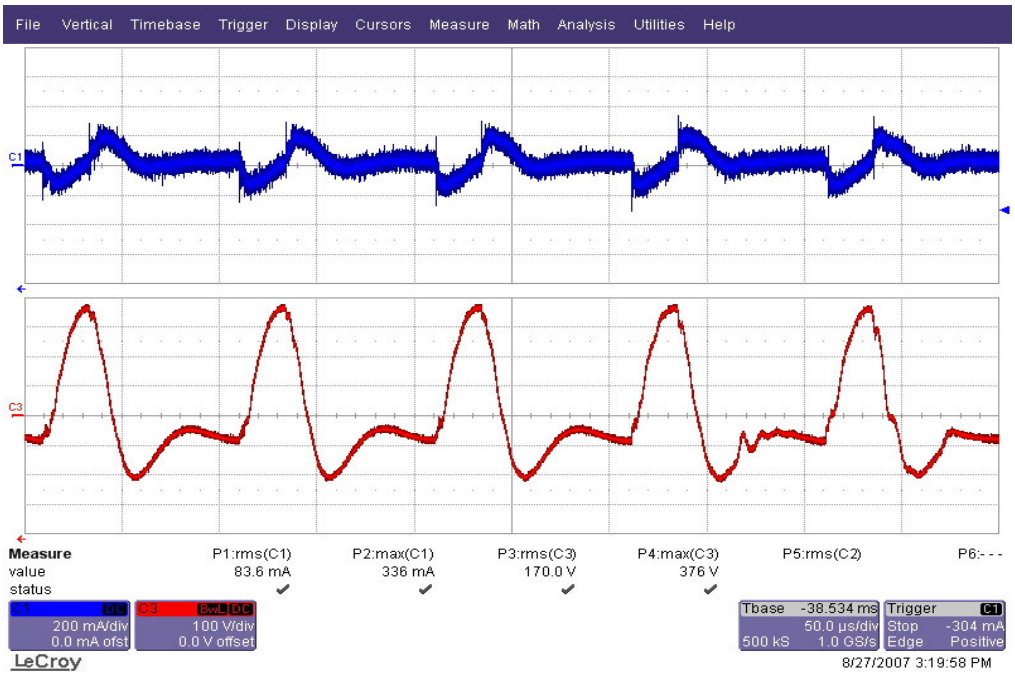


Figure 5.35 DPWM1 zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8 with CMT.

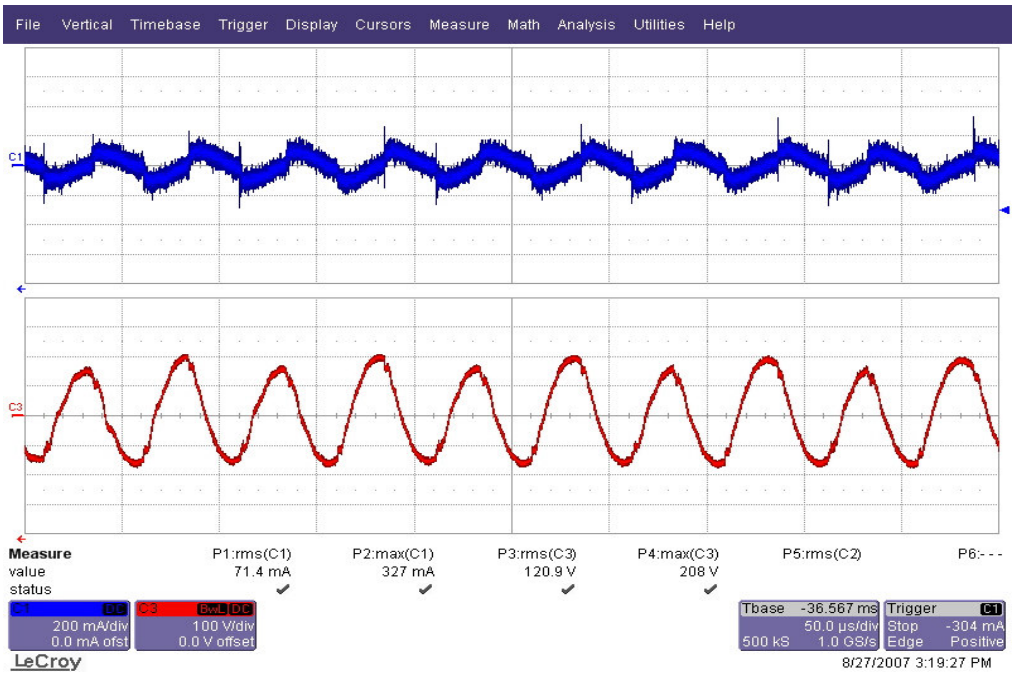


Figure 5.36 NSPWM zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8 with CMT.

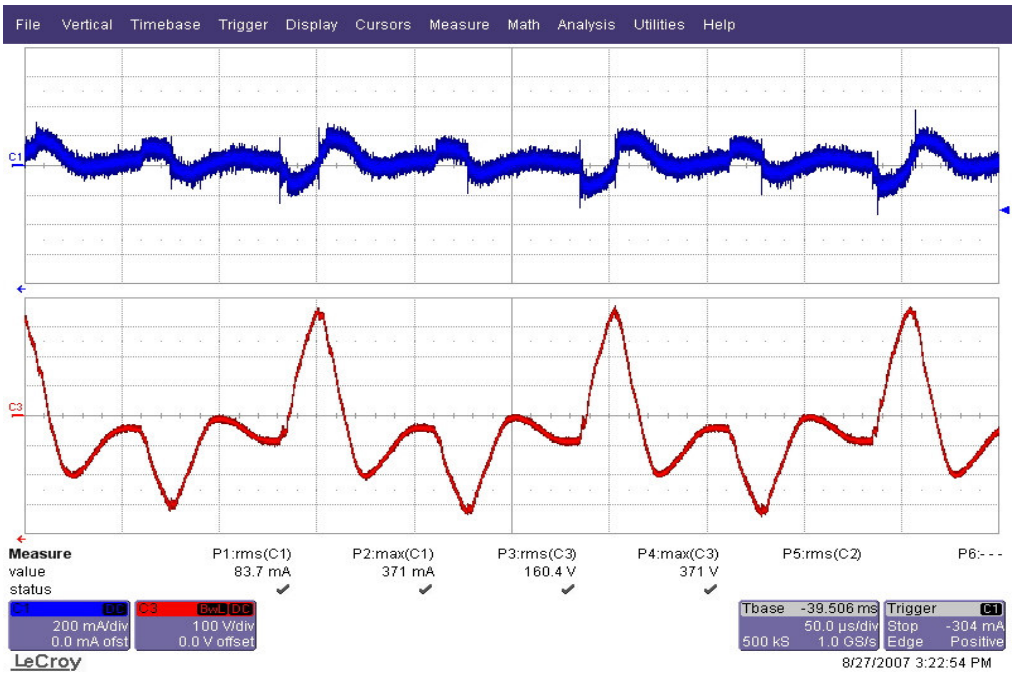


Figure 5.37 SVPWM zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8 with CMT.

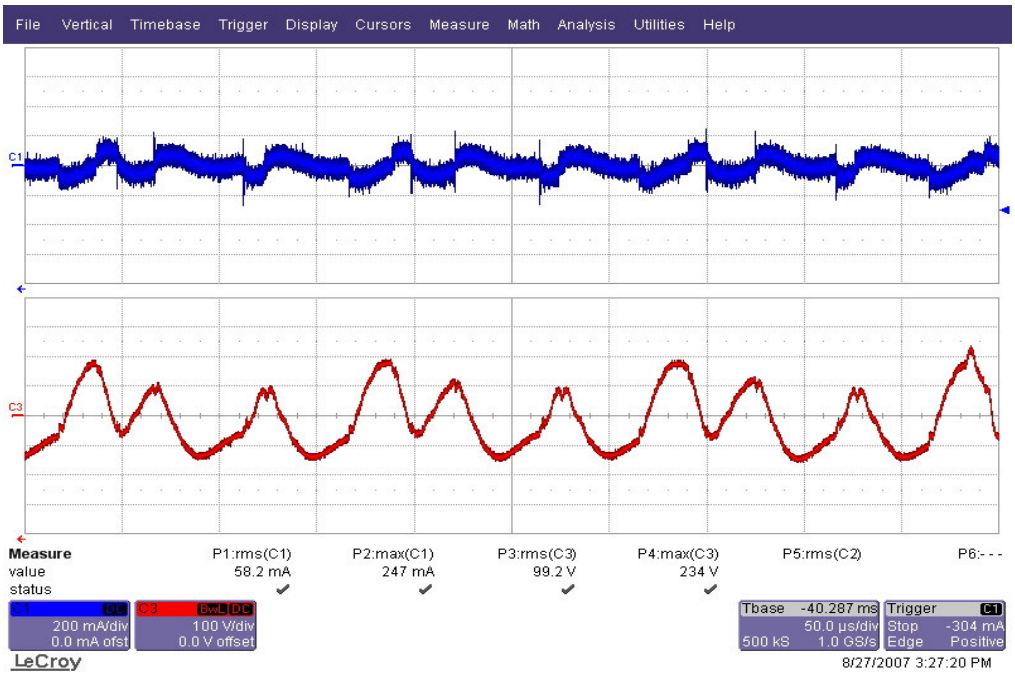


Figure 5.38 AZSPWM1 zoom in CMC (blue) and CMV (red) waveforms for M_i=0.8 with CMT.

5.5.3 CMV/CMC Performance Evaluation of Passive Filters

The experimental results clearly illustrate that inserting a CMI or CMT successfully reduces CMC. However the CMC suppression performance improvement is different for each passive filter and each PWM method.

In Table 5.7 and Table 5.8, peak and rms CMC values are tabulated respectively for various PWM methods when different passive CMC filters are utilized. The experimental results show that increasing the inductance of CMI reduces the peak and rms CMC. Replacing the CMI with a CMT slightly increases the peak CMC but significantly reduces the rms CMC. Also together with a passive CMC filter, utilizing an RCMV-PWM method further reduces the CMC. When RCMV-PWM methods are utilized less CMC may be resulted even with a smaller CMI. The CMC suppression performance of the RCMV-PWM methods improves with utilizing passive filters. This proves that utilizing the CM filters together with RCMV-PWM methods are much more effective and efficient than utilizing only one of the mitigation methods.

The experimental CMC waveforms illustrate that, by adding a CMI, peak CMC overshoots are suppressed while the oscillatory behavior of CMC waveform become dominant and reduction of the rms CMC is less successful. Theoretically this can be explained by the fact that increasing equivalent CM inductance reduces CMC peak value and the CMC rms value is reduced by increasing equivalent CM resistance [7]. CMIs with lossy cores (with low core loss resistances) and CMTs with damping resistors increase the equivalent CM resistance hence reduce the rms CMC. In Table 5.7 it is shown that all CMIs reduce the CMC rms value particularly but the highest performance improvement is achieved by utilizing CMT since it increases the effective CM equivalent resistance. However, CMI-3 and CMT are very bulky compared to other two CMIs. Of these two CMIs, CMI-2 performs satisfactory and it achieves a slightly inferior performance compared to CMI-3 and CMT with much smaller size. Therefore CMI-2 is considered as the most suitable CMI for this operation.

Table 5.7 Experimental Peak CMC measurements (M_i=0.8).

	i_{cm} (A) (No-filter)	i_{cm} (mA) (CMI-1)	i_{cm} (mA) (CMI-2)	i_{cm} (mA) (CMI-3)	i_{cm} (mA) (CMT)
DPWM	1.350	552	460	389	371
NSPWM	0.950	376	301	309	309
SVPWM	1.100	530	442	336	389
AZSPWM1	1.02	464	318	256	292

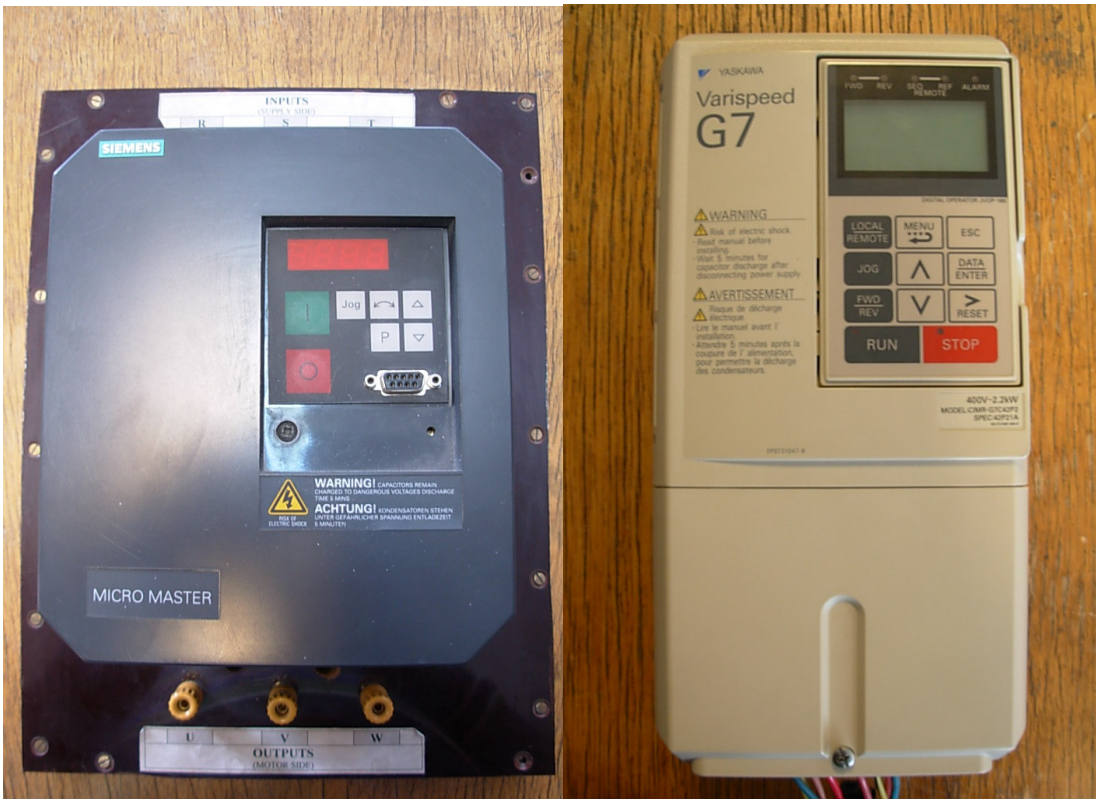
Table 5.8 Experimental RMS CMC measurements (M_i=0.8).

	i_{cm} (mA) (No-filter)	i_{cm} (mA) (CMI-1)	i_{cm} (mA) (CMI-2)	i_{cm} (mA) (CMI-3)	i_{cm} (mA) (CMT)
DPWM	108	100	80.9	88	68
NSPWM	95	86	71.5	67	59
SVPWM	107	104	85.4	72	62
AZSPWM1	98	94	68	55	46

5.6 CMV/CMC Experimental Results for Commercial Inverters

The experimental CMV/CMC measurements of the prototype VSI built in this thesis with and without passive filters were provided in the previous sections. In order to compare the performance attributes of the prototype VSI with the commercial inverters and to investigate the effects of increasing the level of the inverter on the CMV and CMC, additional laboratory experiments are conducted utilizing a commercial two-level VSI and a commercial three-level NPC inverter which are illustrated in Figure 5.39. The commercial two-level VSI is Siemens Micromaster 6SE3121 with output ratings 5.5 kW, 13.2A and input rating of 380-500V. The commercial three-level NPC VSI is Yaskawa Varispeed G7 with output ratings 3.7 kVA, 6.2A and input rating of 380-480V.

During the experiments, the experimental measurement set-up and the test induction motor are kept same as the previous experiments on the prototype two-level inverter. To make a fair comparison, the DC-bus voltage of the inverters is set as 500 V and motor is operated at steady-state with no-load and at M_i=0.8 (180 V_{rms} /50 Hz) and M_i=0.4 (90 V_{rms} /25 Hz). Both inverters are operated at 8 kHz switching frequency. Both drives have finite number of switching frequency choices and they can not be arbitrarily set. Among these, the 8kHz value which is the closest to that of the utilized in the prototype inverter is chosen for the experiments of the commercial drives.

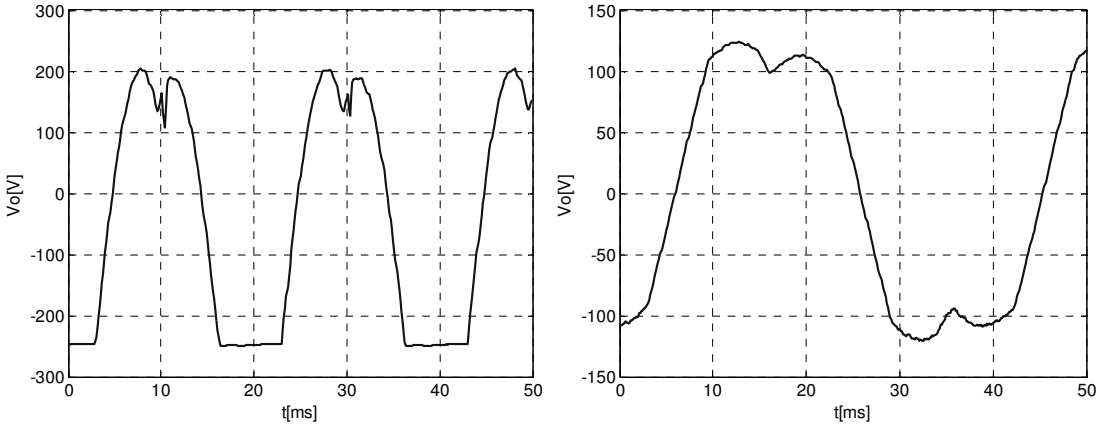


(a) (b)

Figure 5.39 The commercial VSIs utilized in this thesis (a) standard two-level VSI, (b) three-level NPC VSI.

5.6.1 CMV/CMC Experimental Results for The Commercial Two-Level Inverter

In order to observe the CMV/CMC performance of the commercial two-level VSIs a Siemens Micromaster 6SE3121 inverter drive is utilized. This drive employs a DPWM method at low M_i and SVPWM at high M_i. To identify the PWM method employed, the phase output to the DC bus midpoint voltage of the inverter is measured via the oscilloscope, the scope output is stored in a data array, then transferred to MATLAB. This data is averaged over the PWM cycle of the method (8kHz or 125μs). In Figure 5.40 the obtained voltage waveforms of the commercial two-level VSI are illustrated which reveal the PWM method information. The figure shows that the inverter utilizes SVPWM at low M_i and DPWM-MIN [17] at high M_i. The transitions between DPWM-MIN and SVPWM occurs in a hysteresis manner such that when increasing M_i, the VSI starts utilizing DPWM-MIN at approximately M_i=0.63 and when decreasing M_i the VSI starts utilizing SVPWM at approximately M_i=0.51. Since at M_i=0.8 the commercial inverter utilizes DPWM-MIN, which is a DPWM method, the experimental results will be compared with those of prototype VSI when DPWM1 and NSPWM are utilized and at M_i=0.4 the experimental results will be compared with those of SVPWM and AZSPWM1 of the prototype VSI since the commercial inverter utilizes SVPWM at this operating point.



(a) (b)

Figure 5.40 The phase-to-midpoint output voltage (PWM average) of the two-level VSI at a) M_i=0.8 b) M_i=0.4.

The experimental results of the phase current, CMC, and CMV for the two-level commercial VSI are illustrated in Figure 5.41 at M_i=0.8. The CMV performance of commercial VSI is poor such that the peak CMV reaches 424 V in magnitude similar to the prototype VSI when conventional PWM methods are utilized. Similarly in the commercial two-level VSI the CMC is comparable with that of the prototype VSI when DPWM1 is utilized (It is inferior to the prototype VSI when NSPWM is utilized). Since the commercial VSI is utilized at 8 kHz (not at 10 kHz) the rms CMC is slightly less than that of the prototype VSI when DPWM1 is utilized but it is still higher compared to the NSPWM case. In Figure 5.42 the microscopic views of the CMV/CMC waveforms are illustrated. The impulses over the CMC waveform have very high magnitude in the commercial two-level VSI. Similarly, the CMV waveforms are very similar to those of the prototype VSI when DPWM1 is utilized and they are very large.

The experimental results of the phase current, CMC, and CMV for the two-level commercial VSI are illustrated in Figure 5.43 at M_i=0.4. The CMV performance is comparable with the M_i =0.8 case of the commercial VSI and that of the prototype VSI when standard PWM methods are utilized. Similarly the peak CMC measurements are also comparable with those mentioned. But the RMS CMC measurements are increased at low M_i since the number of switchings increases when SVPWM is utilized (The commercial inverter operates at constant switching frequency hence number of switchings are not equal at continuous and discontinuous PWM methods). In Figure 5.44 the microscopic views of the CMV/CMC waveforms are illustrated. The impulses over the CMC waveform have very high magnitude in the commercial two-level VSI. Similarly, the CMV waveforms are very similar to those of the prototype VSI when SVPWM is utilized and they are very large.

To investigate CMV/CMC performance of the commercial two-level VSI together with the passive CM filters, the CMI-2 which was described in section 5.5.2 is connected to the commercial two-level VSI. The experimental results of the phase current, CMC, and CMV for three-level VSI are illustrated at Figure 5.45 for M_i=0.8 such that both peak and rms values of CMC is reduced and they are less than that of

the prototype VSI when DPWM1 is utilized and higher compared to the NSPWM case. CMV is still high (not affected similar to the previous tests in which the CMI-2 was utilized). Figure 5.46 illustrates the microscopic view of the CMV/CMC waveforms and shows oscillatory characteristic of the CMC and CMV exists and their magnitudes are high.

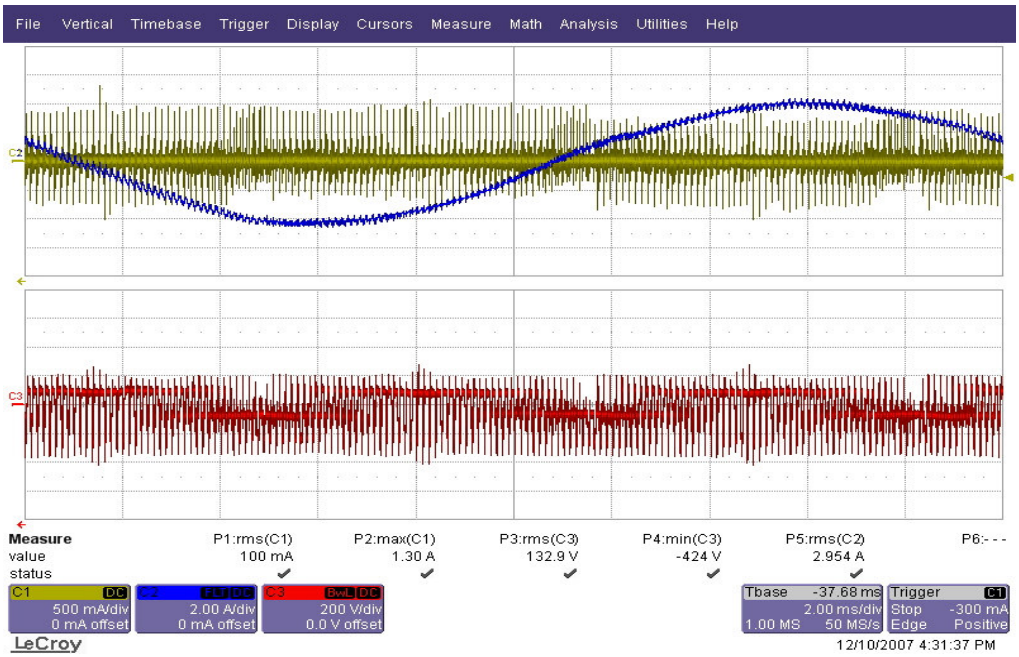


Figure 5.41 Phase current (blue), CMC (yellow), and CMV (red) waveforms of the commercial two-level VSI (M_i=0.8).

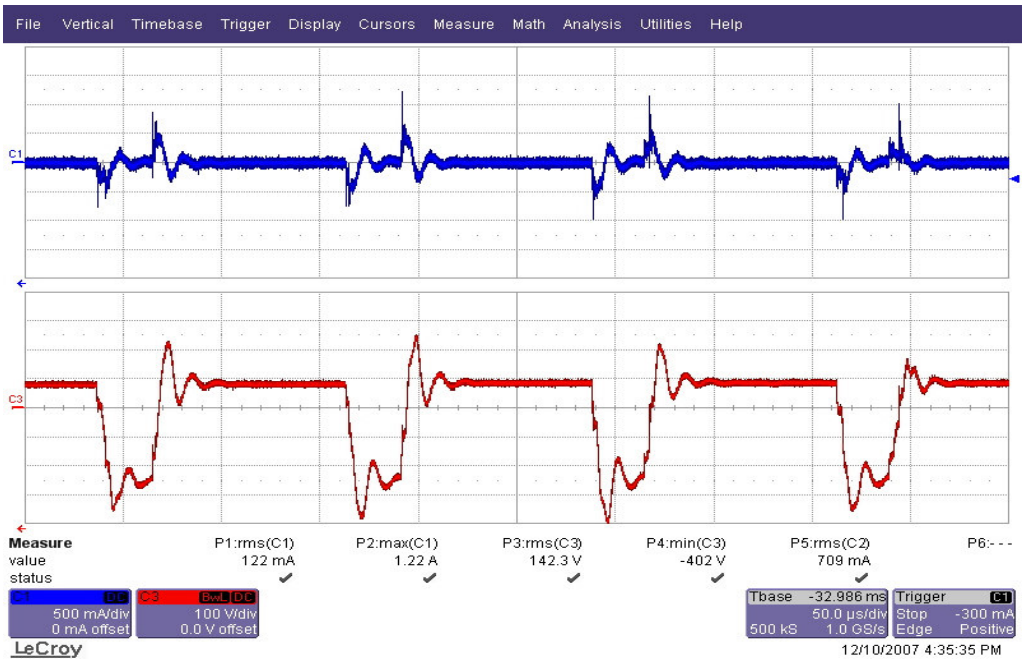


Figure 5.42 Zoom in CMC (blue) and CMV (red) waveforms for the commercial two-level VSI (M_i=0.8).

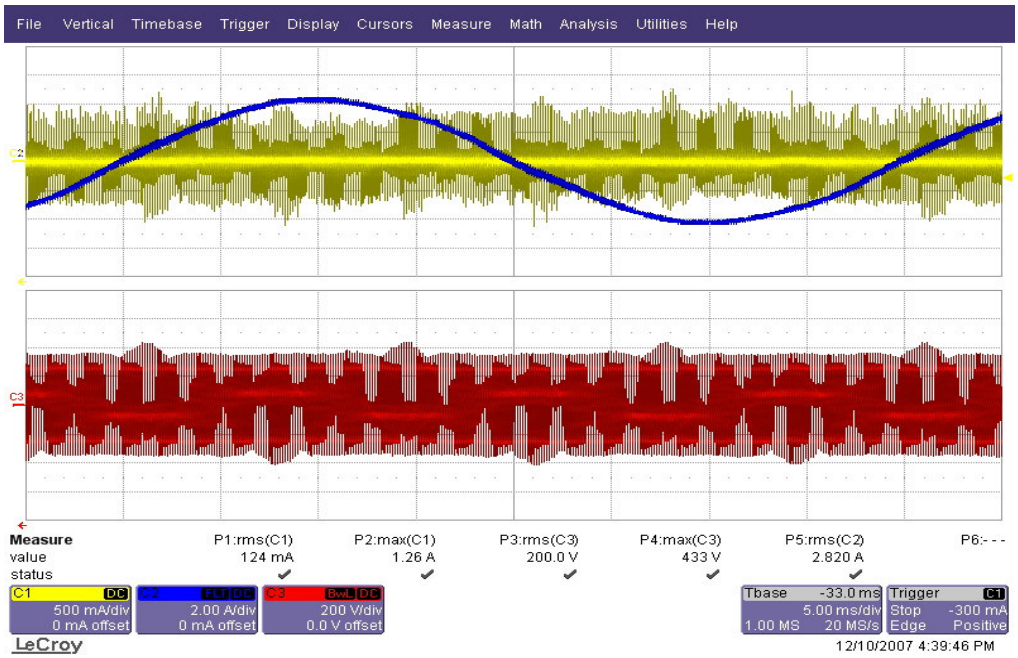


Figure 5.43 Phase current (blue), CMC (yellow), and CMV (red) waveforms for the commercial two-level VSI (M_i=0.4).

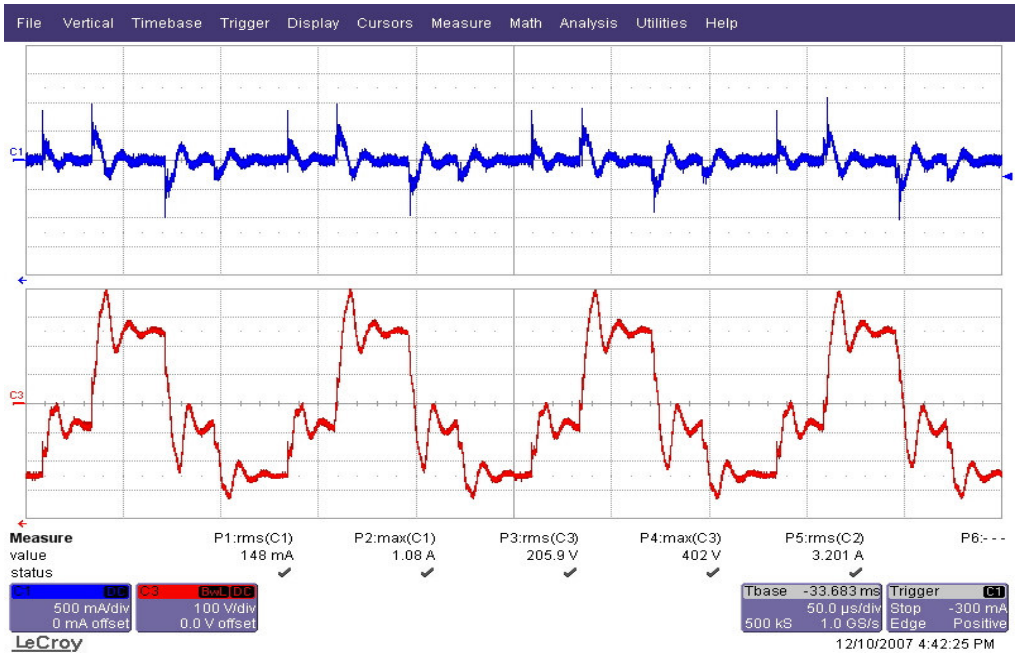


Figure 5.44 Zoom in CMC (blue) and CMV (red) waveforms for the commercial two-level VSI (M_i=0.4).

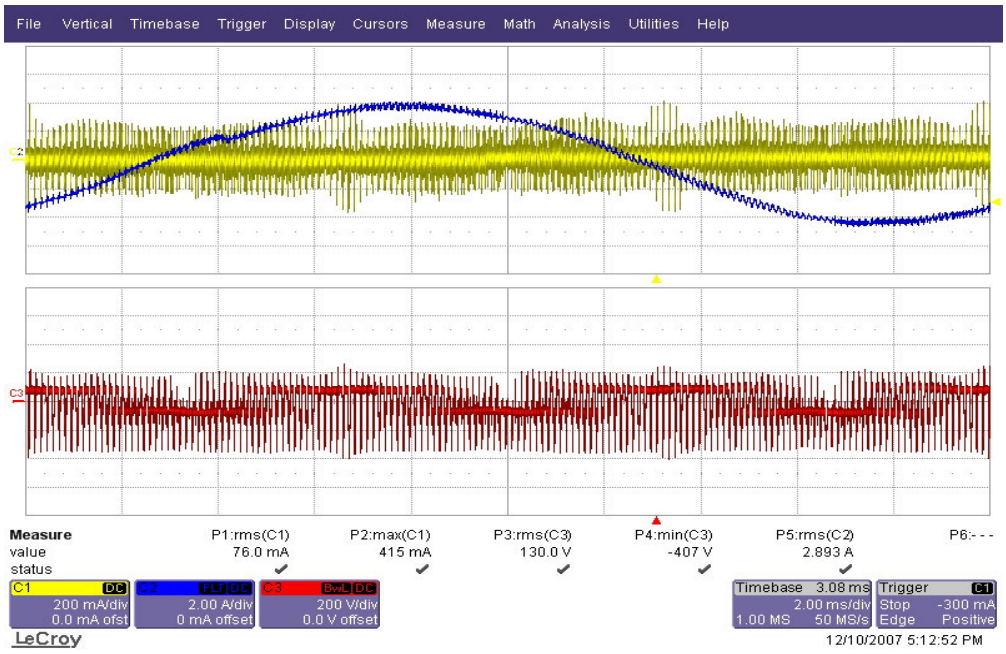


Figure 5.45 Phase current (blue), CMC (yellow), and CMV (red) waveforms for the commercial two-level VSI with CMI-2 (M_i=0.8).

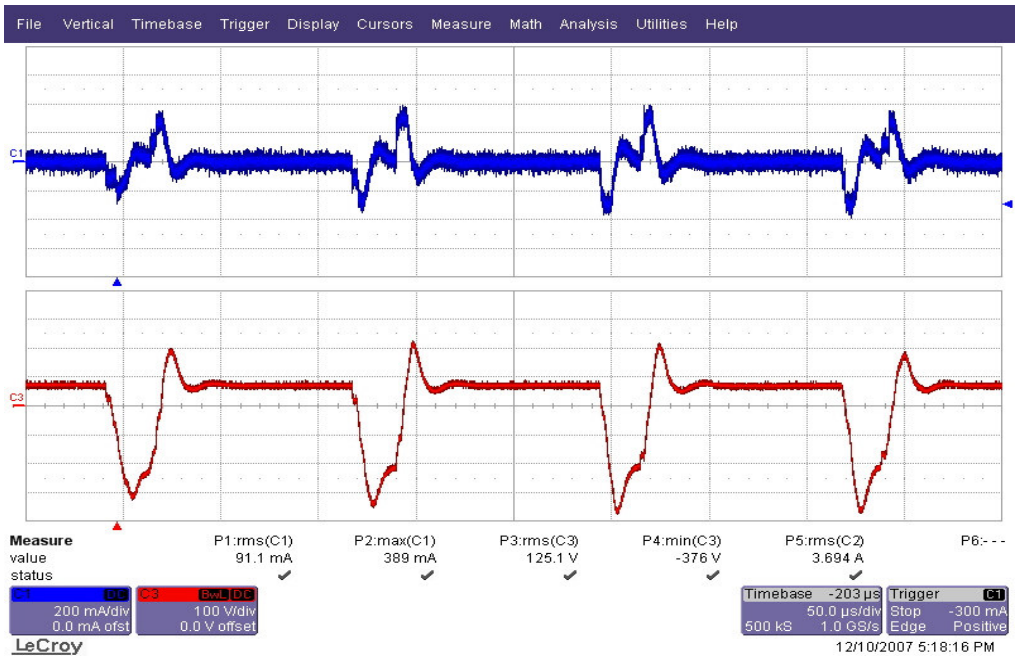
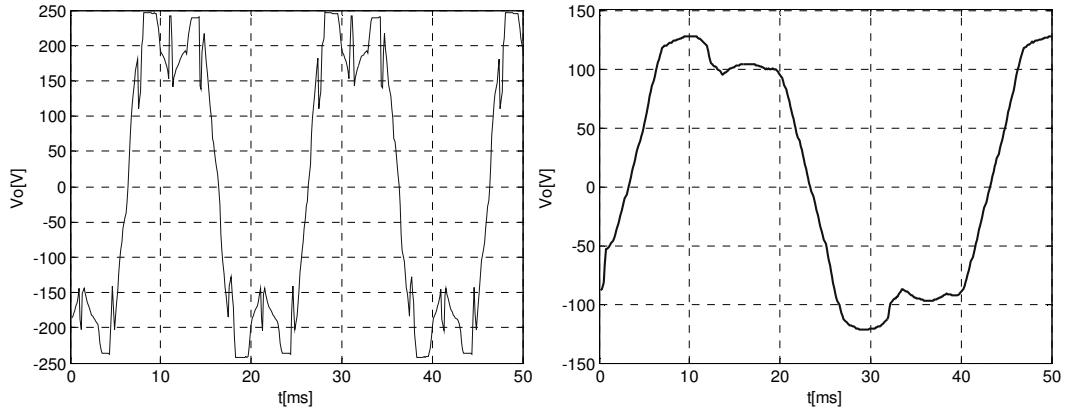


Figure 5.46 Zoom in CMC (blue) and CMV (red) waveforms for the commercial two-level VSI with CMI-2 (M_i=0.8).

5.6.2 CMV/CMC Experimental Results for The Commercial Three-Level NPC Inverter

In the three-level NPC VSI, the rate of change of CMV at the switching instants is reduced from $V_{dc}/3$ to $V_{dc}/6$ which corresponds to the half of that of the two-level inverter. Therefore, less CMC (especially peak CMC) is expected to be generated in the three-level NPC VSI. In order to observe the CMV/CMC performance of the three-level NPC VSI, a commercial VSI, Yaskawa Varispeed G7 is utilized. To identify the PWM method employed, the phase output to the DC bus midpoint voltage of the inverter is measured and processed similarly to the two-level case discussed in the previous section. The resulting PWM averaged output voltage waveforms are shown in Figure 5.47. According to the output voltage waveforms, the low modulation index range involves operation in the internal hexagon of the NPC voltage vector diagram and all switches are manipulated every PWM cycle. In the high modulation index range, however, modulation ceases in some of the phases depending on the voltage vector space angle. For example it is obvious from Figure 5.47 that in each phase and therefore inverter leg switching ceases several times, yielding a discontinuous modulation similar to DPWM1.



(a) (b)

Figure 5.47 The phase-to-midpoint output voltage (PWM average) of the three-level NPC VSI at a) M_i=0.8 b) M_i=0.4.

In order to obtain the detailed pulse pattern information of the NPC inverter, the inverter phase-to-midpoint voltages and the CMV are measured for two M_i levels, namely 0.35 and 0.7. Here the CMV is measured under the condition that the motor body is floating (electrically not connected to anything so that no CMC can flow). The measurement waveforms are shown in Figure 5.48 and 5.49 for M_i=0.7. The pulse pattern is a discontinuous PWM form of the NTV-PWM pattern shown in Figure 4.3. This is achieved by injecting a proper amount of zero sequence voltage to the phase references. The resulting CMV is also shown in the figures illustrating that it has a value less than $V_{dc}/2$ in magnitude. Thus, with the zero sequence signal injection not only the CMV is reduced but also the switching losses of the NPC inverter are reduced. For M_i=0.35, the output voltages and the CMV are shown in Figure 5.50 and Figure 5.51. The waveforms illustrate that the pulse pattern of the commercial inverter is exactly the same as the NTV pulse pattern at low M_i. In the oscillograms it is also obvious that the CMV takes the magnitude value of $V_{dc}/2$ frequently yielding a high CMV in this operating mode. Thus, it can be stated that the drive CMV characteristic changes as the operating point is changed.

Throughout the measurements of floating motor body tests the observed CMV waveforms are more rectangular than the measurements with the motor body connected to the supply ground via a cable. Since the motor body is floating, no CMC flow is possible and no voltage drop on the parasitic high frequency components of the motor occur. Thus, nearly rectangular waveforms, close to the theoretically predicted in Chapter 2 could be obtained. However, in practice the motor body is always connected to the supply ground for safety purposes. For this purpose the floating body waveforms are only considered for pulse pattern identification and will not be considered or discussed further.

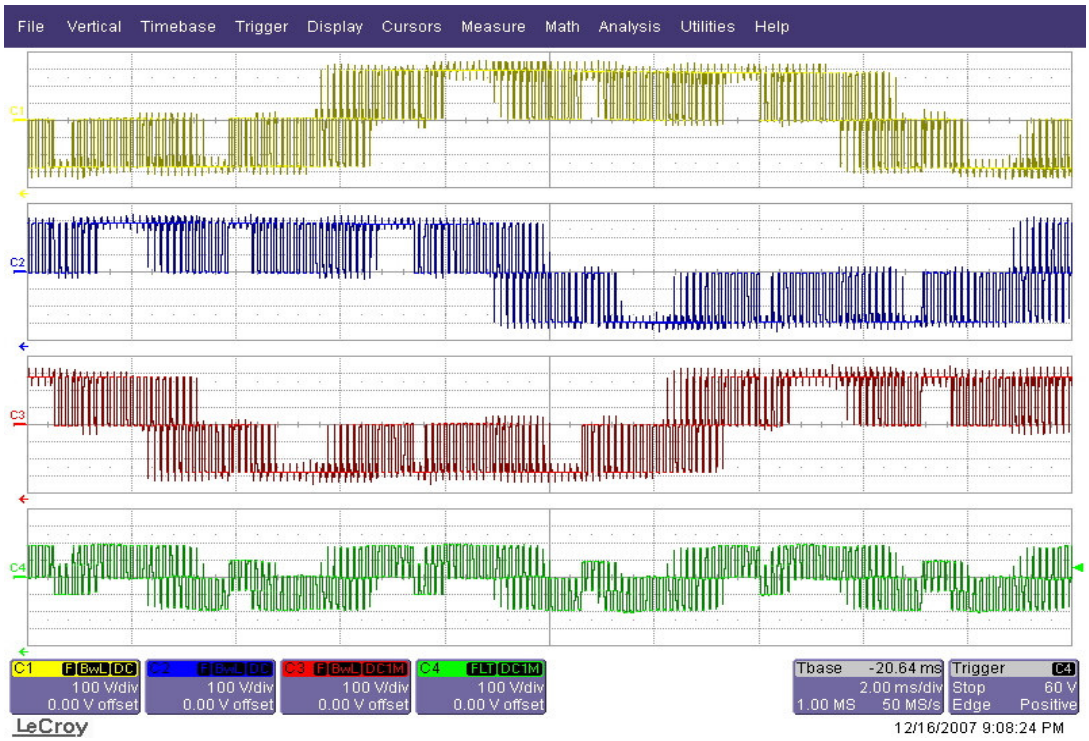


Figure 5.48 The phase-to-midpoint output voltages (top three) and the CMV (bottom) of the three-level NPC VSI at M_i=0.7.

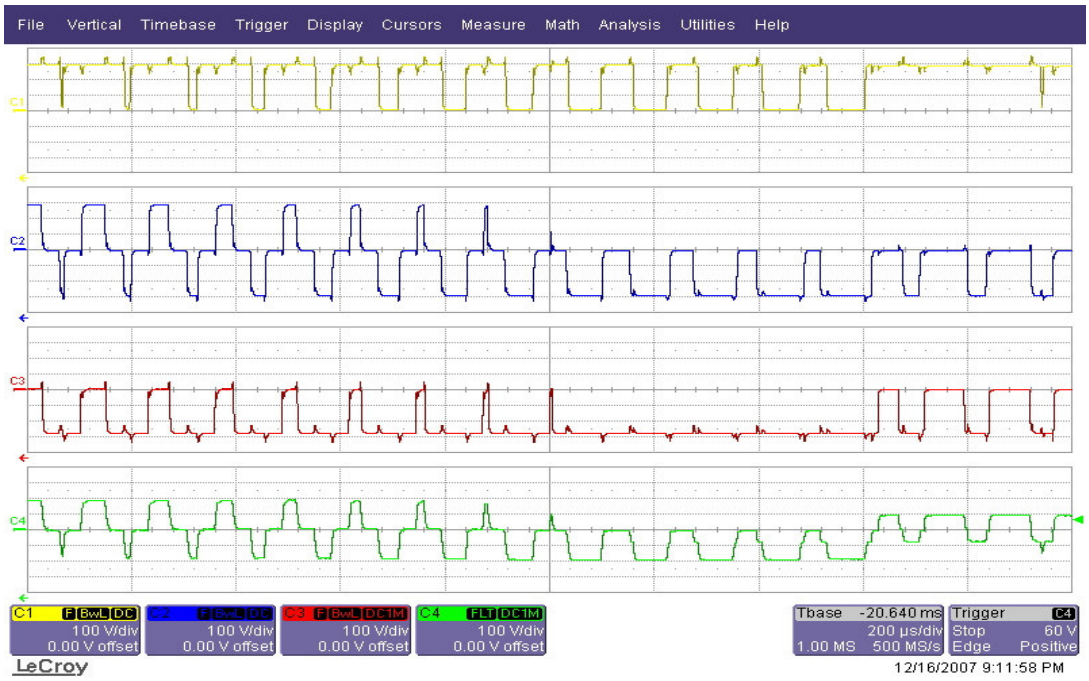


Figure 5.49 The zoom-in view of the phase-to-midpoint output voltages (top three) and the CMV (bottom) of the three-level NPC VSI at M_i=0.7.

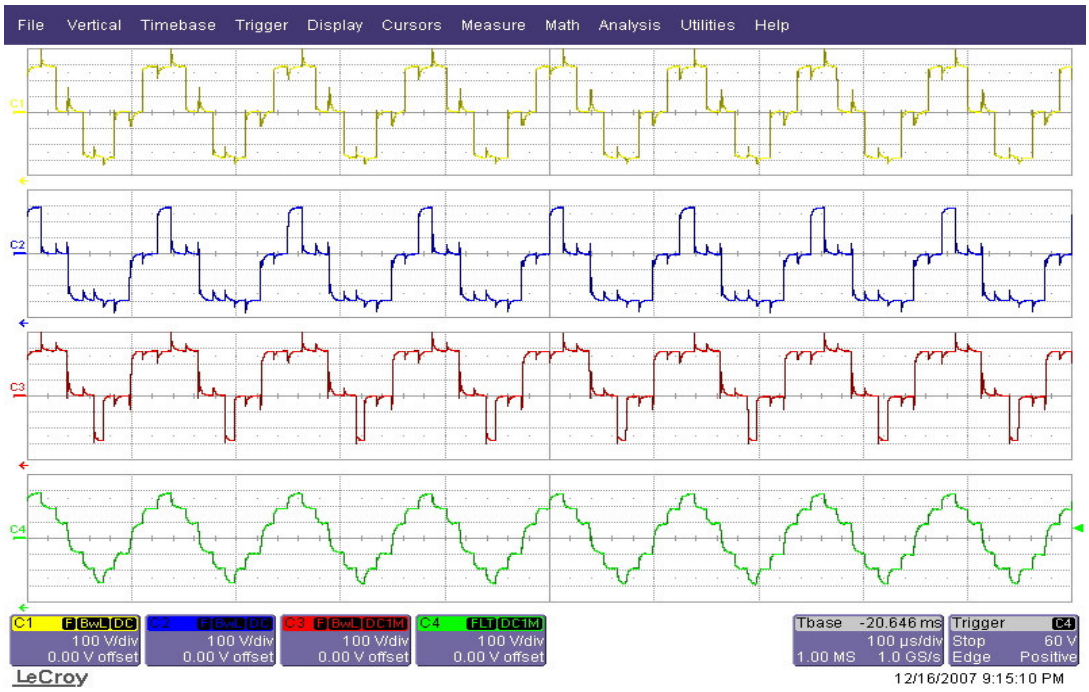


Figure 5.50 The phase-to-midpoint output voltages (top three) and the CMV (bottom) of the three-level NPC VSI at M_i=0.35.

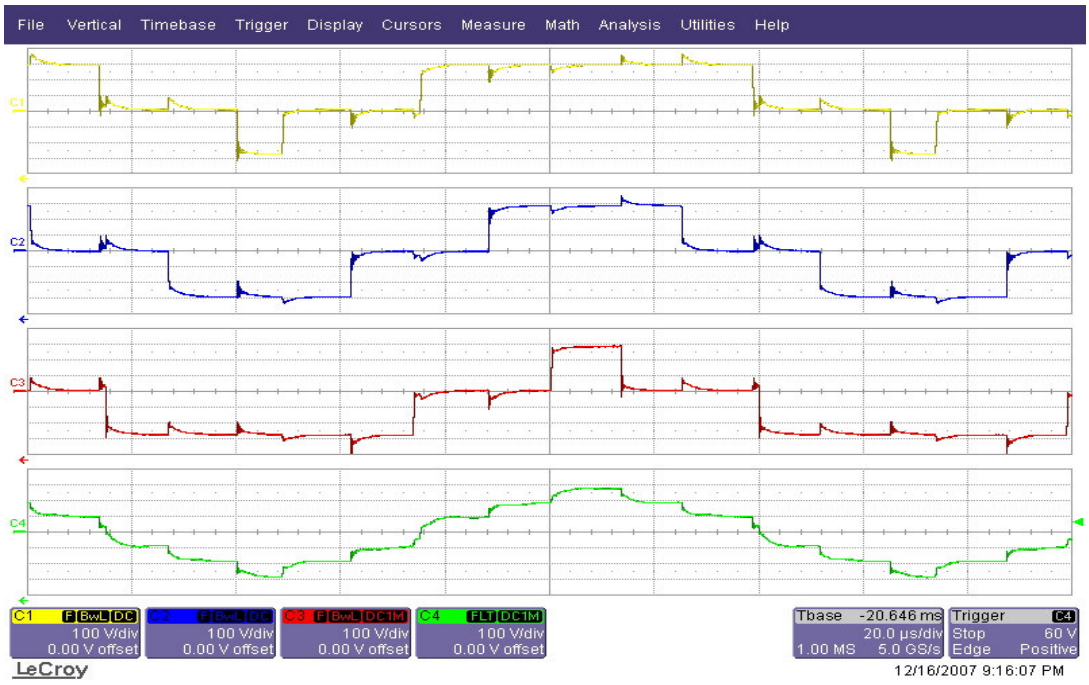


Figure 5.51 The zoom-in view of the phase-to-midpoint output voltages (top three) and the CMV (bottom) of the three-level NPC VSI at M_i=0.35.

Following the identification of the pulse pattern of the NPC inverter, the next step involves the experimental CMV/CMC performance investigation. The experimental results of the phase current, CMC, and CMV for three-level VSI are illustrated at Figure 5.52 for M_i=0.8. In the three-level VSI both rms and peak values of CMC are much lower than those of the two-level VSI. CMV performance is similar to that of the RCMV-PWM methods for the two-level VSI and it is much lower than the standard PWM methods of two-level VSI since the inverter does not utilize the zero voltage vectors at high M_i. In Figure 5.53 the microscopic view of the CMV/CMC waveforms are illustrated. The impulses over the CMC waveform have smaller magnitude in the three-level NPC VSI compared to two-level inverters. Similarly low dV_{no}/dt and low CMV magnitude result in less oscillating CMC with less rms value.

The experimental results of the phase current, CMC, and CMV for three-level VSI are illustrated at Figure 5.54 for M_i=0.4. At low M_i the inverter utilizes zero voltage vectors; therefore the CMV is high and comparable with the two-level VSIs when standard PWM methods are utilized. High CMC results in high rms CMC but the dV_{no}/dt is low the peak CMC is relatively lower and comparable with the two-level VSIs when RCMV-PWM methods are utilized. In Figure 5.55 the microscopic view of the CMV/CMC waveforms are illustrated. At this operation point the CMV waveforms have large magnitude however the impulses over the CMC have low magnitude.

To investigate CMV/CMC performance of the three-level VSI together with the passive CM filters, CMI-2 which was also tested together with two-level VSI is connected to the three-level VSI output and tests conducted. The experimental results of the phase current, CMC and CMV for three-level VSI are illustrated at Figure 5.56 for M_i=0.8 such that both peak and rms values of CMC are further reduced and they are less than those of CMC of all other mitigation methods tested in this thesis. CMV is low and similar to the case where CMI is not connected. Figure 5.57 illustrates the microscopic view of the CMV/CMC waveforms show oscillating characteristic of the CMC exists but the magnitude of the oscillating CMC is very low.

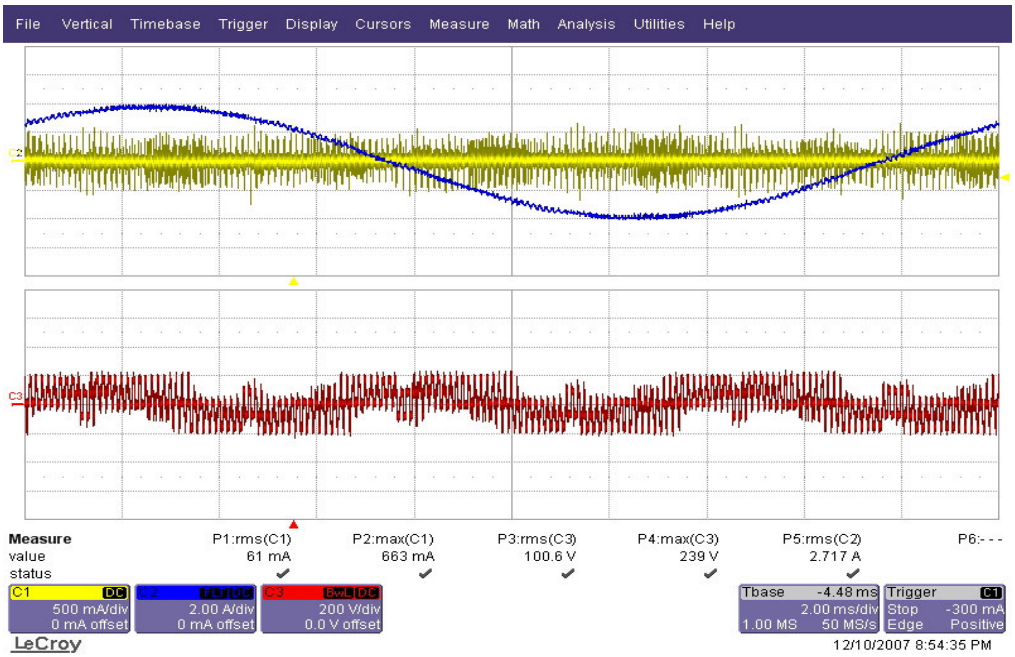


Figure 5.52 Phase current (blue), CMC (yellow) and CMV (red) waveforms for the commercial three-level NPC VSI (M_i=0.8).

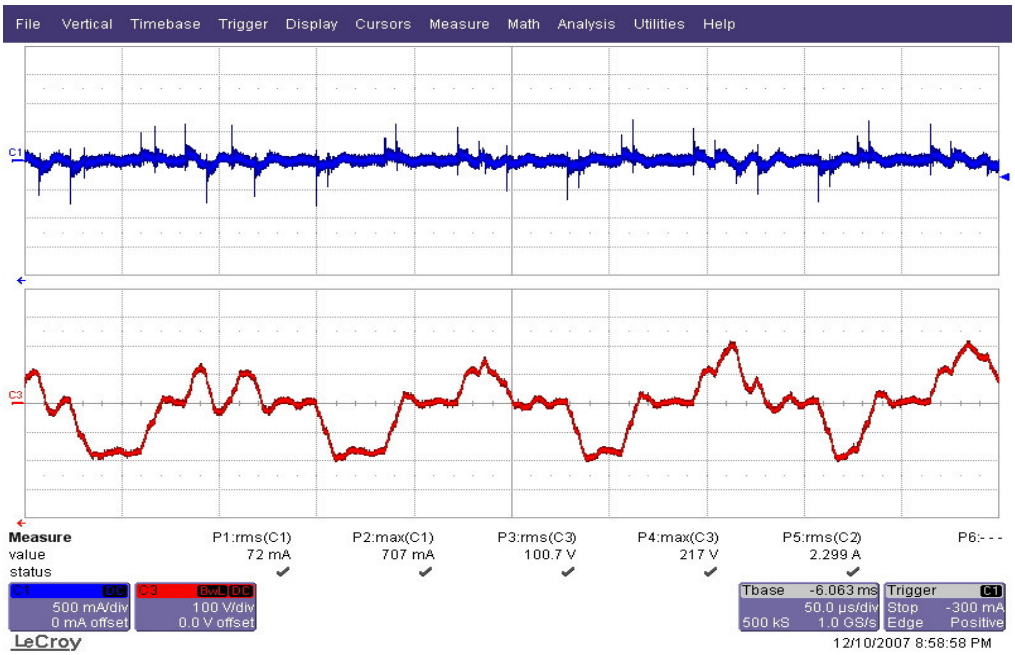


Figure 5.53 Zoom in CMC (blue) and CMV (red) waveforms for the commercial three-level NPC VSI (M_i=0.8).

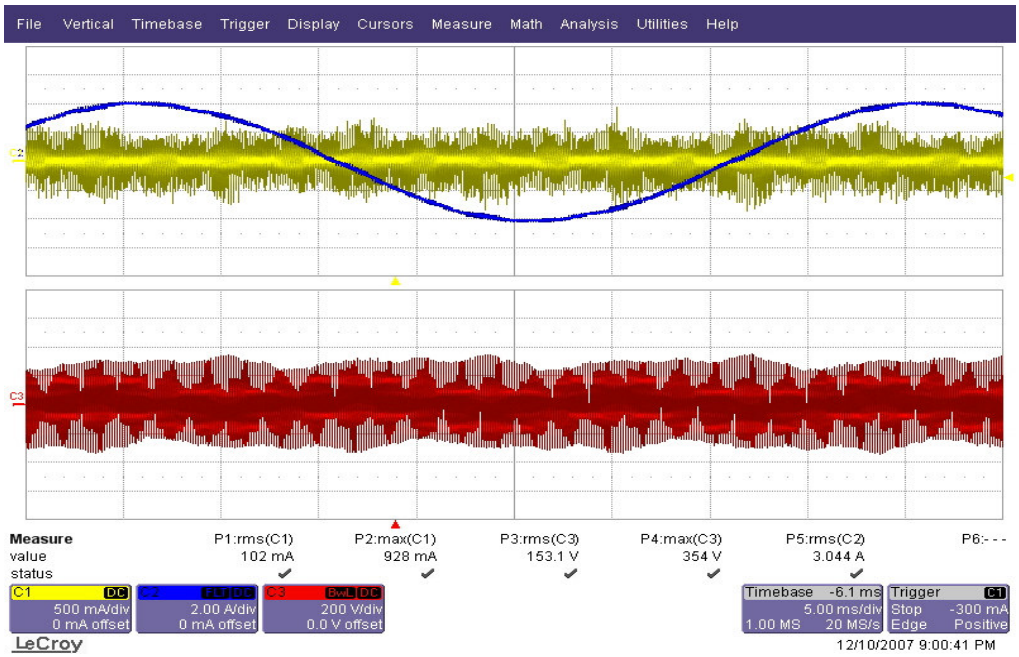


Figure 5.54 Phase current (blue), CMC (yellow) and CMV (red) waveforms for the commercial three-level NPC VSI (M_i=0.4).

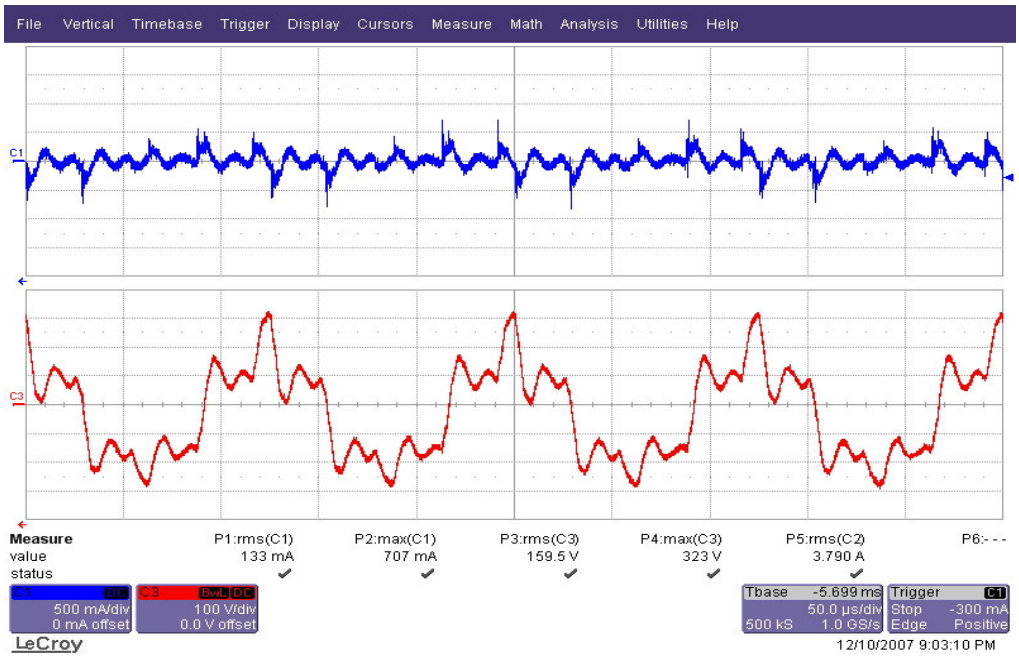


Figure 5.55 Zoom in CMC (blue) and CMV (red) waveforms for the commercial three-level NPC VSI (M_i=0.4).

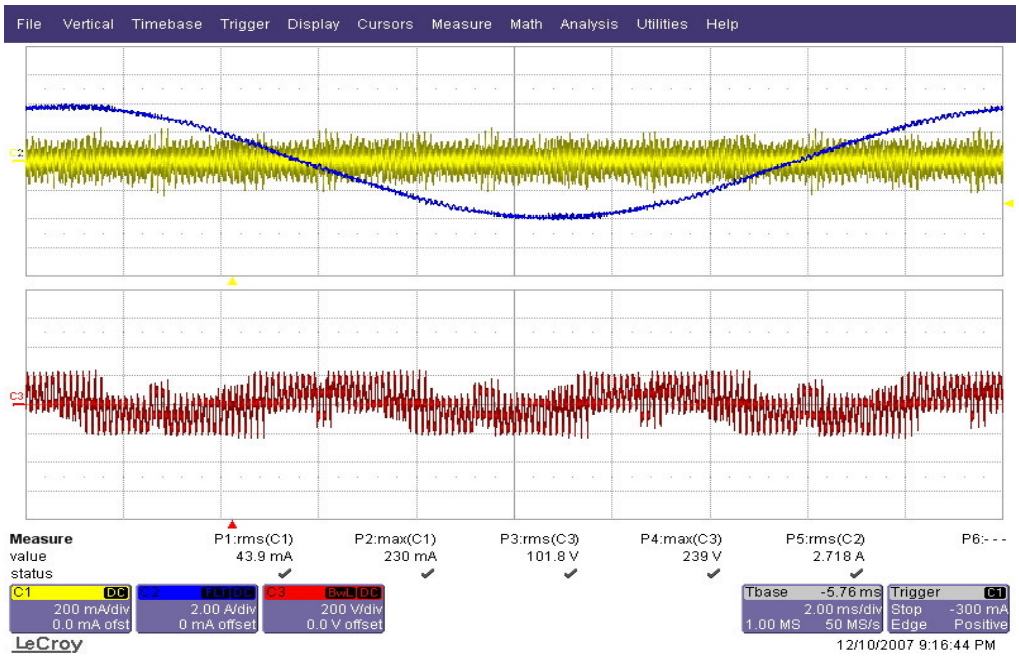


Figure 5.56 Phase current (blue), CMC (yellow) and CMV (red) waveforms for the commercial three-level NPC VSI with CMI-2 (M_i=0.8).

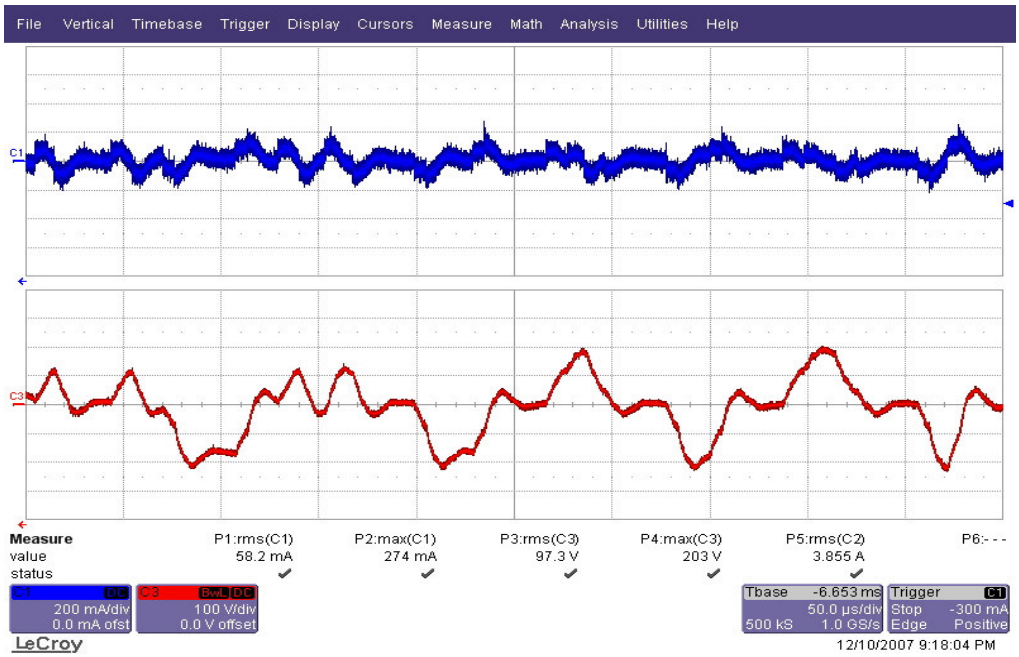


Figure 5.57 Zoom in CMC (blue) and CMV (red) waveforms for the commercial three-level NPC VSI with CMI-2 (M_i=0.8).

5.6.3 CMV/CMC Performance Evaluation of The Commercial VSIs

The experimental CMV/CMC measurement results of the commercial VSIs with their given PWM patterns and the prototype VSI when DPWM1 and NSPWM are utilized are tabulated in Table 5.9 with/without CMI-2 connected for M_i=0.8.

From the table it is observed that in the three-level NPC VSI and in the two-level VSI when NSPWM is utilized; the CMV is low and the CMV values are not effected whether CMI-2 is inserted or not. When CMI-2 is not included the three-level NPC inverter results the least peak and rms CMC due to the low CMV magnitude and low dv_{no}/dt. The two-level commercial VSI and the prototype VSI with DPWM1 modulation result in similar CMC and this CMC is higher than the prototype VSI with NSPWM. When CMI-2 is added to each VSI, the CMC (especially the peak CMC) is significantly reduced. However, the CMC performance ranking of the VSIs remains same such that three-level NPC results in the least CMC.

It is also worth mentioning that three-level NPC VSI without passive filters results in less rms CMC than the two-level VSIs even when both passive filters and PWM pulse pattern modification (NSPWM) are utilized. Therefore, these experiments show the close relationship between dv_{no}/dt and the rms CMC. On the other hand, utilizing a properly designed passive filter is more effective on CMC peak value reduction compared to only reducing the dv_{no}/dt by the inverter topology. Therefore, it is concluded that utilizing a three-level VSI significantly suppresses the CMC but utilization of passive CMI filters is still favorable and beneficial for the leakage current reduction purpose.

Also important is the economical consideration. From the perspective of cost optimization, a two-level inverter and a CMI cost significantly less than a three-level NPC inverter. With NSPWM yielding a significant CMV reduction, the CMI size becomes small and aid the filter size reduction. The small performance difference between the three-level NPC inverter without CMI and the two-level inverter with NSPWM supports this fact.

Table 5.9 CMV/CMC performance comparison of the commercial VSIs and the prototype VSI with/without CMI-2 for M_i=0.8

Filter type	Inverter type	CMV-Peak (V)	CMV-RMS (V)	CMC-Peak (A)	CMC-RMS (mA)
No filter	Prototype VSI with DPWM1	451	133	1.35	108
	Prototype VSI with NSPWM	212	92	0.950	95
	Commercial 2-Level VSI	424	132	1.30	100
	Commercial 3-Level VSI	239	100	0.663	61
CMI-2	Prototype VSI with DPWM1	442	137	0.460	80
	Prototype VSI with NSPWM	194	93	0.301	71
	Commercial 2-Level VSI	407	130	0.415	76
	Commercial 3-Level VSI	239	101	0.230	43

5.7 Experimental Investigation of The Motor Terminal Overvoltages In Long Cable Applications

In previous sections the CMV/CMC performance attributes of the considered PWM methods were investigated by means of laboratory experiments. In addition to the CMV/CMC performance, output line-to-line voltage waveform characteristic is another important characteristic that must be considered when evaluating the PWM methods. As explained in Chapter 2.5.4, PWM methods with bipolar output line-to-line voltage waveform pulse patterns are expected to have problems when there are

no or very little zero-voltage time intervals between the polarity reversals. These problems are peak voltage overshoots on the line-to-line voltages on the motor terminals and they arise when the motor and the VSI are connected via a long cable [6]. In order to observe these overshoots, long cable tests are performed in this section. During these experiments all of the motor and inverter parameters and the drive operating points are the same as those of the previous experiments. Additionally a 70m cable is inserted between the VSI and the induction motor and line-to-line voltage waveforms on the motor terminals are investigated at M_i=0.61 and M_i=0.8 for DPWM1, SVPWM, NSPWM and AZSPWM1.

The cable capacitance is measured between the line-to-line terminals of the cable for both the input and output while both ends are open-circuited. The measured value has been found as 6nF for the line-to-line capacitance value. The switching frequency is same as the previous experiments which are 6.6 kHz for SVPWM and AZSPWM1 and 10 kHz for DPWM1 and NSPWM. For comparison, the line-to-line voltage waveforms of the commercial two-level and three-level NPC VSIs are also investigated at 8 kHz switching frequency and 70m cable condition. To illustrate the waveform of the overshoots and their damping clearly, zoom-in line-to-line voltage waveforms are also provided at the worst cases for each condition. Since the theoretical analysis shows that the narrowest zero-voltage time intervals of NSPWM and AZSPWM1 occur at the edge of 60^o region boundaries, and the PWM other methods do not show space dependency, the expanded line-to-line voltage waveforms are illustrated at these points for all modulation methods.

In Figure 5.58 the line-to-line voltage waveform of DPWM1 is given together with its zoom-in view for M_i=0.8. DPWM1 has unipolar line-to-line voltage pulse pattern. However, in long cable applications, during each switching instant the line-to-line voltage makes an overshoot and starts oscillation. The peak of the oscillation is always similar and it is approximately 1 kV which is equal to twice of the DC bus voltage and the decay of this oscillation takes several microseconds. In Figure 5.59 the line-to-line voltage waveforms of SVPWM are given together with their zoom-in view for M_i=0.8. The line-to-line voltage waveforms resemble those of the DPWM1

such that during switching instants they make overshoots with magnitudes equal to 1 kV and the oscillation resulted by the overshoot decays. With the variation of M_i the line-to-line voltage pulse pattern characteristics do not change at all and the magnitude of the peak overshoots remain equal to 1 kV for SVPWM and DPWM1. Therefore, for these PWM methods the experimental results are provided for only M_i=0.8.

In Figure 5.60 the line-to-line voltage waveform of NSPWM is given together with its zoom-in view for M_i=0.61. As explained in Chapter 2.5.4 in detail, the line-to-line voltage pulse pattern of the NSPWM is bipolar for 120^o of the fundamental cycle and when M_i is close to 0.61, which corresponds to the lower voltage linearity range of NSPWM, the narrowest zero-voltage time available between the polarity reversals is very small. The experimental results support the theory, such that for M_i=0.61, peak overshoots reach 1.24 kV at the points where the zero-voltage time is not sufficient. Based on the experimental evaluation, it has been observed that when the zero-voltage time (t_z) value becomes less than 6μs, the overshoot during polarity reversal exceeds the $2V_{dc}$ value. This time interval is the minimum necessary amount for the transients to damp and the cable voltage to settle before the polarity reverses. The smaller the t_z, the higher the voltage overshoot amount. As can be seen from the zoom-in view of Figure 5.60, in the narrowest t_z case, the line-to-line voltage rises from $-V_{dc}$ to $+V_{dc}$ in a very short time interval resulting in a high voltage overshoot. However as M_i increases the narrowest zero-voltage time intervals between the polarity reversals get wider (t_z becomes larger than 6μs) and they are sufficient for the oscillations to damp. As Figure 5.61 illustrates, at M_i=0.8 the peak overshoots are limited to approximately 1 kV, which is equal to the largest overshoots observed at DPWM1 and SVPWM. From the zoom-in view of the line-to-line voltage waveform, even at the narrowest t_z point, there is sufficient interval is available for the oscillation to damp before another switching occurs (Figure 5.61).

In Figure 5.62 the line-to-line voltage waveform of AZSPWM1 is given together with its zoom-in view for M_i=0.61. AZSPWM1 has bipolar line-to-line voltage pulse pattern for 240^o of the fundamental cycle and the narrowest zero-voltage time

available between the polarity reversals is very narrow regardless of M_i. As seen from the experimental results for M_i=0.61, the peak voltage overshoots reach 1.35 kV at the points where the zero-voltage time is not sufficient ($t_z << 6\mu s$). As seen from the zoom-in view to the narrowest t_z case, the line-to-line voltage rises from $-V_{dc}$ to $+V_{dc}$ in a very short time interval resulting in very high voltage overshoot. Similarly at M_i=0.8 peak overshoots reach 1.37 kV as seen from Figure 5.63 since there is still no sufficient t_z available between the polarity reversals.

In Figure 5.64 the line-to-line voltage waveform of the commercial two-level VSI is given together with its zoom-in view for M_i=0.8. The inverter utilizes standard PWM methods with unipolar line-to-line voltage pulse pattern. Therefore the output line-to-line voltage waveform of the commercial two-level VSI is very similar to those of DPWM1 and SVPWM and the peak overshoots are limited to approximately 1 kV. In Figure 5.65 the line-to-line voltage waveform of the commercial three-level NPC VSI is given together with its zoom-in view for M_i = 0.8. The three-level NPC VSI has five line-to-line voltage levels. Therefore, ΔV_{ll}=250V (V_{dc}/2) in 500V DC-bus voltage applications. Due to this characteristic, line-to-line voltage overshoots are smaller in this type of inverter. During the switching instants, oscillations occur with a magnitude of approximately ΔV_{ll}=250V. When the output line-to-line voltage rises from 250V to 500V, due to the oscillations the peak line-to-line voltage reaches 800V. Thus, the NPC inverter is a superior topology in terms of its voltage overshoot limiting characteristics compared to the two-level inverter.

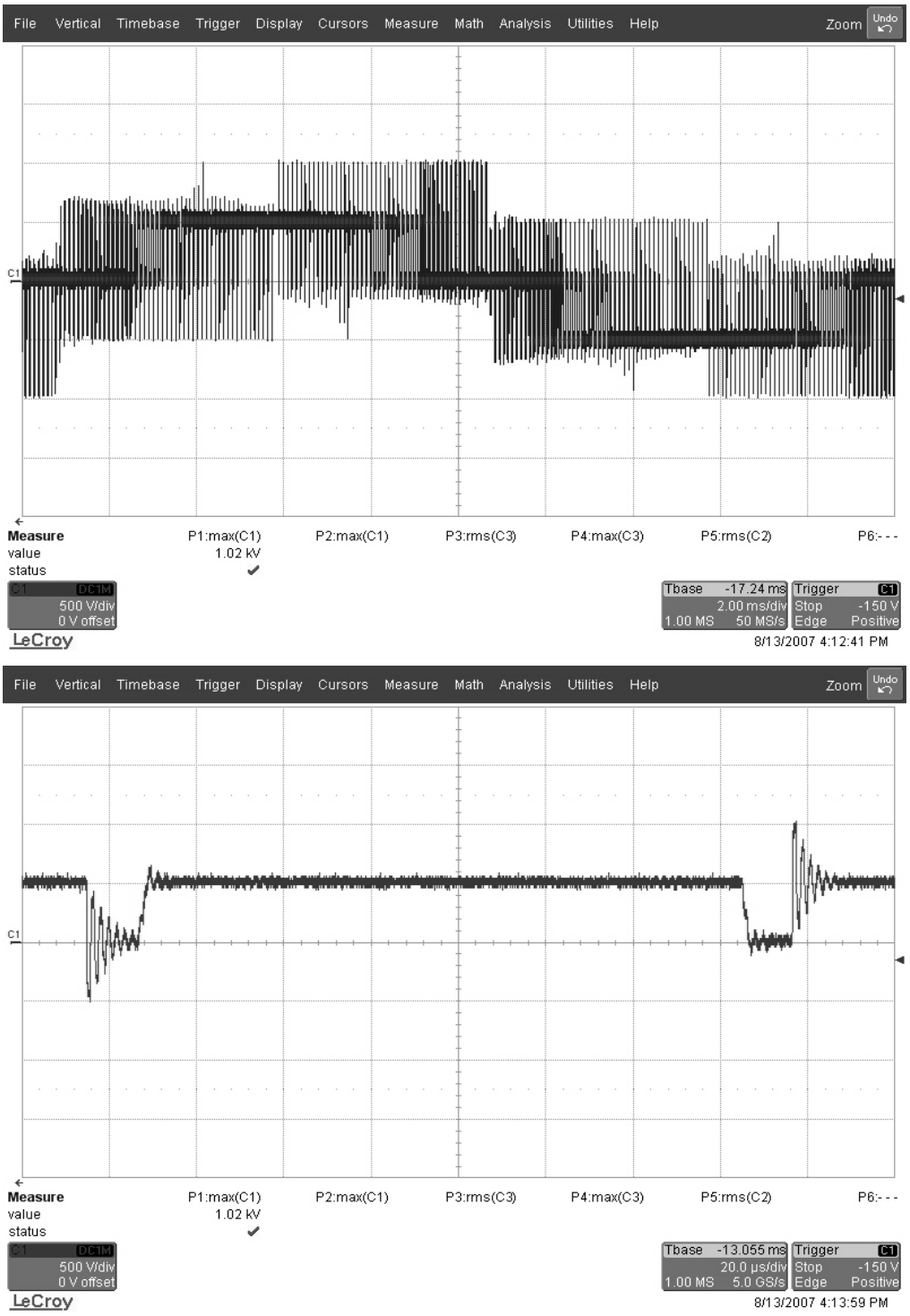


Figure 5.58 Line-to-line voltage waveform of DPWM1 (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.8 and 70m cable.

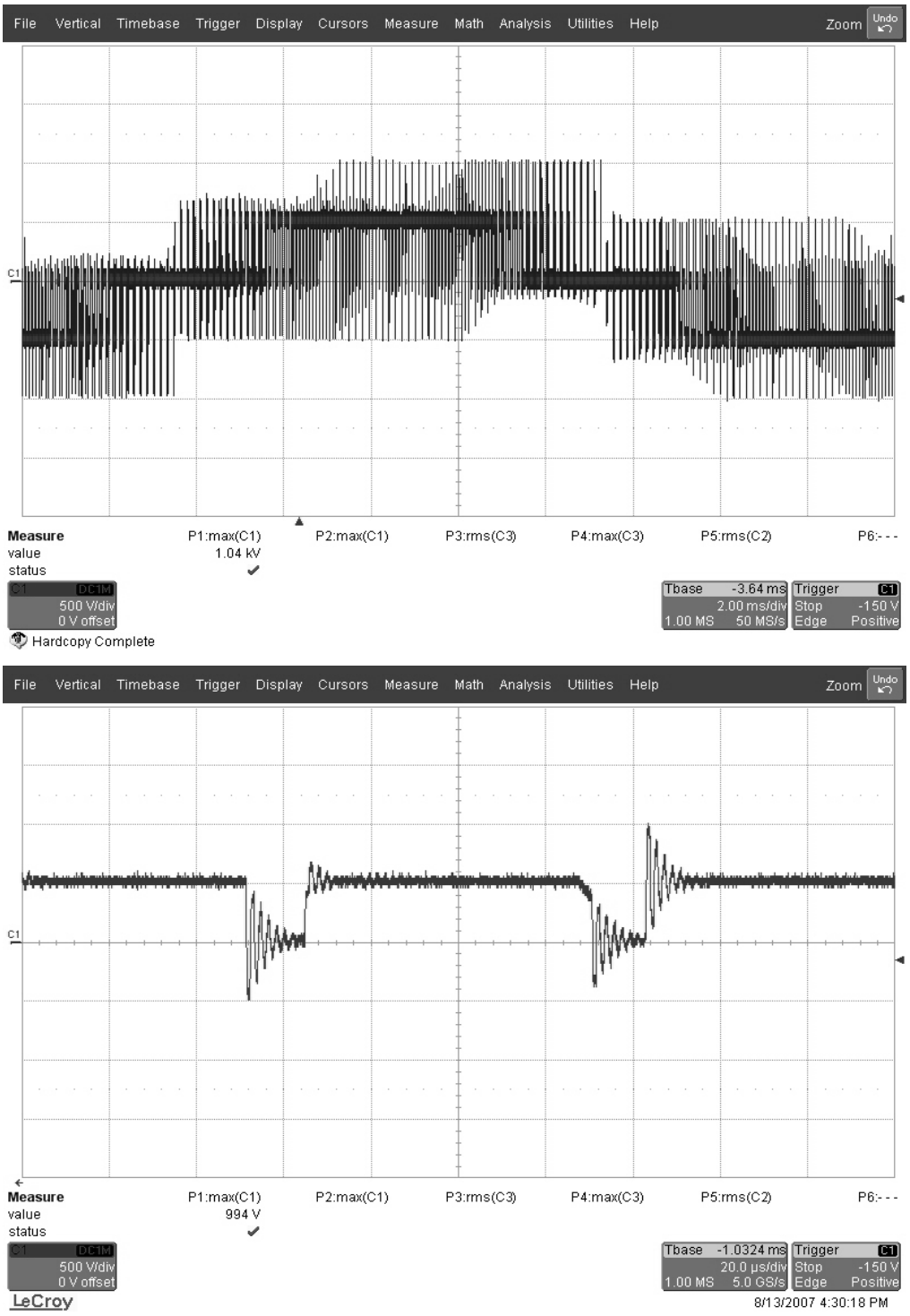


Figure 5.59 Line-to-line voltage waveform of SVPWM (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.8 and 70m cable.

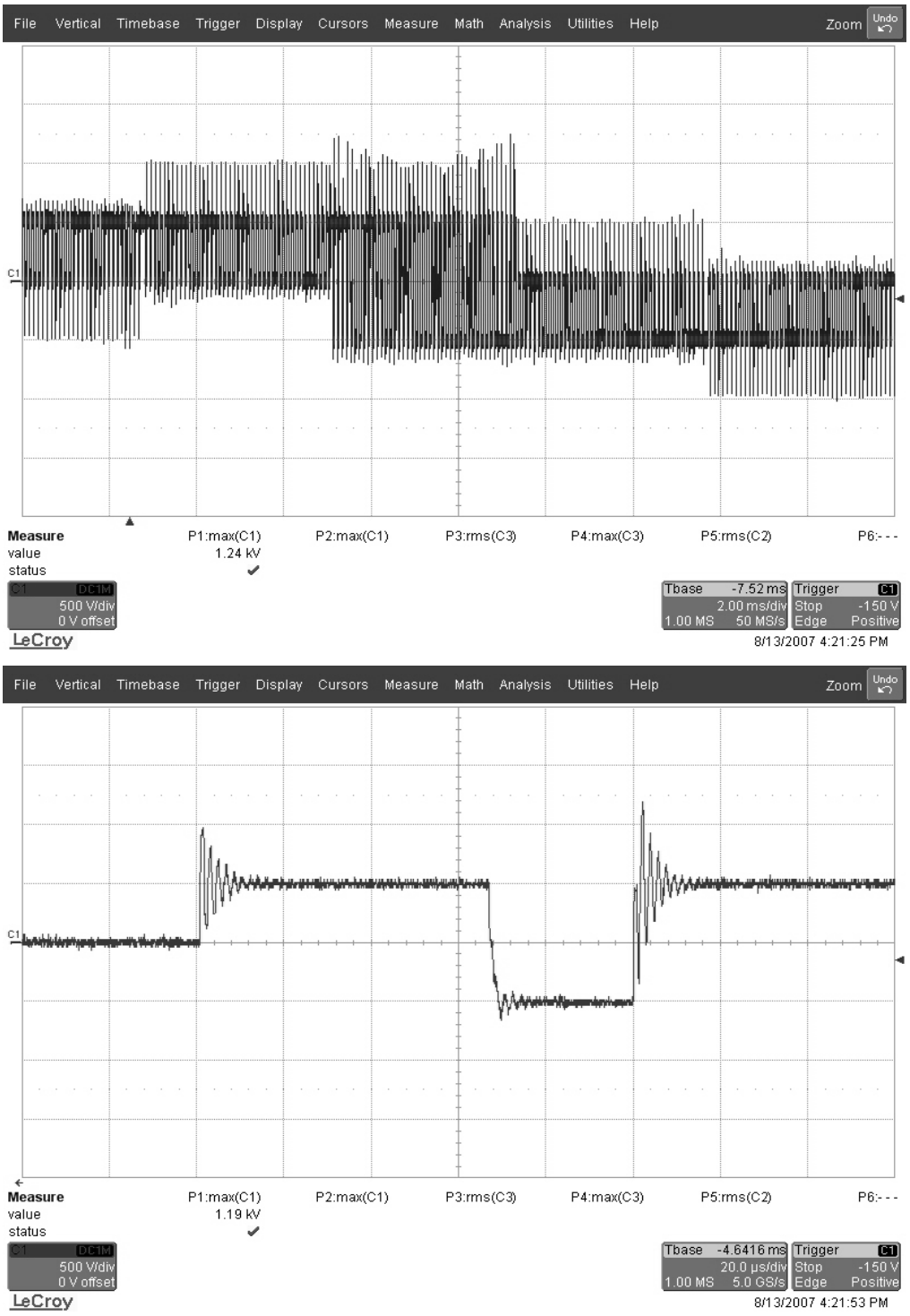


Figure 5.60 Line-to-line voltage waveform of NSPWM (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.61 and 70m cable.

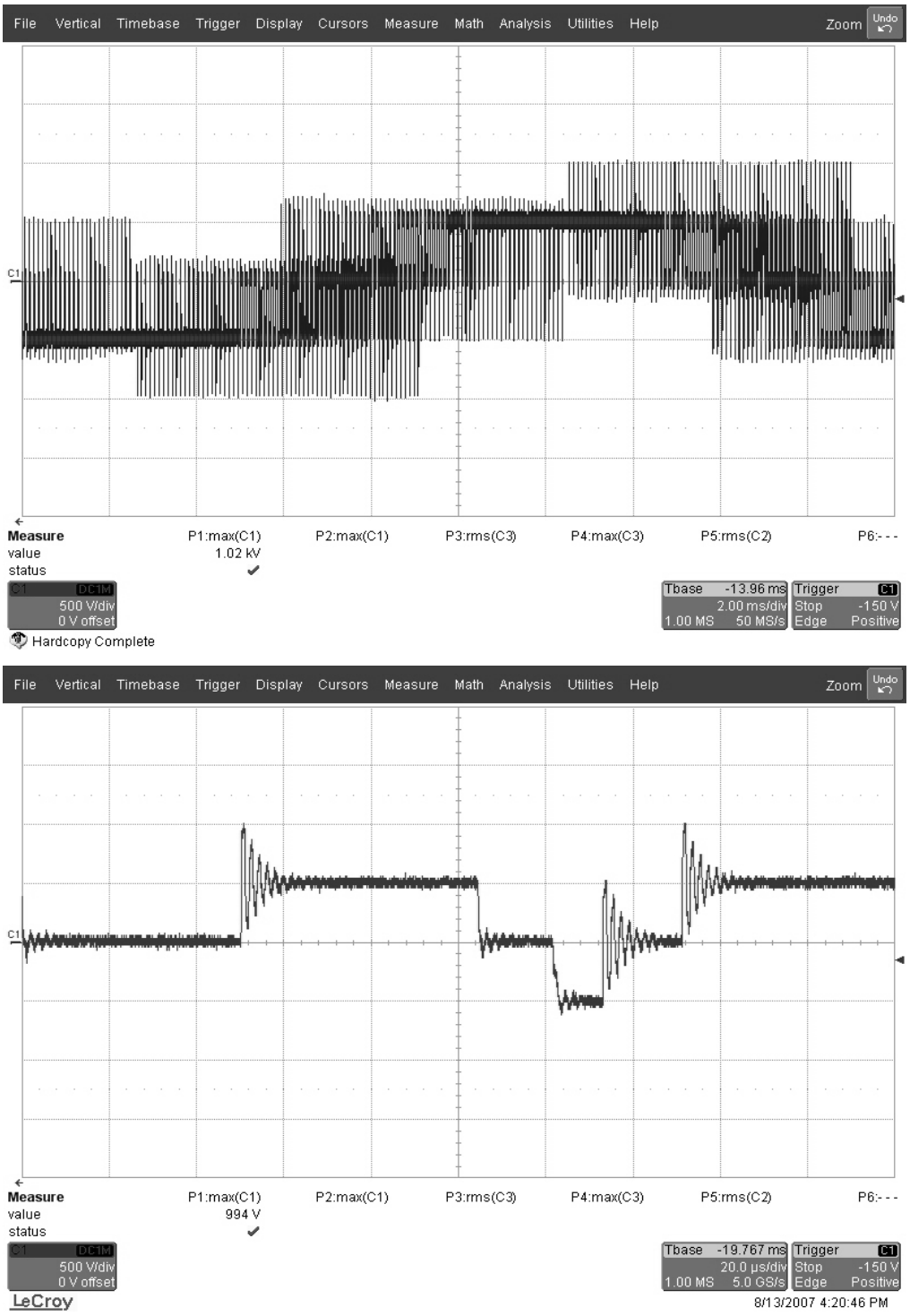


Figure 5.61 Line-to-line voltage waveform of NSPWM (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.8 and 70m cable.

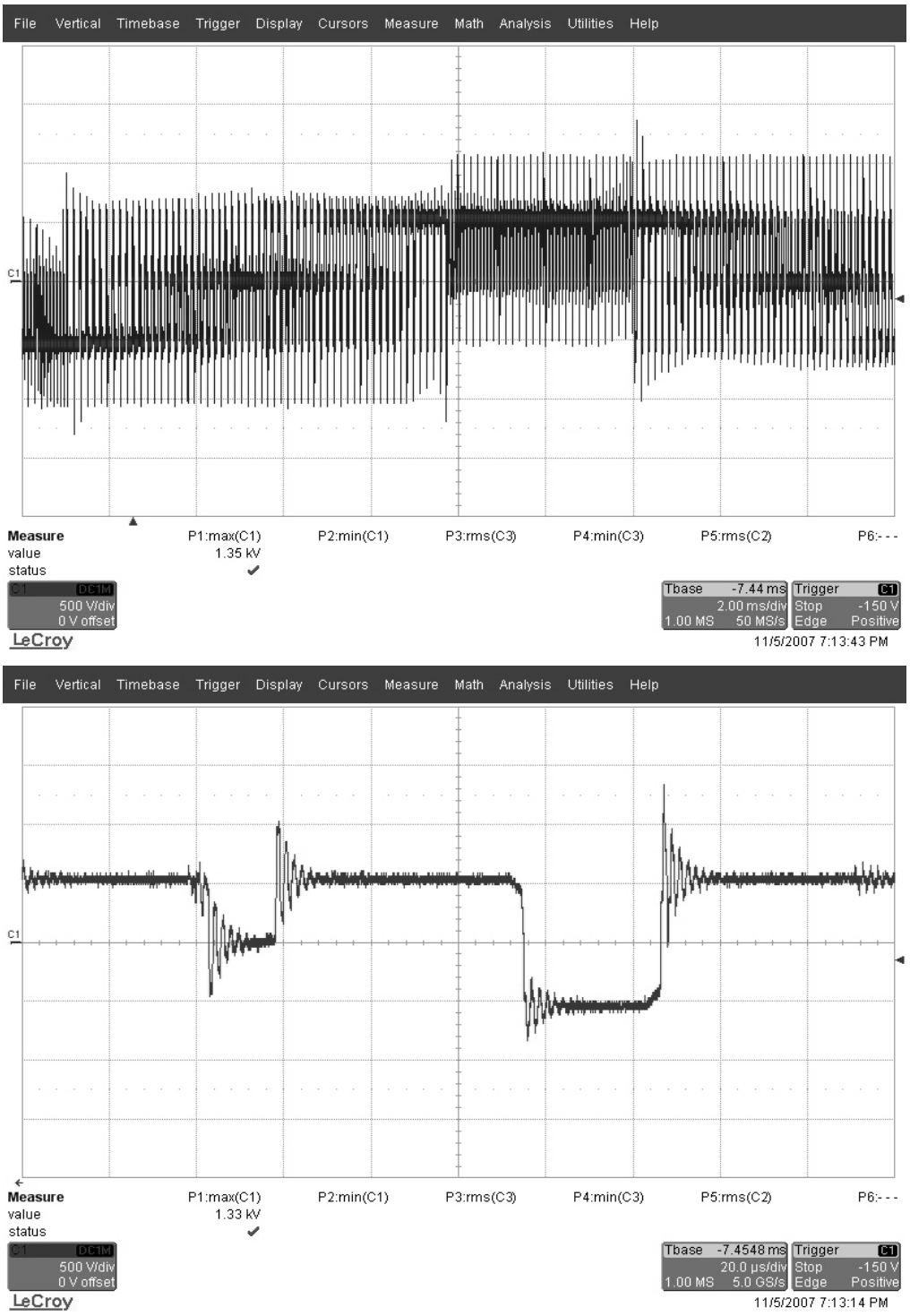


Figure 5.62 Line-to-line voltage waveform of AZSPWM1 (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.61 and 70m cable.

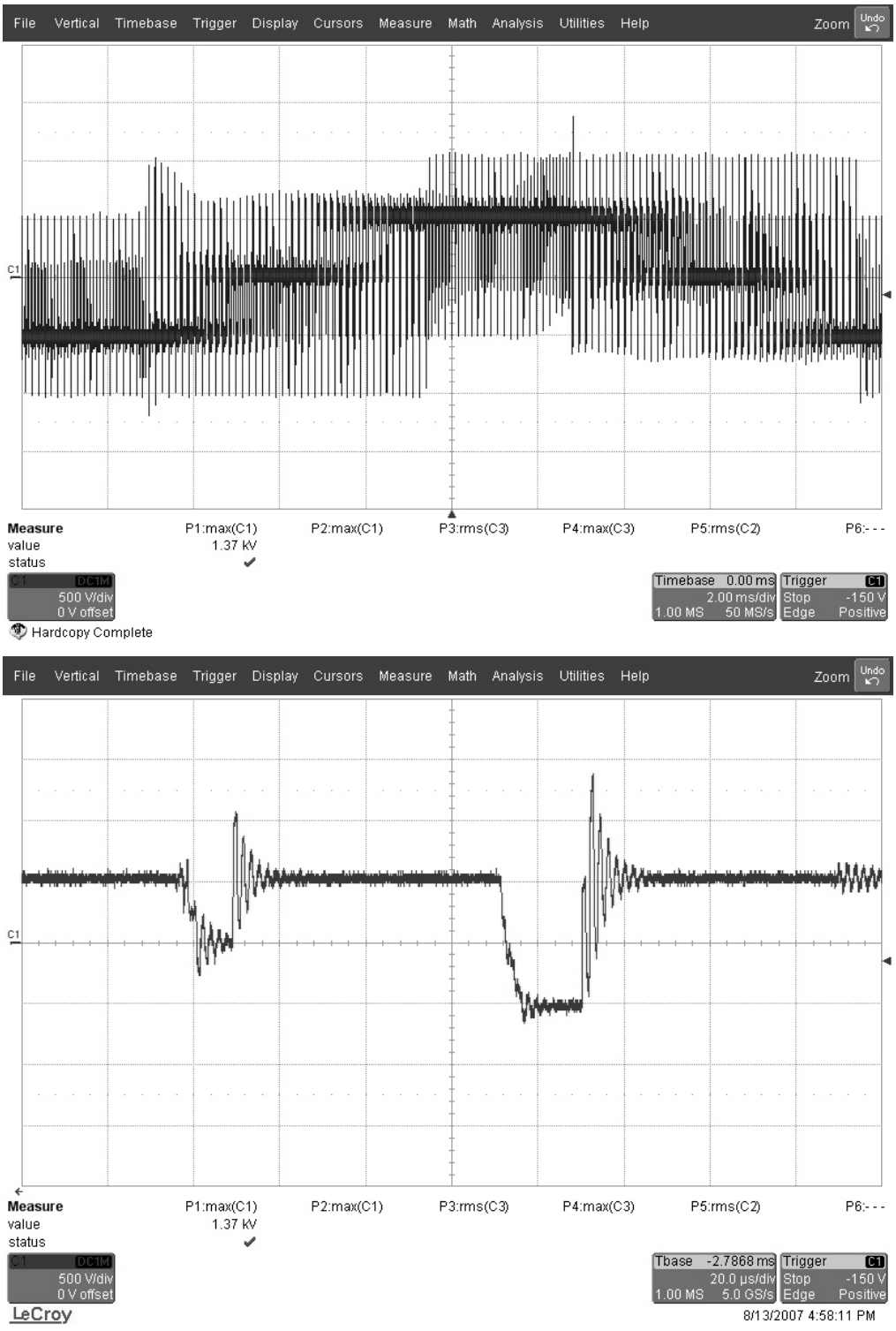


Figure 5.63 Line-to-line voltage waveform of AZSPWM1 (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.8 and 70m cable.

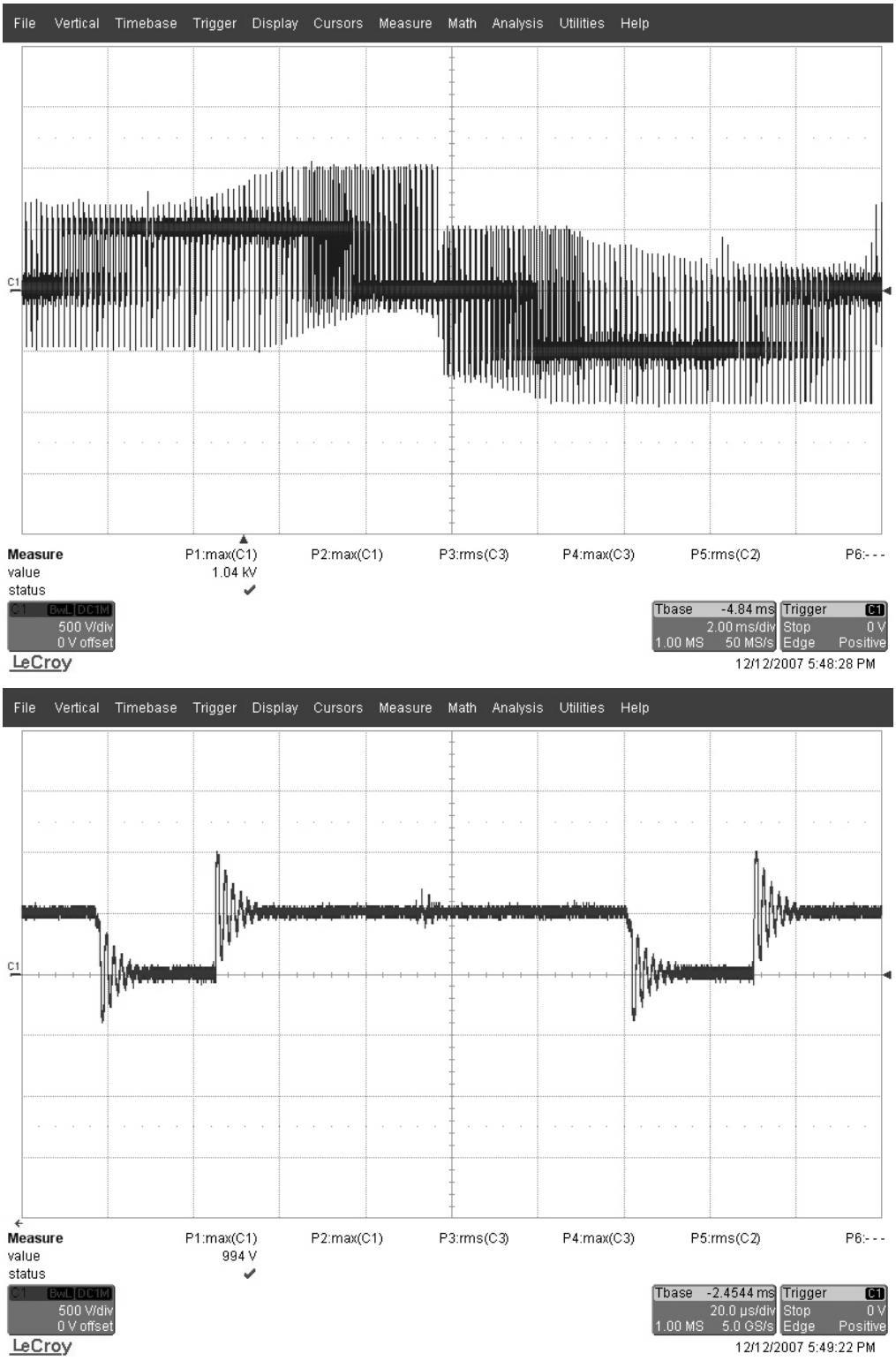


Figure 5.64 Line-to-line voltage waveform of the commercial two-level VSI (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.8 and 70m cable.

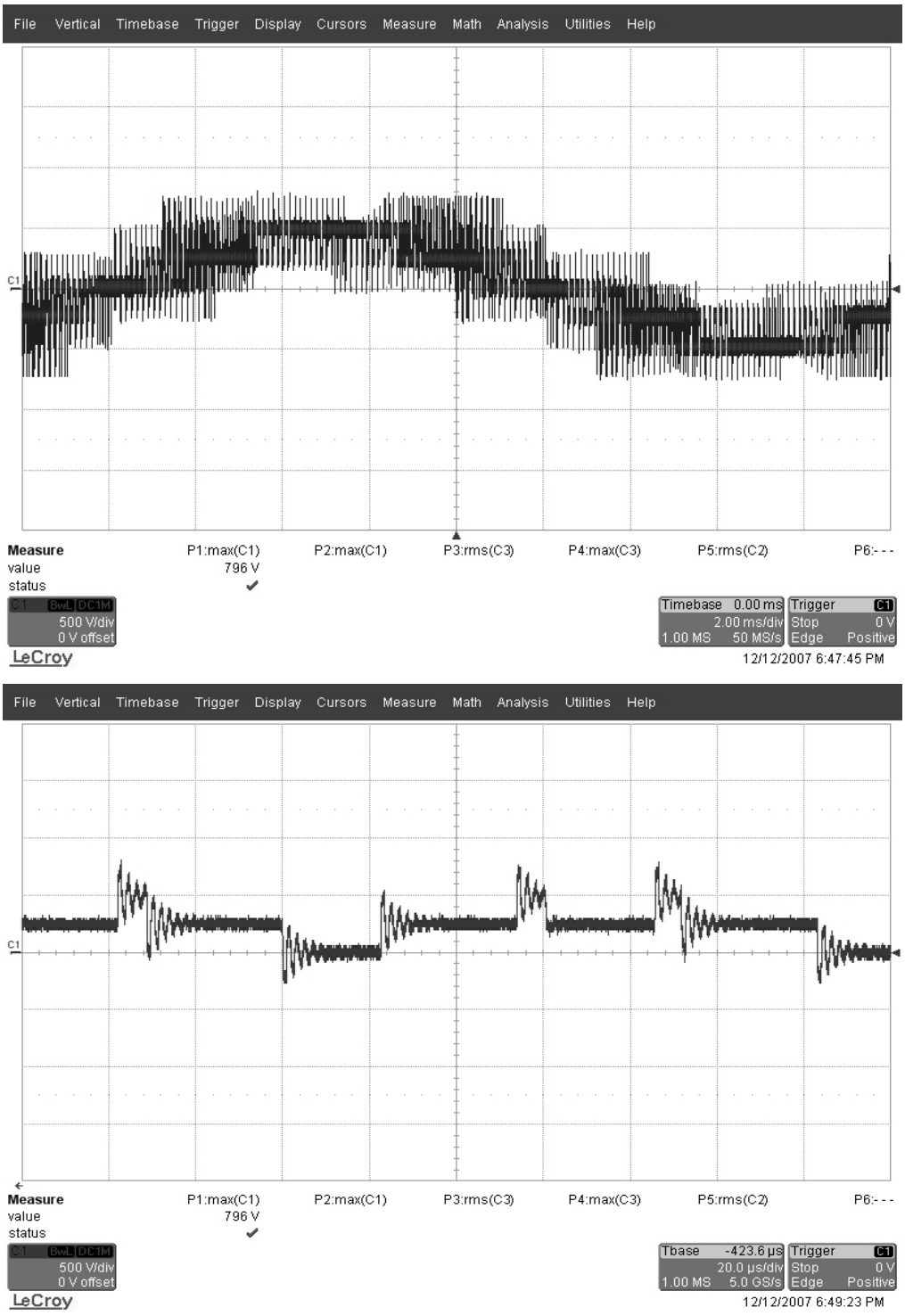


Figure 5.65 Line-to-line voltage waveform of the commercial three-level NPC VSI (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.8 and 70m cable.

The output line-to-line voltage waveforms are also investigated when a short cable with a length of 2m is inserted between the motor and the inverter instead of the long cable. Additionally to investigate the effects of utilization of CMI on the line-to-line voltage waveforms, the line-to-line voltage overshoot tests are repeated when CMI-2 is connected with short (2m) and long cables (70m). Further, the CMV/CMC characteristics of the drive when the 70m cable is utilized are investigated experimentally. During these tests, waveforms of various PWM methods have been investigated. SVPWM, DPWM1, NSPWM, and AZSPWM1 were all tested and for the 2m cable all have exhibited similar behavior. For the purpose of illustration, SVPWM and AZSPWM1 results are reported.

In Figure 5.66 the zoom-in view of the line-to-line voltage waveform of SVPWM is given for M_i=0.8 when the motor is connected to the VSI via a short cable of 2m. It is observed that during the switching instants the line-to-line voltage rises to 566V which is slightly above the DC-bus voltage of 500V. These overshoots are vector space independent and occur at each switching transient with similar magnitudes and they have no practical disadvantage since they are not high enough to result in insulation breakdown. In Figure 5.67 the zoom-in view of the line-to-line voltage waveform of the AZSPWM1 is illustrated during polarity reversal with the narrowest zero-voltage time. In long cable applications these points (narrow zero-voltage time) are very problematic, and result in much more higher overshoot than the sufficient zero-voltage time case. However, in short cable applications, instantaneous polarity reversals result in overshoots of comparable magnitude with those generated with long cable when there is sufficient zero-voltage time. In this experiment, the peak line-to-line voltage is measured as 583V. This is due to the very small cable capacitance and as a result very fast damping characteristic of the oscillation such that even a very narrow zero-voltage time is practically sufficient for these oscillations to damp.

In Figure 5.68 and Figure 5.69 the zoom-in view of the line-to-line voltage waveforms of SVPWM and AZSPWM1 are given respectively for M_i=0.8 when the CMI-2 is inserted in the short cable application. It is observed that for both PWM

methods overshoots occur over line-to-line voltages at the motor terminals. The peak line-to-line voltages are 820V for both PWM methods. These experiments show that CMIs result in voltage rise over the line-to-line voltages. These voltage rises are as a result of the CMI-2 parasitic capacitance and the added differential inductance of the CMI. However, these voltage rises are independent of the zero-voltage time between polarity reversals. Additionally the oscillations damp faster than the oscillations resulting in long cable tests and their oscillation frequencies are much higher. Again this result is a consequence of the fact that the short cable and CMI-2 have significantly smaller capacitance than the long cable.

In Figure 5.70 and Figure 5.71 the zoom-in view of the line-to-line voltage waveforms of SVPWM and AZSPWM1 are given respectively for M_i=0.8 when the CMI-2 is inserted in the long cable application. In the experiment, CMI-2 is placed near the motor and the 70m cable is inserted between the inverter and CMI-2 input terminals. Although in short cable operations the CMI results in voltage rise on the line-to-line voltage waveform, in the long cable test the CMI does not affect the line-to-line voltage waveform. It is observed that the overshoots due to the long cable are dominant and peak overshoots are measured as 1.06 kV for SVPWM and 1.28 kV for AZSPWM1. These peak overshoots are very similar to those when long cable is inserted with no CMI. This is due to the fact that the CMI does not affect the differential mode parasitics significantly. The added parasitic capacitance and inductances due to the CMI are negligible. Thus, the overshoots with the long cable and CMI-2 are the same as without CMI-2. In an experiment the location of CMI-2 and the cable were replaced and the test repeated and practically the same results were obtained. Since CMI-2 can not suppress overvoltages, the cable created overvoltages directly appear at the motor terminals without attenuation, regardless the location of CMI-2.

Finally, to observe the effect of the long cable between the VSI and the motor on the CMV/CMC, the CMV/CMC waveforms are investigated for various PWM methods at M_i=0.8. The experimental results of the phase current, CMC, and CMV for DPWM1 and NSPWM are illustrated at Figures 5.72 and 5.73 respectively. When

the long cable is inserted, the CMV remains similar as the short cable application. Similarly the peak CMC is unchanged however the rms value of the CMC increases with inserting long cable. The rms CMC of the DPWM1 is 147 mA and that of NSPWM is 131 mA. The increase of the capacitance due to the cable reduces the impedance at the CMV frequencies and results in CMC increase. These rms CMC increments are similar for all PWM methods and they correspond to an increment of approximately 30%. Therefore, the results of other PWM methods are not illustrated.

In order to summarize all line-to-line voltage experimental results, the maximum measured peak line-to-line voltages of the prototype VSI with various PWM methods and the commercial VSIs are tabulated in Table 5.10 for various connection configurations at M_i=0.8. It is observed that the short cable results in very little overshoots and when CMI-2 is inserted these overshoots increase. However, the highest overshoots are observed in the long cable tests. In long cable applications the peak voltage overshoots do not get affected significantly whether a CMI is inserted at the motor terminals or not. In short cable applications the performance of all PWM methods of the prototype VSI are similar to each other. In short cable applications with no CMI, the overshoots of the commercial VSIs are higher than those of prototype VSI. For all operating conditions other than the short cable applications with CMI-2; the three-level NPC inverter results in less V_{ll} peak compared to two-level VSIs due to its lower voltage step change. The two-level commercial VSI performs similarly with the prototype VSI.

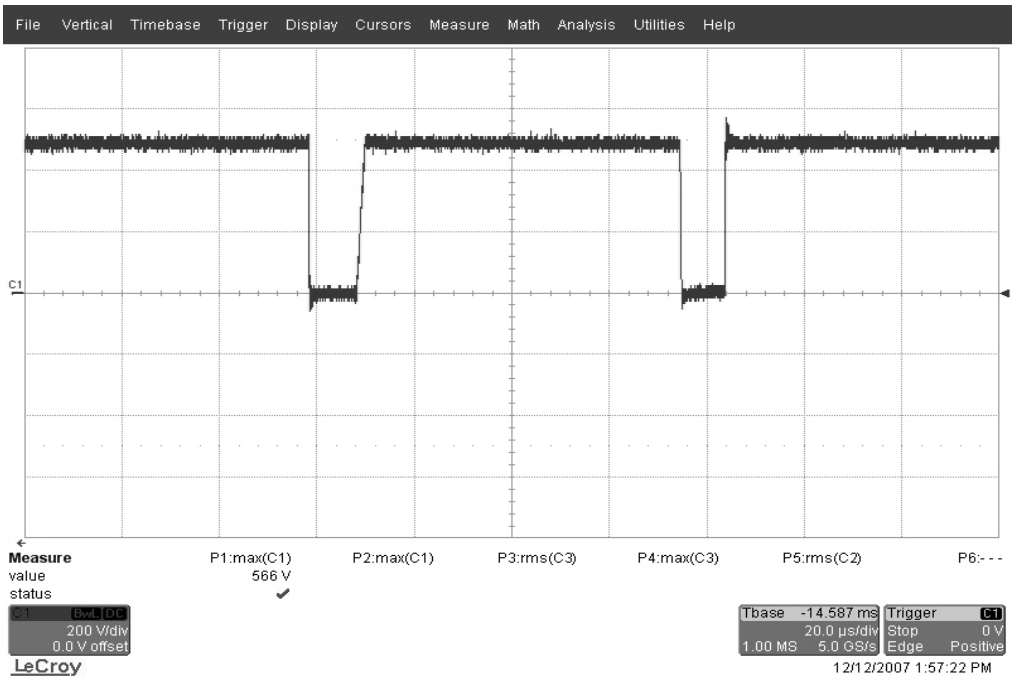


Figure 5.66 The zoom-in view of the line-to-line voltage waveform of SVPWM1 at its worst overshoot voltage region for M_i=0.8 and 2m cable.

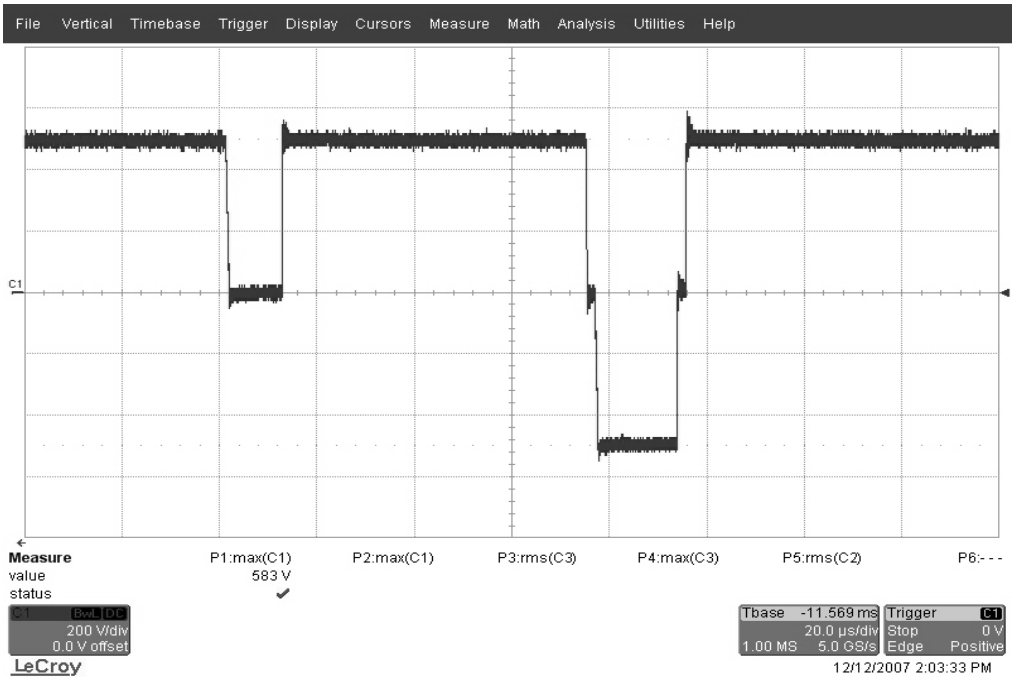


Figure 5.67 The zoom-in view of the line-to-line voltage waveform of AZSPWM1 at its worst overshoot voltage region for M_i=0.8 and 2m cable.

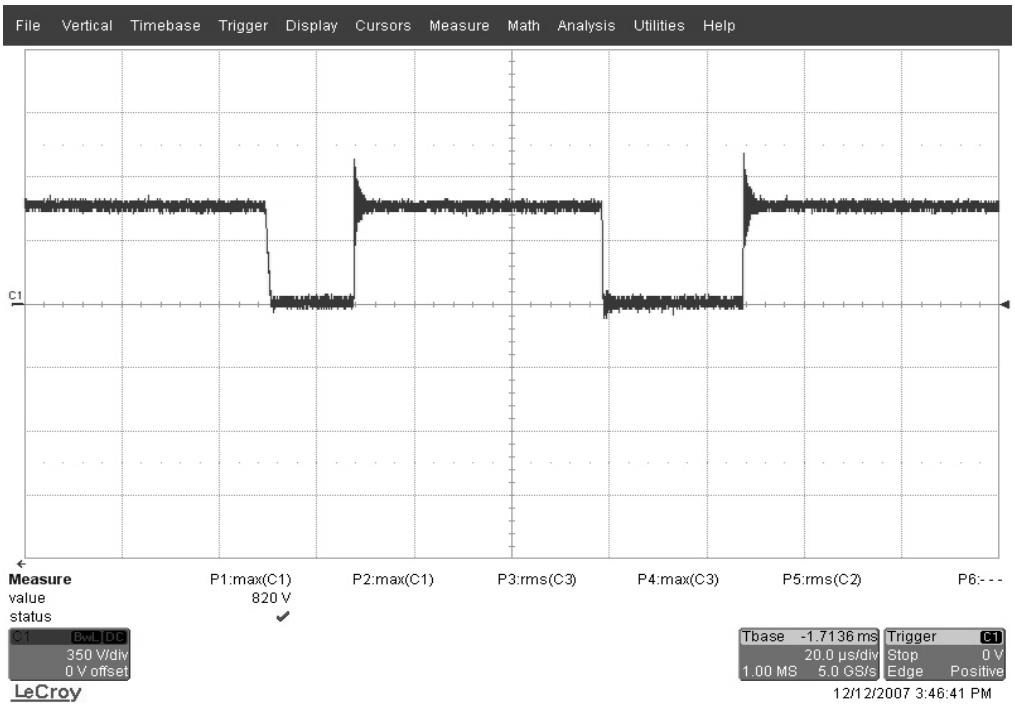


Figure 5.68 The zoom-in view of the line-to-line voltage waveform of SVPWM at its worst overshoot voltage region for M_i=0.8, 2m cable, and CMI-2.

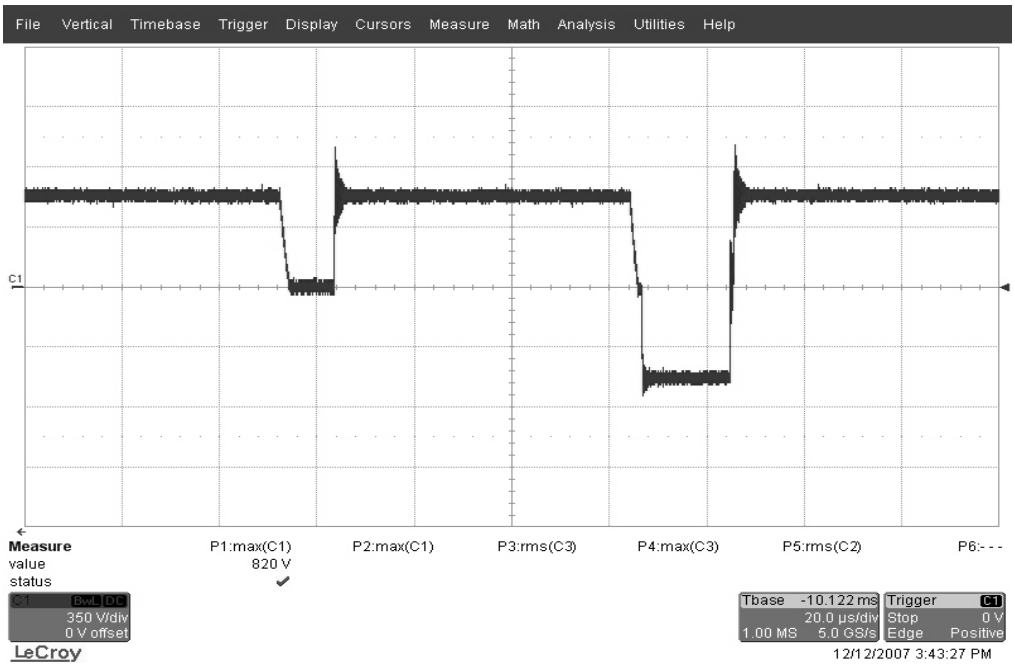


Figure 5.69 The zoom-in view of the line-to-line voltage waveform of AZSPWM1 at its worst overshoot voltage region for M_i=0.8, 2m cable, and CMI-2.

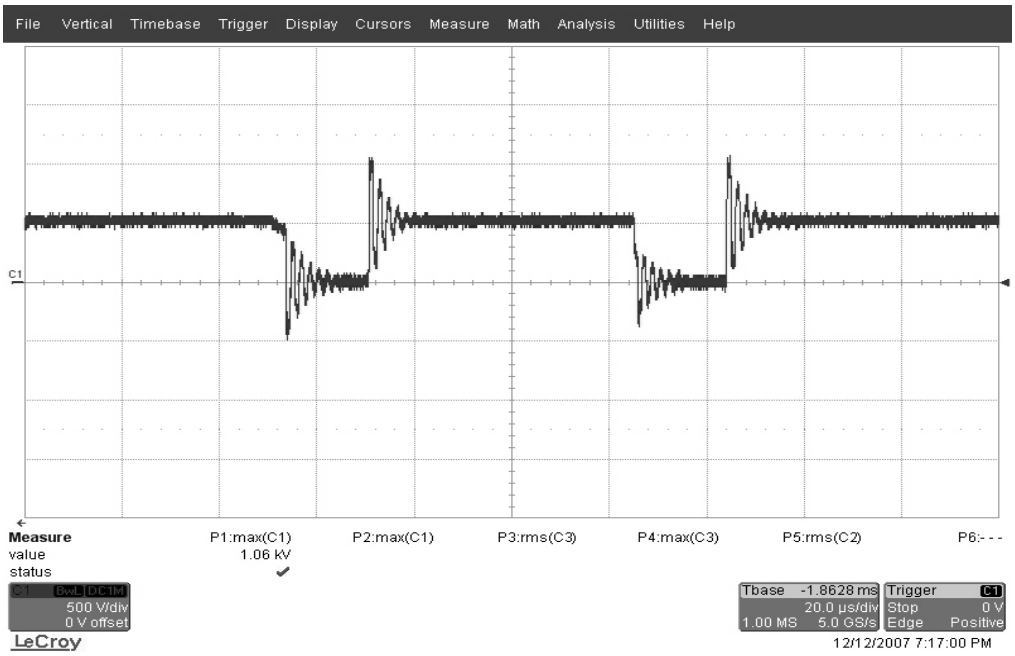


Figure 5.70 The zoom-in view of the line-to-line voltage waveform of SVPWM at its worst overshoot voltage region for M_i=0.8, 70m cable, and CMI-2.

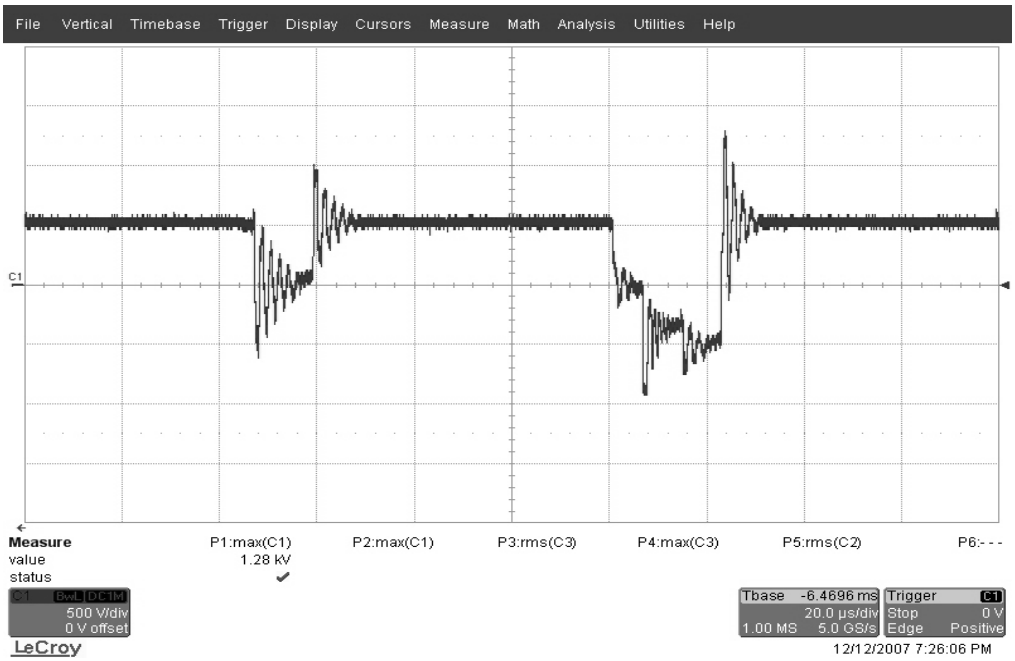


Figure 5.71 The zoom-in view of the line-to-line voltage waveform of AZSPWM1 at its worst overshoot voltage region for M_i=0.8, 70m cable, and CMI-2.

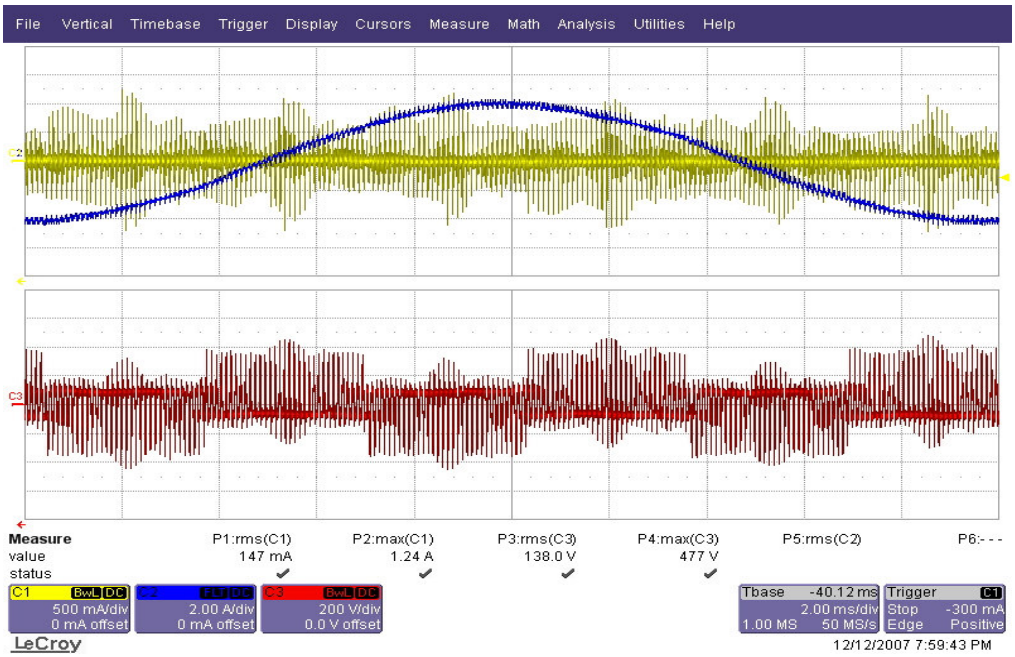


Figure 5.72 Phase current (blue), CMC (yellow), and CMV (red) waveforms for DPWM1 (M_i=0.8 and f_s=10 kHz) (70m cable).

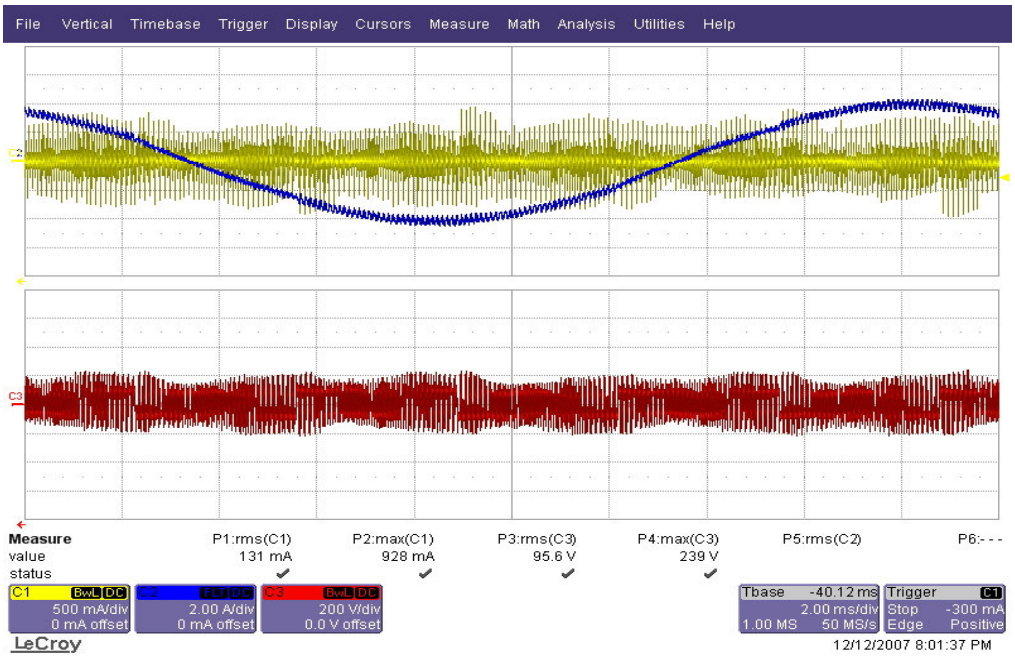


Figure 5.73 Phase current (blue), CMC (yellow), and CMV (red) waveforms for NSPWM (M_i=0.8 and f_s=10 kHz) (70m cable).

Table 5.10 Measured peak line-to-line voltages (kV) for various PWM methods for various operating conditions (M_i=0.8).

		2m cable	2m cable CMI-2	70m cable	70m cable & CMI-2
Prototype VSI	DPWM1	0.54	0.82	1.02	1.06
	SVPWM	0.56	0.82	0.99	1.06
	NSPWM	0.58	0.82	0.99	1.04
	AZSPWM1	0.58	0.82	1.37	1.28
Commercial VSI	2-level VSI	0.65	0.86	0.99	1.13
	3-level VSI	0.65	0.74	0.79	0.88

5.8 Modification Algorithm for AZSPWM1 (MAZSPWM)

AZSPWM1 successfully reduces the CMV and it has satisfactory harmonic ripple performance. Although it is inferior to NSPWM at high M_i, since it is operable at low M_i, it can be favored and at least it can be utilized in the lower M_i region, where NSPWM is not operable. However, as shown in the previous section, AZSPWM1 has overvoltage performance problems prohibiting its practical utilization. AZSPWM1 has bipolar output line-to-line voltage pulse pattern and for all modulation index values there are PWM cycles where no or very narrow zero-voltage time intervals are available between the polarity reversals of the line-to-line voltage. Insufficient zero-voltage time intervals result in voltage reflection problems, especially in long cable applications as the experimental results illustrate. Therefore, a modification to AZSPWM1 is proposed to eliminate the voltage reflection problem while preserving the superior CMV reduction capability without degrading the harmonic ripple performance throughout the operating range of the modulator. The modified AZSPWM1 algorithm is given the name “MAZSPWM”. After the

modification, wide enough zero-voltage time intervals are provided between the polarity reversals of the line-to-line voltages every time they occur. Thus, the large magnitude overvoltages are mostly eliminated and some of them are partially reduced, depending on the operating conditions.

In AZSPWM methods two active voltage vectors and two opposing active zero voltage vectors are utilized. With careful observation of Figure 2.32, in A1, it can be seen that for V_{ab} the zero-voltage time duration is equal to the time of V_2. Likewise for V_{bc}, the zero-voltage time interval between pulse reversal is equal to the time of V_1. Of the two, the vector with the smaller time length is more problematic in terms of pulse reversals and its duration should be increased. MAZSPWM provides this modification while retaining the required volt-seconds over the PWM cycle. This is achieved by increasing the duty cycle of the smaller duty cycle vector by 2ε and decreasing the duty cycle of the larger duty cycle vector by the same amount. However, this alone is not sufficient to maintain vector volt-seconds balance. The created imbalance is compensated via the modification on the two active zero states V_3 and V_6. Their duty cycles, in this case are also modified and while V_3 duty cycle is increased by ε, the V_6 duty cycle is decreased by the same amount. Note that in the MAZSPWM method, same voltage vectors are utilized as the AZSPWM1 and in the modified case active zero state voltage vectors do not totally cancel the effect of each other unlike in AZSPWM1 and AZSPWM2. For modification, the general solution of the duty cycles in region A1 is given in (5.1) – (5.4) where ε is a parameter. Hence this modification is called the epsilon "ε" modification.

$$d_1 = \frac{2\sqrt{3}}{\pi} M_i \sin(60-\theta) + 2\varepsilon \tag{5.1}$$

$$d_2 = \frac{2\sqrt{3}}{\pi} M_i \sin(\theta) - 2\varepsilon \tag{5.2}$$

$$d_3 = 0.5 - \frac{\sqrt{3}}{\pi} M_i \sin(60+\theta) + \varepsilon \tag{5.3}$$

$$d_6 = 0.5 - \frac{\sqrt{3}}{\pi} M_i \sin(60+\theta) - \varepsilon \tag{5.4}$$

Note that with different ε values different solution sets of duty cycles all resulting the same volt-seconds are obtained. For example, if ε=0, the solution set corresponds to that of AZSPWM1, where d_3=d_6. If $\varepsilon = \pm(0.5 - \frac{\sqrt{3}}{\pi} M_i \sin(60+\theta))$, the solution set corresponds to that of NSPWM, where either d_3 or d_6 is zero and the reference volt-second is generated by the 3 near state vectors. Between these two extreme operations there is a wide range for selecting the ε parameter where all of them have solutions with unique characteristics.

Figure 5.74 illustrates the generation of the MAZSPWM voltage vectors by modifying the AZSPWM1 voltage vectors. Note that for AZSPWM1 at the illustrated operating point (near $\theta=60^o$), d_1 is very low (hence the t_z is very narrow) and there is not enough damping time available between the polarity reversals. However after the "ε" modification d_1 and hence t_z are enlarged sufficiently. Since at each half carrier cycle there is one zero-voltage time interval whose duty cycle is increased with ε, d_1 is increased with 2ε and d_2 is decreased with the same amount. The duty cycles of the active zero voltage vectors are also modified by adding and subtracting ε to d_3 and d_6 respectively. If d_2 is very small but d_1 is sufficiently large (near $\theta=0^o$), then d_2 should be increased and ε should be negative.

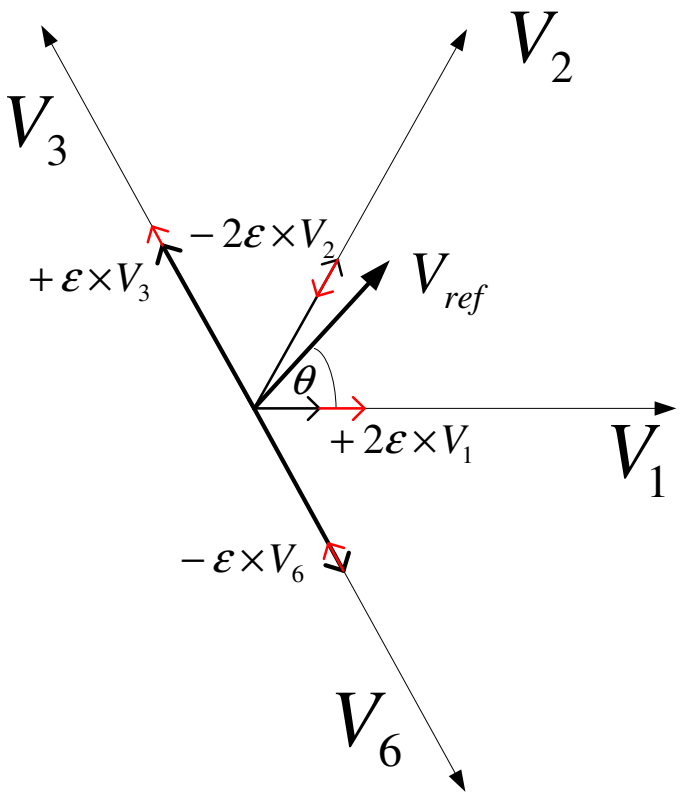


Figure 5.74 Generation of the voltage vectors of MAZSPWM.

Figure 5.75 illustrates the phase switch signals, CMV, and line-to-line voltage pulse patterns of MAZSPWM near $\theta=60^o$ (where the duty cycle of V_1 is insufficiently small). As observed from the figure, after the modification, the zero-voltage time between polarity reversals on V_{bc} gets wider. d_z is increased by ε (total duty cycle of V_1 (d_1) is increased by 2ε). In the figure, ε is exaggerated for a clear illustration of the modification. During the modification the CMV waveform is not affected and still limited at $|V_{dc}/6|$.

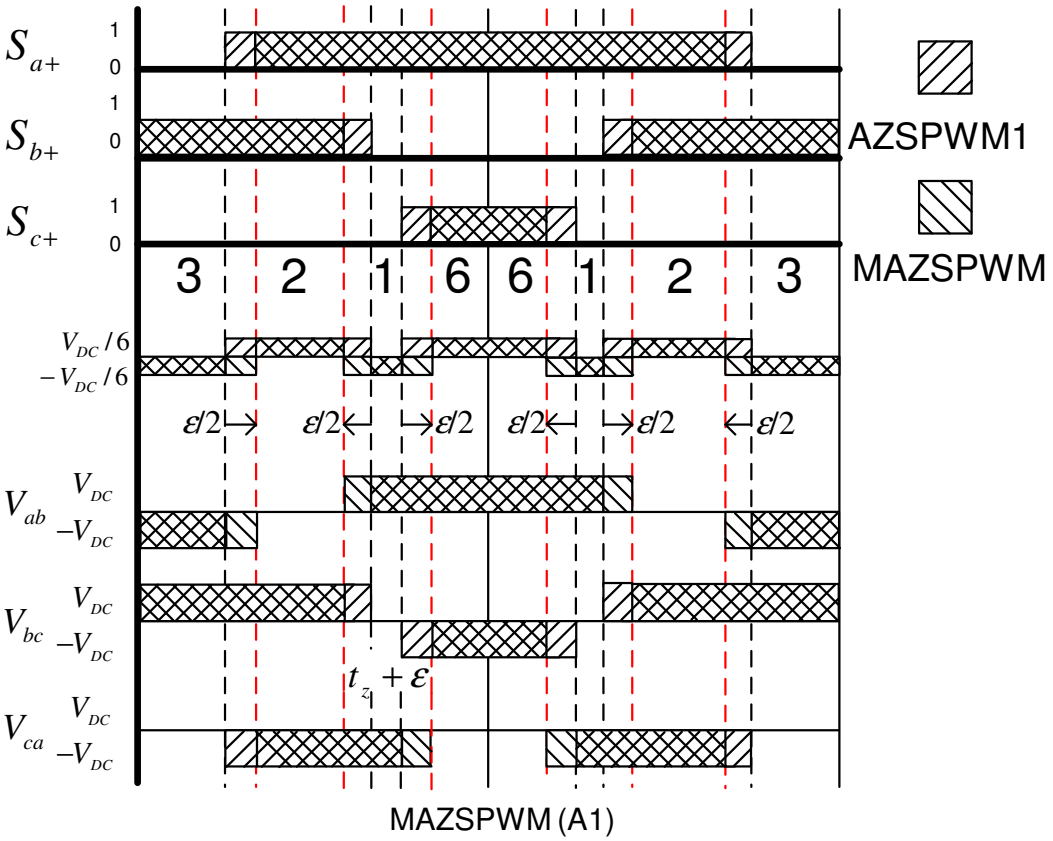


Figure 5.75 PWM pulse pattern, CMV, and line-to-line output voltages of MAZSPWM.

Modifying the duty cycles of AZSPWM1 is possible by infinitely many ε values. Also frequently a modification may not be necessary since in some operating points all bipolar line-to-line voltages have sufficiently wide zero-voltage times. Therefore, selection of the ε parameter is important. For this purpose, first of all, the minimum required zero-voltage interval ($t_{z\text{-}min}$) between the polarity reversals of the line-to-line voltages, not resulting in high peak overshoots should be known, which is typically a few μs. The corresponding $d_{z\text{-}min}$ should be calculated by normalizing $t_{z\text{-}min}$ with the PWM period. Since in each half carrier cycle there is one zero-voltage interval; the total duty cycle of each active voltage vector must be at least $2d_{z\text{-}min}$ and the active voltage vectors with a duty cycle less than $2d_{z\text{-}min}$ require modification. Practically when the reference voltage vector is near the A-type 60° boundaries, the modification is required and when it is near the center of the A-type 60° regions no modification is required. The modification decision diagram is illustrated in Figure 5.76. If both

active voltage vectors have sufficiently large duty cycle, then no modification is required and AZSPWM1 provides a solution (if one of them is less than $2d_{z\text{-}min}$ then modification is required).

If the available d_z is not sufficient and a modification is required, the possibility of achieving a valid solution by modifying AZSPWM1 duty cycles should be tested. There are two different constraints limiting the ε modification. The first one is effective at low M_i, where the duty cycles of the active voltage vectors are low. In some applications where high d_{zmin} is required, the wider of the active voltage vectors is not sufficient to compensate the narrower, such that after the modification the wider of the active voltage vectors become narrower than the required $d_{z\text{-}min}$. This constraint appears when $d_1+d_2<4d_{z\text{-}min}$. In such conditions the ε modification can not be implemented by the selected $d_{z\text{-}min}$ value and the modification should be applied with a reduced $d_{z\text{-}min}$. The consequence will be an additional overvoltage proportional to the error between ideal and realized $d_{z\text{-}min}$.

The other constraint is effective at high M_i where the active zero voltage vectors are narrow. During the modification, the duty cycle of one of the active zero voltage vectors may be calculated as less then zero, which is practically impossible. This constraint appears when any of the active zero voltage vectors is smaller than $2d_{z\text{-}min}$. Similarly, in such conditions the ε modification can not be implemented by the selected $d_{z\text{-}min}$ value and the modification should be applied with a reduced $d_{z\text{-}min}$. The consequence will be an additional overvoltage proportional to the error between ideal and realized $d_{z\text{-}min}$.

Therefore there is an upper limit for the selection of "ε" and the maximum possible $d_{z\text{-}min}$ value is named as $d_{z\text{-}minlimit}$. If the required $d_{z\text{-}min}$ is greater than $d_{z\text{-}minlimit}$, the ε modification should be done for a reduced $d_{z\text{-}min}$ ($d_{z\text{-}min} = d_{z\text{-}minlimit}$). The above explained two constraints define two equations for $d_{z\text{-}minlimit}$. At low M_i $d_{z\text{-}min}$ should be at most $(d_1+d_2)/4$, resulting the equation $d_{z\text{-}minlimit}=(3/4\pi)M_i$ which is obtained from (5.1) and (5.2). This is obtained for the boundary conditions of 0^o and 60^o

where the worst case operating condition is obtained in terms of overvoltages (see Section 2.5.4). Similarly at high M_i $d_{z\text{-}min}$ should be at most the half of the duration active zero voltage vectors, resulting in the equation $d_{z\text{-}minlimit}=(1/2)-(3/2\pi)M_i$, which is obtained from (5.3) and (5.4). Both equations are valid for the whole inverter modulation index range but for $M_i<2\pi/9$ ($\cong 0.7$) the first equation, and for $M_i>2\pi/9$ the second equation is effective.

Figure 5.77 illustrates the maximum $d_{z\text{-}min}$ ($d_{z\text{-}minlimit}$) can be selected for a definite M_i. If the required $t_{z\text{-}min}$ can not be implemented due to $d_{z\text{-}minlimit}$ then the carrier frequency can be decreased and a less $d_{z\text{-}min}$ is selected to implement. If it is not possible to modify the carrier frequency (which is typically the case), then some amount of excessive overvoltage for long cable operation must be accepted.

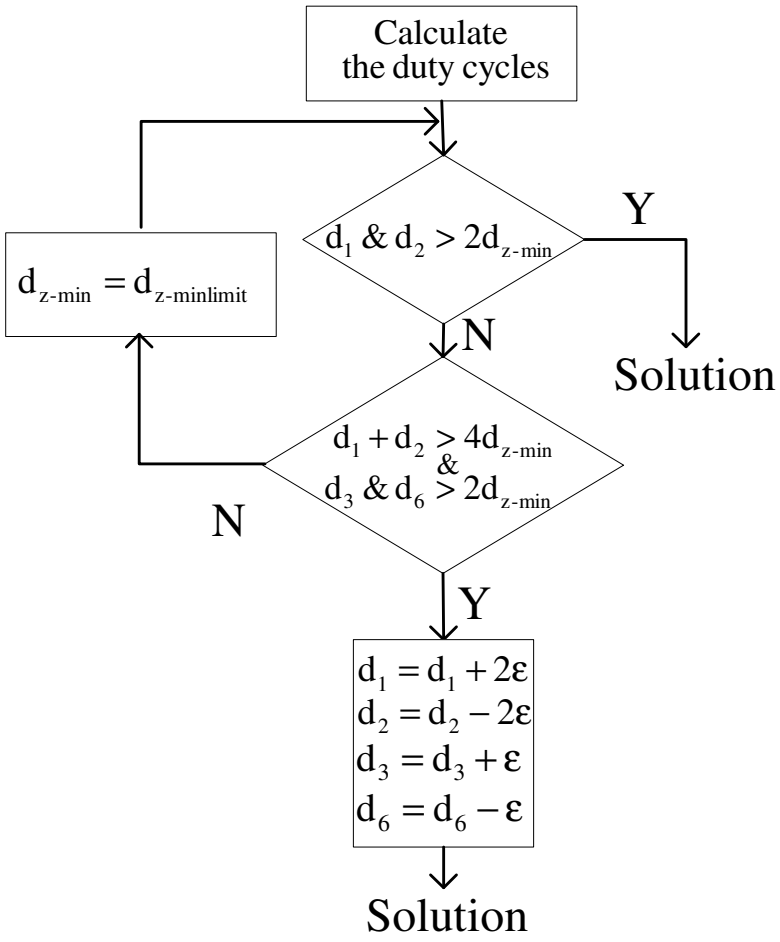


Figure 5.76 Decision flow chart of MAZSPWM.

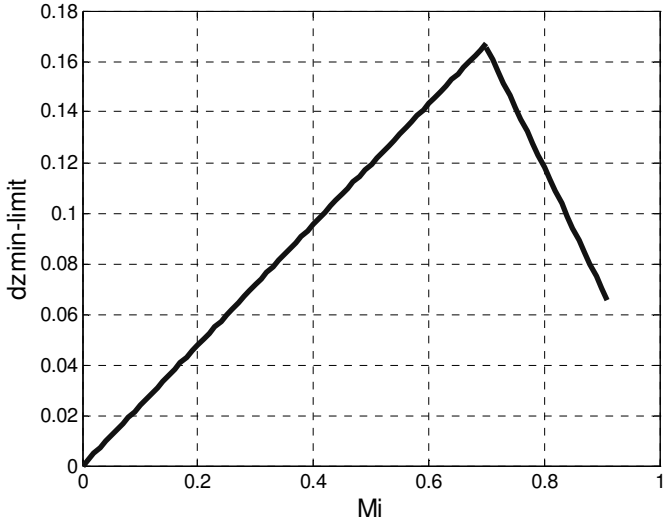


Figure 5.77 Maximum $d_{z\text{-}min}$ ($d_{z\text{-}minlimit}$) for various M_i values.

In Figure 5.78 the zero-voltage times of AZSPWM1 for various M_i values are illustrated together with the ε modification for a required $d_{z\text{-}min}$. In this example, $d_{z\text{-}min}$ is 0.05. Note that the available zero-voltage time of AZSPWM1 is not sufficient for a definite region for all M_i values (near 0^o and 60^o). In these regions, the ε modification is required where $|\varepsilon| = d_{z\text{-}min} - d_{z\text{-}azspwm(x/y)}$ (ε is positive near $\theta=60^o$ and negative for $\theta=0^o$). As the figure illustrates, the required ε varies at different operating points and it is not required where $d_{z\text{-}azspwm(x/y)} > d_{min}$.

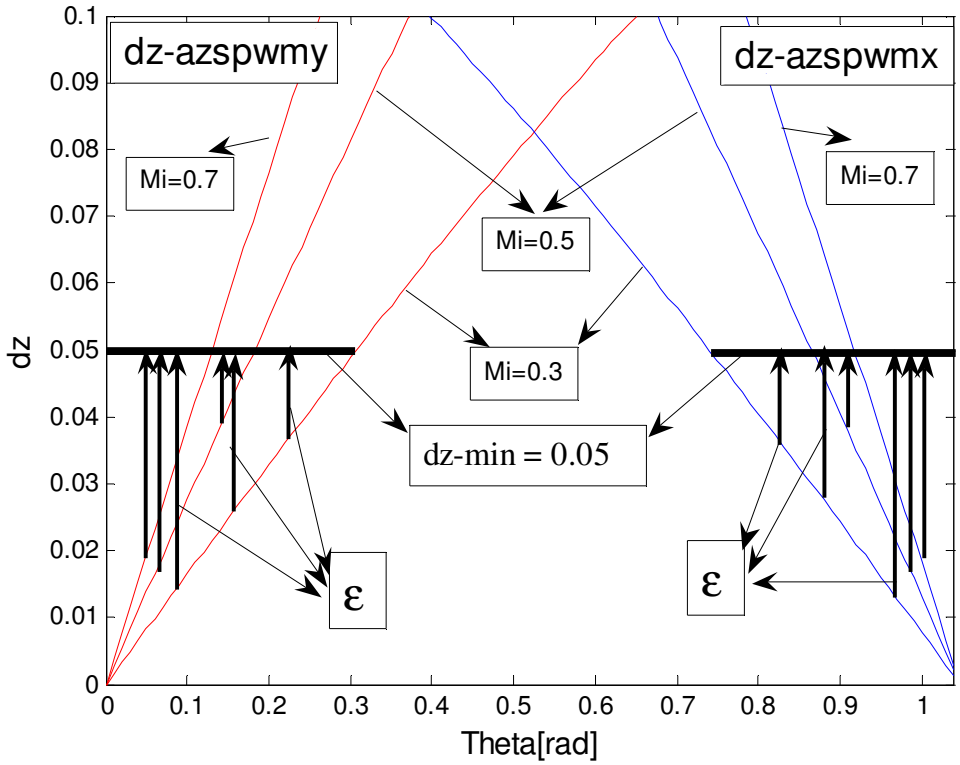


Figure 5.78 Epsilon "ε" modification of the zero-voltage time interval.

The ε modification eliminates the excessive overvoltages when possible and limits them when the conditions are not exactly favoring. Therefore, the ε modification improves the AZSPWM1 modulator performance. And MAZSPWM is a more favorable in the application field from this perspective. However, the symmetric volt-second balancing mechanism is disturbed for the purpose of creating a sufficiently long zero voltage time and this results in output current ripple degradation. In order to observe the effect of the ε modification on the output current ripple, the HDF function is calculated for MAZSPWM for various d_{zmin} values. However, it is observed that the HDF curve of MAZSPWM is nearly identical to that of AZSPWM1 for practical d_{zmin} values but the HDF values slightly increase with d_{zmin}. In Figure 5.79 the HDF curves of MAZSPWM with d_{zmin}=7% and 12% are illustrated together with those of AZSPWM1 and NSPWM. These selected d_{zmin} values are intentionally exaggerated in order to observe the differences clearly. The figure illustrates that even with a very high d_{zmin} selection the output current ripple of

MAZSPWM is very close to that of AZSPWM1 and they can be considered as practically identical. Since AZSPWM1 ripple was found in the experiments acceptable from the motor speed control and acoustic noise performances perspective, MAZSPWM can also be considered satisfactory. However, it should be noted that at high M_i the advantage of NSPWM is now more emphasized in terms of PWM ripple performance when compared to MAZSPWM. Therefore, when mixing modulation methods, NSPWM should be chosen as soon as it is in the operable range and its voltage reflection problem is not apparent.

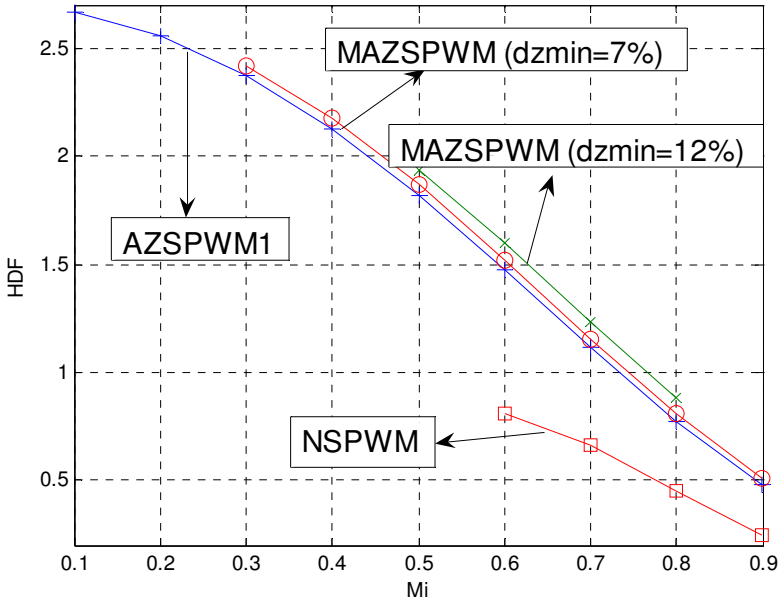


Figure 5.79 The HDF characteristics of NSPWM, AZSPWM1 and MAZSPWM with two different d_{zmin} values.

In order to verify the theory, the ε modification is applied to AZSPWM1 and laboratory experiments are conducted at f_s=6.6 kHz. The main objective of the ε modification is to eliminate the voltage reflection problem of AZSPWM1. Therefore, at first, the long cable test experiments are conducted and the line-to-line voltage waveforms are investigated for MAZSPWM. During these experiments $d_{z\text{-}min}$ is selected as 0.04 which inserts a zero-voltage time interval of at least 6 μs between polarity reversals for 6.6 kHz operation. This is found to be the minimum time

interval for the oscillations on the line-to-line voltages to damp. Experiments are conducted at M_i=0.4, M_i=0.61, and M_i=0.8. As illustrated in Figure 5.77 for the given modulation indices, $d_{z\text{-}min}$=0.04 is less than $d_{z\text{-}minlimit}$. In Figure 5.80, Figure 5.81, and Figure 5.82 the line-to-line voltage waveforms of MAZSPWM are given together with their zoom-in views for M_i=0.4, M_i=0.61, and M_i=0.8, respectively. The maximum peak overshoots are 1.08 kV, 1.04 kV, and 1.08 kV for the given M_i respectively after the modification is applied (with AZSPWM1 the overshoots are 1.33 kV for M_i=0.61 and 1.37 kV for M_i=0.8). As the zoom-in figures illustrate, there are sufficient t_z intervals available at the narrowest zero-voltage time interval cases, for the oscillations to damp.

In addition to line-to-line voltage waveforms the CMV/CMC, and phase current PWM ripple characteristics are investigated. The experimental results of the phase current, CMC, and CMV of MAZSPWM for M_i=0.4, M_i=0.6, and M_i=0.8 are illustrated at Figures 5.83, 5.84 and 5.85 respectively for short cable application (f_s=6.6 kHz). It is observed that for MAZSPWM the CMV and CMC is reduced as other RCMV-PWM methods and the CMV/CMC measurements are nearly identical to those of AZSPWM1.

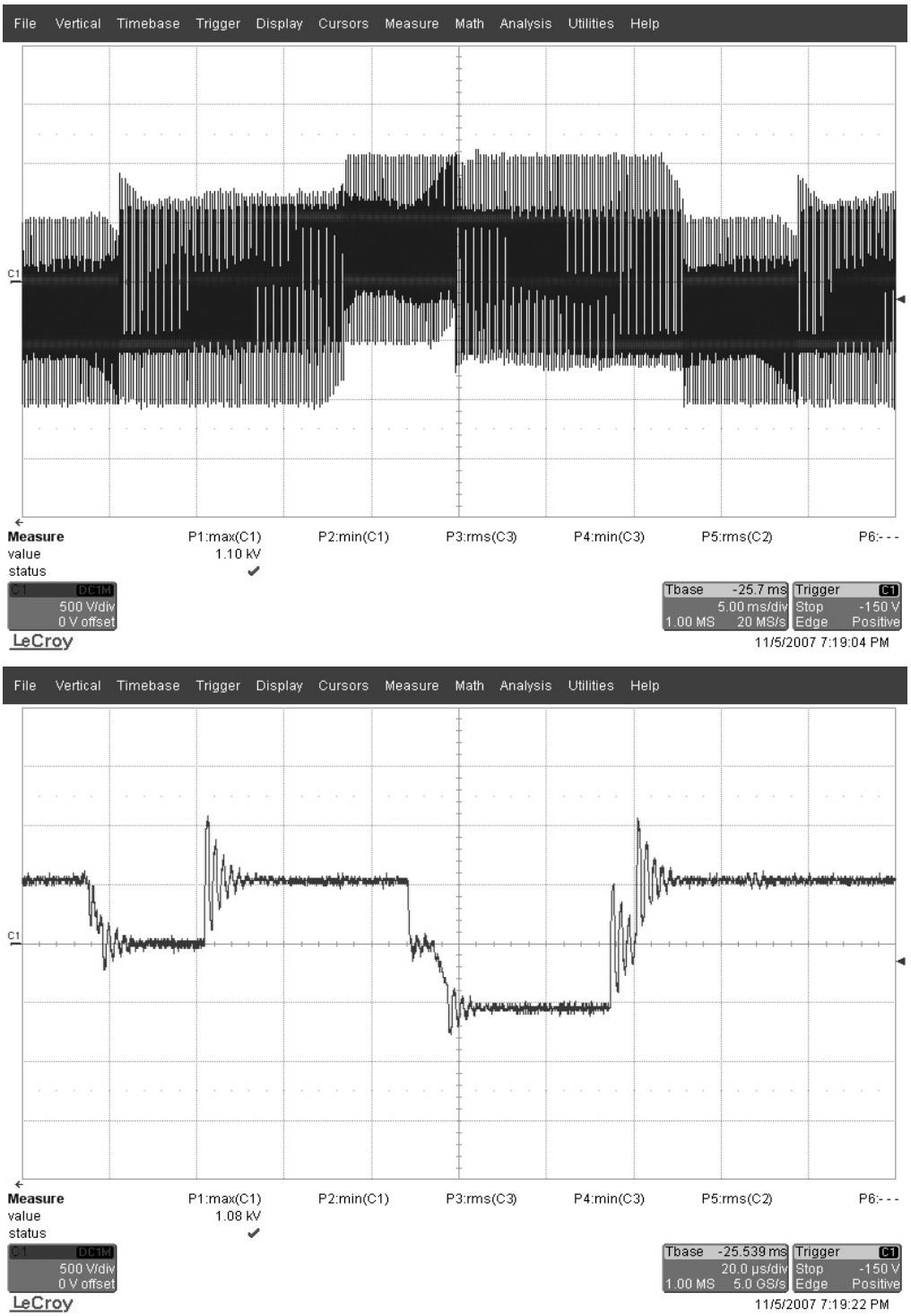


Figure 5.80 Line-to-line voltage waveform of MAZSPWM (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.4 and 70m cable.

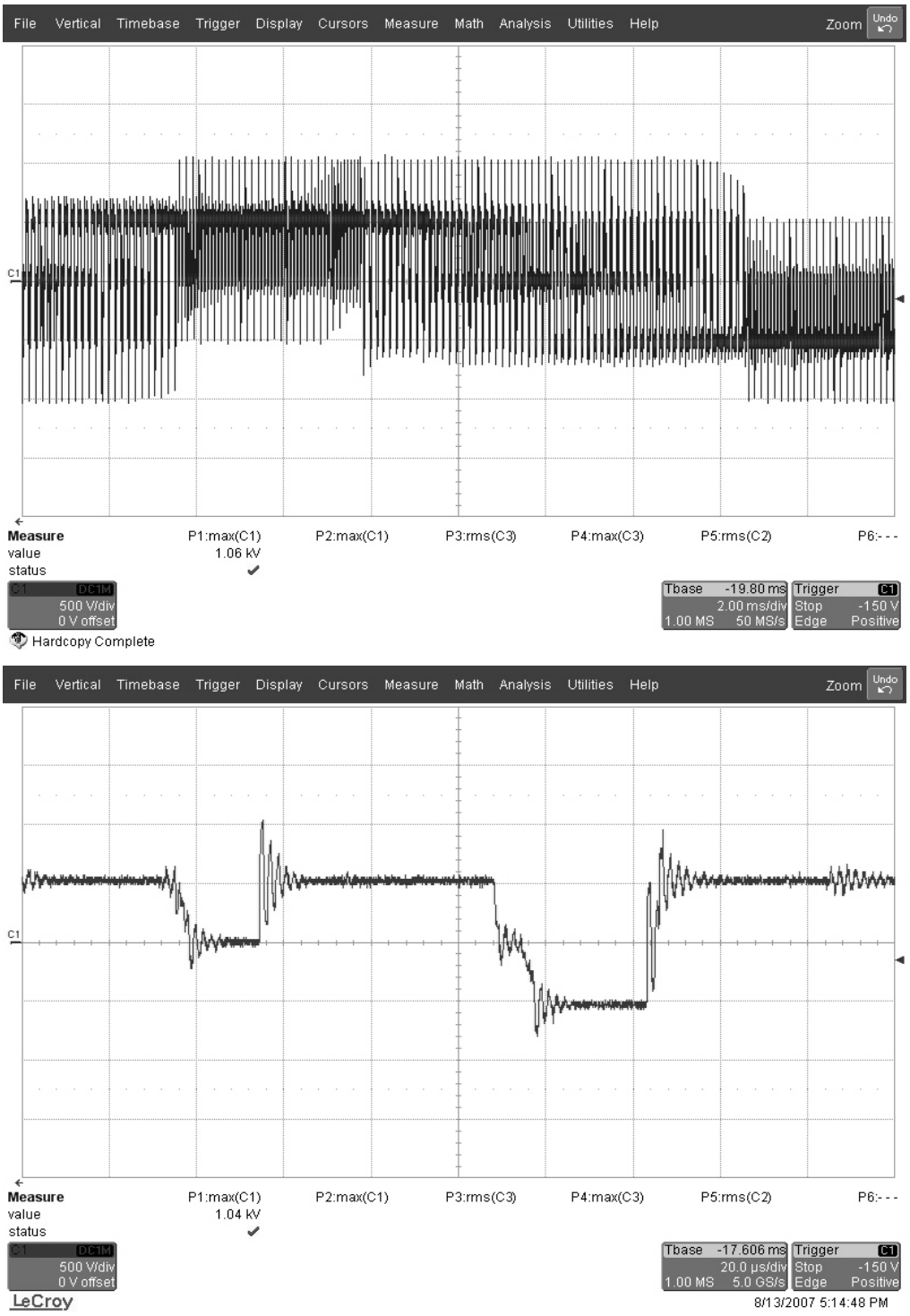


Figure 5.81 Line-to-line voltage waveform of MAZSPWM (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.61 and 70m cable.

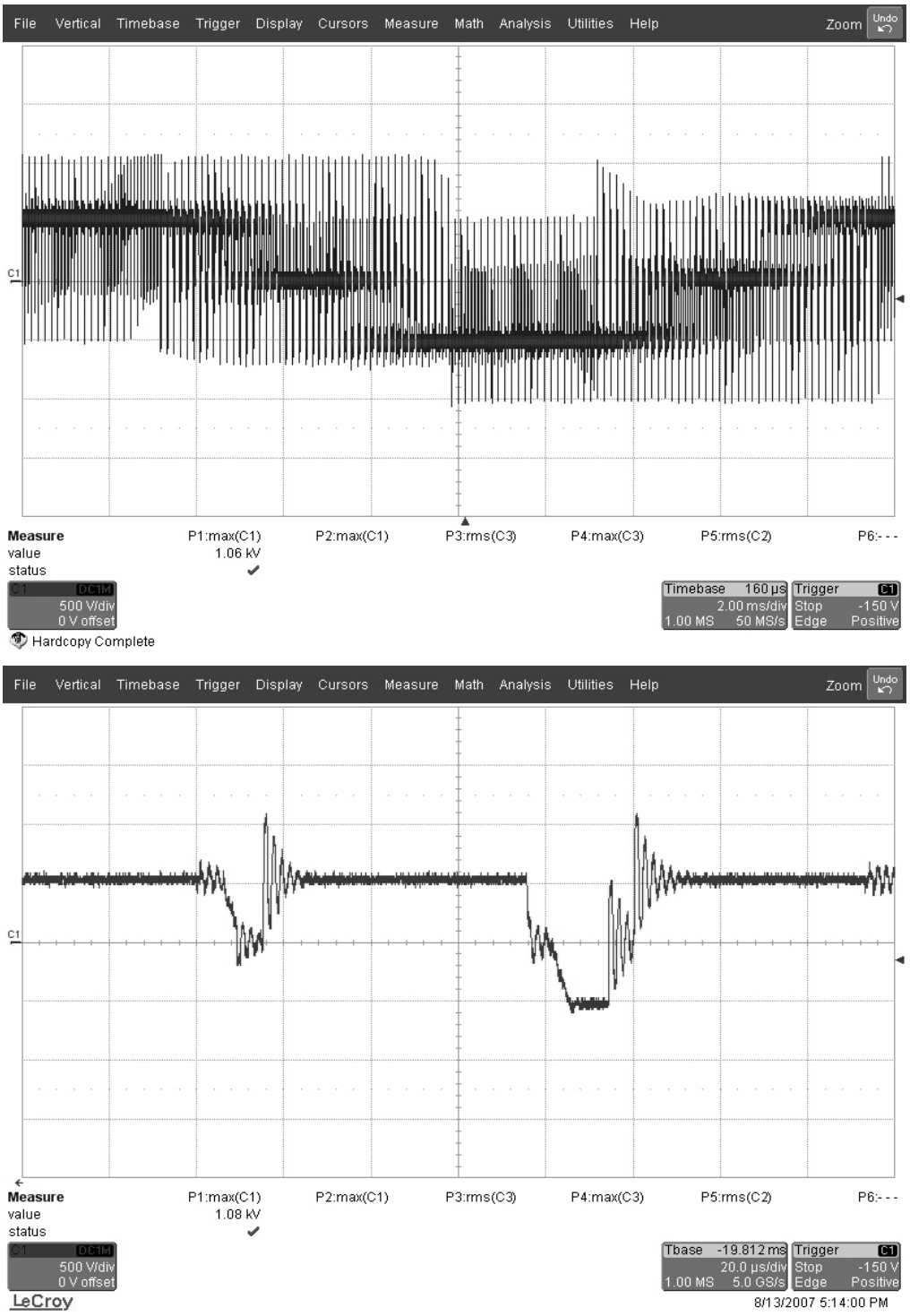


Figure 5.82 Line-to-line voltage waveform of MAZSPWM (top) and its zoom-in view at its worst overshoot voltage region (bottom) for M_i=0.8 and 70m cable.

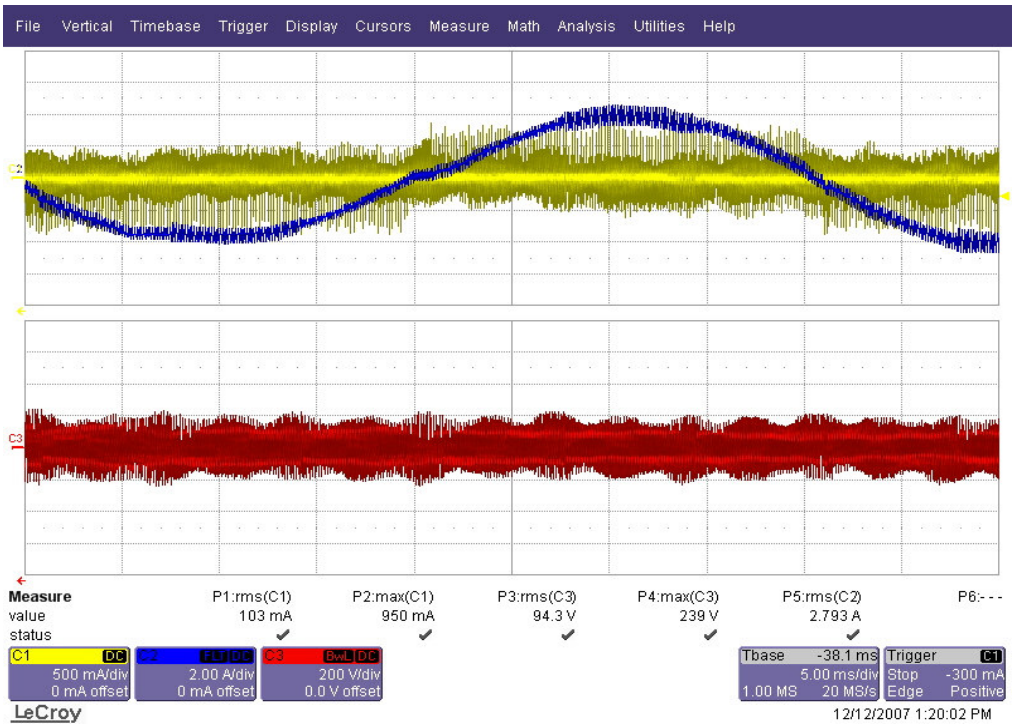


Figure 5.83 Phase current (blue), CMC (yellow) and CMV (red) waveforms for MAZSPWM (M_i=0.4 and f_s=6.6kHz).

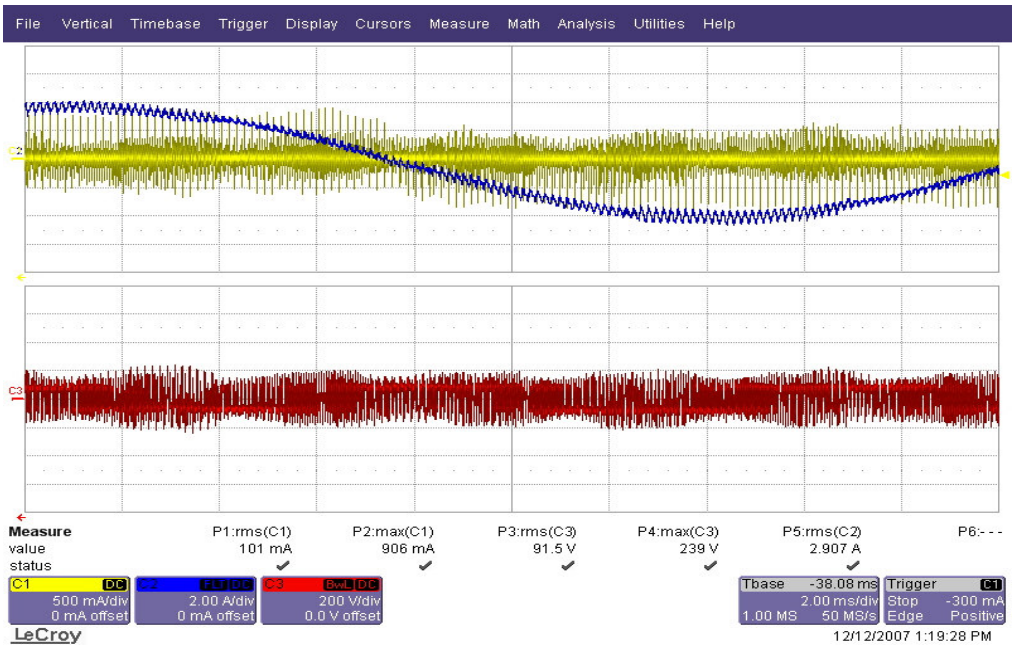


Figure 5.84 Phase current (blue), CMC (yellow) and CMV (red) waveforms for MAZSPWM (M_i=0.61 and f_s=6.6kHz).

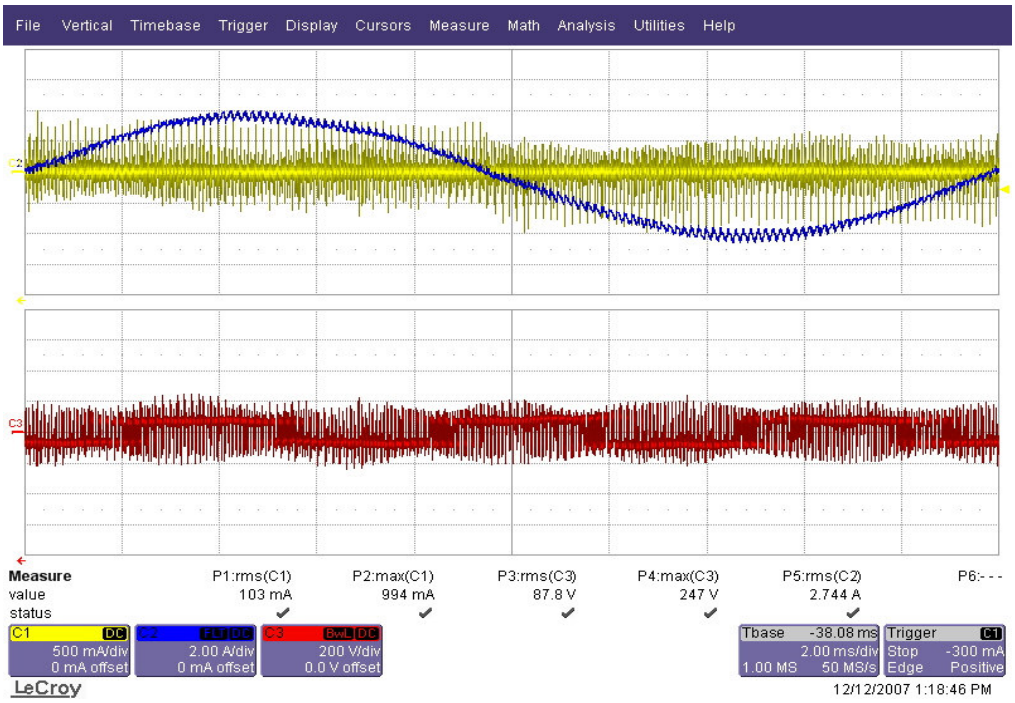


Figure 5.85 Phase current (blue), CMC (yellow) and CMV (red) waveforms for MAZSPWM (M_i=0.8 and f_s=6.6kHz).

5.9 Laboratory Experiments of The Combined Algorithm

A combined algorithm of NSPWM and AZSPWM1 was defined in Chapter 2.6. The simulation results have shown that transition from one method to another is achieved smoothly. In this section laboratory experiments are conducted to verify the feasibility of the combined algorithm. The experimental set-up is exactly same as the previous experiments and in the combined algorithm AZSPWM1 is utilized as its modified version (MAZSPWM) described in the previous section with f_s=10 kHz. In this section the reference signals illustrated as they are obtained by processing the IGBT gate logic signals by a first order analog low pass filter. The ASD is operated at M_i=0.58 for unloaded case such that reference voltage vector enters and exits voltage linearity region of NSPWM several times (six times) in a fundamental cycle.

In Figure 5.86 modulation signal and phase current of the combined algorithm are illustrated at M_i=0.58. The modulation signal is evaluated by the same technique as the phase-neutral voltages of the commercial VSIs (see section 5.6). The reference

signal is the same as that of MAZSPWM when MAZSPWM is utilized and is same as that of NSPWM when NSPWM is utilized. Phase current is sinusoidal and the transitions between two PWM methods do not result in disturbing transients. In Figure 5.87, the phase current, CMV, CMC, and the reference signal of the combined algorithm are illustrated at M_i=0.58. In the waveforms, at each instant, the CMV and CMC characteristics are those of the corresponding PWM utilized. CMV and CMC are successfully reduced and they do not reach high values even at the transition instants. The experimental results show that combining the NSPWM and MAZSPWM methods in a single algorithm provides superior CMC/CMV performance together with low switching losses and harmonic ripple throughout the voltage linearity range of $0<M_i<0.91$.

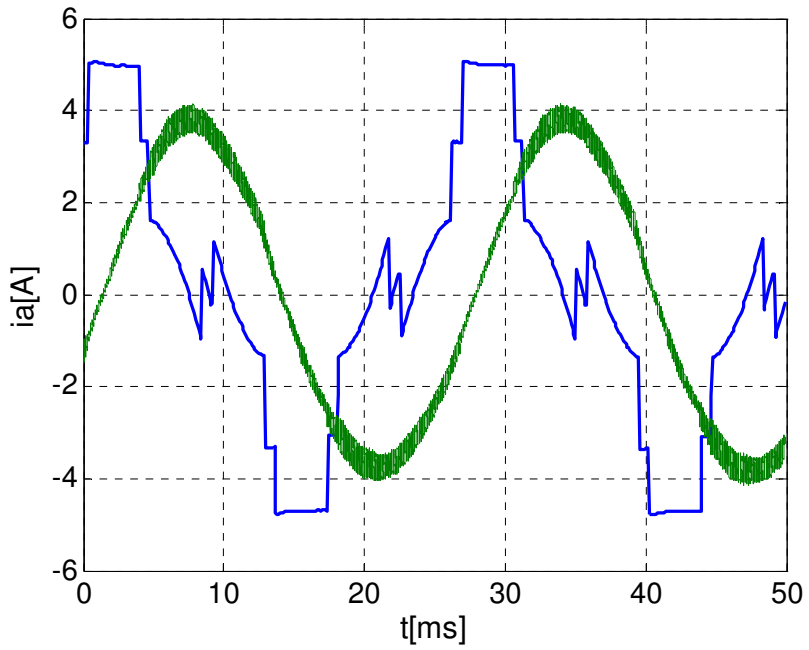


Figure 5.86 Phase current (green) and modulation signal (x5) (blue) for the combined PWM algorithm (M_i=0.58).

As a final experiment the CMC performance improvement with CMI-2 is provided. As Figure 5.88 shows, with the CMI included, the drive CMC also decreases significantly yielding a drive with low CMV/CMC and acceptable PWM ripple performance.

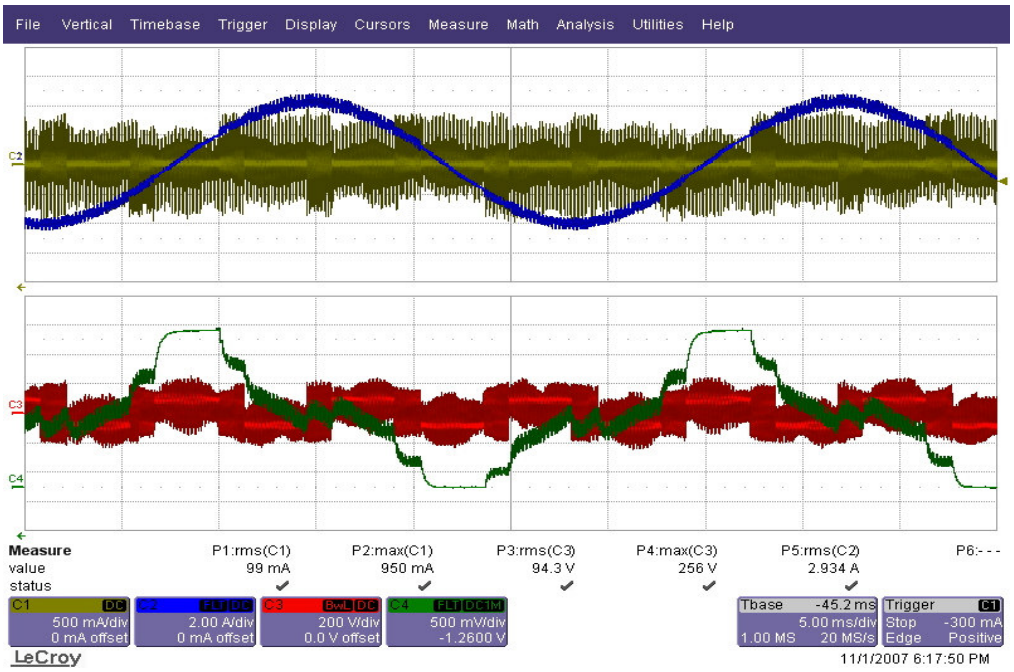


Figure 5.87 Phase current (blue), CMC (yellow), CMV (red), and modulation signal (green) waveforms for the combined PWM algorithm (M_i=0.58).

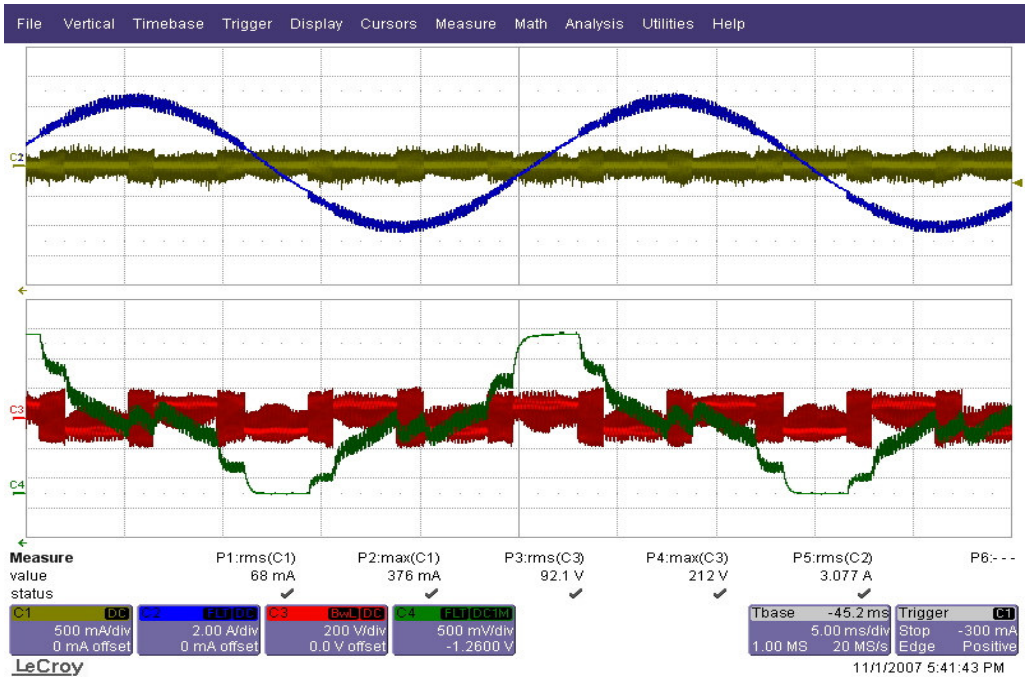


Figure 5.88 Phase current (blue), CMC (yellow), CMV (red), and modulation signal (green) waveforms for the combined PWM algorithm with CMI-2 (M_i=0.58).

5.10 Summary

In this chapter, laboratory experimental results are conducted to verify the theoretical results. DPWM1, SVPWM, NSPWM, and AZSPWM1 are implemented and tested. Experimental results show that RCMV-PWM methods significantly reduce CMV. However, decrement in CMC is less successful. In order to observe the performances of passive mitigation methods, three CMIs and one CMT are tested. It is observed that passive mitigation methods do not reduce CMV. However, they reduce CMC successfully. The decrement is even more successful when they are utilized together with RCMV-PWM methods. Therefore, it is concluded that utilization of passive filters and RCMV-PWM methods together provides superior CMC/CMV mitigation. Also a commercial two-level inverter and a commercial three-level NPC inverter are tested and it is observed that the CMV performance of the three-level NPC inverter is comparable with that of two-level VSIs with RCMV-PWM methods and its CMC performance is superior to all PWM methods for two-level VSIs.

In this chapter, in addition to CMV and CMC performances of PWM methods, line-to-line voltage waveforms of PWM methods are investigated for long-cable applications and voltage reflections and overshoots are studied. It is observed that there are always voltage overshoots resulted during the switching instants on the motor terminals in long cable applications. However, the magnitudes of these overshoots are much higher in AZSPWM1 than other methods. To mitigate this, constraint of MAZSPWM is proposed and implemented by applying a described modification algorithm to AZSPWM1.

The combined algorithm of NSPWM and MAZSPWM is implemented such that NSPWM is utilized when the reference voltage is inside voltage linearity region of NSPWM and MAZSPWM is utilized when the reference voltage is in the voltage non-linearity region of NSPWM. The experimental results illustrate that this algorithm can be successfully implemented without resulting in any problems. The phase currents are smooth and not disturbed during transition from one method to another.

CHAPTER 6

CONCLUSION

This thesis investigates the common mode voltage (CMV) of the three-phase two-level inverters as applied to induction motor drives. The effects of the common mode voltage on the motor drive and its the dependency of the common mode voltage on the inverter topology and PWM method are investigated in detail. Then, methods that effectively mitigate this effect are proposed and their viability is proven by means of theory, simulation, and laboratory experiments.

The main contribution of this thesis involves the development of the Near State PWM (NSPWM) method with reduced CMV and satisfactory harmonic ripple performance. The NSPWM method does not involve any practical constraints except the operating range limitations (the method is operable at high modulation index, that is M_i>0.61). In this thesis, the PWM pulse pattern of NSPWM is defined and utilizing the space vector approach the vector duty cycles of the method are calculated. The optimal vector sequence is determined and the simple scalar implementation is discussed. The output phase current and the DC-link current harmonic characteristics of NSPWM are investigated and shown to be better than those of the other RCMV-PWM methods and comparable with those of the standard PWM methods. NSPWM has lower CMV than the conventional methods and results in lower CMC. The line-to-line voltage pulses of NSPWM are bipolar and pulse polarity reversals occur in a similar manner to other RCMV-PWM methods. However, in NSPWM there is always sufficient interval between the voltage pulses. Therefore, the line-to-line voltage pulse polarity reversals of

NSPWM do not cause significant overvoltages (unlike AZSPWM1). Thus, the method is proven to be viable for practical industrial applications.

The second contribution of this thesis involves the review of the major standard and reduced common mode voltage PWM methods and the investigation of their practical applicability and PWM performance attributes such as voltage linearity range, inverter output harmonic flux, inverter output current ripple, DC-link current ripple, and inverter output line-to-line voltage pulse pattern. The analytical study indicates that standard PWM methods result in less harmonic content on both DC and AC side of the VSI with respect to RCMV-PWM methods. NSPWM performs superior to the other RCMV-PWM methods due to its less DC and AC side harmonic ripple and satisfactory line-to-line voltage pulse pattern characteristics. Harmonic ripple performance of NSPWM is comparable to those of standard PWM methods. The analytical results of PWM performance attributes are verified by computer simulations. During the simulations important performance characteristics such as inverter input and output harmonic content and inverter flux of all RCMV-PWM methods and standard PWM methods are compared and the simulation results are in a strong agreement with theoretical results. Superior performance of NSPWM is verified by the simulation results with low CMV, low output and DC-link current harmonics, and low harmonic flux especially at high M_i and PF.

The third contribution of this thesis involves the modification of the PWM algorithm for the AZSPWM1 method (MAZSPWM) in order to eliminate the output line-to-line voltage pulse pattern problem of the method. Although AZSPWM1 has satisfactory PWM performance attributes, it has bipolar line-to-line voltage pulse pattern and at some operating instants it has insufficient zero-voltage time between the polarity reversals resulting in very high peak voltage overshoots at line-to-line voltages at the motor terminals. In order to eliminate this voltage reflection problem of AZSPWM1 its space vector duty cycles and hence pulse pattern are modified without degrading its PWM performance attributes and RCMV characteristics. The line-to-line voltage

waveforms are investigated by means of laboratory experiments. A 70m cable is inserted between motor and VSI. When utilizing AZSPWM1 very high peak overshoots are resulted on line-to-line voltages at the motor terminals for all M_i. However after the modification, it is observed that peak overshoots of MAZSPWM are reduced to an acceptable value which is comparable with those of SVPWM, DPWM1 and NSPWM.

The fourth contribution of this thesis involves proposition of a combined algorithm of NSPWM and MAZSPWM for superior PWM performance attributes with reduced CMV throughout the inverter hexagon. The NSPWM has a drawback of having a limited voltage linearity range and is incapable of operating with low CMV at low modulation index. MAZSPWM has higher harmonic content than NSPWM but it does not have voltage linearity region drawback and it has superior PWM performance comparing to the RCMV-PWM methods other than NSPWM. Therefore these two methods are combined in a single algorithm such that NSPWM is utilized when it is linear and elsewhere (at low M_i) MAZSPWM is utilized. The combined algorithm is implemented by means of computer simulations and laboratory experiments and it is concluded that this algorithm is practically feasible and it does not result in any problems. Transition from one method to another is achieved smoothly and the motor phase currents are sinusoidal.

The last contribution of this thesis involves the total CMV/CMC reduction in a drive via the combination of simple passive common mode inductor filter and the proposed RCMV combined PWM algorithm. For this purpose common mode inductor filters are designed, built and tested with various PWM methods and the proposed RCMV methods to illustrate the difference between various common mode filters and PWM methods. It is shown with a properly designed small common mode inductor and with the proposed RCMV algorithm, a drive has low CMV and low CMC characteristics resulting in an overall low common mode voltage and current problems.

The work conducted in this research is investigated thoroughly via theory, simulations, and detailed laboratory experiments and strong correlation has been obtained between theory and experiments.

With the motor high frequency models being involved, in this work mainly the PWM effects and their readily measurable effects could be investigated in the theoretical and experimental studies. Further studies are the subject of future research. With the complete effect of the CMV magnitude and dv/dt not completely understood and separated, further work is necessary in this area. The bearing currents, their components, etc. could not be easily measured but only the motor leakage current could be measured and quantified. Establishment of hardware and precise measurement of these effects and their components is an important future work to be conducted.

Overall this thesis contributed to the inverter generated common mode voltage and its effects on the motor drive and proposed effective and economic methods to mitigate these effects on the motor such that the drive and the whole system operate more reliably.

REFERENCES

[1] J.A. Rooks and A.K. Wallace, "Energy efficiency of variable speed drive systems," *IEEE Industry Applications Magazine,* vol. 10, pp. 57-64, May/June 2004.

[2] M.D. Murphy and F. G. Turnbull. *Power electronic control of AC motors.* Pergamon Press, 1988.

[3] J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proceedings of the IEEE,* vol 82, pp. 1194-1214, August 1994

[4] J. Holtz, "Pulsewidth modulation – a survey," *IEEE Trans. on Industrial Electronics,* vol 39, pp. 410-420, October 1992.

[5] A.M. Hava, R.J. Kerkman, and T.A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Trans. on Power Electronics,* vol. 14, pp. 49-61, January 1999.

[6] R.J. Kerkman, D. Leggate, and G.L. Skibinski, "Interaction of drive modulation and cable parameters on AC motor transients," *IEEE Trans. on Industry Applications,* vol. 33, pp. 722-731, May/June 1997.

[7] J.M. Erdman, R.J. Kerkman, D.W. Schlegel, and G.L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Trans. on Industry Applications,* vol. 32, pp. 250-259, March/April 1996.

[8] E. Ün and A.M. Hava, "Performance analysis and comparison of reduced common mode voltage PWM and standard PWM techniques for three phase voltage source inverters," in *Proc. IEEE-APEC'06*, 2006, pp. 303-309.

[9] S. Ogasawara and H. Akagi, "Modeling and damping of high-frequency leakage currents in PWM inverter-fed AC motor drive systems," *IEEE Trans. on Industry Applications*, vol 32, pp. 1105-1114, September/October 1996.

[10] A. Binder and A. Mütze, "Scaling effects of inverter-induced bearing currents in AC machines," in *Proc. IEEE-IEMDC'07,* 2007, pp. 1477-1483.

[11] H. Akagi, H. Hasegawa, and T. Doumoto, "Design and performance of a passive EMI filter for use with a voltage-source PWM inverter having sinusoidal output voltage and zero common-mode voltage," *IEEE Trans. on Power Electronics,* vol 19, pp. 1069-1076, July 2004.

[12] S. Ogasawara, H. Ayano, and H. Akagi, "An active circuit for cancellation of common-mode voltage generated by a PWM inverter," *IEEE Trans. on Power Electronics,* vol 13, pp. 835-841, September 1998.

[13] Y.S. Lai and F.S. Shyu, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: basic development," *IEEE Trans. on Industry Applications,* vol 40, pp.1605-1612, November/December 2004.

[14] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Trans. on Industry Applications,* vol. 35, pp. 469-476, March/April 1999.

[15] E. Ün and A.M. Hava, "A near state PWM method with reduced switching frequency and reduced common mode voltage for three-phase voltage source inverters," in *Proc. IEEE-IEMDC'07,* 2007, pp. 235-240.

[16] A.M. Hava, "Carrier based PWM-VSI drives in the overmodulation region," Ph.D. Thesis, University of Wisconsin-Madison, 1998.

[17] A.M. Hava, R.J. Kerkman, and T.A. Lipo, "A high performance generalized discontinuous PWM algorithm," *IEEE Trans. Industry Applications,* vol. 34, pp. 1059-1071, September/October 1998.

[18] E. Ün and A.M. Hava, "Performance characteristics of the reduced common mode voltage near state PWM method," in *Proc. EPE'07,* 2007, ISBN: 9789075815108.

[19] Ansoft Simplorer V7.0. A power electronics simulation software, Ansoft Corporation.

[20] M. Cacciato, A. Consoli, G. Scarcella, G. Scelba, and A. Testa, "A novel space-vector modulation technique for common mode emissions reduction," in *Proc. ACEMP'07,* 2007, pp. 199-204.

[21] A. Kempski, R. Smolenski, and R. Strzelecki, "Common mode current paths and their modeling in PWM inverter-fed drives," in *Proc. IEEE-PESC'02*, 2002, pp. 1031-1036.

[22] M. Cacciato, A. Consoli, G. Scarcella, S. De Caro, and A. Testa, "High frequency modeling of DC/AC converters," in *Proc. EPE'05,* 2005, ISBN: 9075815085.

[23] A. Nabae, I. Takahashi, and H. Akagi, "A new Neutral-Point-Clamped PWM inverter," *IEEE Trans. on Industry Applications,* vol.17, pp. 518-523, September/October 1981.

[24] B. Üstüntepe, A.M. Hava, "Üç-fazlı üç-düzeyli nötr Noktası bağlantılı evirici ve uygulamaları," *ELECO 2006, Elektrik-Elektronik-Bilgisayar Mühendisliği Sempozyumu,* Bursa, sayfa 126-130, 6-10 Aralık 2006.

[25] H.J. Kim, H.D. Lee, and S.K. Sul, "A new PWM strategy for common mode voltage reduction in neutral-point clamped inverter-fed AC motor drives," *IEEE Trans. on Industry Applications*, vol. 37, pp. 1840 – 1845, November/December 2001.

[26] P.C. Loh, D.G. Holmes, Y. Fukuta, and T.A. Lipo, "Reduced common-mode modulation strategies for cascaded multilevel inverters," *IEEE Trans. on Industry Applications*, vol. 39, pp. 1386 – 1395, September/October 2003.

[27] A. Videt, M.L. Moigne, N. Idir, P. Baudesson, and J. Ecrabey, "A new carrier-based PWM for the reduction of common mode currents applied to neutral-point-clamped inverters," in *Proc. IEEE-APEC'07*, 2007, pp. 1224-1230.

[28] A. Consoli, G. Oriti, A. Testa, and A.L. Julian, "Induction motor modeling for common mode and differential mode emission evaluation," in *Conf. Rec. IEEE-IAS Annual Meeting, 1996,* pp. 595 – 599.

[29] E. Gubia, P. Sanchis, A. Ursua, J. Lopez, and L. Marroyo, "Frequency domain model of conducted EMI in electrical drives," *IEEE Power Electronics Letter,* vol. 3, pp. 45-49, June 2005.

[30] S. Chen, T.A. Lipo, and D. Fitzgerald, "Modeling of motor bearing currents in PWM inverter drives," *IEEE Trans. on Industry Applications,* vol 32, pp. 1365-1370, November/December 1996.

[31] A. Mütze and A. Binder, "Generation of high-frequency common mode currents in machines of inverter-based drive systems," in *Proc. EPE'05,* 2005, ISBN: 9075815085

[32] A. Mütze and A. Binder, "Practical rules for assessment of inverter-induced bearing currents in inverter-fed AC motors up to 500 kW" *IEEE Trans. on Industrial Electronics,* vol 54, pp. 1614-1622, June 2007.

[33] S. Chen and T.A. Lipo, "Circulating type motor bearing current in inverter drives," *IEEE Industry Applications Magazin,* pp. 32-38, January/February 1998.

[34] A. Mütze and A. Binder, "High frequency stator ground currents of inverter-fed squirrel-cage induction motors up to 500 kW," in *Proc. EPE'03,* 2003, ISBN: 9075815077

[35] H. Akagi and S. Tamura, "A passive EMI filter for eliminating both bearing current and ground leakage current from an inverter-driven motor," *IEEE Trans. on Power Electronics,* vol 21, pp. 1459-1469, September 2006.

[36] S. Ogasawara, H. Ayano, and H. Akagi, "Measurement and reduction of EMI radiated by a PWM inverter-fed AC motor drive system," *IEEE Trans. on Industry Applications,* vol 33, pp. 1019-1026, July/August 1997.

[37] H. Akagi and T. Doumoto, "A passive EMI filter for preventing high-frequency leakage current from flowing through the grounded inverter heat sink of an adjustable-speed motor drive system," *IEEE Trans. on Industry Applications*, vol. 41, pp. 1215 – 1223 September/October 2005.

[38] H. Akagi and T. Doumoto, "An approach to eliminating high-frequency shaft voltage and ground leakage current from an inverter-driven motor," *IEEE Trans. on Industry Applications*, vol. 40, pp. 1162 – 1169, July/August 2004.

[39] H. Akagi, "Influence of high dv/dt switching on a motor drive system: a practical solution to EMI issues," in *Proc. ISPSD'04, 2004*, pp. 139-142.

[40] S. Ogasawara and H. Akagi, "Analysis and reduction of EMI conducted by a PWM inverter-fed AC motor drive system having long power cables," in *Proc. IEEE-PESC'00*, 2000, pp. 928-933.

[41] M.M. Swamy, K. Yamada, and T. Kume, "Common mode current attenuation techniques for use with PWM drives," *IEEE Trans. on Power Electronics,* vol. 16, pp. 248-255, March 2001.

[42] N. Hanigovszki, J. Landkildehus, and F. Blaabjerg, "Output filters for AC adjustable speed drives," in *Proc. IEEE-APEC'07*, 2007, pp. 236-242.

[43] A. Mütze and C.R. Sullivan, "Simplified design of common-mode chokes for reduction of motor ground currents in inverter drives," in *Conf. Rec. IEEE-IAS Annual Meeting, 2006,* pp. 2304-2311.

[44] Y. Murai, T. Kubota, and Y. Kawase, "Leakage current reduction for a high-frequency carrier inverter feeding an induction motor," *IEEE Trans. on Industry Applications*, vol. 28, pp. 858 – 863, July/August 1992.

[45] D. Rendusara and P. Enjeti, "New inverter output filter configuration reduces common mode and differential mode dv/dt at the motor terminals in PWM drive systems," in *Proc. IEEE-PESC'97*, 1997, pp. 1269-1275.

[46] C. Mei, J.C. Balda, and W.P. Waite, "Cancellation of common-mode voltages for induction motor drives using active method," *IEEE Trans. on Energy Conversion*, vol. 21, pp. 380 – 386, June 2006.

[47] A. Kempski, R. Smolenski, E. Kot, and Z. Fedyczak, "Active and passive series compensation of common mode voltage in adjustable speed drive system," in *Conf. Rec. IEEE-IAS Annual Meeting, 2004,* pp. 2665-2671.

[48] Y.C. Son and S.K. Sul, "A new active common-mode EMI filter for PWM inverter," *IEEE Trans. on Power Electronics,* vol 18, pp. 1309-1314, November 2003.

[49] David K. Chang. *Fundamentals of engineering electromagnetics.* Addison Wesley, 1993.

[50] H.D. Lee and S.K. Sul, "Common-mode voltage reduction method modifying the distribution of zero-voltage vector in PWM converter/inverter system," *IEEE Trans. on Industry Applications*, vol. 37, pp. 1732-1738, November/December 2001.

[51] A.M. De Broe, A.L. Julian, and T.A. Lipo, "Neutral to grond voltage minimization in a PWM rectifier/inverter configuration," in *Proc. IEE-PEVD'96, 1996,* pp. 564-568.

[52] H.D. Lee and S.K. Sul, "A common mode voltage reduction in boost rectifier/inverter system by shifting active voltage vector in a control period" *IEEE Trans. on Power Electronics,* vol 15, pp. 1094-1101, November 2000.

[53] eZdsp™ F2808 USB Technical Reference, Spectrum Digital, November 2004.

[54] Texas Instruments, "TMS320x280x Enhanced Pulse Width Modulator (ePWM) Module Referance Guide," Literature Number: SPRU791D, November 2004-Revised October 2007.

[55] A.F. Moreira, T.A. Lipo, G. Ventakataramanan, and S. Bernet, "High-frequency modeling for cable and induction motor overvoltage studies in long cable drives," *IEEE Trans. on Industry Applications*, vol 38, pp. 1297-1306, September/October 2002.

[56] G.L. Skibinski, R.J. Kerkman, and D. Schlegel, "EMI emissions of modern PWM AC drives," *IEEE Industry Applications Magazin,* pp. 47-81, November/December 1999.

[57] W. Hofmann and J. Zitzelsberger, "PWM-control methods for common mode voltage minimization - a survey," in *Proc. SPEEDAM'06,* 2006, pp. 8-30 - 8-35.

[58] Y.S. Lai, P.S. Chen, H.K. Lee, and J. Chou, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part II: applications to IM drives with diode front end," *IEEE Trans. on Industry Applications*, vol. 40, pp. 1613-1620, November/December 2004.

[59] Q. Yin, R.J. Kerkman, T.A. Nondahl, and H. Lu, "Analytical investigation of the switching frequency harmonic characteristic for common mode reduction modulator," in *Conf. Rec. IEEE-IAS Annual Meeting, 2005,* pp. 1398-1405.

[60] L.H.Kim, N.K. Hahm, W.C. Lee, J.S. Yu, Y.C. Kim, C.Y. Won, and Y.R. Kim, "Analysis of a new PWM method for conducted EMI reduction in a field oriented controlled induction motor," in *Proc. IEEE-APEC'06*, 2006, pp. 204-210.

[61] Y.S. Lai, "Investigations into the effects of PWM techniques on common mode voltage for inverter-controlled induction motor drives," in *Proc. IEEE-PES Winter Meeting,*1999, pp. 35-40.

[62] Y.S. Lai, "New random technique of inverter control for common mode voltage reduction of inverter-fed induction motor drives," *IEEE Trans. on Energy Conversion* , vol. 14, pp. 1139 – 1146, December 1999.

[63] A.V. Jouanne and H. Zhang, "A dual-bridge inverter approach to eliminating common-mode voltages and bearing and leakage currents," *IEEE Trans. on Power Electronics,* vol 14, pp. 43-48, January 1999.

[64] A. Mütze and H.W. Oh, "Application of static charge dissipation to mitigate electric discharge bearing currents," in *Proc. IEEE-IEMDC'07,* 2007, pp. 1059-1066.

[65] B.A. Welchko, S.E. Schulz, and S. Hiti, “Effects and compensation of dead-time and minimum pulse-width limitations in two-level PWM voltage source inverters,” in *Conf. Rec. IEEE-IAS Annual Meeting, 2006,* pp 889-896.

[66] S. Chen and T.A. Lipo, “Bearing currents and shaft voltages of an induction motor under hard- and soft-switching inverter excitation,” *IEEE Trans. on Industry Applications*, vol 34, pp. 1042-1048, September/October 1998.

[67] A. Mütze and A. Binder, “Don’t lose your bearings – mitigation techniques for bearing currents in inverter-supplied drive systems,” *IEEE Industry Applications Magazine,* vol. 12, pp. 22-31, July/August 2006.

APPENDIX

HDF CALCULATION MATLAB CODE

%SVPWM

```
%Calculate the HDF for SVPWM, for 9 different modulation indices,
%integration in first 30 degree period (space dependency is
%symmetric within 30 degree)

%Modulation index from 0.1 to 0.9
m = 0.1
for n = 1:9,

%Theta is from 0 to 30 (First 30 degree period) at 53 data points
%(total 628 data points per fundamental cycle)
theta = 0:0.01:0.52;

%Calculate duty cycles
d_1 = 0.954 * m * cos(theta) - 0.954 * m * sin(theta) / 1.733;
d_2 = 0.954 * m * sin(theta) / 0.866;
d_7 = (1 - d_1 - d_2) / 2  ;
d_0 = d_7 ;

%Initialize
Harm_flux(i) = zeros(1,53);

%Integrate the harmonic flux vectors.
for i = 1:size(theta,2),
    temp = 0;

    d = 0 : 0.001 : d_7(i);
    y = -m*(cos(theta(i))+j*sin(theta(i))).*d;
    temp = temp + sum(abs(y).^2)*0.001;

    d = d_7(i) : 0.001 : d_7(i)+d_2(i);
    y = -(pi/3)*(cos(pi/3)+j*sin(pi/3))*d_7(i)  +
            ((pi/3)*(cos(pi/3)+j*sin(pi/3))  -
            m*(cos(theta(i))+j*sin(theta(i)))).*d;
    temp = temp + sum(abs(y).^2)*0.001;

    d = d_7(i)+d_2(i) : 0.001 : 1-d_0(i);
    y = -m*(cos(theta(i))+j*sin(theta(i)))*(d_7(i)+d_2(i))  +
            (pi/3)*(cos(pi/3)+j*sin(pi/3))*d_2(i)  +
            ((pi/3)-m*(cos(theta(i))+j*sin(theta(i)))).*(d-d_7(i)-
            d_2(i));
    temp = temp + sum(abs(y).^2)*0.001;

    d = 1-d_0(i) : 0.001 : 1;
    y = pi/3 * (d_1(i) + d_2(i)*(cos(pi/3)+j*sin(pi/3)))  -
            m*(cos(theta(i))+j*sin(theta(i))).*d;
    temp = temp + sum(abs(y).^2)*0.001;
```

```
    Harm_flux(i) = temp;

end

%Calculate and Normalize HDF for an Mi
HDF(n) = ((288/pi^2)/53)*sum(Harm_flux);
mi(n) = m ;

%Mi increment
m = m+0.1

end

%Draw HDF versus Modulation Index
plot(mi,HDF);
```

%END of SVPWM

%NSPWM

```
%Modulation index from 0.6 to 0.9
m = 0.6;
for n = 1:4

%Theta is from 30 to 90 (B2 period) at 105 data points
%(total 628 data points per fundamental cycle)
theta = 0.52:0.01:1.57;

d_1 = 1 - (0.954 * m * sin(theta) * 1.154);
d_2 = -1 + 0.954 * m * cos(theta)+ 0.954 * m * sin(theta) * 1.732;
d_3 = 1 - 0.954 * m * cos(theta) - 0.954 * m * sin(theta) * 0.577;

Harm_Flux(i) = zeros(1,105);

for i = 1:size(theta,2),
    temp = 0;

    d = 0 : 0.001 : d_1(i);
    y = (pi/3).*(d)  -  m*(cos(theta(i))+j*sin(theta(i))).*(d);
    temp = temp + sum(abs(y).^2)/1000;

    d = d_1(i) : 0.001 : d_1(i) + d_2(i);
    y = (pi/3)*(cos(pi/3)+j*sin(pi/3)).*(d-d_1(i))  +
            (pi/3)*d_1(i)  -  m*(cos(theta(i))+j*sin(theta(i))).*d;
    temp = temp + sum(abs(y).^2)/1000;

    d = d_1(i) + d_2(i) : 0.001 : 1;
    y = (pi/3).*(cos(2*pi/3)+j*sin(2*pi/3)).*(d-d_1(i)-d_2(i))  +
            (pi / 3)*(cos(pi/3)+j*sin(pi/3)).*(d_2(i))  +
            (pi/3)*d_1(i)  -  m*(cos(theta(i))+j*sin(theta(i))).*d;
    temp = temp + sum(abs(y).^2)/1000;

    Harm_Flux(i) = temp;

end

HDF(n) = ((288/pi^2)/105)*sum(Harm_Flux);
mi(n)=m ;
m = m+0.1;

end

%Scale with K_f and plot.
plot(mi,0.44*HDF);
```

%END of NSPWM

%AZSPWM1

```
m = 0.1
for n = 1:9,

theta = 0 : 0.01 : 1.04;

d_1 = 0.954 * m * cos(theta) - 0.954 * m * sin(theta) / 1.733;
d_2 = 0.954 * m * sin(theta) / 0.866;
d_3 = (1 - d_1 - d_2) / 2  ;
d_6 = d_3 ;
Harm_Flux = zeros(1,105);

for i = 1:size(theta,2),
    temp = 0;

    d = 0 : 0.001 : d_3(i);
    y = (pi/3).*(cos(2*pi/3)+j*sin(2*pi/3)).*d  -
            m*(cos(theta(i))+j*sin(theta(i))).*d;
    temp = temp + sum(abs(y).^2)/1000;

    d = d_3(i) : 0.001 : d_3(i) + d_2(i);
    y = (pi/3)*(cos(pi/3)+j*sin(pi/3)).*(d-d_3(i))  +
            (pi/3)*d_3(i)*(cos(2*pi/3)+j*sin(2*pi/3))  -
            m*(cos(theta(i))+j*sin(theta(i))).*d;
    temp = temp + sum(abs(y).^2)/1000;

    d = d_3(i) + d_2(i) : 0.001 : 1 - d_6(i);
    y = (pi/3)*d_2(i)*(cos(pi/3)+j*sin(pi/3))  +
            (pi/3)*d_3(i)*(cos(2*pi/3)+j*sin(2*pi/3))  +
            (pi/3).*(d-d_3(i)-d_2(i))  -
            m*(cos(theta(i))+j*sin(theta(i))).*(d);
    temp = temp + sum(abs(y).^2)/1000;

    d = 1 - d_6(i) : 0.001 : 1;
    y = (pi/3)*(d_1(i) + d_2(i)*(cos(pi/3)+ j*sin(pi/3))  +
            d_3(i)*(cos(2*pi/3)+j*sin(2*pi/3))  +
            (cos(5*pi/3)+j*sin(5*pi/3)).*(d-d_1(i)-d_2(i)-d_3(i))) -
            m*(cos(theta(i))+j*sin(theta(i))).*d;
    temp = temp + sum(abs(y).^2)/1000;

    Harm_Flux(i) = temp;

end
HDF(n) = ((288/pi^2)/105)*sum(Harm_Flux);
mi(n)=m ;
m = m+0.1;
end

plot(mi,HDF);
```

%END of AZSPWM1