# SERIES ACTIVE FILTER DESIGN, CONTROL, AND IMPLEMENTATION WITH A NOVEL LOAD VOLTAGE HARMONIC EXTRACTION METHOD

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## ABSTRACT

SERIES ACTIVE FILTER DESIGN, CONTROL, AND IMPLEMENTATION WITH A NOVEL LOAD VOLTAGE HARMONIC EXTRACTION METHOD

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Series Active Filters (SAF) are designed for harmonic isolation and load voltage regulation of single-phase and three-phase voltage harmonic source type nonlinear loads. The novel Absolute Value Method (AVM) for load voltage harmonic extraction is proposed and applied in the control algorithm of SAF. The SAF compensated systems are represented by simplified linear models such that SAF controller gains can be easily determined. Harmonic isolation and load voltage regulation performances of 2.5 kW single-phase and 10 kW three-phase SAF compensated systems are evaluated by detailed simulations. Laboratory prototype single-phase and three-phase SAFs and loads are designed and manufactured. Digital signal processor based control platform is employed. Exclusive laboratory tests are conducted. Via laboratory experiments and simulations it is shown that AVM yields superior harmonic isolation and load voltage regulation performance compared to the conventional low/high pass filtering method. Theory, simulations, and experiments are well correlated and illustrate the feasibility of the proposed method.



Keywords: Series active filter, harmonic extraction, absolute value method, voltage harmonics, voltage sag, unbalance, voltage source inverter, series injection transformer, switching ripple filter, discrete time control, rectifier.

# ÖZ


ÖZGÜN YÜK GERİLİMİ AYRIŞTIRMA YÖNTEMİ KULLANILAN
SERİ ETKİN SÜZGEÇ TASARIMI, DENETİMİ VE GERÇEKLEŞTİRİLMESİ

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Seri Etkin Süzgeç (SES), tek-faz ve üç-faz gerilim harmoniği kaynağı türündeki doğrusal olmayan yüklerin harmonik yalıtımını ve yük gerilimi düzeltimini yapmak üzere tasarlanmıştır. Özgün Mutlak Değer Yöntemi (MDY) yük gerilimi harmoniği ayrıştırması için önerilmiştir ve denetim algoritmasında uygulanmıştır. SES'in denetçi kazançlarının kolaylıkla belirlenebilmesi için basitleştirilmiş doğrusal modeller kullanılmıştır. 2.5 kW tek-faz ve 10 kW üç-faz SES ile denetlenen sistemlerin harmonik yalıtımı ve yük gerilimi düzeltimi başarımları ayrıntılı benzetimler ile değerlendirilmiştir. Tek-faz ve üç-faz SES'lerin ve yüklerin laboratuvar prototipleri tasarlanmış ve üretilmiştir. Denetim için sayısal işaret işlemci tabanlı platform kullanılmıştır. Ayrıntılı deneysel çalışmalar yapılmıştır. Laboratuvar deneyleri ve benzetimler ile geleneksel alçak/yüksek geçirgen süzgeç yöntemine göre MDY'nin üstün harmonik yalıtımı ve yük gerilimi düzeltimi başarımı gösterilmiştir. Teori, benzetim ve deney sonuçları arasındaki kuvvetli uyum, önerilen yöntemin uygulanabilirliğini göstermektedir.



Anahtar Kelimeler: Seri etkin süzgeç, harmonik ayrıştırma, mutlak değer yöntemi, gerilim harmoniği, gerilim çökmesi, dengesizlik, gerilim kaynaklı evirici, seri transformatör, anahtarlama dalgacık süzgeci, ayrık zamanlı denetim, doğrultucu.

*To my family*

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| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| ASD | Adjustable Speed Drive |
| AVM | Absolute Value Method |
| CM | Conventional Method |
| DSP | Digital Signal Processor |
| DVR | Dynamic Voltage Restorer |
| FCC | Fundamental Component Controller |
| HFE | Harmonic/Fundamental Extractor |
| HIC | Harmonic Isolation Controller |
| HPF | High-Pass Filter |
| IGBT | Insulated Gate Bipolar Transistor |
| IPM | Intelligent Power Module |
| LPF | Low-Pass Filter |
| NF | Notch Filter |
| P | Proportional |
| PAF | Parallel Active Filter |
| PCC | Point of Common Coupling |
| PF | Power Factor |
| PI | Proportional-Integral |
| PLL | Phase Locked Loop |
| PWM | Pulse Width Modulator |
| RDC | Resonance Damping Controller |
| SAF | Series Active Filter |
| SIT | Series Injection Transformer |
| SPAVM | Single-Phase Absolute Value Method |
| SPSAF | Single-Phase Series Active Filter |

| | |
|---|---|
| SPFB | Single-Phase Full-Bridge |
| SRF | Switching Ripple Filter |
| TDD | Total Demand Distortion |
| THD | Total Harmonic Distortion |
| TPAVM | Three-Phase Absolute Value Method |
| TPSAF | Three-Phase Series Active Filter |
| UPQC | Unified Power Quality Conditioner |
| UPS | Uninterruptible Power Supply |
| V-type | Harmonic Voltage Source Type |
| VSI | Voltage Source Inverter |

# CHAPTER 1

# INTRODUCTION

## 1.1. Background

The electric power quality in a power system is determined by the quality of the voltage waveform supplied by the utility and the quality of the current waveform drawn by the load. The power quality is perfect as long as a utility supplies the load with rated voltage at rated frequency such that a pure sinusoidal voltage is applied to the load and the load draws sinusoidal currents at rated frequency and in phase with the voltage supplied by the utility. Nevertheless, in practice, neither utilities provide the voltage with perfect power quality nor loads draw current with perfect power quality.

Power quality problems are defined as problems manifested in voltage, current, or frequency deviations that result in failure or misoperation of customer equipment. These problems can be classified into two groups considering sources of problems: utility and load related problems. Utility related problems are mainly interruption, voltage sag (undervoltage), voltage swell (overvoltage), voltage unbalance (imbalance), and voltage fluctuation (flicker). Load related problems are load harmonic current and excess of reactive current [1], [2], [3].

In order to mitigate the power quality problems, i.e., to enhance the power quality, power system authorities and customers share the responsibility. The authorities should take such measures as better system planning, operation, and protection against problems related to utility. In parallel to this, the authorities should also force

customers to take measures such as using harmonic current and reactive power compensators. Moreover, the customers may/should use extra equipments such as generators and voltage regulators to protect their loads from any problem which may occur in a power system. As a consequence, the customers should provide both compensation for their reactive and harmonic power and protection from the problems originating from the power system.

Customers should have the uppermost awareness of the power quality because they may be both the source and the victim of a power quality problem. For example, loads with front-end diode/thyristor rectifiers such as Adjustable Speed Drives (ASDs), Uninterruptible Power Supplies (UPSs) and converters of electronic devices draw considerable amount of harmonic current such that they distort voltage waveform at the point of common coupling (PCC), where other loads of the same (or other) customer are connected to the utility, as shown in Figure 1.1. If the harmonic creating customer has also a voltage distortion sensitive load, this distorted voltage mostly affects the customer who is the source of the problem. Other harmonic sensitive loads connected to the same PCC are likewise affected from this power quality problem. Consequently, customers should determine their power quality requirements and the requirements imposed by the authority and then apply a viable solution satisfying both requirements.

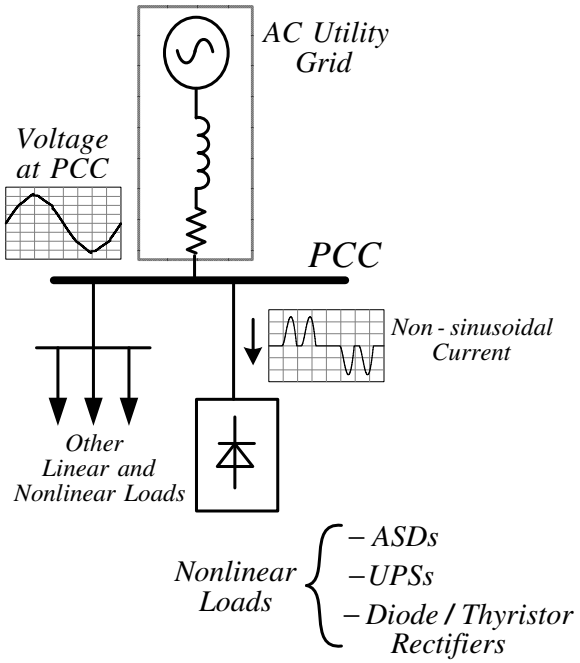



Figure 1.1 Illustration of harmonic distortion problems at the point of common coupling (PCC).

In order to classify and evaluate the power quality problems, some power quality criteria should be taken into account. In IEEE 1159 utility voltage variation and in IEEE 519 harmonic control related recommended practices define the power quality problems related to utility and loads, respectively. For reactive power, the limits of the local authority (for example, Energy Market Regulatory Authority (EMRA-EPDK) in Turkey) are considered. According to IEEE 1159, the classification of voltage magnitude variation considering the problem duration is given in Table 1.1. It can be seen from the table that a deviation larger than 0.1 pu of the voltage from the rated value is considered as problematic and classified as sag or swell condition [1].

In IEEE 519, the harmonic content of a waveform is defined by Total Harmonic Distortion (THD). The THD of a current waveform is defined as

$$THD_I = \frac{\sqrt{\sum_{h=2}^{h_{max}} I_h^2}}{I_1} \tag{1.1}$$

where the $I_h$ is the rms value of the current harmonics and $I_1$ is the rms value of the fundamental current. Similarly, the THD of a voltage waveform is defined as

$$THD_V = \frac{\sqrt{\sum_{h=2}^{h_{max}} V_h^2}}{V_1} \tag{1.2}$$

where $V_h$ is the rms value of the voltage harmonics and $V_1$ is the rms value of the fundamental voltage. Moreover, another definition called Total Demand Distortion (TDD) is introduced because nonlinear loads have very high $THD_I$ under light loading inspite of limited voltage harmonic distortion effect on the utility. TDD is defined as

$$TDD = \frac{\sqrt{\sum_{h=2}^{h_{max}} I_h^2}}{I_L} \tag{1.3}$$

where $I_h$ is the rms value of current harmonics and $I_L$ is the rated rms value of the fundamental load current. The harmonic current limits recommended by IEEE 519 are expressed in terms of TDD and given in Table 1.2 for customers. In the table, short circuit ratio ($I_{SC}/I_L$) is used to define the TDD limits for the customers at different power utilization levels. The recommended THD limits for the utility voltage at different voltage levels are tabulated in Table 1.3. As for reactive power limits, EMRA limitations are 0.25 for the ratio of to real power inductive reactive power, which means inductive power factor of 0.97, and 0.15 for the ratio of capacitive reactive power to real power, which means capacitive power factor of 0.99 [1], [2], [4], [5].

Table 1.1 IEEE 1159 voltage variation limits

| Category | | Typical duration | Typical voltage magnitude |
|---|---|---|---|
| Instantaneous | Sag | 0.5 – 30 cycles | 0.1 – 0.9 pu |
| | Swell | 0.5 – 30 cycles | 1.1 – 1.8 pu |
| Momentary | Interruption | 0.5 – 3 s | < 0.1 pu |
| | Sag | 0.5 – 3 s | 0.1 – 0.9 pu |
| | Swell | 0.5 – 3 s | 1.1 – 1.4 pu |
| Temporary | Interruption | 3 s – 1 min | < 0.1 pu |
| | Sag | 3 s – 1 min | 0.1 – 0.9 pu |
| | Swell | 3 s – 1 min | 1.1 – 1.2 pu |
| Long duration | Interruption | > 1 min | 0.0 pu |
| | Sag (Undervoltage) | > 1 min | 0.8 – 0.9 pu |
| | Swell (Overvoltage) | > 1 min | 1.1 – 1.2 pu |
| Voltage unbalance (Imbalance) | | Steady-state | 0.5 – 2 % |
| Voltage fluctuation (Flicker) | | Intermittent | 0.1 – 7 % (< 25 Hz) |

Table 1.2 IEEE 519 harmonic current limits

| $I_{SC}/I_{L1}$ | h<11 | 11≤h<17 | 17≤h<23 | 23≤h<35 | 35≤h | TDD (%) |
|---|---|---|---|---|---|---|
| <20 | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0 |
| 20-50 | 7.0 | 3.5 | 2.5 | 1.0 | 0.5 | 8.0 |
| 50-100 | 10.0 | 4.5 | 4.0 | 1.5 | 0.7 | 12.0 |
| 100-1000 | 12.0 | 5.5 | 5.0 | 2.0 | 1.0 | 15.0 |
| >1000 | 15.0 | 7.0 | 6.0 | 2.5 | 1.4 | 20.0 |

Table 1.3 IEEE 519 voltage distortion limits

| Bus voltage at PCC | Individual harmonic component (%) | THD (%) |
|---|---|---|
| 69kV and below | 3.0 | 5.0 |
| 69.001kV through 161kV | 1.5 | 2.5 |
| 161.001kV and above | 1.0 | 1.5 |

Once the power quality problems of a particular load are characterized by means of the criteria given, the power quality conditioning solution(s) to the problems can be determined. Power quality conditioners reported in literature can be classified into two: passive power quality conditioners and active power quality conditioners. Passive power quality conditioners involve either uncontrolled or limited-controlled power circuits such as passive tuned filters for harmonic mitigation, capacitor banks for reactive power compensation, and tap-changing transformers for voltage sag correction [3]. Active power quality conditioners involve high performance power electronics circuits consisting of passive components, power semiconductor switches, and controllers. Active power quality conditioners are divided into two groups based on their functionality. The first group includes active filters, which are designed to mitigate harmonic problems. These are the well known Series Active Filter (SAF), Parallel Active Filter (PAF), and hybrid active filters [6], [7], [8]. The second group includes power electronics circuits, which are designed to correct the utility voltage variations and they are devices such as thyristor tap changer based voltage regulator, UPS, and Dynamic Voltage Restorer (DVR) [3], [9], [10]. The Unified Power Quality Conditioner (UPQC), which is formed by back to back connection of a SAF and a PAF, is an active power quality conditioner providing solution for both utility and load caused power quality problems [11] and therefore can be considered as a universal solution to power quality problems.

Among the active solutions, PAF, DVR, and SAF represent three established approaches to power quality problems. A PAF connected in shunt at the PCC of a harmonic current source type nonlinear load, i.e., a diode/thyristor rectifier with a DC and/or AC inductor, as shown in Figure 1.2 compensates for the harmonic and/or reactive power demand of the load via supplying harmonic current, reactive current, and load unbalance current (by taking advantage of high impedance of the load with respect to the impedance of the utility). However, PAF is not suitable for voltage harmonic type (V-type) loads, such as diode rectifiers with DC capacitor because the impedance of the load is very low (with respect to the utility). For such loads, PAF can be applied to the load after adding AC and/or DC side inductors to change the

type of the load to current harmonic source or SAF is applied between the utility and the load, as shown in Fig 1.3. A SAF injects a series harmonic compensation voltage between the utility and the load such that it cancels the voltage harmonics and eliminates the harmonic currents [5], [6].

A DVR is connected between the utility and the load in the same manner as a SAF. Its power circuit topology is the same. Nonetheless, DVR corrects only the fundamental component of the load voltage and solves power quality problems related to the utility such as utility voltage sag, swell, and unbalance. Since SAF and DVR have the same circuit topology, SAF can be used as both harmonic mitigator and voltage corrector by adding a fundamental voltage control algorithm to SAF. Thus, SAF can provide a solution for both the utility and load related power quality problems and has more functionalities than PAF and DVR [12], [13], [14]. This thesis will be concerned with SAF. Therefore, in the following the topology, controller, and application of SAF are reviewed.

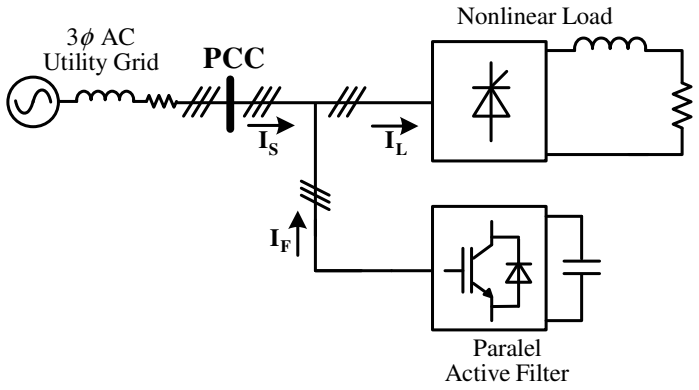



Figure 1.2 The parallel active filter basic connection diagram.

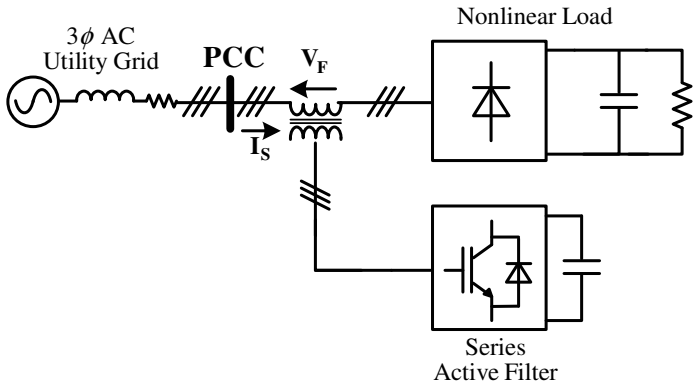



Figure 1.3 The series active filter basic connection diagram.

## 1.2. Series Active Filter

SAF isolates the harmonic voltages of a nonlinear load and utility from each other such that harmonic current flow is prohibited and it regulates the load voltage against the voltage variations of the utility. Shown in Figure 1.4, the circuit topology and control of the SAF are described briefly as follows.

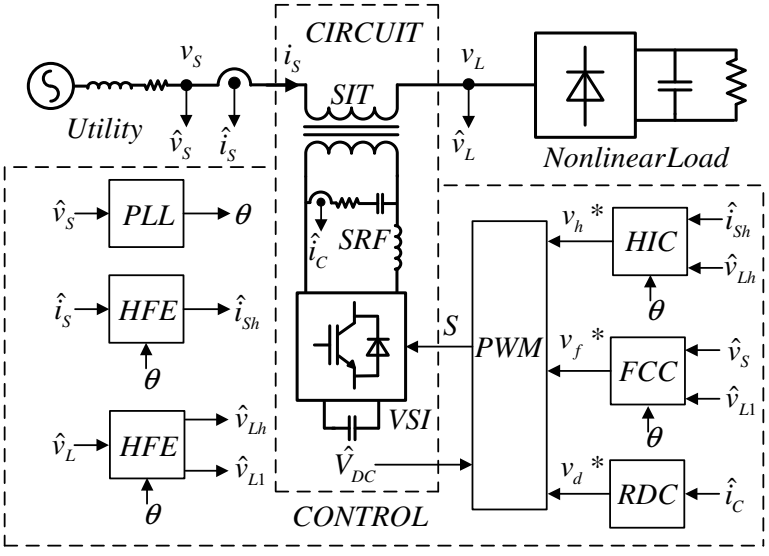



Figure 1.4 The power circuit and the control system of SAF.

Although the power circuit of SAF depends on whether it is designed for single-phase or three-phase loads, the main circuit blocks remain the same for either case. The main circuit blocks are Voltage Source Inverter (VSI), Switching Ripple Filter (SRF), and Series Injection Transformer (SIT), as shown in Figure 1.4 in the single-phase configuration. The function of each block is explained in the following.

The VSI synthesizes a voltage that is equal to the reference, which is generated by the control algorithm, via pulse width modulation. Thus, the output of the inverter consists of high frequency rectangular voltage. Connected to the VSI output terminals, the SRF filters out the high frequency PWM components of the VSI output voltage. The SIT applies the voltage filtered out by the SRF between the utility and the load. Thus, galvanic isolation is provided between the VSI and the utility-load system. This galvanic isolation is beneficial to a single-phase SAF (SPSAF) when the DC bus is fed from a converter through the utility and to a three-phase SAF (TPSAF) when multi-inverter units are fed from the same DC bus. Furthermore, the SIT provides voltage & current matching between the primary side (the VSI side) and the secondary (the utility-load side) [13], [14], [15] such that compensation becomes efficient. The thyristor by-pass and other auxiliary components which are the auxiliary elements of the SAF system are left out from this discussion and will be elaborated in later stages.

The SAF control system consists of six main units. Shown in Figure 1.4, these are Harmonic Isolation Controller (HIC), Fundamental Component Controller (FCC), Resonance Damping Controller (RDC), Pulse Width Modulator (PWM), Phase Locked Loop (PLL), and Harmonic/Fundamental Extractor (HFE).

The HIC aims to block harmonic current flow between the utility and the load and it uses the line current harmonic ($i_{Sh}$) and the load voltage harmonic ($v_{Lh}$) signals as inputs in order to generate the voltage reference for harmonic isolation. The FCC is designed to isolate the fundamental component voltage problems of the utility from the load. Its inputs are the utility and the load fundamental voltage ($v_{S1}$ & $v_{L1}$) signals and its output is the voltage reference for load voltage regulation. The purpose of the

RDC is to maintain stable operation of the SRF by damping out the resonance between the L and C filter elements in the SRF by means of the capacitor current ($i_C$) feedback. The PWM unit receives the sum of the reference voltages generated by the control algorithms and it generates on/off signals for the switches of the VSI. The PLL unit generates the phase angle information ($\theta$) of the utility voltage. The phase angle is required to realize the control in the synchronous reference frame ('de-qe' frame) [11], [13], [14].

The HFE unit is vital for the controllers as it quantifies the amount of distortion to be compensated by the controllers. Thus, the performances of the controllers depend on fast and accurate signal decomposition the HFE provides. In this thesis, two methods for the extraction are considered; the Conventional Method (CM) and the novel Absolute Value Method (AVM). In CM, signal decomposition is based on low/high-pass filtering (LPF/HPF) of the signals in 'de-qe' frame [5], [16]. Therefore, the bandwidth and the accuracy of the signal decomposition depend on the cut-off frequency of the LPF (or the HPF) such that the higher the cutoff, the wider the bandwidth, and the less the accuracy. In this thesis, the load harmonic current is extracted by means of CM without alternative. Unlike the load harmonic current extraction, the load harmonic and fundamental voltages voltage extraction can be provided via either CM or AVM with the latter yielding superior overall performance results. As will be shown throughout the thesis, unlike CM, AVM decomposes the harmonic and the fundamental components of the load voltage with high bandwidth and high accuracy. Thus, the HIC and the FCC performances become very satisfactory.

### 1.3. Scope of The Thesis

With the main focus involving the control algorithms, this thesis is dedicated to analysis, design, control, and implementation of SPSAF and TPSAF for isolating harmonic voltages of single-phase and three-phase voltage type nonlinear loads and isolating voltage sags such that the line current is harmonic-free and the load voltage

is well regulated and therefore high power quality is maintained on both sides of the power system.

The main contribution of the thesis is the development of the novel Absolute Value Method (AVM) which is utilized in the HFE unit for the load voltage. With AVM, which utilizes the geometric properties of rectangular load voltage waveforms to do signal decomposition, both the harmonic and fundamental components of the load voltage are extracted fast and accurately such that the steady-state and dynamic performance of the SAF are improved significantly compared to when using CM. The method is suitable for both SPSAF and TPSAF applications involving diode rectifier loads with a DC bus capacitor (V-type loads). With the main contribution of the thesis involving AVM, the thesis will focus on illustrating the performance of SAF with AVM and CM and provide a comparison by means of theory, simulation, and laboratory experiments.

In the thesis, two SAF circuits, SPSAF and TPSAF, are studied. The first circuit is the single-phase circuit connected between a 2.5 kW single-phase diode rectifier type load and 220 V – 50 Hz utility. The second circuit is the three-phase circuit connected between a 10 kW diode rectifier type load and 380 V - 50 Hz utility. The second circuit simply consists of three identical single-phase circuits considered in the first case. In both cases AVM and CM will be considered and thoroughly studied.

The thesis is organized as follows.

In the second chapter, the power circuit and the control algorithms of SAF are described in detail. Then the conventional fundamental/harmonic extraction methods are reviewed and their attributes are discussed. Then, AVM is introduced and discussed in detail for single-phase and three-phase cases. With the theory completed, first the SAF compensated system is simplified via low frequency and high frequency linear models for the purpose of controller design (controller parameter determination), then the following chapters concentrate on the performance evaluation of the proposed method and comparison with CM.

In the third chapter, the linear models at low frequency and high frequency of the SAF systems are built separately for both CM and AVM. Through these models, HIC and RDC are designed by linear analysis of the high frequency linear model. Likewise, FCC is designed by linear analysis of the low frequency linear model. Additionally, the simulations of the low frequency models are conducted and the results are reported for CM and AVM. The latter's superiority is illustrated.

In the fourth chapter, the Ansoft-Simplorer software based detailed computer simulations of the above described single-phase and three-phase systems are conducted. Results are reported for both AVM and CM and the superior performance of SAF with AVM is verified for single-phase and three-phase cases. With the comparison of these results with the simulation results of the low frequency model, the eligibility of the low frequency model is confirmed.

In the fifth chapter, the experimental studies are reported. The laboratory system is described and laboratory test results for SPSAF and TPSAF are presented. Correlation between the simulation results of the previous chapter and the experimental results is verified and the superior performance of the SAF with AVM over the one with CM is proven.

The final chapter summarizes the contributions of the thesis, provides the concluding remarks, and recommends future work.

# CHAPTER 2

# THE SERIES ACTIVE FILTER

## 2.1 Introduction

The Series Active Filter (SAF) is a power electronics solution to such power quality problems as load harmonic current flow and voltage magnitude variation such that it operates as a harmonic isolator between a nonlinear load and utility and a load voltage regulator. Especially, the application of SAF is suitable for the harmonic voltage source type (V-type) nonlinear loads [5], [6]. In this thesis, single-phase and three-phase diode bridge rectifiers with RC load are used as V-type nonlinear loads and power quality improvement is provided via SAF. These loads and their characteristic line current and load voltage waveforms are as shown in Figure 2.1.

In this Chapter, the theory, the power circuit, and the control of SAF are discussed for single-phase and three-phase systems in detail. First, the theory of SAF is discussed under the titles of harmonic isolation and load voltage variation regulation. Secondly, the components of the power circuit are described along with the design rules for the component ratings. Lastly, the controllers of SAF are introduced to control the power circuit such that SAF eliminates the harmonic current flowing between the utility and a nonlinear load and regulates the load fundamental voltage against the utility voltage variations. As a very important part of a SAF control algorithm, the signal decomposition algorithm is given particular attention and decomposition methods of the fundamental and the harmonic components of the load voltage are discussed in detail. Then a novel signal decomposition method, the Absolute Value Method (AVM), is developed as an application-specific method and

the details of AVM are covered. In this chapter, throughout the investigations, the single-phase and three-phase systems are studied in parallel with the former being considered first.

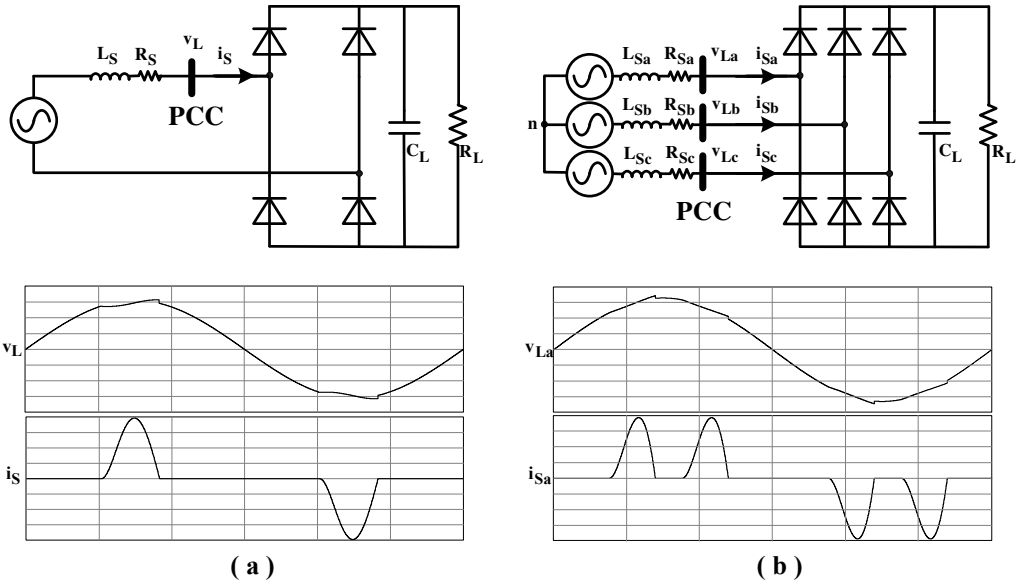



Figure 2.1 The circuit configuration of diode rectifiers and their characteristic waveforms; (a) single-phase and (b) three-phase.

## 2.2 The Theory of SAF

SAF is a power quality conditioner for both load and utility sides. For a V-type nonlinear load, a SAF conditions the power quality in two ways; it provides voltage harmonic isolation between the load and the utility and it provides load voltage regulation against the utility voltage variations. The theory of SAF is discussed with the aid of the single-phase Thévenin's equivalent circuits of the utility and the load and SAF is represented as a superposition of the harmonic and fundamental components of voltage and currents magnitudes, as shown in Figure 2.2. In the figure, $Z_S$ and $Z_L$ represent the practically very small impedances of the utility and the load,

respectively. The voltages and currents are defined as a superposition of the harmonic and the fundamental frequency components. For example, the load voltage ($v_L$) is the sum of the load fundamental ($v_{L1}$) and the load harmonic ($v_{Lh}$) voltages. The utility voltage ($v_S$) and the line current ($i_S$) are described likewise. The signals with the " ^ " sign on top are signals that are either measured signals or signals that are obtained after the measured signals are decomposed. The primed signals (signals with " ′ " on top) are internal signals which are not directly reachable.

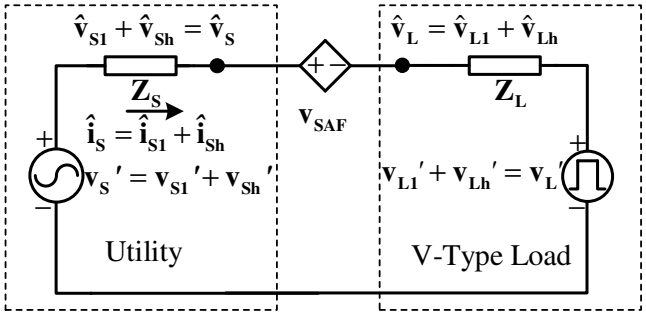



Figure 2.2 The Thévenin's equivalent circuit representation of the utility, SAF, and V-type nonlinear load.

### 2.2.1 Harmonic Isolation

The voltage harmonic isolation by SAF is based on two control principles. The first principle is that SAF emulates a virtual resistor ($K_{hi}$) for the line harmonic current ($i_{Sh}$) (which is the same as the load harmonic current). This requires the measurement of the line current and the decomposition of its harmonic component. The second principle is that SAF applies the load harmonic voltage ($v_{Lh}$) with opposite sign to the measured and decomposed load harmonic voltage value. This principle can be regarded as a feedforward controller while the first one acts as a feedback controller. The total control rule for the harmonic isolation is given in (2.1). Applying this reference voltage ($v_{SAFh}$*) between the utility and the load in series, the equivalent circuit for the harmonic quantities is analyzed in frequency domain. As found in (2.2),

$i_{Sh}$ approaches zero provided that $K_{hi} >> Z_S + Z_L$ and $K_{hv} = 1$.

$$v_{SAFh}^{*} = K_{hi} \cdot \hat{i}_{Sh} - K_{hv} \cdot \hat{v}_{Lh} \tag{2.1}$$

$$I_{Sh} = \frac{V'_{Sh} - V'_{Lh} - V_{SAFh}^{*}}{Z_S + Z_L} \approx \frac{V'_{Sh} - V'_{Lh} + K_{hv} \cdot \hat{V}_{Lh}}{K_{hi} + Z_S + Z_L} \approx 0 \tag{2.2}$$

The load internal harmonic voltage and load terminal harmonic voltage are related with the impedance voltage division equation given in (2.3). According to this equation, if $K_{hi}$ becomes dominant compared to the physical impedances of the circuit, the load terminal harmonic voltage approaches the load internal harmonic voltage. In this case, the load terminal harmonic voltage $v_{Lh}$ can be successfully utilized in the feedforward controller of the SAF to cancel the load harmonic voltage.

$$\hat{V}_{Lh} = V'_{Lh} \frac{K_{hi} + Z_S}{K_{hi} + Z_L + Z_S}, \; where \; V'_{Sh} = 0 \; , \; K_{hv} = 0 \tag{2.3}$$

With the harmonic isolation rule, SAF isolates the harmonic voltage of the load and suppresses the line harmonic current. As shown in Figure 2.3, the load voltage waveforms become rectangular-shaped and the line currents become sinusoidal for the single and three-phase cases provided that perfect isolation is maintained. As the current becomes more sinusoidal, the conduction time of each rectifier diode increases and the absolute value of the load voltage approaches the DC bus voltage of the rectifier for the single-phase SAF (SPSAF). For the three-phase case, the sum of the absolute values of any two load voltages approaches the DC bus voltage. For three-phase SAF (TPSAF), the load voltage waveform is a 6-step waveform since each diode conducts for 120˚.

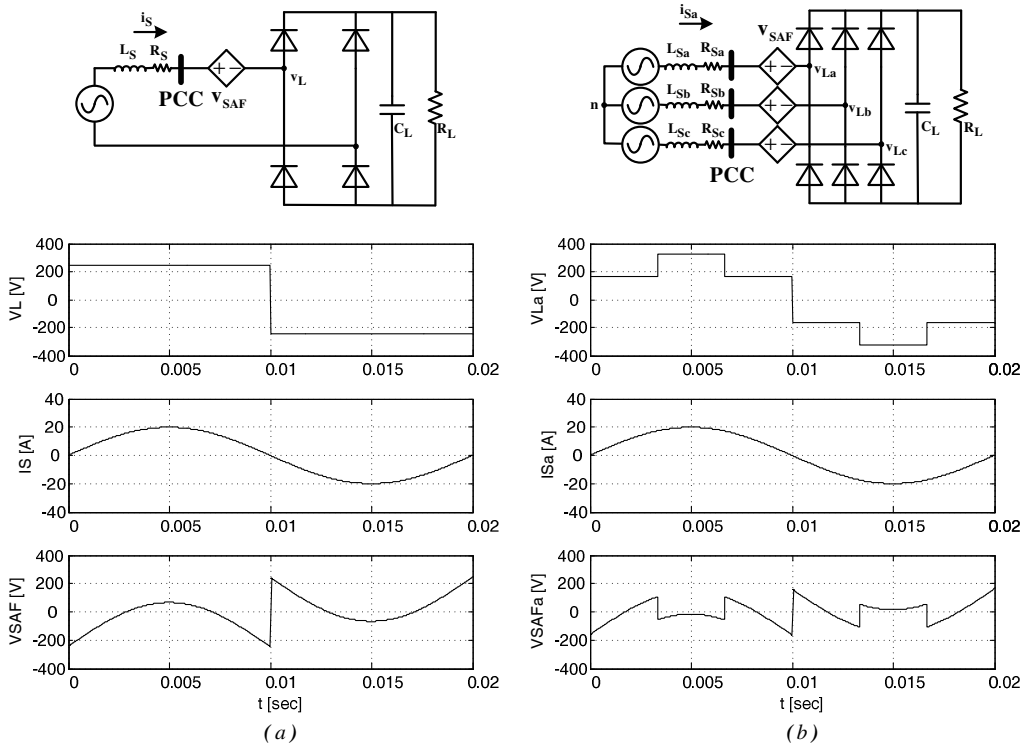



Figure 2.3 Perfect load voltage harmonic isolations for (a) single-phase and (b) three-phase diode bridge rectifiers.

Under the perfect harmonic isolation condition, the mathematical relations between the load voltage and the line voltage for the single-phase and three-phase cases can be found by means of the active power transfer from the utility to the load during a quarter period (since there is a quarterwave symmetry in the power waveforms) by using (2.4). The relations are found as given in (2.5) and (2.6) for the single-phase and the three-phase loads, respectively. These characteristic equations will be utilized later in the design and controller development study.

$$\int_0^{\pi/2} P_S(\theta)d\theta = \int_0^{\pi/2} P_L(\theta)d\theta \tag{2.4}$$

$$\int_0^{\pi/2} V_{S1}\sin\theta \cdot I_{S1}\sin\theta d\theta = \int_0^{\pi/2} V_{L,dc}\cdot I_{S1}\sin\theta d\theta \Rightarrow V_{L,dc} = \frac{\pi}{4}V_{S1} \tag{2.5}$$

$$\int_0^{\pi/2} V_{S1}\sin\theta \cdot I_{S1}\sin\theta d\theta = \int_0^{\pi/3} \frac{V_{L,dc}}{2}\cdot I_{S1}\sin\theta d\theta + \int_{\pi/3}^{\pi/2} V_{L,dc}\cdot I_{S1}\sin\theta d\theta \Rightarrow V_{L,dc} = \frac{\pi}{3}V_{S1} \tag{2.6}$$

### 2.2.2 Load Voltage Regulation

The load voltage regulation involves the control of the fundamental component of load voltage. Therefore, the fundamental component model of the Thévenin equivalent circuit of Figure 2.2 is taken into account. In order to analyze the circuit and design the controllers for the fundamental frequency AC quantities, the fundamental frequency equivalent circuit should be revised by three assumptions. The first assumption is that the system is assumed to be linear such that the nonlinear behavior of the load is canceled by the harmonic voltage isolation. The second assumption is that the fundamental frequency AC quantities can be represented with their peak values (or a DC quantity proportional to the peak) by an appropriate space-vector transformation. The last assumption is that there is no coupling between the space vector transformed quantities. Using these assumptions, all the AC quantities in the fundamental frequency circuit can be defined as DC quantities. The viability of these assumptions will be investigated in the control implementation section.

In order to regulate the load fundamental voltage ($v_{L1}$), a feedback controller ($G_C(s)$) can be utilized to reject disturbances originating from the load and/or the utility. Moreover, in order to reject the line voltage disturbances, a feedforward controller for the line fundamental frequency voltage ($v_{S1}$) can be used. Using these controllers, the reference voltage generated for the load voltage regulation in s-domain ($V_{SAFf}^*(s)$) is given in (2.7). The feedback controller $G_C(s)$ will be elaborated on in later sections of this chapter in detail.

$$V_{SAFf}^*(s) = G_C(s)\left(\hat{V}_{L1}(s) - V_{L1}^*\right) + \left(\hat{V}_{S1}(s) - V_{S1}^*\right) \tag{2.7}$$

After generating the reference voltage for the harmonic isolation and the load voltage regulation, the power circuit of the SAF system realizes this reference voltage such that the power conditioning is achieved. In the following the power circuit of the SAF system is discussed in detail.

### 2.3 The Power Circuit of SAF

The power circuit of SAF is composed of three main power units and auxiliary units. The main power units per phase are a voltage source inverter (VSI), a series injection transformer (SIT), and a switching ripple filter (SRF). The auxiliary units are a thyristor by-pass circuit per phase and if utilized an auxiliary power supply or energy storage element.

The power circuit of SAF in the single-phase form is shown in Figure 2.4. The main units are involved in generating the SAF voltage to condition the power quality and will be detailed in this section. The thyristor by-pass circuit is used to disconnect SAF from the line and load pair for maintenance and protection purposes. The auxiliary power supply or energy storage element is necessary when the continuous real power transfer between the SAF and the rest of the system is required (such as line voltage sag/swell conditions). In this work a diode rectifier fed from the three-phase AC line will be utilized as auxiliary power supply.

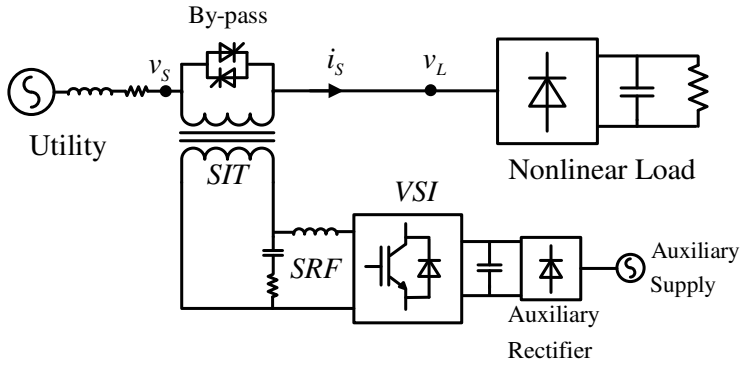
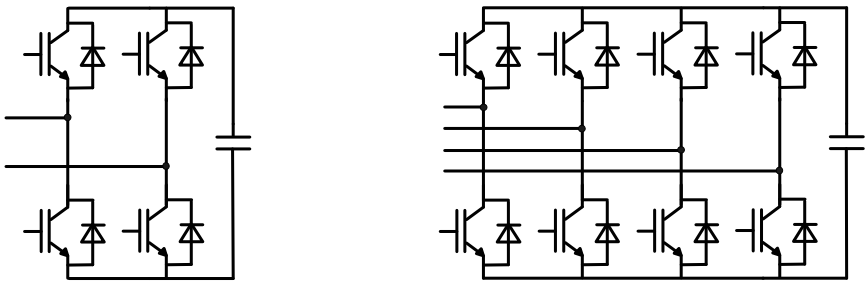



Figure 2.4 The single-phase diagram of the power circuit of the SAF system.

### 2.3.1 Voltage Source Inverter (VSI)

The VSI is the core circuit of SAF such that it synthesizes the reference voltage at its output terminals by using its DC bus voltage under the control of Pulse Width Modulator (PWM). A VSI is composed of power electronics switches and DC bus capacitor(s). The switch type chosen for the VSI depends on the application's specifications such as DC bus voltage, output current, and switching frequency. In the SAF applications for low voltage distribution systems, Insulated Gate Bipolar Transistor (IGBT) is the most appropriate device among the modern power electronics switches [7].

In SAF applications, the full-bridge inverter topologies (without usage of the middle point of DC bus) utilizing IGBTs with antiparallel diodes are favored over other topologies due to their high DC bus voltage utilization and low current ripple [17]. Shown in Figure 2.5, the Single-Phase Full-Bridge (SPFB) VSI is widely utilized in SPSAF applications [13], [14], [18], [19]. In TPSAF applications, there are two options: three SPFB VSIs or a four-leg VSI which are shown in Figure 2.5. For TPSAF which are not intended to compensate for zero sequence utility voltage unbalances, a 3-leg VSI can be used. Although it has more devices and therefore higher cost, in this study, three SPFB VSIs sharing the same DC bus are chosen since this topology has advantages over the four-leg VSI such as higher DC bus voltage utilization capability, intrinsic decoupling of phases, and less complex control.



(*a*) (*b*)

Figure 2.5 The circuit diagrams of VSIs; (a) a SPFB VSI and (b) a four-leg VSI.

The DC bus voltage and capacitance determine the maximum voltage that VSI can generate at its output terminals and the energy storage capacity, respectively. In this study, in applications involving auxiliary power supply with diode rectifier and 380 $V_{rms}$ line-to-line voltage, the rated DC bus voltage is selected as 550V and in applications involving a SAF and a PAF combination (to form a UPQC) it is selected as 700V.

The DC bus capacitance is determined depending on whether there is an auxiliary DC power supply connected to the DC bus or not. Without any auxiliary power supply on the DC side of the SAF, the energy storage required to ride-through a voltage sag/swell fault determines the capacitance of the DC bus. For illustration, for a 3 kW single-phase SAF application, lets consider a design to guarantee full compensation for a voltage sag of 30% ($\Delta V$) with 0.5 s duration ($T_{sag}$) for a system with a DC bus nominal voltage of 550 V ($V_{DC,nom}$) and a minimum operating DC bus voltage of 450 V ($V_{DC,min}$). Under these circumstances, the DC bus capacitance is determined by the power transfer between DC bus and the load during the sag, as given in (2.8) [10]. For the given application, the minimum capacitance is 9.0 mF.

$$C_{DC} = \frac{2 \cdot \Delta P \cdot T_{sag}}{V_{DC,nom}^{\ 2} - V_{DC,min}^{\ 2}} \tag{2.8}$$

If there is an auxiliary power supply available on the DC bus, the DC bus capacitor size is determined by the output voltage range and dynamic properties of the power supply. For example, if a three-phase diode rectifier is fed from the utility, due to the sag condition, initially the rectifier will not take energy from the utility. The capacitor will temporarily provide energy for compensation until its voltage drops to a level that the rectifier starts charging again. Then, the rectifier will provide continuous power for the sag compensation, provided that the rectifier voltage is sufficient for the VSI to operate and for the compensation to be full. If the capacitor is not expected to be utilized as energy source, its design will be based on steady-state ripple calculation (as conventional). Otherwise, it will be calculated based on (2.8). Note that the ripple based design gives significantly smaller value than 9.0 mF of the energy storage based design.

### 2.3.2 Series Injection Transformer (SIT)

SIT is used to inject the SAF voltage between the utility and load. Though it adds to the cost and size of the system, it is vital as it provides galvanic isolation between the legs of VSI. Its turns-ratio matches the voltage magnitudes of primary and secondary sides so that the required compensation voltage between the utility and load (the secondary side) can be maintained in an optimized manner by the VSI with a specified DC bus voltage. As it is a vital part of the system and will be mentioned frequently, its equivalent circuit is shown in Figure 2.6 and its parameters are defined on Table 2.1.

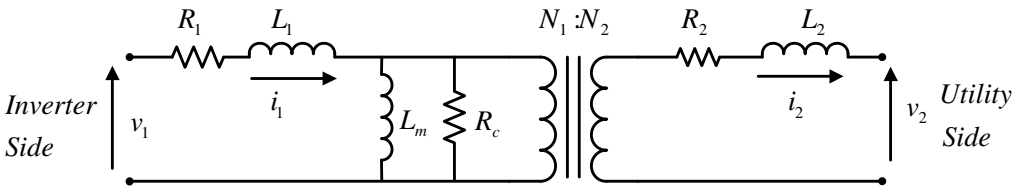



Figure 2.6 The equivalent circuit of SIT.

Table 2.1 The SIT parameters

| | |
|---|---|
| $L_1$ | The primary side leakage inductance |
| $L_2$ | The secondary side leakage inductance |
| $R_1$ | The primary side copper resistance |
| $R_2$ | The secondary side copper resistance |
| $L_m$ | The magnetizing inductance referred to the primary side |
| $R_c$ | The core loss resistance referred to the primary side |
| N | The turns-ratio of the primary to the secondary ($N_1$:$N_2$) |

Since SIT differs in purpose from general purpose transformers, its design rules are also different. An SIT should have low leakage inductance, low core and copper

losses at high frequency (f >> 50 Hz), and high flux density.

Since the rated load current passes through the SIT, the leakage inductance must be kept low in order to keep voltage drop on it low. Secondly, the harmonic voltage content applied to SIT should not overheat it; therefore the core of SIT should have low loss at the harmonic frequency present. The high flux density constraint guarantees that SIT in specific physical dimensions (as small as possible) is capable of transferring the compensation voltage of SAF from the primary to the secondary without magnetic saturation such that overcurrent condition of the VSI is avoided. Within the magnetic saturation issue, the flux offset problem due to the VSI operation and the phase of the voltage applied should be also taken into account. In order to fulfill these constraints, the core and the windings of SIT should be designed accordingly [16].

Silicon steel is the most appropriate material to form the core such that it has high flux density ($B_{max}$ = 1.2-1.6 T) and low cost. E-type laminations of the material to form a core are advantageous such that its high enclosure capability of magnetic field decreases the leakage inductance. Thinner laminations provide lower core losses; therefore the thickness should be much less than a millimeter (typically 0.5mm or less). The winding type affects the leakage inductance as well. Interleaving of the primary and secondary windings provides the maximum cancellation of leakage magnetic fields such that low leakage inductance is obtained [20].

In the following, the turns-ratio and the flux requirement are determined and the design of SIT, which is realized for the SAF application, is given.

#### 2.3.2.1 Turns-ratio

The turns-ratio ($N = N_1/N_2$) of the SIT is determined based on the ratio of the maximum voltage that VSI generates at the primary side of SAF ($V_{pri,max}$) and the maximum required voltage of SAF at the secondary side ($V_{sec,max}$). Ideally, $V_{pri,max}$ is equal to the DC bus voltage for SPFB VSI.

The series injection voltage at the secondary side (the utility-load side) is composed of the harmonic isolation voltage and the load voltage regulation voltage. The perfect harmonic isolation voltage waveform is as seen in Figure 2.3. For the load voltage regulation, the SAF voltage to be generated is limited by the maximum compensation that SAF should provide. In the SAF application, 50% of rated line voltage is a reasonable limit as most voltage sags occur below this limit [21]. In Figure 2.7, the SPSAF and TPSAF voltage waveforms are shown as the superpositions of their harmonic and fundamental components. As seen in the figure, $V_{sec,max}$ is $V_{L,dc}$ for the single-phase case and very close to $V_{L,dc/2}$ for three-phase case. Using the relations of (2.5) and (2.6), $V_{sec,max}$ for the single-phase and three-phase cases are given in (2.9) and (2.10).

$$V_{sec,\max 1\phi} = \frac{\pi}{4} V_{S1} \tag{2.9}$$

$$V_{sec,\max 3\phi} \approx \frac{\pi}{6} V_{S1} \tag{2.10}$$

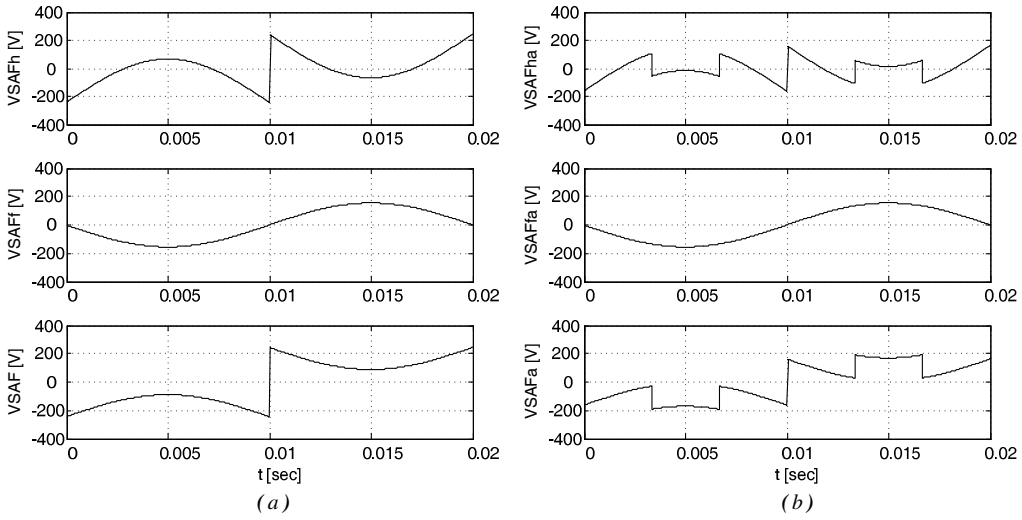



Figure 2.7 The voltage waveforms for the harmonic isolation ($V_{SAFh}$), the load voltage regulation ($V_{SAFf}$), and both ($V_{SAF}$) of (a) SPSAF and (b) TPSAF.

Using the $V_{pri,max}$ and $V_{sec,max}$ expressions, the turns-ratios (N) for SPSAF and TPSAF are found as given in (2.11) and (2.12). For the above discussed diode rectifier based auxiliary supply case, given that $V_{DC}$ is in between 550 V and 700 V and $V_{S1}$ is equal to $220\sqrt{2}$ V, $N_{1\varphi}$ is found to be 2.25, whereas $N_{3\varphi}$ is 3.38 for the worst case (for $V_{DC}$ = 550V). Using the lower N values than the found values enhances the inverter control capability by leaving a DC voltage margin. Besides, the large gap between $N_{1\varphi}$ and $N_{3\varphi}$ implies that single and three-phase SITs should have different turns-ratios and the compensation efficiency is higher in TPSAF compared to SPSAF.

$$N_{1\phi} = \frac{N_1}{N_2} = \frac{V_{pri,\max}}{V_{sec,\max 1\phi}} = \frac{4}{\pi} \cdot \frac{V_{DC}}{V_{S1}} \tag{2.11}$$

$$N_{3\phi} = \frac{N_1}{N_2} = \frac{V_{pri,\max}}{V_{sec,\max 3\phi}} = \frac{6}{\pi} \cdot \frac{V_{DC}}{V_{S1}} \tag{2.12}$$

#### 2.3.2.2 Flux Linkage Requirement

While the compensation voltage is transferred from the primary to the secondary side of the SIT, the maximum flux linkage capacity of the core should not be exceeded so that the transformer does not saturate magnetically and overcurrent conditions are avoided.

The secondary flux linkage ($\lambda_{SAF}$) is given in (2.13). It is obvious from the formula that the initial flux linkage of the SIT ($\lambda_{SAF}(\theta_0)$) and the integral of SAF voltage initially may result in flux linkage DC offset leading to inverter overcurrent. Therefore, this issue should be emphasized in the design of SIT.

$$\lambda_{SAF}(\theta) = \int_{\theta_0}^{\theta} v_{SAF}(\theta) d\theta + \lambda_{SAF}(\theta_0) \tag{2.13}$$

With the assumption of the flux linkage with no DC bias, the flux linkage waveforms with respect to $V_{SAFh}$, $V_{SAFf}$, and $V_{SAF}$ given in Figure 2.7 are shown in Figure 2.8 for the single-phase and the three-phase cases. These waveforms are generated for the worst case compensation conditions defined in the previous section. In these waveforms the peak flux linkages are $\lambda_{SAF1\varphi}$ = 0.72 Wb-turn and $\lambda_{SAF3\varphi}$ = 0.60 Wb-turn under no DC bias condition, i.e., $\theta_0 = \pi/2$ or $3\pi/2$. In the worst DC bias case, i.e., $\theta_0 = \pi$ or $2\pi$, the flux linkages are doubled such that $\lambda_{SAF1\varphi}$ = 1.44 Wb-turn and $\lambda_{SAF3\varphi}$ = 1.20 Wb-turn. Double flux linkage implies double the core size; therefore, the DC bias issue should be taken into account in both the design of the transformer and the control of the SAF [22].

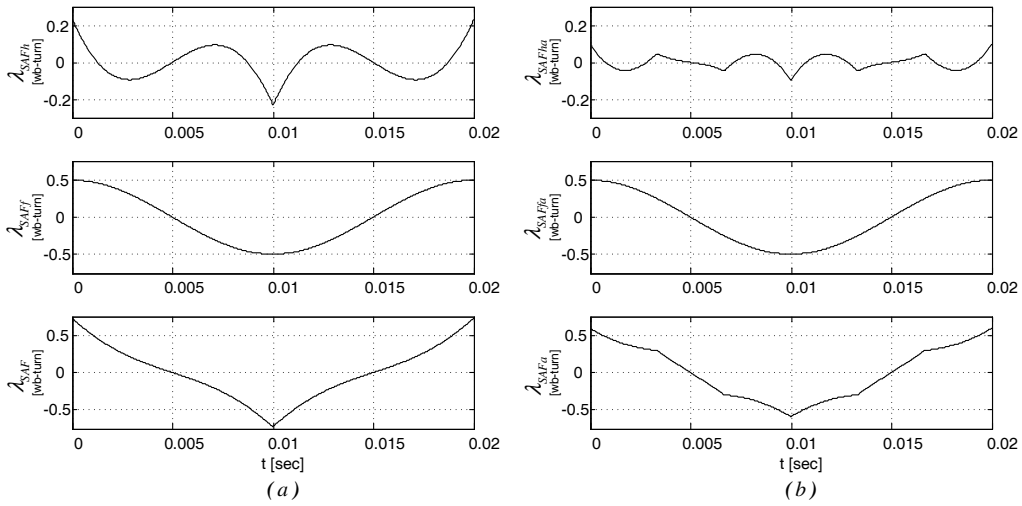



Figure 2.8 The harmonic isolation ($\lambda_{SAFh}$), the load voltage regulation ($\lambda_{SAFf}$), and the overall SAF ($\lambda_{SAF}$) flux linkage waveforms for (a) SPSAF and (b) TPSAF.

### 2.3.2.3 Design of SIT

The core material of the SIT to be utilized in this thesis is chosen as M5-type silicon steel with 0.5 mm E-type laminations ($B_{max}$ = 1.4 T) due to fulfillment of the design constraints and availability of the material. The rest of the design is conducted with

respect to the properties of this material. In the design, in order to decrease the magnetic saturation due to the DC bias of the flux linkage, the maximum flux linkage ($\lambda_{SAF,max}$) should be chosen to be higher than what has been previously found ($\lambda_{SAF,1\varphi}$ and $\lambda_{SAF,3\varphi}$). Moreover, the saturation caused by the VSI DC offset voltage is lessened by means of using a small air-gap in the core.

The formula (2.14) and (2.15) are the main formulas for the transformer design, where $N_2$ is the secondary side turns, $I_2$ is the secondary (utility) side rated current, J is the current density of the conductors of the windings, $A_w$ is the window area of the core, $K_u$ is the window utilization factor of the windings, and $A_c$ is the cross-sectional area of the core [20]. By using these two formulas, the area-product of the core ($A_p$) is found in (2.16). $A_p$ is the main parameter to determine the dimensions of the core. Having found the specific dimensions of the core via $A_p$, $N_2$ can be determined. In order to get low leakage inductance, $N_2$ can be selected lower and this decrease in the turns is compensated by $A_c$ to restrain the same flux in the core. Furthermore, interleaving of the primary and secondary turns decreases the leakage inductance [20].

$$\lambda_{SAF,\max} = N_2 \cdot \phi_{SAF,\max} = N_2 \cdot B_{\max} \cdot A_c \tag{2.14}$$

$$N_2 \cdot I_2 = J \cdot K_u \cdot A_w \tag{2.15}$$

$$A_p = A_c \cdot A_w = \frac{\lambda_{SAF,\max} \cdot I_2}{B_{\max} \cdot J \cdot K_u} \tag{2.16}$$

### 2.3.3 Switching Ripple Filter (SRF)

SRF is the circuit composed of an inductor, a capacitor, and a resistor in the connection form shown in Figure 2.9. The circuit has the characteristic of a second order low pass filter, as given in (2.17). Thus, SRF is used to filter out the high frequency PWM ripple of the output voltage of VSI. Its resonance frequency, which is determined by $L_f$ and $C_f$, is critical such that it defines the high frequency filtering

performance such that the lower the resonance frequency the better the switching ripple filtering and the lower the bandwidth. The resonance frequency is excited when there is not enough damping. The required damping can be provided by the resistor, $R_d$. However, the excessive use of $R_d$ worsens the filtering performance of SRF. Therefore, active damping methods can be used for increasing the damping ratio without degrading the filtering performance [23], [24].

$$G_f(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1 + sR_dC_f}{1 + sR_dC_f + s^2L_fC_f} \tag{2.17}$$

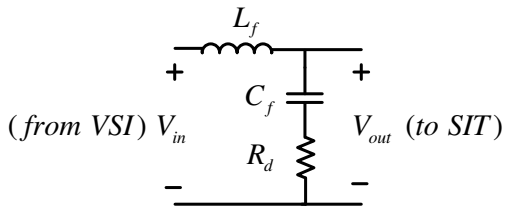



Figure 2.9 The switching ripple filter circuit.

In the SAF application, when the resonance frequency of SRF is selected there are an upper limit and a lower limit of frequency. The upper limit is determined by the PWM frequency of VSI since the switching ripple filter performance degrades as the resonance frequency gets close to the PWM frequency. The lower limit is determined by the required bandwidth of the SAF.

Among the components of SRF, the inductance $L_f$ is the most critical component. $L_f$ limits the PWM current ripple of the VSI at the input side and it determines the fundamental frequency voltage drop on the SAF circuit provided that its value is significantly larger than the leakage inductance of the SIT. Therefore, the design range for $L_f$ is determined considering the trade-off relations such that its minimum value ($L_{f,min}$) is determined by the allowed maximum peak-to-peak ripple current ($\Delta I_{r,max}$) while its maximum value ($L_{f,max}$) is determined by the allowed maximum fundamental frequency voltage drop ($\Delta V_{d,max}$). For $L_{f,min}$ determination, Figure 2.10

illustrates the voltage and current waveforms over a PWM period ($T_{PWM}$) where D stands for the duty cycle and $\Delta V$ is the voltage on the inductor. Equation (2.18) is used to determine $L_{f,min}$. It is obvious that the worst case occurs for D = 0.5. For illustration, choosing $\Delta I_{r,max}$ as 25% of the peak of the secondary rated current. This peak current is approximately 20/N A for the 3 kW/phase load, where N is 2 for the single-phase case and 2.5 for the three-phase case. The $V_{DC}$ value is 700 V for the worst case and $T_{PWM}$ is equal to 50 μs ($f_{PWM}$ = 20 kHz). $L_{f,min}$ values for SPSAF and TPSAF are found as 1.65 mH and 2.06 mH, respectively for the given data. $L_{f,max}$ is found with respect to the primary side of the transformer by (2.19). Given that $\Delta V_{d,max}$ is 1% of rated voltage (2.2 $V_{rms}$) on the primary side, $L_{f,max}$ values for SPSAF and TPSAF are found as in 1.87 mH and 2.92 mH, respectively. From the limit values found in above discussion, the $L_f$ values can be chosen as $L_{f,1\varphi}$ = 1.75 mH and $L_{f,3\varphi}$ = 2.5 mH, respectively.

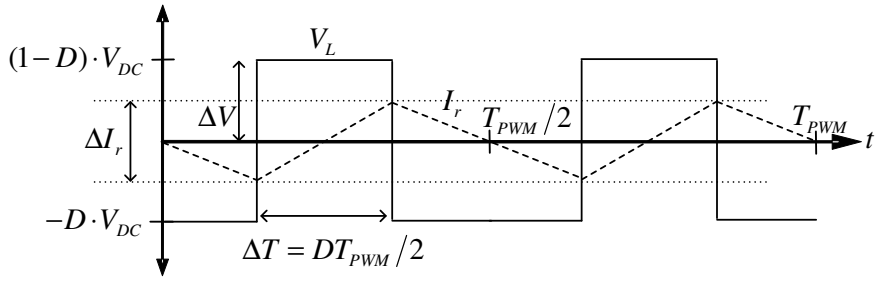



Figure 2.10 The voltage and the ripple current of the filter inductance in a PWM period with unipolar modulation.

$$L_f = \frac{\Delta V \cdot \Delta T}{\Delta I_r} \Rightarrow L_{f,min} = \left.\frac{(1-D)\cdot V_{DC}\cdot D\cdot T_{PWM}}{2\cdot \Delta I_{r,max}}\right|_{D=0.5} \tag{2.18}$$

$$L_{f,max} = \frac{\Delta V_{d,max}\cdot N^2}{\omega_e \cdot I_S} \tag{2.19}$$

The filter capacitance ($C_f$) is determined based on the resonance frequency ($\omega_o$) and the filter inductance using (2.20). The resonance frequency is selected as multiples of kHz to obtain high bandwidth to generate the harmonic isolation voltage. For illustration, $f_o$ = 2.5 kHz can be chosen for a SAF application which aims to isolate effectively the harmonics with the frequency below 2.5 kHz ($50^{th}$ harmonic). Using the given resonance frequency and the $L_f$ values found above, the capacitances for SPSAF and TPSAF are found as $C_{f,1\varphi}$ = 2.3 μF and $C_{f,3\varphi}$ = 1.6 μF.

$$C_f = \frac{1}{L_f \cdot \omega_0^{\,2}} \tag{2.20}$$

While determining $R_d$, the internal resistance of the inductance ($R_f$) and the core loss of the SIT around the resonance frequency, which can be represented as an equivalent resistance ($R_c$), should be considered. Adding up these components to SRF, as shown in Figure 2.11, the modified characteristic transfer function is given in (2.21).

$$G_f(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1 + sC_f R_d}{\frac{R_c + R_f}{R_c} + s\frac{C_f\left(R_c R_d + R_c R_f + R_d R_f\right) + L_f}{R_c} + s^2 L_f C_f \frac{R_c + R_d}{R_c}} \tag{2.21}$$

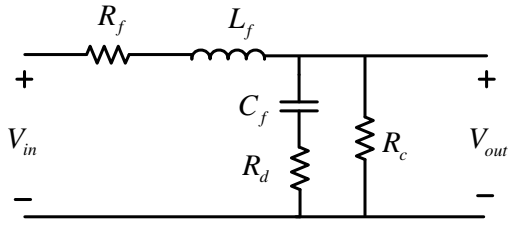



Figure 2.11 The switching ripple filter circuit with $R_f$ and $R_c$.

## 2.4 The Control of SAF

The control system of SAF encompasses six main controller units, which are Harmonic Isolation Controller (HIC), Fundamental Component Controller (FCC), Resonance Damping Controller (RDC), Pulse Width Modulator (PWM), Phase Locked Loop (PLL), and Harmonic/Fundamental Extractor (HFE). The details of each unit are provided in the following.

### 2.4.1 Harmonic Isolation Controller (HIC)

HIC aims to block harmonic current flow between the utility and the load and it uses the line current harmonic ($i_{Sh}$) and the load voltage harmonic ($v_{Lh}$) signals as inputs in order to generate the harmonic isolating voltage reference ($v_{SAFh}$*). The methods used in HIC are to emulate a resistor ($K_{hi}$) for the line harmonic current ($i_{Sh}$) and to apply the load harmonic voltage ($v_{Lh}$), as noted in Section 2.2.1. Nevertheless, the harmonic signals cannot be reached by direct measurements. Therefore, the measured signals should be decomposed such that the fundamental and the harmonic contents of the signals are separated. In the control of SAF, this task is done by the HFE unit, which will be explained Section 2.4.6 in detail. With the application of HFE, the control rule for harmonic isolation is given in (2.22), where $g_{hi}$ and $g_{hv}$ are the functions for the harmonic current extraction and the harmonic voltage extraction. The performance of the harmonic isolation depends on the accuracy and the bandwidth of $g_{hi}$ and $g_{hv}$ as well as the values of $K_{hi}$ and $K_{hv}$. HIC block diagrams for the single-phase and three-phase applications are illustrated in Figure 2.12.

$$v_{SAFh}^{*} = K_{hi} \cdot g_{hi}(\hat{i}_S) - K_{hv} \cdot g_{hv}(\hat{v}_L) \tag{2.22}$$

The value of $K_{hi}$ is limited by the stability of the power circuit. Especially, the delay time due to measurement and controllers ($T_d$) strictly constrains $K_{hi}$ [30]. In Section 2.4.6, the relation between $K_{hi}$ and $T_d$ and a method for the delay time compensation will be investigated.

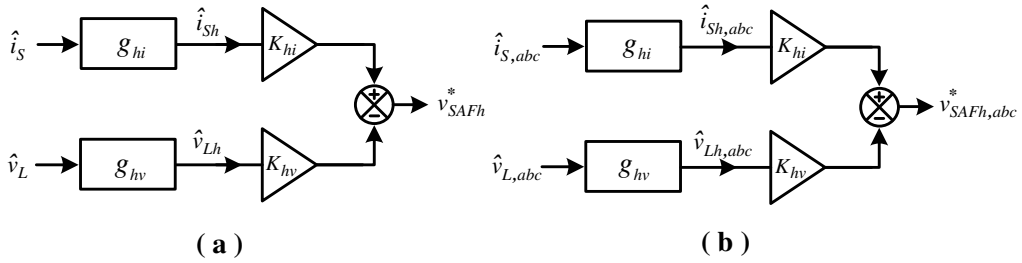



Figure 2.12 The controller block diagrams of HIC for (a) SPSAF and (b) TPSAF.

In practice, the value of $K_{hv}$ is chosen between 0 and 1 such that $K_{hv}$ = 0 means no voltage harmonic feedforward control and $K_{hv}$ = 1 means applying the entire feedforward voltage signal. However, if the accuracy of the harmonic load voltage is not high, then the feedforward voltage harmonic contribution to harmonic isolation should be restrained by choosing $K_{hv}$ less than 1.

### 2.4.2 Fundamental Component Controller (FCC)

FCC compensates for the line and load disturbances by processing the utility and the load fundamental voltages ($v_{S1}$ & $v_{L1}$) and it generates the voltage reference for load voltage regulation ($v_{SAF1}$*). However, $v_{L1}$ cannot be directly measured in the V-type load; therefore, HFE should be used to process the rectangular-shaped load voltage. Obtaining $v_{L1}$ fast and accurately is very important to have a high performance feedback controlled system. In the HFE section, this issue will be addressed and the novel AVM will be introduced.

In this section, after the discussion of space-vector transformations which are utilized to obtain the DC quantities of $v_{S1}$ and $v_{L1}$, the feedback and the feedforward parts of FCC are introduced.

#### 2.4.2.1 Coordinate Transformations

The magnitude of the fundamental frequency component of a single-phase signal or three-phase signals can be obtained as a real and an imaginary (reactive) components

at the synchronous reference frame ('de-qe' frame) rotating with the reference phase angle ($\theta_e = \omega_e t$) [5], [25].

For the three-phase case, the power invariant stationary reference frame ('ds-qs' frame) transformation (C), as shown in (2.23), is applied to three-phase signals ($x_{abc}$) and then the outputs of the C transformation ($x_{dqs}$) are passed through the 'de-qe' transformation (T), as shown in (2.24). Similarly, $x_{abc}$ can be obtained from $x_{dqe}$ by means the inverse transformations $C^{-1}$ (2.25) and $T^{-1}$ (2.26).

$$\begin{bmatrix} x_{ds} \\ x_{qs} \end{bmatrix} = C \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{2.23}$$

$$\begin{bmatrix} x_{de} \\ x_{qe} \end{bmatrix} = T \begin{bmatrix} x_{ds} \\ x_{qs} \end{bmatrix} = \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} x_{ds} \\ x_{qs} \end{bmatrix} \tag{2.24}$$

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = C^{-1} \begin{bmatrix} x_{ds} \\ x_{qs} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} x_{ds} \\ x_{qs} \end{bmatrix} \tag{2.25}$$

$$\begin{bmatrix} x_{ds} \\ x_{qs} \end{bmatrix} = T^{-1} \begin{bmatrix} x_{de} \\ x_{qe} \end{bmatrix} = \begin{bmatrix} \cos\theta_e & -\sin\theta_e \\ \sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} x_{de} \\ x_{qe} \end{bmatrix} \tag{2.26}$$

The negative sequence signal can be extracted by utilizing the negative phase angle ($-\theta_e$) in the 'de – qe' transformation. Besides, if there is a zero sequence component in $x_{abc}$, then this component ($x_0$) can be found by the power invariant formula given in (2.27).

$$x_0 = \frac{x_a + x_b + x_c}{\sqrt{3}} \tag{2.27}$$

For the single-phase case, a single signal ($x = x_{ds}$) is not enough to perform 'de-qe' vector transformation, therefore another signal ($x_{qs}$) which is orthogonal to the available signal should be generated by processing $x_{ds}$ such that $x_{qs}$ lags $x_{ds}$ by 90°. This lag can be realized by two means: the Hilbert Transform and the data delay methods [25], [26]. The second method is preferred in this study due to its less complex algorithm with respect to the former. The data delay method is based on buffering the information of $x_{ds}$ and using this information after a quarter of fundamental period as the $x_{qs}$ output. The 'de-qe' transformation for the single-phase is given in (2.28).

$$\begin{bmatrix} x_{de} \\ x_{qe} \end{bmatrix} = T \begin{bmatrix} x_{ds} \\ x_{qs} \end{bmatrix} = \begin{bmatrix} \cos\theta_e & \sin\theta_e \\ -\sin\theta_e & \cos\theta_e \end{bmatrix} \begin{bmatrix} x_{ds}(\theta) \\ x_{ds}(\theta - \pi/2) \end{bmatrix} \tag{2.28}$$

#### 2.4.2.2 The Feedback Controller

The load voltage feedback controller is designed in the 'de-qe' frame so that the controller results in zero steady-state error for the fundamental frequency component of the load voltage ($v_{L1}$). In the design, the SAF system is represented as a single-phase equivalent circuit in the 'de-qe' frame as shown in Figure 2.13. In this circuit, the coupling impedance terms ($\omega_e L_S$) between the 'de-qe' coordinates are neglected considering that $L_S$ is small in the SAF application.

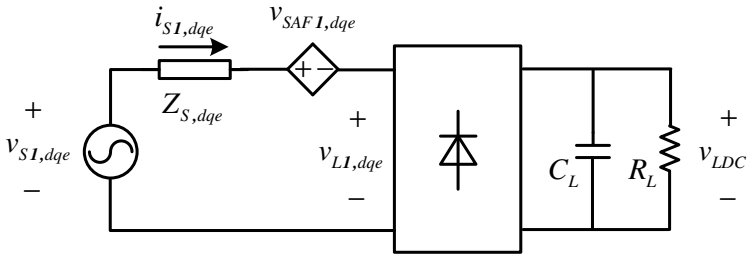



Figure 2.13 The equivalent circuit of the SAF system in the 'de-qe' frame.

For the SAF application with the V-type nonlinear load, provided that perfect harmonic isolation is maintained, the line current ($i_{S1}$) becomes in phase with the load voltage ($v_{L1}$). The phase difference between $v_{L1}$ and $v_{S1}$ is small due the small line impedance as shown in the phasor diagram, Figure 2.14. With the defined transformation, most of the voltage is on the 'de' axis. This implies that $v_{L1,qe}$ and $i_{S1,qe}$ can be assumed to be zero considering that $v_{S1,qe}$ is zero as it is the reference for the 'de-qe' transformation. With this assumption, the SAF circuit is simplified to a single-phase circuit associated with the 'de' axis as shown in Figure 2.15. In this simplified circuit, the rectifier act as an ideal transformer with the turns-ratio of $N_V$ (AC/DC transformation ratio) by ignoring the non-ideal properties of the rectifier such as commutation, on-state voltage drop [27]. By means of $N_V$, the capacitor and the resistor in the output side of the rectifier are referred to the input side as given in (2.29) and the circuit is simplified as given in Figure 2.16.

$$\begin{aligned} R_{Lde} &= N_V{}^2 R_L \\ C_{Lde} &= C_L / N_V{}^2 \end{aligned} \tag{2.29}$$

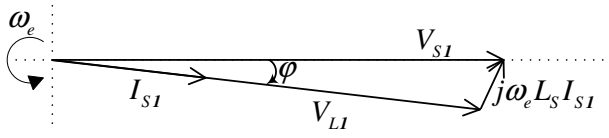



Figure 2.14 The phasor diagram.

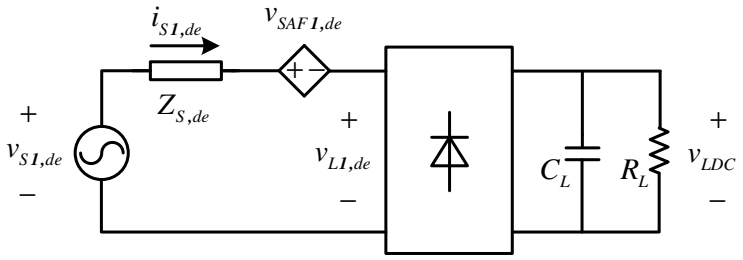



Figure 2.15 The simplified SAF system circuit in the 'de' axis.

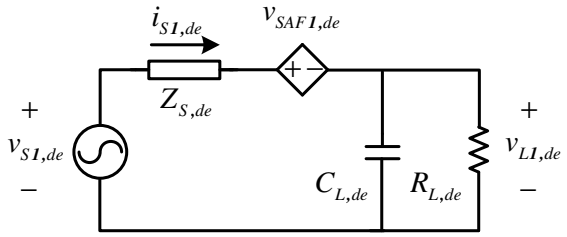



Figure 2.16 The simplified SAF system circuit with the referred $R_L$ and $C_L$ to the input side in 'de' axis.

The relation between $v_{L1,de}$ and $v_{LDC}$ determines $N_V$ as given in (2.30). The values of $N_V$ for the single-phase and the three-phase cases ($N_{V,1\varphi}$ and $N_{V,3\varphi}$) can be found by utilizing (2.4) and (2.5), which are based on the peak values of the line and load voltages ($V_{S1}$ and $V_{L,dc}$). It should be noted that since $Z_S$ is small $V_{L1}$ and $V_{S1}$ are assumed to be equal. For SPSAF, $V_{L1} = v_{L1,de}$ and $V_{L,dc} = v_{LDC}$. By using these equalities and (2.4), $N_{V,1\varphi}$ is found as given in (2.31). For TPSAF, $V_{L1} = (\sqrt{2}/\sqrt{3})v_{L1,de}$ and $V_{L,dc} = (2/3)v_{LDC}$. Using (2.5), $N_{V,3\varphi}$ is found as given in (2.32) .

$$N_V = \frac{v_{L1,de}}{v_{LDC}} \tag{2.30}$$

$$N_{V,1\varphi} = \frac{v_{L1,de}}{v_{LDC}} = \frac{V_{L1}}{V_{L,dc}} = \frac{4}{\pi} \tag{2.31}$$

$$N_{V,3\varphi} = \frac{v_{L1,de}}{v_{LDC}} = \frac{v_{L1,de}}{V_{L1}} \frac{V_{L1}}{V_{L,dc}} \frac{V_{L,dc}}{v_{LDC}} = \sqrt{\frac{3}{2}} \frac{3}{\pi} \frac{2}{3} = \frac{\sqrt{6}}{\pi} \tag{2.32}$$

The control block diagram of the circuit without any fundamental controller appears as seen in Figure 2.17, where $G_{S,de}(s)$ and $G_{L,de}(s)$ represent the transfer functions of the line (2.33) and the load (2.34), respectively. The transfer function of the system without a controller ($D_{de}(s)$) is given in (2.35) for $V_{SAF1,de}(s) = 0$.

$$G_{S,de}(s) = \frac{1}{R_{S,de} + sL_{S,de}} \tag{2.33}$$

$$G_{L,de}(s) = N_V{}^2 \frac{R_L}{1 + sC_L R_L} = \frac{R_{L,de}}{1 + sC_{L,de} R_{L,de}} \tag{2.34}$$

$$D_{de}(s) = \frac{V_{L1,de}(s)}{V_{S1,de}(s)} = \frac{1}{\frac{R_{L,de} + R_{S,de}}{R_{L,de}} + s\frac{C_{L,de}R_{L,de}R_{S,de} + L_{S,de}}{R_{L,de}} + s^2 L_{S,de}C_{L,de}} \tag{2.35}$$

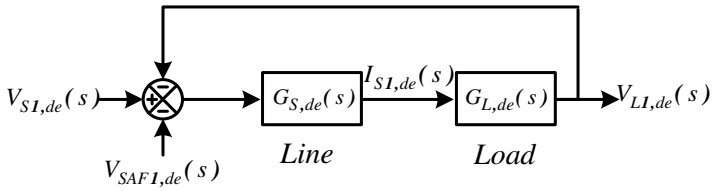



Figure 2.17 The control block diagram of the simplified SAF circuit in 'de' axis without any load voltage controller.

When a feedback controller ($G_{C,de}(s)$) is applied to the error in the load voltage, the control block diagram is shown in Figure 2.18. $G_{C,de}(s)$ is selected such that the overall performance of the system becomes satisfactory in dynamic response, steady-state error, and the line voltage disturbance rejection. When $G_{C,de}(s)$ is a proportional (P) controller such that $G_{C,de}(s) = K_{Pv}$, the transfer functions of the system ($G_{P,de}(s)$) for $V_{S1,de}(s) = 0$ is given in (2.36). It is seen from the function that the steady-state error due to a unit-step input depends on the $K_{Pv}$ value as given in (2.37). Moreover, the proportional regulator cannot manipulate the poles of the transfer functions freely due to its limited effect on the coefficients of the function in order to have the optimized performance.

$$G_{P,de}(s)=\frac{V_{L1,de}(s)}{V^{*}_{L1,de}(s)}=\frac{1}{\frac{(K_{Pv}+1)R_{L,de}+R_{S,de}}{K_{Pv}R_{L,de}}+s\frac{C_{L,de}R_{L,de}R_{S,de}+L_{Sde}}{K_{Pv}R_{L,de}}+s^{2}\frac{L_{S,de}C_{L,de}}{K_{Pv}}} \tag{2.36}$$

$$e_{ss}=\lim_{s\to 0}s(1-G_{P,de}(s))V^{*}_{L1,de}(s)=\frac{R_{L,de}+R_{S,de}}{(K_{Pv}+1)R_{L,de}+R_{S,de}}\approx\frac{1}{K_{Pv}+1} \tag{2.37}$$

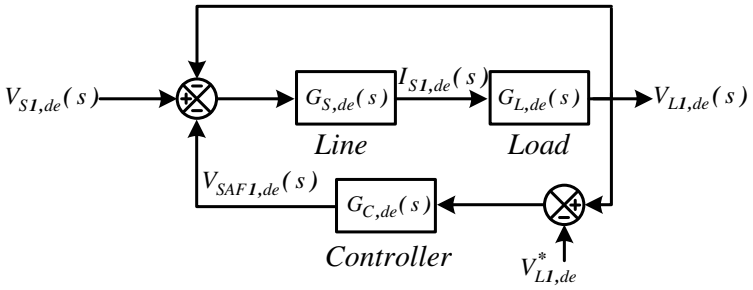



Figure 2.18 The control block diagram of the simplified SAF circuit in 'de' axis with the feedback controller.

The transfer function $D_{P,de}(s)$ as given in (2.38) shows the rejection capability of the disturbances originated from the utility. As compared with $D_{de}(s)$ at steady-state, while the system without controller is susceptible to disturbances of $V_{S1,de}$ at steady-state, i.e., $D_{de}(s = 0) \approx 1$, the system with P controller is affected from approximately $1/(K_{Pv}+1)$ of a line voltage disturbance such that $D_{P,de}(s = 0) \approx 1/ (K_{Pv}+1)$. Thus, the P controller decreases the effect of a line voltage disturbance but cannot totally eliminate its effect on the load side.

$$D_{P,de}(s)=\frac{V_{L1,de}(s)}{V_{S1,de}(s)}=\frac{1}{\frac{(K_{Pv}+1)R_{L,de}+R_{S,de}}{R_{L,de}}+s\frac{C_{L,de}R_{L,de}R_{S,de}+L_{S,de}}{R_{L,de}}+s^{2}L_{S,de}C_{L,de}} \tag{2.38}$$

For high performance load voltage regulation and line voltage disturbance rejection, a proportional-integral (PI) controller can be used such that $G_{C,de}(s) = K_{Pv} + K_{Iv}/s$. As seen in the transfer functions of the system ($G_{PI,de}(s)$) with a pole-zero cancellation for $V_{S1,de}(s) = 0$ (2.39), the poles of the overall system can be arranged so that the load regulation performance of the system is optimized. For the unit-step input, the PI controller provides zero steady-state error as shown in (2.40). The line voltage disturbance rejection is given in (2.41). $D_{PI,de}(s)$ shows that at steady-state the PI controller decouples the line disturbance from the load, i.e., $D_{PI,de}(s) = 0$.

$$G_{PI,de}(s) = \frac{V_{L1,de}(s)}{V^{*}_{L1,de}(s)} = \frac{1}{1 + s\dfrac{R_{L,de} + R_{S,de}}{K_{Iv}R_{L,de}} + s^2\dfrac{L_{S,de}C_{L,de}}{K_{Pv}}} \tag{2.39}$$

$$e_{ss} = \lim_{s\to 0} s(1 - G_{PI,de}(s))V^{*}_{L1,de}(s) = 0 \tag{2.40}$$

$$D_{PI,de}(s) = \frac{V_{L1,de}(s)}{V_{S1,de}(s)} = \frac{s}{K_{Iv} + s\dfrac{R_{L,de}(K_{Pv}+1) + R_{S,de}}{R_{L,de}} + s^2\dfrac{C_{L,de}R_{L,de}R_{S,de} + L_{S,de}}{R_{L,de}} + s^3 L_{S,de}C_{L,de}} \tag{2.41}$$

So far, the system has been modeled and the controller has been designed considering a complete linear system without the effect of the HIC on the fundamental equivalent circuit. Nevertheless, in practice the harmonic extractors of the line current and the load voltage are not ideal whereas $G_{HE,de}(s) = 1$ for the harmonic frequencies and $G_{HE,de}(s) = 0$ for fundamental frequency are assumed in the controller design discussion above. Moreover, the non-ideal fundamental extractor of the load voltage ($G_{FE,de}(s)$) should also be taken into account. Consequently, the PI controller may not be sufficient such that a compensator is required to obtain desired SAF system characteristic. With the addition of HFE transfer functions to the system, the control diagram of the fundamental equivalent system is shown in Figure 2.19. The transfer functions of the HFEs and the SAF system with HFEs and the control of the system will be investigated in Chapter 3.

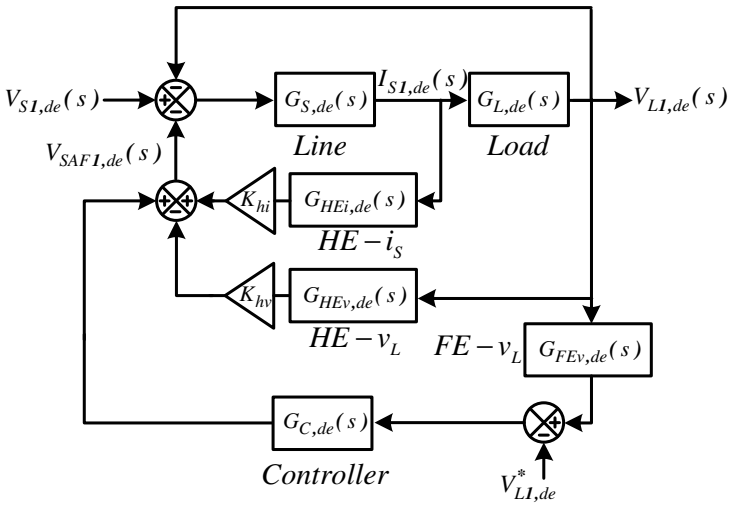



Figure 2.19 The control block diagram of the simplified SAF circuit in 'de' axis with the feedback controller and the HFEs.

Although 'qe' axis is not modeled in the simplified system due to its small contribution to responses of the SAF system at the fundamental frequency, the feedforward controller of the HIC is sensitive to the phase difference between the load and the line voltages. Therefore, FCC should be modified for the control of 'qe' axis load voltage with respect to the type of load voltage harmonic extraction methods; Conventional Method (CM) and Absolute Value Method (AVM) as follows. For CM, a PI regulator is applied to $v_{L1,qe}$ with zero reference value. For AVM, a P controller is applied to $i_{S1,qe}$ with zero reference value where $v_{L1,qe}$ is not available in AVM.

For TPSAF, negative sequence component at $2\omega_e$ appears on the 'de' frame representation of the system under unbalanced line voltage conditions. In order to eliminate the negative sequence effect on the load voltage, extra controllers for negative sequence such as resonant controllers can be designed. Fortunately, the low bandwidth of the SAF system attenuates this negative sequence effectively. Additionally, the feedforward controller, which will be introduced in the next section, mitigates the negative sequence disturbance totally.

For the zero sequence, the zero sequence line voltages do not lead to the flow of the zero sequence line current due to the fact that the total of three-phase currents is zero in three-wire systems. However, the zero sequence line voltages directly appear on the load side when the utility ground is taken as reference ground. With vector transformations, the zero sequence line voltage is manipulated thus it has no effect on the controller and can be disregarded. The measured line voltage zero sequence component could be identified and canceled on the load side via series injection of SAF (although it has no effect on the load behavior). In this thesis this approach is preferred.

#### 2.4.2.3 The Feedforward Controller

In the FCC, the feedforward controller is utilized to help the feedback controller by responding fast to the line voltage variations. The controller, which is based on the 'de-qe' and the zero sequence transformations, compensates for the error between the reference line voltage and the measured line voltage. The advantage of using 'de-qe' frame is that the error signal can be filtered by low pass filters (LPFs) to eliminate the unwanted high frequency signals (noise) without resulting in phase lag in the fundamental frequency part of the error signal. The feedforward controllers for SPSAF and TPSAF are represented in Figure 2.20 and Figure 2.21, respectively. It should be noted that the zero sequence compensation is applicable for only TPSAF.

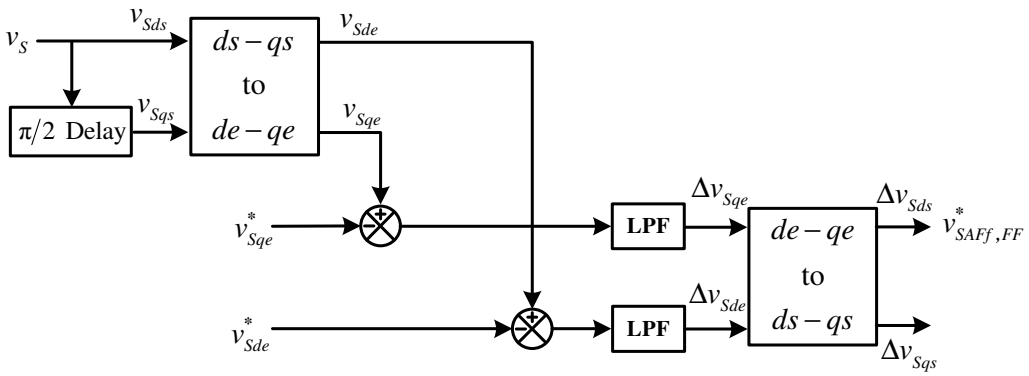



Figure 2.20 The control block diagram of the feedforward controller for SPSAF.

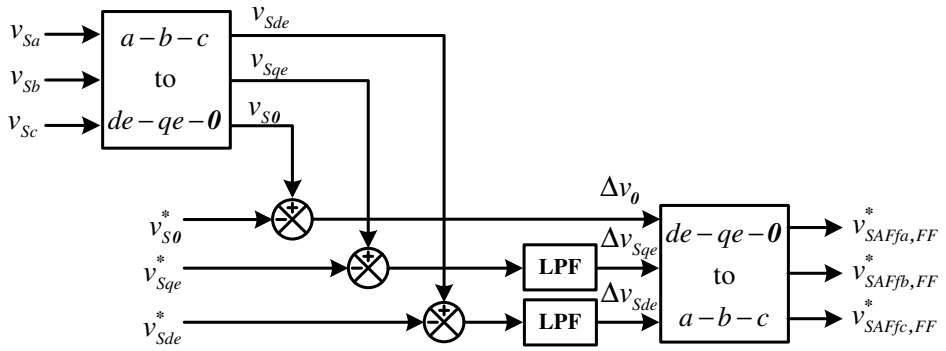



Figure 2.21 The control block diagram of the feedforward controller for TPSAF.

### 2.4.3 Resonance Damping Controller (RDC)

RDC provides the SRF circuit with an extra damping at the filter resonance frequency. The damping is strictly required for HIC with high $K_{hi}$, which drives the SAF system unstable. If the series resistance ($R_d$) is increased for the damping the filtering performance for switching ripples worsens. Therefore, active damping is required to damp the resonance without degrading the SRF performance. In this study, the capacitor current feedback is used to increase the stability margin of SRF. The control rule of RDC is given in (2.42). Using the rule, the new transfer function for SRF is given in (2.43). It is obvious from the transfer function that the feedback gain ($K_d$) acts as a series resistor just like $R_d$ for damping as seen on the denominator of the function. However, it does not contribute to the numerator of the function as $R_d$ does such that the switching ripple filtering performance does not decline as the frequency increases.

$$v_{SAFd} = K_d \cdot \hat{i}_C \tag{2.42}$$

$$G_f(s) = \frac{1 + sC_f R_d}{\frac{R_c + R_f}{R_c} + s\frac{C_f\left(R_c\left(R_d + K_d\right) + R_c R_f + R_d R_f\right) + L_f}{R_c} + s^2 L_f C_f \frac{R_c + R_d}{R_c}} \tag{2.43}$$

### 2.4.4 Pulse Width Modulator (PWM)

The PWM unit generates on/off signals for each SPFB VSI's switches with respect to the per phase SAF reference voltage given in (2.44). For the SAF application, unipolar modulation method is used due to its higher bandwidth and lower current ripple than bipolar modulation for the same switching frequency [17]. In order to reject disturbances originating from the DC bus of SAF, the PWM unit uses the DC bus voltage measurement such that the peak value of the triangular wave, which the reference voltage is compared to, is proportional to the DC bus voltage. Additionally, the PWM signals should have deadtimes, which are required by the IGBTs in order not to cause shoot-through fault.

$$v_{SAF}^{*} = v_{SAFh}^{*} + v_{SAFf}^{*} + v_{SAFd}^{*} \tag{2.44}$$

The PWM frequency is chosen with respect to the two limits: the bandwidth of SAF and the switching losses. The first limit determines the minimum frequency while the latter does the maximum. In this thesis, IGBTs are driven by 20 kHz unipolar PWM [17].

### 2.4.5 Phase Locked Loop (PLL)

PLL generates the phase angle information of the utility ($\theta_e$) using the utility voltage. Since 'de-qe' transformation is realized by using $\theta_e$, PLL is vital for the control of SAF. In this study, the PLL method based on 'de-qe' transformation of the line voltages is preferred due to its fast and noise-insensitive operation [28]. For three-phase case, the approach is illustrated in Figure 2.22. As shown in the figure, after $v_S$ is transformed to its dc quantities using the phase information ($\theta$) a proportional-integral (PI) controller is applied to the error between the reference DC quantity ($v_{Sqe}^{*}$) and the feedback DC quantity ($v_{Sqe}$). This output of the PI gives the compensation magnitude of the line voltage frequency in radian ($\omega$) and the PI operates so that the error is diminished, i.e., $\theta = \theta_e$. The nominal frequency of the utility ($\omega_{ff}$) is added up as a feedforward controller. As a result, the phase angle ($\theta$) is

obtained by means of taking integral of ω. For the single-phase, the data delay method is utilized as shown in Figure 2.23 [29].

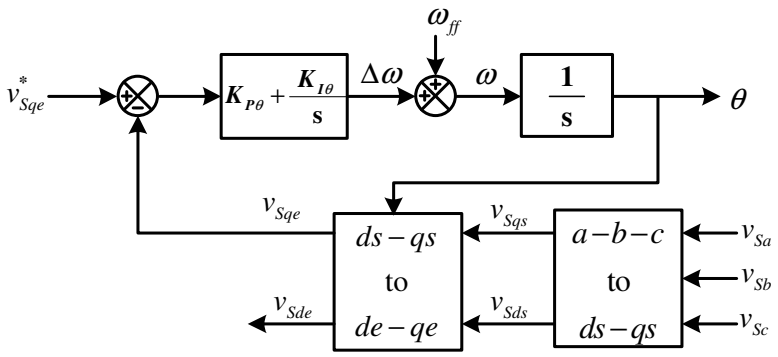



Figure 2.22 The three-phase vector PLL.

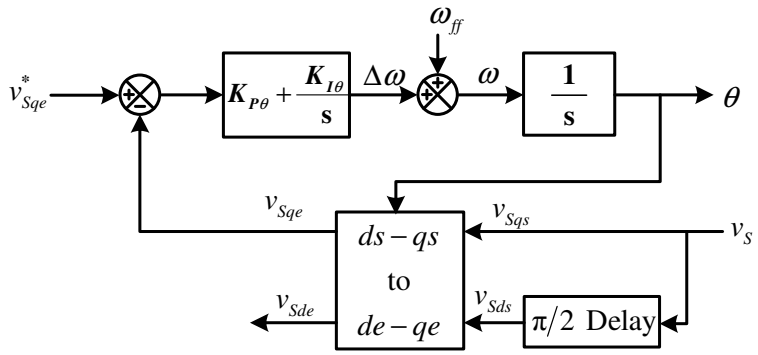



Figure 2.23 The single-phase vector PLL.

In order to prove the operation of PLL theoretically, the transfer function of the PLL can be found by a small signal analysis where ($\theta \approx \theta_e$) as follows. Assuming $v_{Sds} = V\sin\theta$ and $v_{Sqs} = V\cos\theta$ are the preprocessed signals of the line voltages for the single-phase or the three-phase utility before the 'de-qe' transformation. Then, $v_{Sqe}$ is found by 'de-qe' transformation using θ as given in (2.45). Given that $\theta \approx \theta_e$, Equation (2.45) can be linearized as given in (2.46). For $v_{Sqe}^* = 0$, the PLL can be simplified in a control block diagram as shown in Figure 2.24. The transfer function

of the linearized PLL is given in (2.47). Seen on the $G_\theta(s)$, using appropriate proportional and integral gains ($K_{P\theta}$ and $K_{I\theta}$) can optimize the response of the PLL. As shown in (2.48), the PLL has no steady-state error for the unit-ramp input ($\theta_e$ (s) = $1/s^2$), which represents the behavior of $\theta_e$. Consequently, the PLL algorithm used is appropriate for the SAF application that requires accurate phase angle information.

$$v_{Sqe} = -V\cos\theta_e \sin\theta + V\sin\theta_e \cos\theta = V\sin(\theta_e - \theta) \tag{2.45}$$

$$v_{Sqe} = V(\theta_e - \theta) \; where \; \theta \approx \theta_e \tag{2.46}$$

$$G_\theta(s) = \frac{\theta(s)}{\theta_e(s)} = \frac{1 + s\dfrac{K_{P\theta}}{K_{I\theta}}}{1 + s\dfrac{K_{P\theta}}{K_{I\theta}} + s^2\dfrac{1}{VK_{I\theta}}} \tag{2.47}$$

$$e_{ss} = \lim_{s\to 0} s(1 - G_\theta(s))\theta_e(s) = \lim_{s\to 0} \frac{s}{VK_{I\theta} + sVK_{P\theta} + s^2} = 0 \tag{2.48}$$

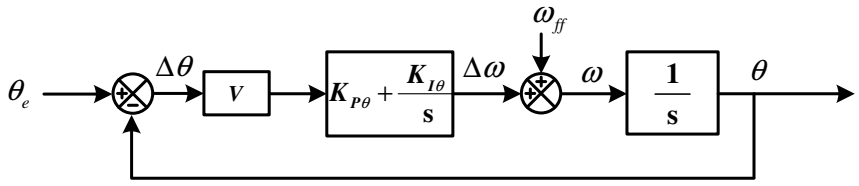



Figure 2.24 The small-signal control block diagram of the vector PLL.

### 2.4.6 Harmonic/Fundamental Extractor (HFE)

There are different approaches for harmonic and fundamental frequency signal extraction. In this study, the most popular method based on the 'de – qe' frame in the literature, which is called Conventional Method (CM) in this thesis and the

application-specific novel method called Absolute Value Method (AVM) developed to decompose the harmonic and fundamental components of the load voltage for the SAF applications with the single-phase and the three-phase diode rectifier loads with a DC bus capacitor and a resistor are considered.

#### 2.4.6.1 Conventional Method (CM)

In CM, signal decomposition is realized in 'de-qe' frame such that the transformations from the measured single-phase and three-phase signals to two-phase signals are performed as noted in Part 2.4.2.1. These two signals are composed of a DC and an AC components, which represents the fundamental frequency and the harmonic frequency components as given in (2.49). By means of low and/or high pass filters (LPF/HPF), these DC and AC components can be separated as shown in (2.50). Moreover, (1-LPF) can be used instead of HPF [30].

$$\begin{bmatrix} x_{de} \\ x_{qe} \end{bmatrix} = \begin{bmatrix} \overline{x}_{de} + \tilde{x}_{de} \\ \overline{x}_{qe} + \tilde{x}_{qe} \end{bmatrix} \tag{2.49}$$

$$\begin{bmatrix} \overline{x}_{de} \\ \overline{x}_{qe} \end{bmatrix} = \begin{bmatrix} LPF & 0 \\ 0 & LPF \end{bmatrix} \begin{bmatrix} x_{de} \\ x_{qe} \end{bmatrix} \; and \; \begin{bmatrix} \tilde{x}_{de} \\ \tilde{x}_{qe} \end{bmatrix} = \begin{bmatrix} HPF & 0 \\ 0 & HPF \end{bmatrix} \begin{bmatrix} x_{de} \\ x_{qe} \end{bmatrix} \tag{2.50}$$

Although the first order filter is used commonly due to its simple structure and fair performance, the second or third order butterworth filters are preferred for the applications requiring more sensitive harmonic extraction. For illustration, the transfer function of a first order LPF is given in (2.51), where $\omega_c$ represents the cut-off frequency of the filter in radians.

$$LPF(s) = \frac{\omega_c}{\omega_c + s} \tag{2.51}$$

The cut-off frequency of the filter is chosen such that fast response and accuracy requirements are fulfilled. However, these requirements may conflict each other

where the harmonic frequencies are within the bandwidth required for the application. The optimal value for the cut-off frequency can be determined by the Bode diagrams of a filter. For example, the Bode diagram of a first order LPF is as shown in Figure 2.25. The beginning frequency of harmonic content, $\omega_h$ is utilized such that the gain at $\omega_h$ ($|LPF(\omega_h)|$) is chosen small enough for a given application. Taking $\omega_h$ and $|LPF(\omega_h)|$, $\omega_c$ is easily determined to fulfill the accuracy requirement where $|LPF(\omega_c)| = (1/\sqrt{2})$. If the bandwidth requirement is not satisfied for the $\omega_c$ found, the attenuation may be chosen smaller. Nonetheless, the accuracy of the filter is more important than the bandwidth in the active filter applications, therefore the bandwidth of the filter is sacrificed mostly. Besides, it is important to note that the phase of the DC component stays the same after the filtering, which shows that the DC component (representing the fundamental frequency component) can be used for the fundamental controller.

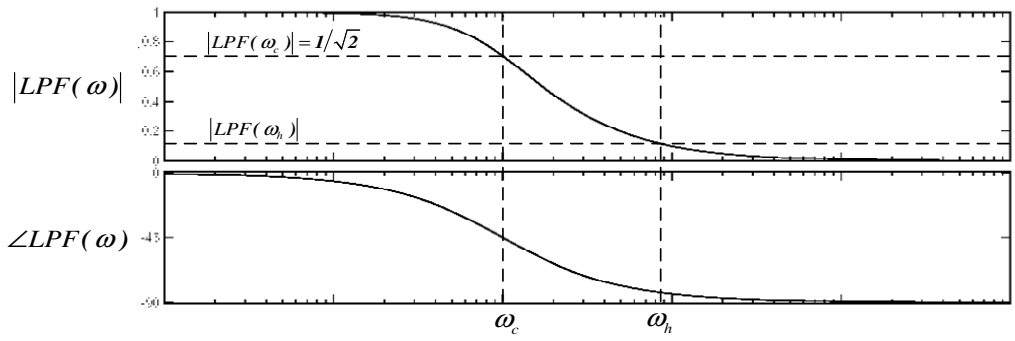



Figure 2.25 The Bode diagram of a first order LPF.

#### 2.4.6.1.1 Harmonic Extraction of Line Current

For the single-phase applications, the harmonic spectrum of the line current in 'de-qe' frame ($i_{S,dqe}$) is composed of the harmonic components at the 4n multiples of the fundamental frequency ($\omega_e$). Therefore, for the filter design $\omega_h = 4\omega_e$. For illustration, specified that the LPF is the first order filter with $|LPF(\omega_h)| = 2.5\%$, $\omega_{ch}$ is found to

be close to $0.1\omega_e$. For the three-phase case, ($i_{S,dqe}$) is composed of 6n multiples of $\omega_e$. Considering the same attenuation as the single-phase case, $\omega_{ch}$ is found to be close to $0.15\omega_e$ [11].

In the SAF applications, the harmonic content of the line current can be obtained by means of HPF or '1-LPF' as shown in Figure 2.26. In analog applications, the difference between two methods is that the latter does not contribute to the total delay time ($T_d$) of the controllers by the process time ($T_p$) such that the high frequeny content of the line current signal passes through the filter without the process time delay. In the figure, $T_m$ represents the measurement delay [30].

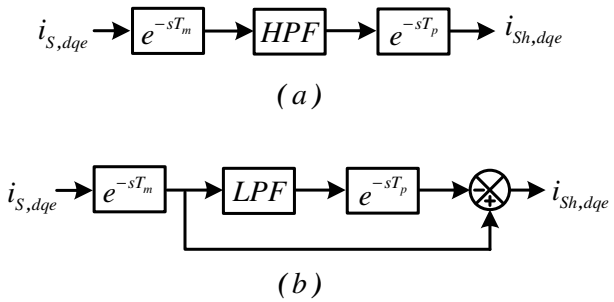



Figure 2.26 The harmonic current extraction by (a) HPF and (b) '1-LPF'.

In order to comprehend the effectiveness of '1-LPF', the impact of $T_d$ on the stability should be investigated via the equivalent SAF circuit defined at the harmonic frequencies as shown in the Figure 2.27. The Nyquist stability criterion for the simplified system (SRF and SIT are assumed to be ideal), given in (2.52), describes the relation between $K_{hi}$ and $T_d$ such that the higher $K_{hi}$ the lower $T_d$ for the stable operation [30]. Consequently, decreasing $T_d$ by eliminating $T_e$ enhances the stability margin and increases the maximum applicable $K_{hi}$.

$$\frac{T_d K_{hi}}{L_S} < \frac{\pi}{2} \tag{2.52}$$

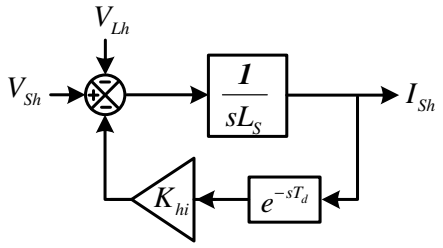



Figure 2.27 The simplified control block diagram of the SAF with HIC.

However, the '1-LPF' discussed is not applicable for digital controllers because a digital controller samples the line current measured at the beginning of each sampling period and in this case $T_p = T_S$. Therefore, the modification should be made on the '1-LPF' in order to alleviate the delay time such that the Digital Signal Processor (DSP) samples the line current before the next period beginning by the nearness of $T_n$ and uses it for the harmonic extraction as shown in Figure 2.28. In this thesis, this proposed near-next-state sampling method is used for the line current harmonic extraction.

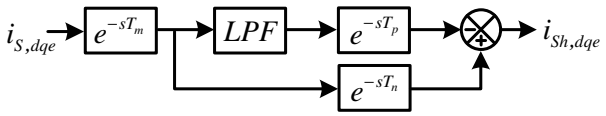



Figure 2.28 The harmonic current extraction by the modified '1-LPF' for digital controller.

#### 2.4.6.1.2 Harmonic and Fundamental Extraction of Load Voltage

The load voltage is decomposed to its harmonic and fundamental components to be used in the HIC and FCC, respectively. Considering that the load voltage waveform is rectangular when the harmonic isolation is maintained, the harmonic contents of

the rectangular wave shaped load voltages for the single-phase and the three-phase loads determine the LPF cut-off frequency.

For the single-phase applications, the harmonic spectrum of $v_{L,dqe}$ involves the components of 4n multiples of $\omega_e$. For example, the 3rd and 5th harmonic components are translated to the 4th harmonic in the synchronous frame, and the 7th and 9th harmonics translate to the 8th harmonic and so on. In the filter design, for illustration, assuming that the LPF is the first order filter with $|LPF(\omega_h = 4\omega_e)| = 2.5\%$, $\omega_{ch}$ is found to be close to $0.1\omega_e$. For the three-phase case, ($v_{L,dqe}$) is composed of 6n multiples of $\omega_e$. Considering the same attenuation as the single-phase case, $\omega_{ch}$ is found to be close to $0.15\omega_e$. However, the cut-off frequency for the LPF for the fundamental component extraction ($\omega_{c1}$) should be higher than the HPF for the harmonic extraction ($\omega_{ch}$) so that FCC can regulate the load voltage with larger bandwidth against HIC effects (due to HPF) on the fundamental frequency components. In this study, $\omega_{c1}$ is chosen as twice $\omega_{ch}$.

Unlike the HFE for the line current, for the load voltage HPF and LPF can be directly used as shown in Figure 2.29 since the measurement and process delays in $v_{Lh,dqe}$ do not contribute to instability due to its feedforward behavior in HIC and the measurement and process delays for $v_{L1,dqe}$ are negligible considering the narrow bandwidth of the system for the fundamental component controller.

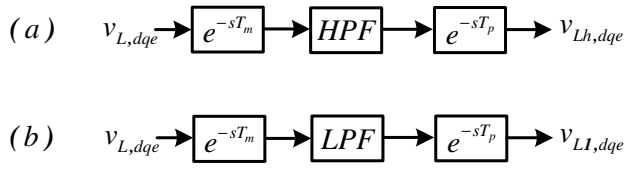



Figure 2.29 The load voltage (a) harmonic component extraction by HPF and (b) fundamental component extraction by LPF.

#### 2.4.6.2 Absolute Value Method (AVM)

In CM, the fundamental component of the load voltage is extracted by the LPF with low cut-off frequency, therefore the feedback controller of the FCC responds sluggishly. For the harmonic extraction of the load voltage in CM, the accuracy of the HPF depends on not only the filter characteristic but also the feedback part of the HIC, i.e., $K_{hi}$, as stated by (2.3) in Part 2.2.3. Thus, a new method for the load voltage decomposition is required to avoid from these weaknesses of CM.

To fulfill the bandwidth and accuracy requirements, the novel AVM has been developed in this thesis as an application-specific extraction method in order to decompose the harmonic and the fundamental components of the load voltage in an accurate and rapid manner for the SAF applications with the single-phase and three-phase diode rectifier loads with only DC bus capacitor and resistor (V-type nonlinear loads).

AVM is based on processing the rectangular wave shape of the load voltage with the phase angle information of the utility voltage provided that the harmonic isolation between the utility and the load is maintained. The method can be outlined by two processes: the fundamental component extraction and the voltage synthesis. In the fundamental component extraction process, the DC voltage quantity which represents the magnitude of the fundamental frequency component of the load voltage in the 'de' coordinate is found using the load voltage. In the voltage synthesis process, the load voltage in the rectangular wave shape and the fundamental frequency AC component of the load voltage waveforms are regenerated from the DC voltage quantity and the phase angle information. Lastly, the load harmonic voltage is obtained by the subtraction of the synthesized fundamental frequency component from the synthesized load voltage.

The phase angle ($\theta'$) to be used for processing the load voltage in AVM should be compensated for lead or lag caused by the circuit and the controller operation in order to increase the performance of the AVM. In the phasor diagram shown in of

the circuit Figure 2.14, the line voltage leads the load voltage and the lag can be found by (2.53) considering φ is very small due to low $L_S$ and $R_S$. Moreover, SRF introduces a delay time approximately as much as the rise time of the unit-step response of SRF ($t_{r,SRF}$), which is approximated by (2.54) [32], where ξ is the damping ratio of SRF. In the digital controller, $\theta_e$ is attained within a PWM cycle ($T_S$) and the application of the reference voltage generated by AVM requires a PWM cycle, as well, i.e., the total delay time of the digital controller is $2T_S$. Consequently, the compensated phase angle information (θ′) using the compensation time ($T_\theta$) for the AVM is found to be in (2.55).

$$\varphi \approx \tan^{-1}\left(\frac{\omega_e L_S I_{S1}}{V_{S1}}\right) \approx \frac{\omega_e L_S I_{S1}}{V_{S1}} \tag{2.53}$$

$$t_{r,SRF} = \left(1.25 + 2.94\xi\right)\sqrt{L_f C_f} \quad for\ 0.8 > \xi > 0 \tag{2.54}$$

$$\theta' = \theta_e + \omega_e T_\theta = \theta_e + \omega_e\left(2T_S + t_{r,SRF} - \frac{L_S I_{S1}}{V_{S1}}\right) \tag{2.55}$$

The AVM is applicable for both SPSAF and TPSAF. The following is the detailed introduction of the AVM under the titles of single-phase AVM (SPAVM) and three-phase AVM (TPAVM).

#### 2.4.6.2.1 SPAVM

In SPSAF, the block diagram and the waveforms of the AVM are illustrated in Figure 2.30 and Figure 2.31, respectively. The details of the method are revealed by means of these figures correspondingly.

The waveform of the load voltage ($v_L$) is getting closer to a square wave when the HIC operates (a). In the AVM, first of all, the absolute value of the load voltage ($|v_L|$) is taken (b). Then, $|v_L|$ is multiplied with a sine wave with the phase angle ($\sin\theta'$) in order to diminish the effect of the rise and the fall of $|v_L|$ considering that the $\sin\theta'$ is

close to zero during the rise and fall (natural filtration) (c). The signal $|v_L|\sin\theta'$ is transformed by the 'de - qe' transformation with $\theta'$ to obtain $|v_L|_{de}$, which has the $4\omega_e$ harmonic component due to the power transfer and the high frequency distortion due to the rise and the fall of $|v_L|$ (d). In order to eliminate the $4\omega_e$ harmonic component the Notch Filter (NF) with the resonance frequency of $4\omega_e$ is utilized and for eliminating the high frequency distortion is filtered out by the first order low pass filter (LPF) with the cut-off frequency around 500 Hz typically. The pureness of the output of the NF and the LPF ($V'_{L,dc}$), which is the peak value of $v_L$, is a measure of the filter performance (e). Using the relation (2.5), the peak of the fundamental frequency component ($V'_{L1}$), which can be used as the input for the FCC, is obtained. Then, the multiplication of $V'_{L1}$ and $\sin\theta'$ is the fundamental frequency component of the load voltage ($v'_{L1}$) (f). In order to acquire the harmonic component of the load voltage ($v'_{Lh}$), the load voltage ($v'_L$) is synthesized by using $V'_{L,dc}$ and $\theta'$ (g). The subtraction of $v'_{L1}$ from $v'_L$ results $v'_{Lh}$ (h).

Within the synthesis of $v'_L$, the square waveform may be regenerated purely from $V'_{L,dc}$ and $\theta'$ as given in (2.56). However, when $v'_{Lh}$ generated from this ideal waveform is used for the harmonic load voltage reference ($v^*_{Lh}$) in the HIC, neither the $v^*_{Lh}$ is correctly generated by the SAF due to the bandwidth limits of the SAF nor the SAF operates stably and appropriately due to resonances excited and overstresses on the circuit components. Thus, the maximum limit for the $dv'_L/dt$ is defined by the bandwidth of the system which is determined by the resonance frequency of the SRF ($f_o$). Thus, the rise/fall time of $v'_L$ ($T_r$) is found as in (2.57). The synthesis with the linearization around $\theta' = 0$ and $\theta' = \pi$ using $T_r$ is given in (2.58).

$$v''_L(\theta') = \begin{cases} V'_{L,dc} & ;0 \le \theta' < \pi \\ -V'_{L,dc} & ;\pi \le \theta' < 2\pi \end{cases} \tag{2.56}$$

$$\frac{1}{T_r} < f_o = \frac{1}{\sqrt{L_f C_f}} \tag{2.57}$$

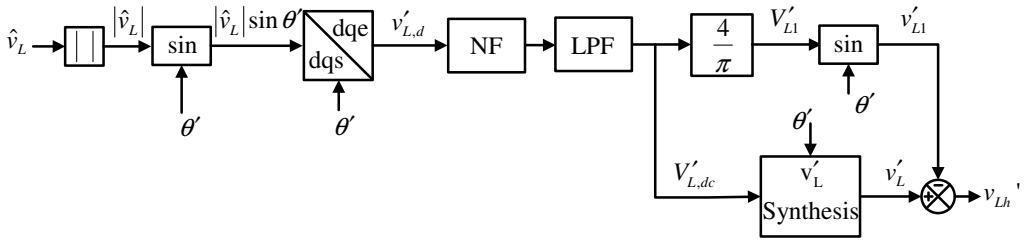



Figure 2.30 The SPAVM block diagram.

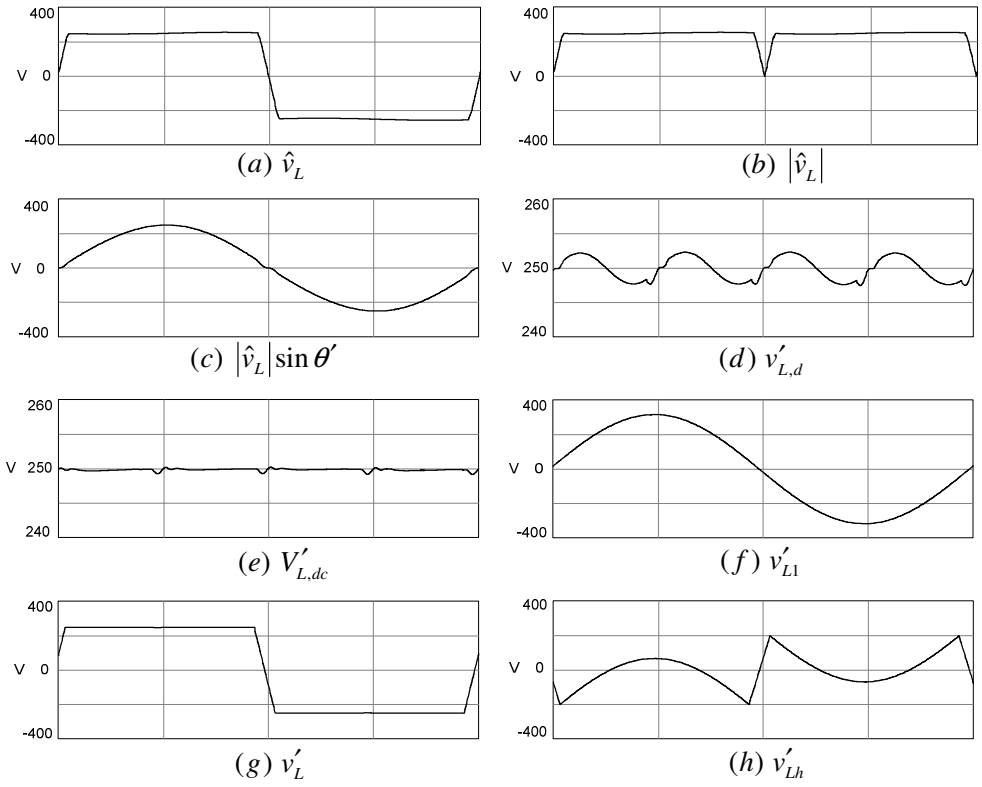



Figure 2.31 The waveforms of the process of SPAVM.

$$v'_L(\theta') = \begin{cases} V'_{L,dc}\dfrac{\theta'}{\omega_e T_r} & ;0 \le \theta' < \omega_e T_r \\ V'_{L,dc} & ;\omega_e T_r \le \theta' < \pi - \omega_e T_r \\ V'_{L,dc}\dfrac{\pi - \theta'}{\omega_e T_r} & ;\pi - \omega_e T_r \le \theta' < \pi + \omega_e T_r \\ -V'_{L,dc} & ;\pi + \omega_e T_r \le \theta' < 2\pi - \omega_e T_r \\ V'_{L,dc}\dfrac{\theta' - 2\pi}{\omega_e T_r} & ;2\pi - \omega_e T_r \le \theta' < 2\pi \end{cases} \quad (2.58)$$

#### 2.4.6.2.2 TPAVM

TPAVM is more complex than SPAVM. The block diagram and the waveforms of AVM are illustrated in Figure 2.32 and Figure 2.33. The details of the method are discussed by means of these waveforms correspondingly as in the single-phase case.

The waveforms of the line-to-line voltages ($v_{Lab}$, $v_{Lbc}$, and $v_{Lac}$) approach a rectangular wave (a) and the phase voltages ($v_{La}$, $v_{Lb}$, and $v_{Lc}$) become six-step waveform when the HIC operates (b). In the AVM, the absolute values of the line-line load voltages are summed up to form a DC voltage equal to two times the load DC bus voltage ($|v_L|$), then, $|v_L|$ is multiplied with '1/3' to find the peak value of the load AC side phase voltage (c). The signal $|v_L|/3$ has the $6\omega_e$ harmonic component due to the power transfer and has the $2\omega_e$ harmonic component if there is negative sequence in the load voltages. In order to eliminate the harmonic components the notch filters with the resonance frequencies of $2\omega_e$ and $6\omega_e$ (NF-2$^{nd}$ and NF-6$^{th}$) are utilized. The pureness of the DC output of the NF ($V'_{L,dc}$), which is the peak value of the load phase voltages, is a measure of the filter performance (d). Using the relation (2.6), the peak of the fundamental frequency component of the load phase voltage ($V'_{L1}$), which can be used as the input for the FCC, is obtained. Then, the multiplications of $V'_{L1}$ with $\sin\theta'$, $\sin(\theta'-2\pi/3)$, and $\sin(\theta'+2\pi/3)$ give the fundamental frequency component of the load phase voltages ($v'_{La1}$, $v'_{Lb1}$, and $v'_{Lc1}$) (e). In order to acquire the harmonic component of the load phase voltages ($v'_{Lah}$, $v'_{Lbh}$, and $v'_{Lch}$), the load phase voltages ($v'_{La}$, $v'_{Lb}$, and $v'_{Lc}$) are synthesized by using $V'_{L,dc}$ and $\theta'$ (f). The subtractions of $v'_{La1}$, $v'_{Lb1}$, and $v'_{Lc1}$ from $v'_{La}$, $v'_{Lb}$, and $v'_{Lc}$ result $v'_{Lah}$, $v'_{Lbh}$, and $v'_{Lch}$ correspondingly (g).

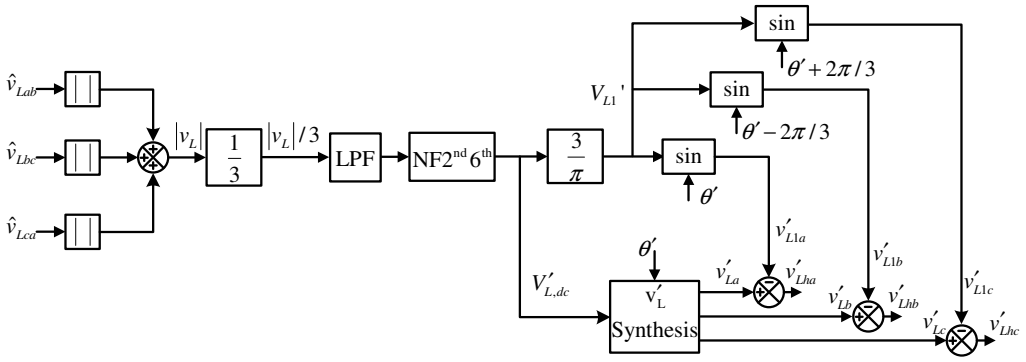



Figure 2.32 The TPAVM block diagram.

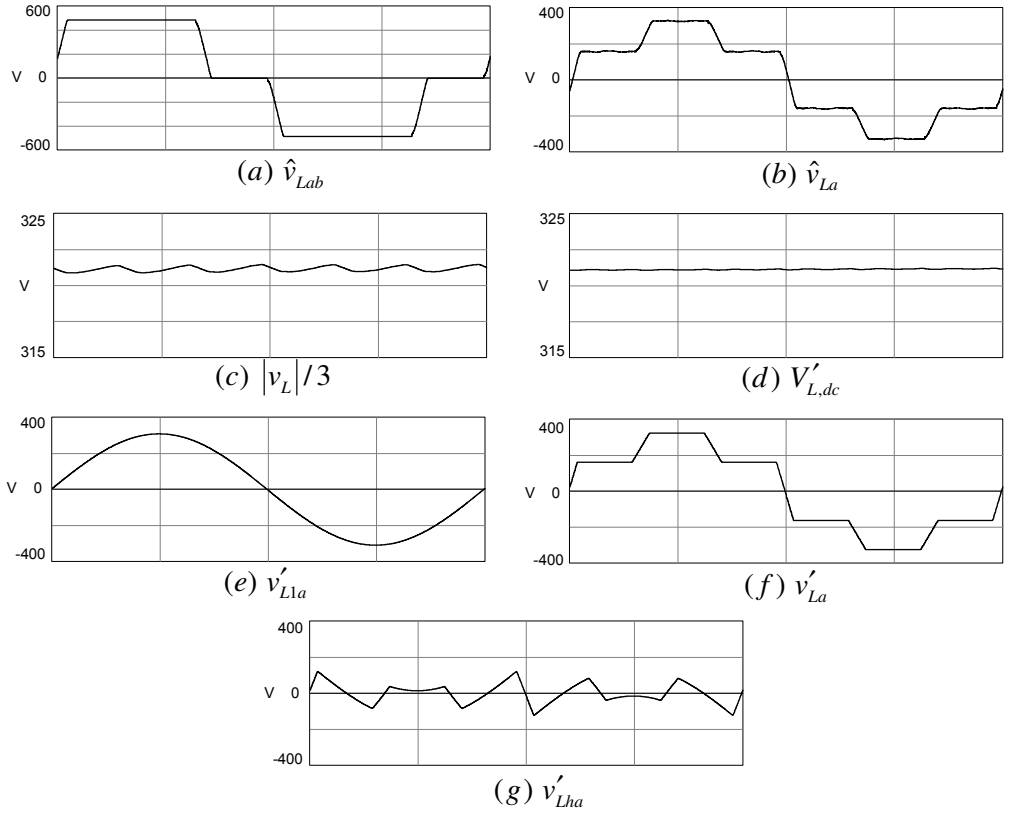



Figure 2.33 The waveforms of the process of TPAVM.

The rules for the synthesis of the load phase voltages as pure six-step waveforms are given in (2.59) for each phase. In order to limit $dv'_L/dt$, $T_r$ is bounded in the same manner as for the single-phase case. However, the linearization with $T_r$ is cumbersome for the three-phase case due to six linearization regions whereas there are two linearization regions in SPAVM. Therefore, a rate-of-change limiter, with simpler structure, is utilized per phase for TPAVM as shown in Figure 2.34 [31]. Considering inherent phase delays the rate of change limiter introduces at the rise and fall regions of pure six-step load voltage waveform, the input voltage of the rate-of-change limiter is modified as given in (2.60). It should be noted that a low-pass filter per-phase may be used instead of the rate-of-change limiter provided that the phase lag is compensated.

$$v''_{Labc}(\theta'') = \begin{cases} V'_{L,dc}/2 & ;0 \le \theta'' < \pi/3 \\ V'_{L,dc} & ;\pi/3 \le \theta'' < 2\pi/3 \\ V'_{L,dc}/2 & ;2\pi/3 \le \theta'' < \pi \\ -V'_{L,dc}/2 & ;\pi \le \theta'' < 4\pi/3 \\ -V'_{L,dc} & ;4\pi/3 \le \theta'' < 5\pi/3 \\ -V'_{L,dc}/2 & ;5\pi/3 \le \theta'' < 2\pi \end{cases} \quad where\ \theta'' = \begin{cases} \theta' & ;v'_{Labc} = v'_{La}(\theta') \\ \theta' - 2\pi/3 & ;v'_{Labc} = v'_{Lb}(\theta') \\ \theta' + 2\pi/3 & ;v'_{Labc} = v'_{Lc}(\theta') \end{cases} \tag{2.59}$$

$$v''_{Labc}(\theta'') = \begin{cases} V'_{L,dc}/2 & ;-\omega_e T_r \le \theta'' < \pi/3 - \omega_e T_r/2 \\ V'_{L,dc} & ;\pi/3 - \omega_e T_r/2 \le \theta'' < 2\pi/3 - \omega_e T_r/2 \\ V'_{L,dc}/2 & ;2\pi/3 - \omega_e T_r/2 \le \theta'' < \pi - \omega_e T \\ -V'_{L,dc}/2 & ;\pi - \omega_e T \le \theta'' < 4\pi/3 - \omega_e T_r/2 \\ -V'_{L,dc} & ;4\pi/3 - \omega_e T_r/2 \le \theta'' < 5\pi/3 - \omega_e T_r/2 \\ -V'_{L,dc}/2 & ;5\pi/3 - \omega_e T_r/2 \le \theta'' < 2\pi - \omega_e T_r \end{cases} \quad where\ \theta'' = \begin{cases} \theta' & ;v'_{Labc} = v'_{La}(\theta') \\ \theta' - 2\pi/3 & ;v'_{Labc} = v'_{Lb}(\theta') \\ \theta' + 2\pi/3 & ;v'_{Labc} = v'_{Lc}(\theta') \end{cases} \tag{2.60}$$

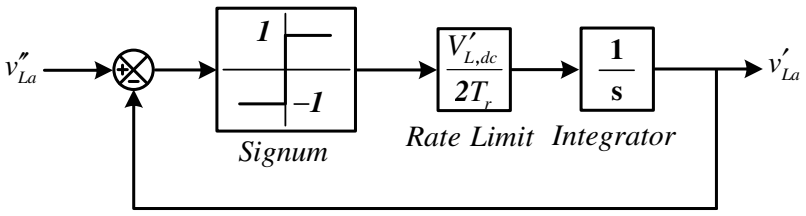



Figure 2.34 The per-phase diagram of the rate-of-change limiter for the load voltage synthesis in TPAVM.

## 2.5 Summary

In this chapter, the power circuit and the control of the single-phase and the three-phase SAF have been investigated and the novel approach for the decomposition of the harmonic and the fundamental components of the load voltage, AVM has been proposed. The power units; VSI, SIT, and SRF inject the SAF voltage corresponding to the reference voltage, produced by the controllers, between the utility and the V-type nonlinear load. The selection and design of the main power units are involved procedure to encompass all the constraints of the SAF application. HIC, FCC, PLL, HFE, and RDC units of the control system of the SAF are responsible for producing the reference voltage for the harmonic voltage isolation, the load voltage regulation, and increasing stability margin of the system. The PWM unit of the control system generates on/off signals to drive the VSI of the power circuit with respect to the reference voltage produced and closes the control loop.

The performances of the HIC and the FCC strongly depend on the HFE performance. Conventionally, the HFE for the V-type load voltage is sluggish and lacks of accuracy. The novel approach, AVM decomposes the V-type load voltage fast and accurately. Hence, the HIC and the FCC performances are improved significantly. In the following chapter the controller design is discussed and the upcoming chapters will illustrate the superior performance of the SAF with the proposed method.

# CHAPTER 3

# THE SIMPLIFIED LINEAR MODELS OF THE SERIES ACTIVE FILTER COMPENSATED SYSTEM

## 3.1 Introduction

In this chapter, the simplified linear models of SAF compensated systems at low frequency (valid for the fundamental frequency and under) and high frequency (valid above the fundamental frequency and below the switching frequency) are derived considering the characteristics of power circuits and control algorithms at low and high frequency for single-phase and three-phase circuits (SPSAF and TPSAF). In derivation of the models, simplifications are made in order to ease the analysis of the models. The model parameters are the same as the parameters that will be used in the simulations and the experiments. In the computer software MATLAB-Simulink V7.0, these models are analyzed via Bode diagrams and step-response tests.

By means of the analysis of the high frequency model, the gains of the harmonic isolation controller (HIC) and the resonance damping controller (RDC) are determined. Likewise, the fundamental component controller (FCC) is designed via the linear analysis of the low frequency model. In the models, CM and AVM are used separately as load voltage harmonic/fundamental decomposition methods. Moreover, the responses of the SAF systems to voltage sags and load dynamics are simulated on the low frequency model and the simulation results obtained using CM and AVM are compared.

### 3.2 Linear Models

The linear models of the SAF system are derived at high frequency and low frequency in consistency with the theory given in Chapter 2. In the linear models, the SAF compensated system units which are negligible at the high frequency and/or the low frequency are ignored in the corresponding model. In the following, the derivation of these models and the analyses of the SPSAF and TPSAF linear models are presented.

#### 3.2.1 High Frequency Model

At frequencies above the fundamental frequency and below the switching frequency, the SAF system can be represented with the equivalent circuit given in Figure 3.1. SIT is simplified as an ideal transformer with the turns-ratio of N and the leakage inductances ($L_1$ and $L_2$) and the winding resistances ($R_1$ and $R_2$). It should be noted that the core losses (eddy and hysteresis) are not modeled for the sake of simplicity but their effects will be interpreted in the context. Hence, the equivalent line resistance and inductance are found in (3.1). SRF is modeled as it is referred to the utility side by the turns-ratio N of SIT. The referred SRF parameters are given in (3.2). Using these parameters, the SRF transfer functions, which are used in the model, are given in (3.3) and (3.4).

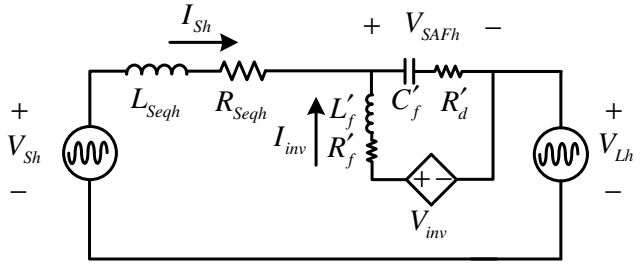



Figure 3.1 The high frequency equivalent circuit of the SAF compensated system.

$$R_{Seqh} = R_S + R_2 + R_1 / N^2$$
$$L_{Seqh} = L_S + L_2 + L_1 / N^2 \tag{3.1}$$

$$R'_d = R_d / N^2$$
$$C'_f = N^2 C_f$$
$$L'_f = L_f / N^2 \tag{3.2}$$
$$R'_f = R_f / N^2$$

$$\frac{V_{SAFh}(s)}{V_{inv}(s)} = \frac{1 + sC'_f R'_d}{1 + sC'_f \left(R'_d + R'_f\right) + s^2 L'_f C'_f} \tag{3.3}$$

$$\frac{I_C(s)}{V_{SAFh}(s)} = \frac{sC'_f}{1 + sC'_f R'_d} \tag{3.4}$$

The control block diagram of the SAF compensated system at high frequency is shown in Figure 3.2. In the figure, an additional first order delay block stands for the inverter delay time which is required in order that the inverter generates the voltage at its output terminals ($V_{inv}$) in consistency with its reference voltage ($V_{inv}$*) (3.5). The delay time ($T_d$) is the sum of measurement, process, and PWM delays ($T_m$, $T_p$, and $T_{PWM}$) (3.6). Assuming $T_m$ is significantly smaller than $T_S$, $T_{PWM} = T_S$ (its maximum value for double-update), and $T_p = T_S/5$ (by means of the near-next-state sampling approach as discussed in Section 2.4.6.1.1, by the nearness of $T_n = T_S/5$, which is applicable in practice); $T_d$ turns out to be $6T_S/5$. In the model, the feedforward part of HIC is not given because it does not affect the characteristic equation of the system.

$$\frac{V_{inv}(s)}{V_{inv}^{*}(s)} = \frac{1}{1 + sT_d} \tag{3.5}$$

$$T_d = T_m + T_p + T_{PWM} \approx T_n + T_{PWM} \approx T_S / 5 + T_S = 6T_S / 5 \tag{3.6}$$

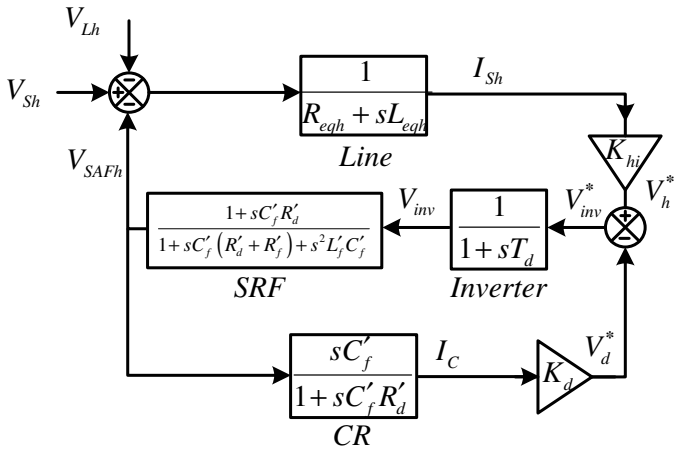



Figure 3.2 The control block diagram of the high frequency linear model of the SAF compensated system.

### 3.2.2 Low Frequency Model

The low frequency model has been derived at the 'de' frame based on the theoretical background given in Chapter 2, where the low frequency model is derived for the ideal SAF circuit, i.e., an ideally controllable voltage source. Therefore, this model should be revised considering the presence of SIT and SRF. In the revised model, SRF is represented with the filter inductance ($L_f$) and the filter resistance ($R_f$). The SRF components which are effective at high frequency such as the filter capacitance ($C_f$) and the damping resistance ($R_d$) are ignored due to the low bandwidth (<100 Hz) of the low frequency model of the SAF system. In the equivalent circuit at the low frequency, SIT is modeled as the same in the high frequency equivalent circuit. The low frequency equivalent circuit is illustrated in the Figure 3.3. In the figure, $R_{Seq1}$ and $L_{Seq1}$ are the equivalent series resistance and the equivalent series inductance given in (3.7). The load parameters, $C_{Leq}$ and $R_{Leq}$, are given in (3.8) as found in Chapter 2, where $N_V$ is the AC/DC transformation ratio of the load rectifier.

$$\begin{aligned} R_{Seq1} &= R_S + R_2 + (R_1 + R_f)/N^2 \\ L_{Seq1} &= L_S + L_2 + (L_1 + L_f)/N^2 \end{aligned} \tag{3.7}$$

$$R_{Leq} = N_V{}^2 R_L$$
$$C_{Leq} = C_L / N_V{}^2 \tag{3.8}$$

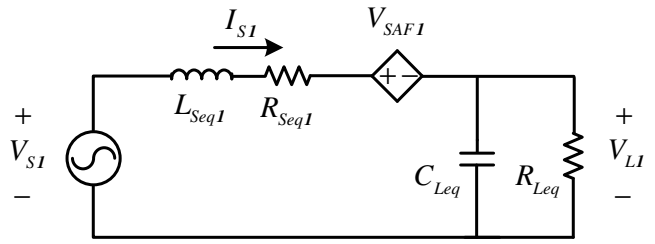



Figure 3.3 The low frequency equivalent circuit of the SAF compensated system.

The control block diagram of the SAF system at low frequency is shown in Figure 3.4. In the figure, the line and the load transfer functions were given as in the previous chapter. The line current harmonic feedback is composed of harmonic extraction function ($G_{HEi}(s)$), which is a first order high pass filter (HPF), and an equivalent gain ($K_{hi,eq}$) in 'de' frame. For TPSAF, $K_{hi,eq} = K_{hi}$ due to the power invariant transformations (C and T) for three-phase. However, T ('de-qe' transformation matrix) is not power invariant for single-phase signals; therefore, the relation between $K_{hi}$ and $K_{hi,eq}$ is found by the equalization of the power before and after the transformation as given in (3.9).

$$P = \frac{V_{S1,rms}{}^2}{K_{hi}} = \frac{V_{S1}{}^2}{K_{hi,eq}} \Rightarrow K_{hi,eq} = 2K_{hi} \tag{3.9}$$

The fundamental and the harmonic frequency extraction transfer functions ($G_{HEv}(s)$ and $G_{FEv}(s)$) depend on the extraction methods, CM, single-phase AVM (SPAVM), and three-phase AVM (TPAVM), of which the transfer functions are given in (3.10) and (3.11). It should be noted that the AVM transfer functions are simplified such that the low pass filters with 500 Hz for SPAVM and 300 Hz for TPAVM are ignored considering the bandwidth of the systems well below these cut-off frequency.

Another point worth noticing is that while the damping ratio of the other notch filters are chosen as 1 to ensure stable operation, the damping ratio of the notch filter of TPSAF at the second harmonic frequency (100 Hz) is 0.25 in order that the filter does not restrict the bandwidth of the system severely. Besides, the feedforward controller of FCC is not shown in the figure considering that it does not affect the characteristic equation of the SAF system.

$$G_{FEv}(s)=\begin{cases}\dfrac{\omega_{c1v}}{\omega_{c1v}+s} & ;CM\\ \dfrac{\omega^2{}_{4th}+s^2}{\omega^2{}_{4th}+s2\omega_{4th}+s^2} & ;SPAVM\\ \dfrac{\omega^2{}_{6th}+s^2}{\omega^2{}_{6th}+s2\omega_{6th}+s^2}\dfrac{\omega^2{}_{2nd}+s^2}{\omega^2{}_{2nd}+s0.5\omega_{2nd}+s^2} & ;TPAVM\end{cases} \tag{3.10}$$

$$G_{HEv}(s)=\begin{cases}\dfrac{s}{\omega_{c1v}+s} & ;CM\\ 0 & ;SPAVM\\ 0 & ;TPAVM\end{cases} \tag{3.11}$$

In the control block diagram, FCC is composed of a PI controller and a phase-lead compensator for CM. The PI controller provides high gain for the system at low frequency to obtain good steady-state performance and the compensator improves the phase margin of the system for good transient response. Advantageously, a PI controller is sufficient for both good steady-state and transient response when AVM is used as a load voltage harmonic/fundamental extractor.

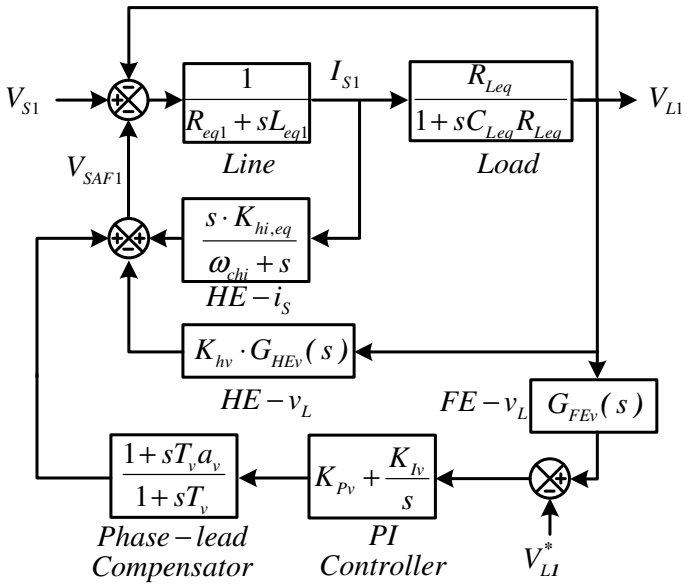



Figure 3.4 The control block diagram of the low frequency linear model of the SAF compensated system.

### 3.3 SPSAF

Via the high and low frequency control block diagrams derived in the previous section, the controllers of SPSAF are designed such that $K_{hi}$ and $K_d$ are determined to ensure stable harmonic isolation; and the PI controller gains ($K_{Pv}$ and $K_{Iv}$) and the phase-lead compensator gains ($a_v$ and $T_v$) are optimized to regulate the load voltage against line and load disturbances. In order to analyze the linear models derived, the SPSAF parameters, which are used in the simulations and the experiments, are listed in Table 3.1.

#### 3.3.1 High Frequency Model

To be used in the high frequency linear model of SPSAF, the parameters derived from the Table 3.1 are listed in Table 3.2 and the model is built up in MATLAB-Simulink as shown in Figure 3.5.

Table 3.1 The linear model parameters (SPSAF)

| | | |
|---|---|---|
| $V_S$ | Rated utility voltage | 220 $V_{rms}$ |
| $L_S$ | Utility inductance | 200 μH |
| $R_S$ | Utility resistance | 100 mΩ |
| $C_L$ | Load capacitance | 2.2 mF |
| $R_L$ | Load resistance | 24 Ω |
| $L_f$ | SRF inductance | 1.8 mH |
| $C_f$ | SRF capacitance | 2.35 μF |
| $R_f$ | Resistance of the SRF inductance | 300 mΩ |
| $R_d$ | SRF damping resistance | 5.6 Ω |
| $L_1$ | Primary side leakage inductance of SIT | 40 μH |
| $L_2$ | Secondary side leakage inductance of SIT | 10 μH |
| $R_1$ | Primary side copper resistance of SIT | 140 mΩ |
| $R_2$ | Secondary side copper resistance of SIT | 35 mΩ |
| N | Turns-ratio of SIT ($N_1$:$N_2$) | 2 |
| $N_V$ | AC/DC transformation ratio (4/π) | 1.27 |
| $f_{PWM}$ | PWM frequency | 20 kHz |
| $T_S$ | Sampling time (Double update) | 25 μs |

Table 3.2 The parameters of the high frequency model (SPSAF)

| | | |
|---|---|---|
| $L_{Seqh}$ | Equivalent line inductance | 220 μH |
| $R_{Seqh}$ | Equivalent line resistance | 170 mΩ |
| $L'_f$ | The line side referred SRF inductance | 450 μH |
| $C'_f$ | The line side referred SRF capacitance | 9.4 μF |
| $R'_f$ | The line side referred resistance of the SRF inductance | 75 mΩ |
| $R'_d$ | The line side referred SRF damping resistance | 1.4 Ω |
| $T_d$ | Total delay time of the inverter | 30 μs |

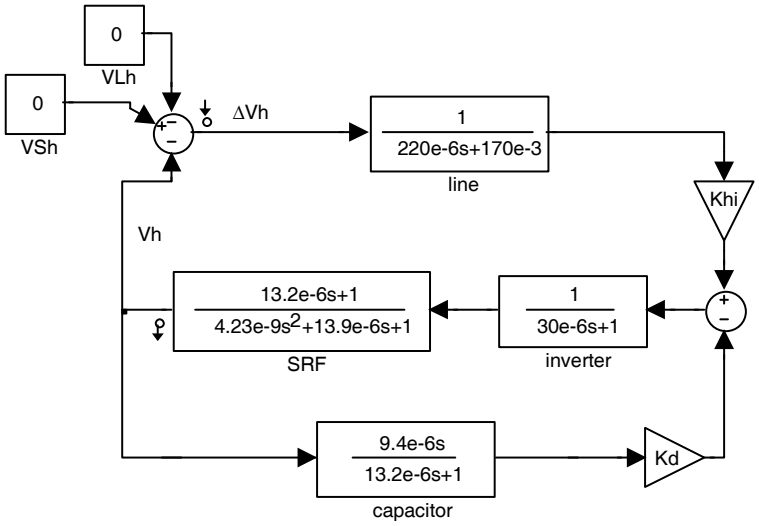



Figure 3.5 The control block diagram of the high frequency linear model in MATLAB-Simulink (SPSAF).

The controller design can be carried by the open loop transfer function of the system defined as $\Delta V_h/V_h(s)$ and represents the harmonic voltage to the compensation voltage transfer function. Thus, by means of the $\Delta V_h/V_h(s)$ Bode diagrams, $K_d$ and $K_{hi}$ can be determined as follows. For example, the Bode diagram of the system is given in Figure 3.6 for $K_d = 20$ and $K_{hi} = 8$. Although the gain margin ($G_M$=8.38 dB) is good for relative stability, the low phase margin ($\varphi_M = 20.5^\circ$) shows that the increase in $K_{hi}$ leads to instability. In order to see the effects of the gains on the margins, two cases are considered. For the first case, $K_d = 20$ and $K_{hi} = 4$, 6, 8, 10, and 12 are used in Bode diagrams of the system as seen in Figure 3.7. In the figure, as $K_{hi}$ increases $G_M$ and $\varphi_M$ decrease. In the second case, Bode diagrams for $K_{hi} = 8$ and $K_d = 10$, 15, 20, 25, and 30 are seen in Figure 3.8, where as $K_d$ increases $G_M$ increases and $\varphi_M$ does not change significantly. In the selection of $K_{hi}$, it should be noted that high $K_{hi}$ means better harmonic isolation in practice; therefore, the phase margin can be selected as low as 20° with reasonable $G_M$ (> 6 dB) in order not to sacrifice harmonic isolation performance. Besides, it should be also taken into account that the core losses of SIT at high frequency, which are not modeled, provide extra damping and improve $\varphi_M$ in practice. For $K_{hi} = 10$ and $K_d = 25$, the conditions given for the stability margins are satisfied such that $G_M = 10$ dB and $\varphi_M = 20^\circ$.

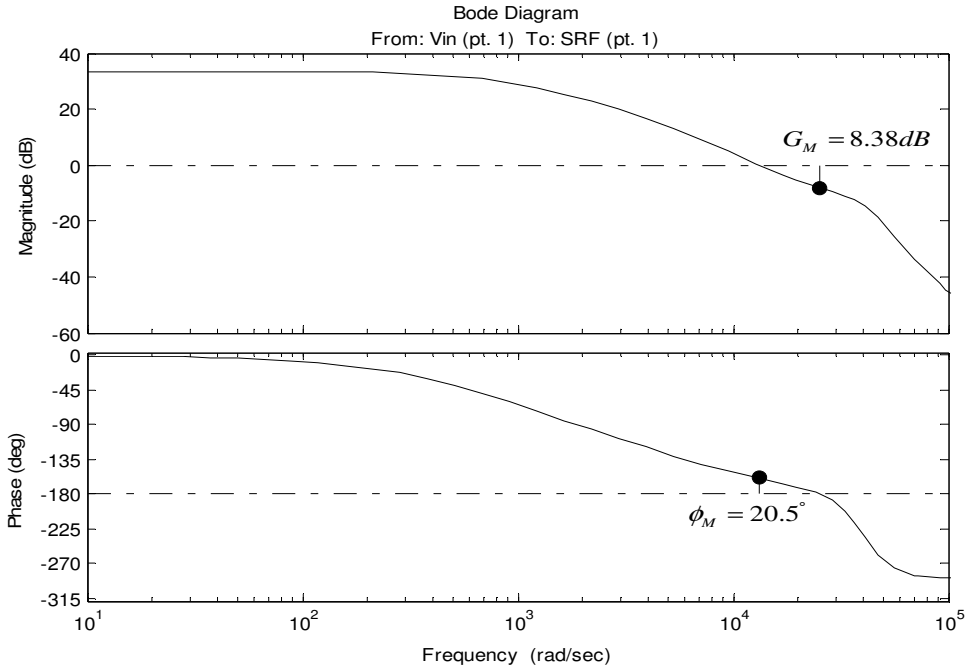



Figure 3.6 The open-loop Bode diagram of $\Delta V_h/V_h(s)$ for $K_{hi} = 8$ and $K_d = 20$ (SPSAF).

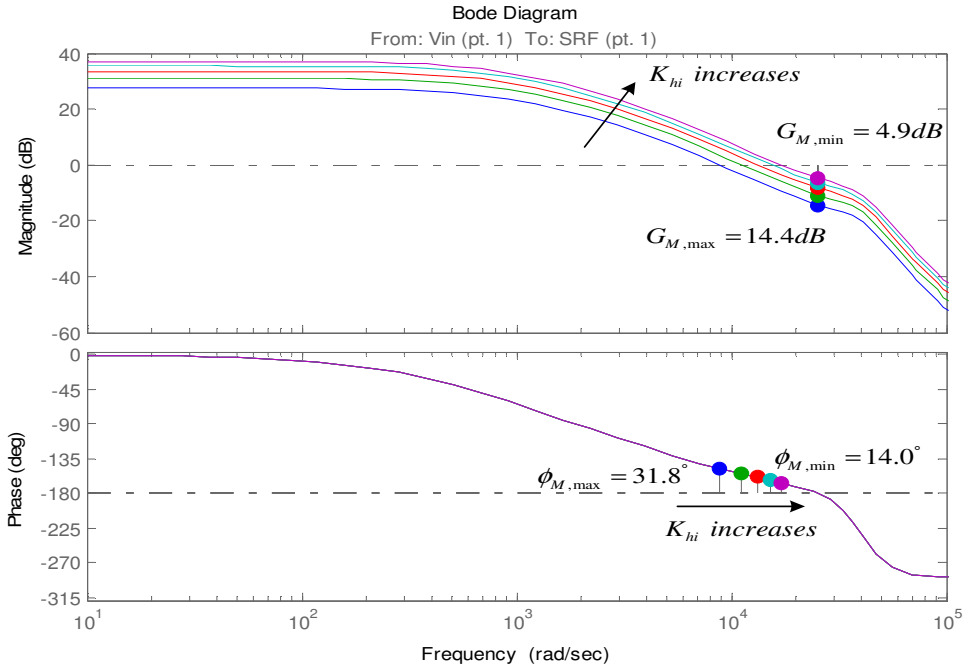



Figure 3.7 The open-loop Bode diagrams of $\Delta V_h/V_h(s)$ for $K_d = 20$ (SPSAF).

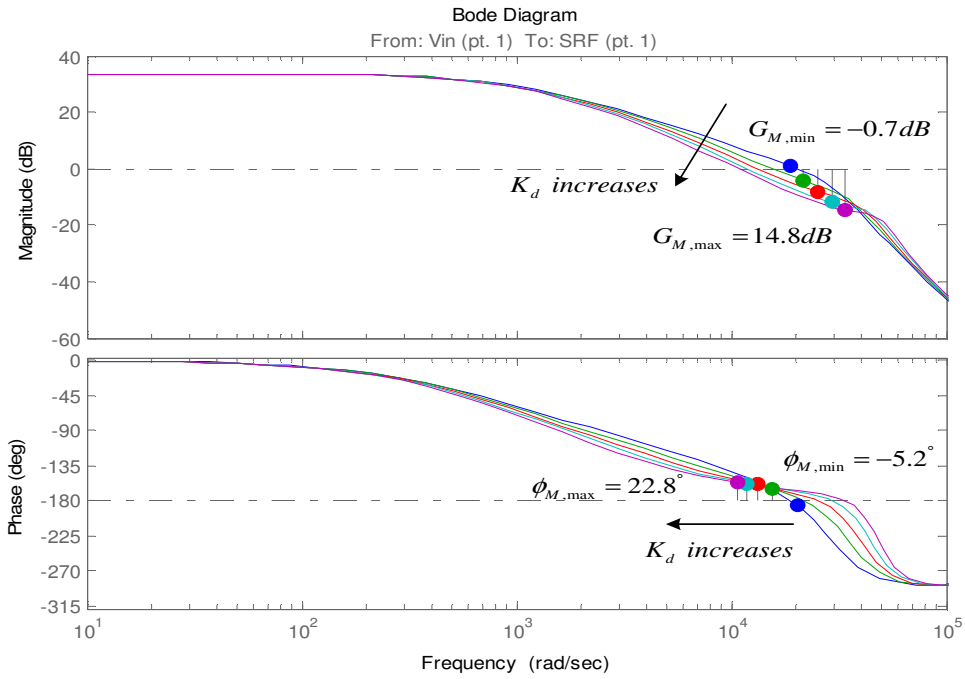



Figure 3.8 The open-loop Bode diagrams of $\Delta V_h/V_h(s)$ for $K_{hi} = 8$ (SPSAF).

In the closed loop system, $I_{Sh}/V_{Lh}(s)$ represents the admittance of the system. As shown in the Bode diagram of $I_{Sh}/V_{Lh}(s)$ in Figure 3.9, the circuit has low admittance for lower harmonic frequencies such that $|I_{Sh}/V_{Lh}| < 0.2$ for $f < 900$ Hz. Considering $K_{hi} = 10\ \Omega$, the admittance is 0.1 *S* ideally. However, the admittance significantly increases as the frequency approaches the resonant frequency of the switching ripple filter ($f_o \approx 2.5$ kHz). Thus, the feedback controller of HIC is more effective at lower harmonic frequencies.

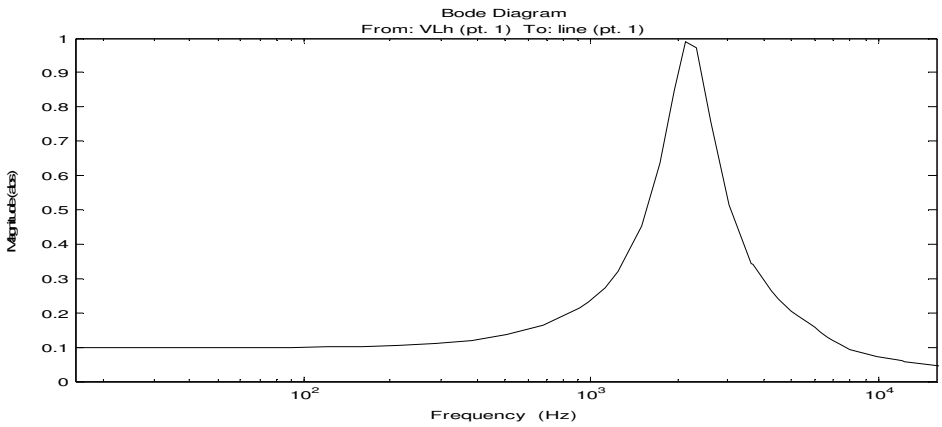



Figure 3.9 The closed-loop Bode diagram of $I_{Sh}/V_{Lh}(s)$ (SPSAF).

### 3.3.2 Low Frequency Model

The parameters which are used in the low frequency linear model are derived from Table 3.1 and these parameters are listed in Table 3.3. The linear models can be derived for CM and AVM by using these parameters. In order to design the PI controller and the phase-lead compensator, the linear models can be analyzed by Bode diagrams for the open-loop control block diagram of the SPSAF system. First of all, for $K_{Iv} = 0$, $K_{Pv}$ is determined such that $K_{Pv}$ provides sufficient $G_M$ and $\varphi_M$. Then, $K_{IV}$ is selected as high as possible in order to improve steady-state behavior provided that $G_M$ and $\varphi_M$ are tolerable. If $\varphi_M$ with the PI controller is not sufficient, then the phase-lead compensator is designed by means of conventional design methods [32], [33]. Then, the step-response of the controlled and compensated system shows whether the design is suitable for the system or not. Finally, the responses of the system against voltage sags and load dynamics are simulated for the designed feedback loop. Besides, the effects of the harmonic isolation controller gains on the low frequency system are investigated by the Bode diagrams for the open loop system.

Table 3.3 The parameters of the low frequency model (SPSAF)

| | | |
|---|---|---|
| $V_{S1}$ | Rated equivalent fundamental frequency utility voltage | 220√2 V |
| $L_{Seq1}$ | Equivalent line inductance | 670 μH |
| $R_{Seq1}$ | Equivalent line resistance | 245 mΩ |
| $C_{Leq}$ | Equivalent load capacitance | 1.36 mF |
| $R_{Leq}$ | Equivalent load resistance | 38.7 Ω |
| $N_V$ | AC/DC transformation ratio | 1.27 |
| $K_{hi,eq}$ | HIC gain for line current | 20 |
| $K_{hv}$ | HIC gain for load voltage (CM) | 0.9 |
| $K_{hv}$ | HIC gain for load voltage (AVM) | 1 |
| $f_{chi}$ | HIC HPF cut-off frequency for line current | 5 Hz |
| $f_{chv}$ | HIC HPF cut-off frequency for load voltage (CM) | 5 Hz |
| $f_{c1v}$ | FCC LPF cut-off frequency (CM) | 10 Hz |
| $f_{4th}$ | AVM resonant filter frequency | 200 Hz |

#### 3.3.2.1 CM

The low frequency linear model for CM is built up in MATLAB-Simulink, as shown in Figure 3.10. For $K_{Iv} = 0$ and $T_v = 0$, $K_{Pv}$ is chosen in order that $\varphi_M$ of the open-loop transfer function of $V_f/V_{S1}(s)$ $G_M$ is larger than 6 dB and $\varphi_M$ is around 50˚ as a rule of thumb. For $K_{Pv} = 1.5$, $G_M = 53.7$ dB and $\varphi_M = 49.2$˚. However, $\varphi_M$ decreases when $K_{Iv}$ is used to eliminate the steady-state error of the system. For $K_{Pv} = 1.5$ and $K_{Iv} = 40$, $G_M = 47.8$ dB and $\varphi_M = 23.4$˚. In order to increase $\varphi_M$, a phase-lead compensator is designed such that $a_v$ and $T_v$ are found to be 4.6 and 10 ms respectively. The stability margins of the compensated system turn out to be $G_M = 46.2$ dB and $\varphi_M = 44.4$˚. The open-loop Bode diagrams of $V_f/V_{S1}(s)$ during the design procedure of the PI controller and the phase-lead compensator show the effects of the PI controller and the compensator, as shown in Figure 3.11. The step-

responses of $V_f/V_{S1}(s)$ with and without the compensator are given in Figure 3.12, which shows that the compensator improves the step response such that it damps oscillations and enhances the settling time ($t_{ss}$ : 0.32 → 0.25 s) and the overshoot percentage ($M_p$ : 0.32% → 17%). As seen in Figure 3.13, which is the Bode diagram of $V_f/V_{S1}(s)$ for the closed-loop system, the bandwidth of the system is 170 rad/s (27 Hz).

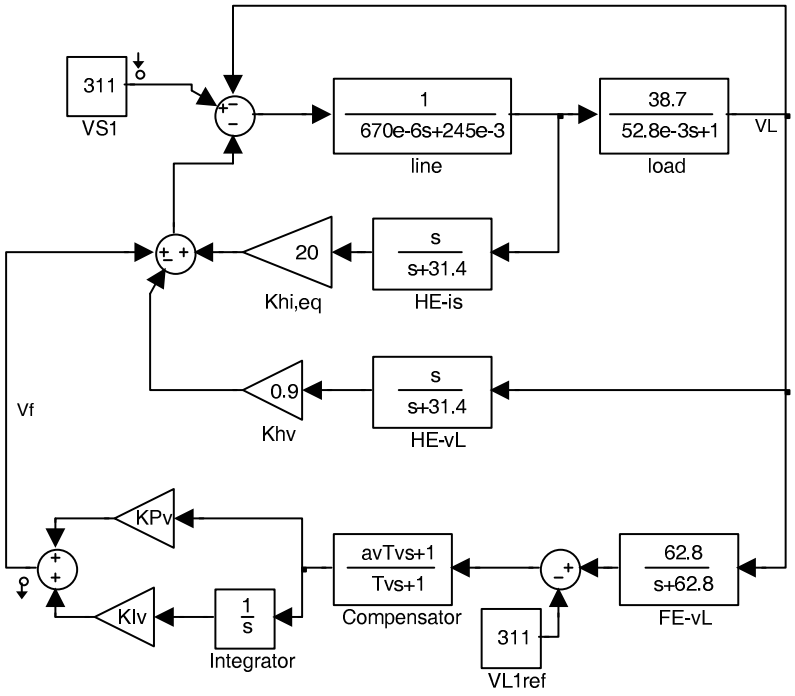



Figure 3.10 The control block diagram of the low frequency linear model in MATLAB-Simulink (SPSAF-CM).

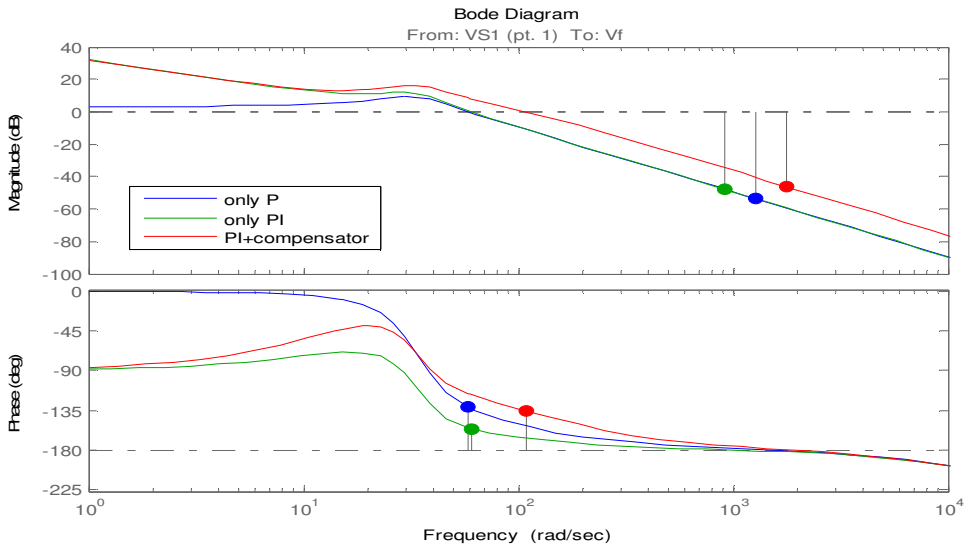



Figure 3.11 The open-loop Bode diagrams of $V_f/V_{S1}(s)$ during the controller design procedure (SPSAF-CM).

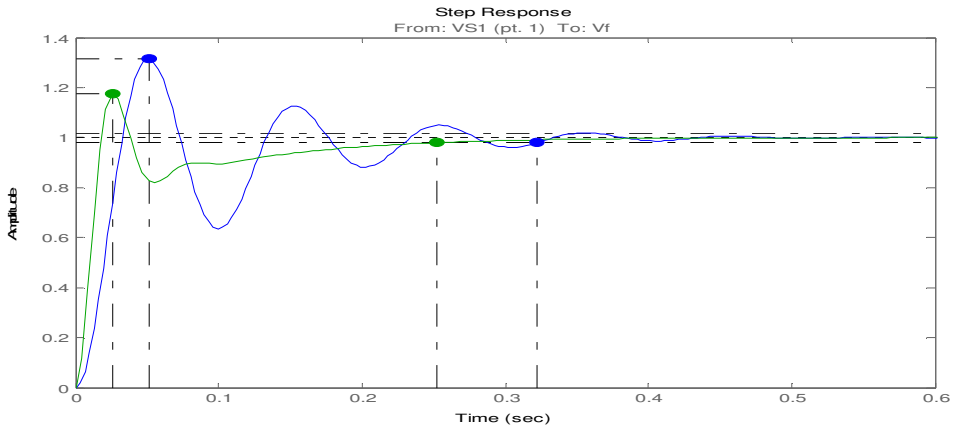



Figure 3.12 The step-responses of $V_f/V_{S1}$ (s) for the uncompensated (blue) and the compensated (green) closed-loop systems (SPSAF-CM).

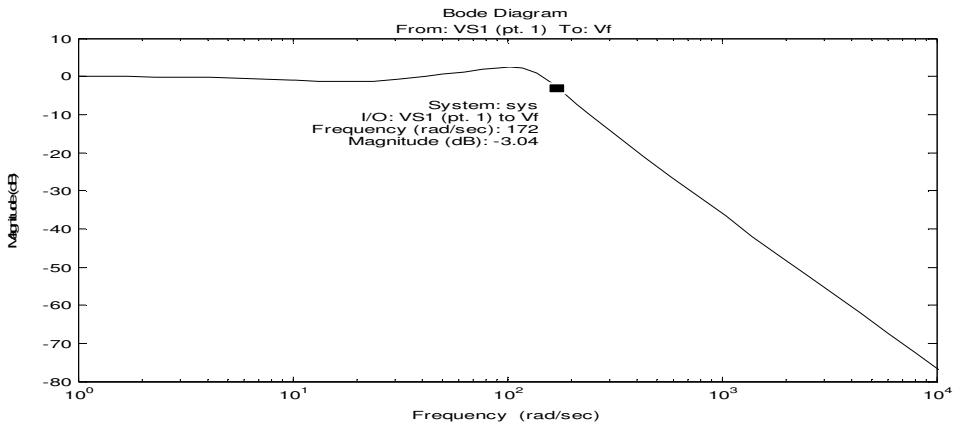



Figure 3.13 The closed-loop Bode diagram of $V_f/V_{S1}$ (s) (SPSAF-CM).

In order to see the effects of HIC on the low frequency model, the open-loop Bode diagram of the system is analyzed for sets of $K_{hi,eq}$ and $K_{hv}$ values. In Figure 3.14, keeping $K_{hi,eq}$ = 20, $K_{hv}$ values are swept from 0.5 to 0.9 in the open-loop Bode diagrams and it is observed that $\varphi_M$ decreases slightly (53.2˚ to 44.4˚) as $K_{hv}$ increases. In Figure 3.15, keeping $K_{hv}$ = 0.9, the open-loop Bode diagrams with $K_{hi,eq}$ = 4, 8, 12, 16, and 20 show that $\varphi_M$ increases significantly (22.4˚ to 44.4˚) as $K_{hi,eq}$ increases.

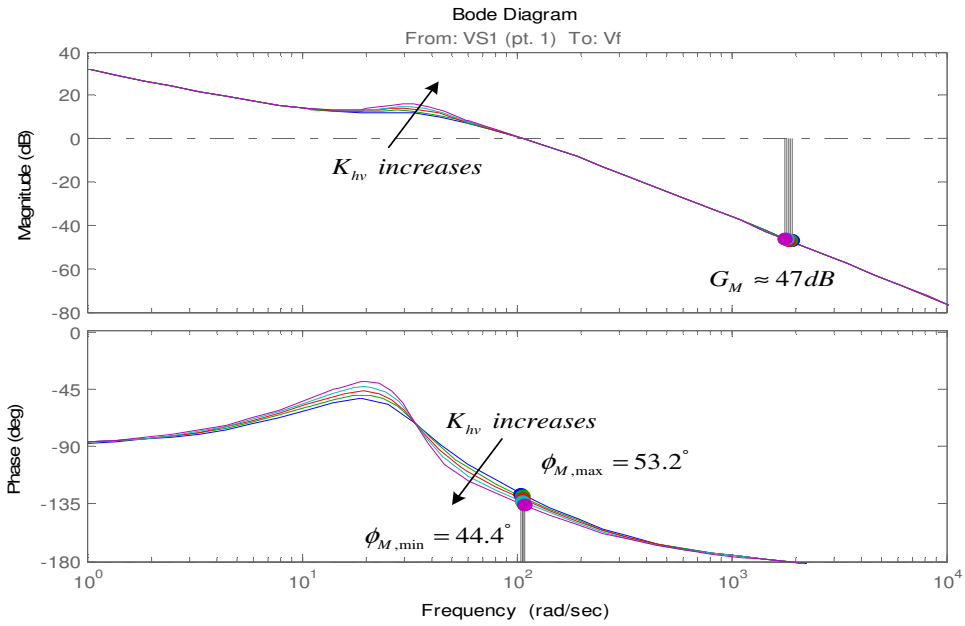



Figure 3.14 The open-loop Bode diagrams of $V_f/V_{S1}(s)$ as $K_{hv}$ changes (SPSAF-CM).

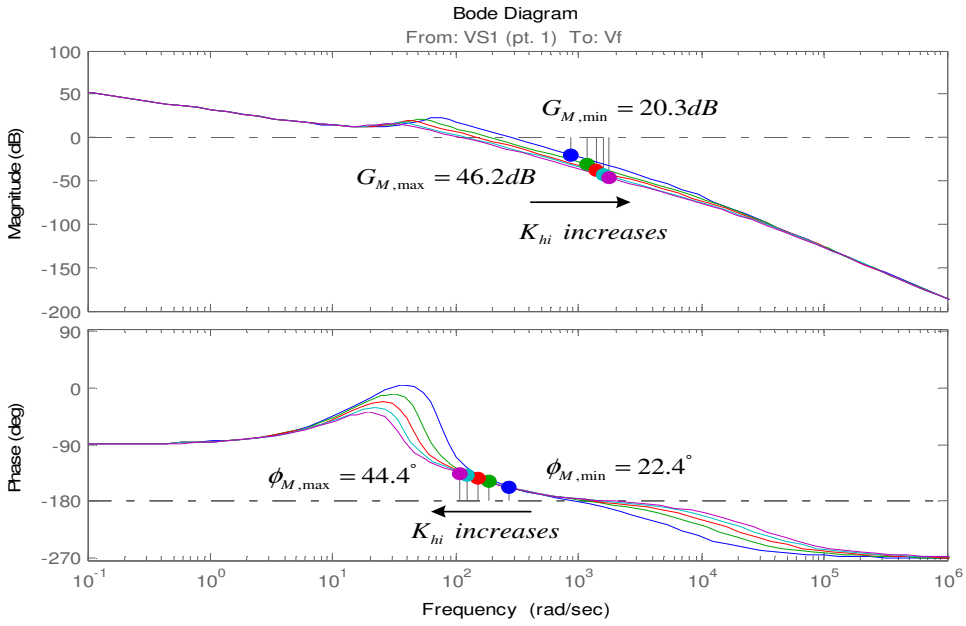
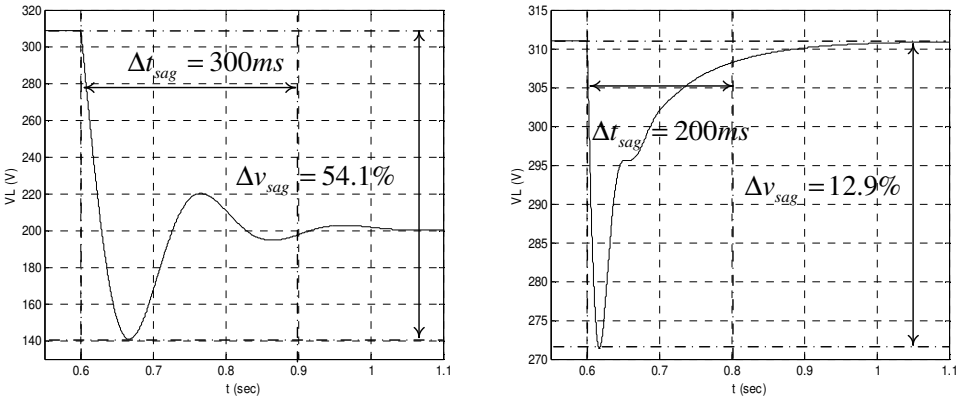



Figure 3.15 The open-loop Bode diagrams of $V_f/V_{S1}(s)$ as $K_{hi}$ changes (SPSAF-CM).

By means of the low frequency closed-loop model, the simulations of SPSAF under the circumstances of the voltage sag by 35% and the load increase by 20% can be conducted for the SPSAF system with and without the feedback controller (the PI controller and the compensator) via MATLAB-Simulink. The load voltage response of the SPSAF system to the voltage sag is shown in Figure 3.16. In the figure, while the feedback regulates the load voltage, the system without feedback cannot perform this job. The comparisons of the maximum voltage drop and the settling time due to the voltage sag ($\Delta v_{sag}$ and $\Delta t_{sag}$) for the controlled and the uncontrolled cases show the effectiveness of the controller. The disturbance rejection against the load power increase is shown in Figure 3.17. The feedback enhances the performance of the system against the load dynamics regarding the maximum voltage drop ($\Delta v_{dyn}$) and the time elapsed for steady-state condition ($\Delta t_{dyn}$).




(*a*) (*b*)

Figure 3.16 The load voltage responses to the voltage sag by 35% (a) without feedback control and (b) with feedback control (SPSAF-CM).

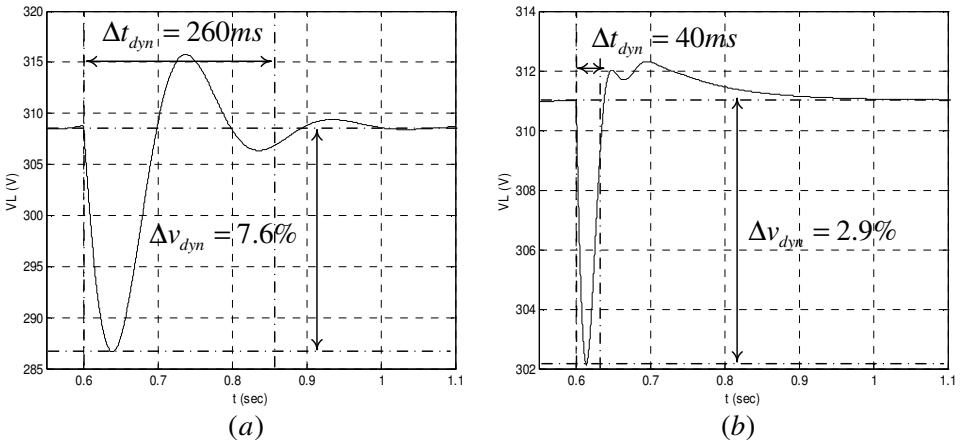



Figure 3.17 The load voltage responses to the load power increase by 20% (a) without feedback and (b) with feedback (SPSAF-CM).

### 3.3.2.2 AVM

The low frequency linear model of the SPSAF system using AVM is shown in Figure 3.18. By means of Bode diagrams of the open-loop transfer function of $V_f/V_{S1}(s)$, $K_{Pv}$ and $K_{Iv}$ are chosen as 8 and 250, respectively. As shown in Figure 3.19, $G_M$ = 39.2 dB and $\varphi_M = 64.1^\circ$, which are appropriate margins; therefore, there is no need for a phase-lead compensator. The unit step-response of $V_f/V_{S1}(s)$ shows both good transient and steady-state performances in Figure 3.20. The bandwidth of $V_f/V_{S1}(s)$ in the closed-loop system is 420 rad/s (67 Hz) as shown in Figure 3.21.

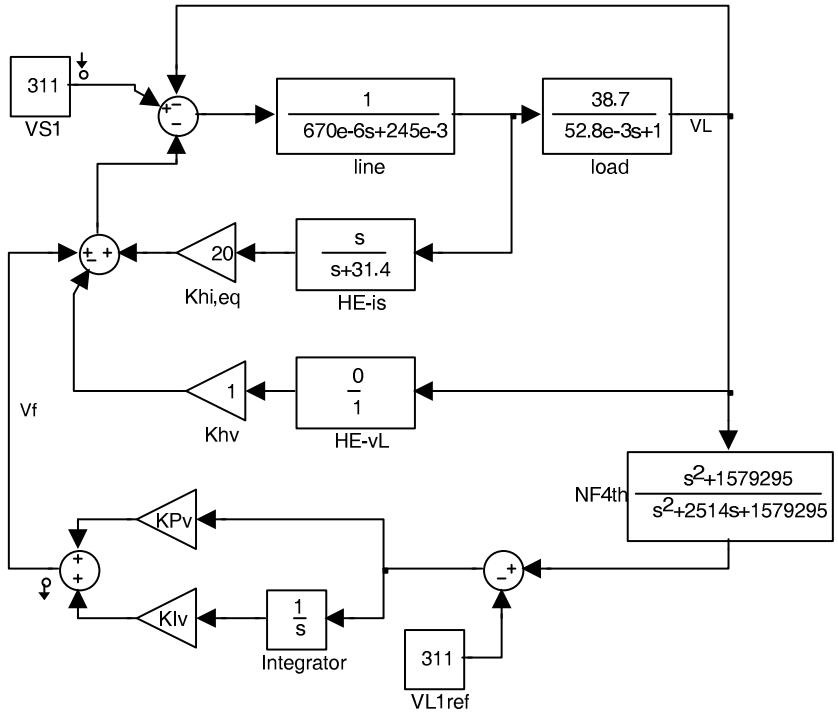



Figure 3.18 The control block diagram of the low frequency linear model in MATLAB-Simulink (SPSAF-AVM).

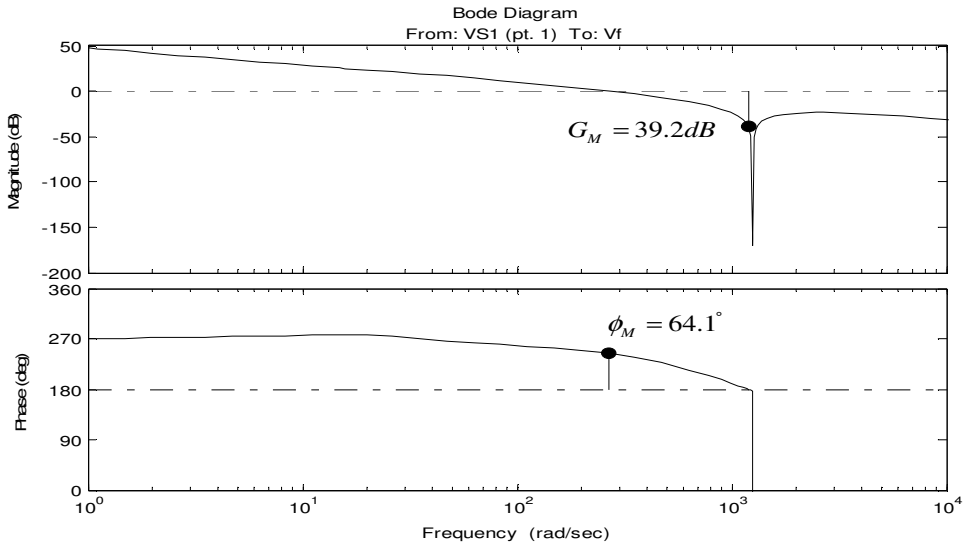



Figure 3.19 The open-loop Bode diagram of $V_f/V_{S1}(s)$ (SPSAF-AVM).

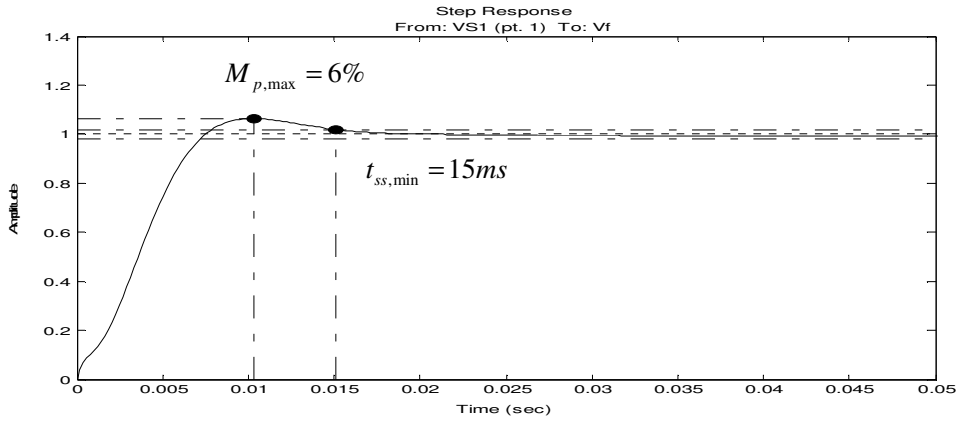



Figure 3.20 The closed-loop unit step-response of $V_f/V_{S1}(s)$ (SPSAF-AVM).

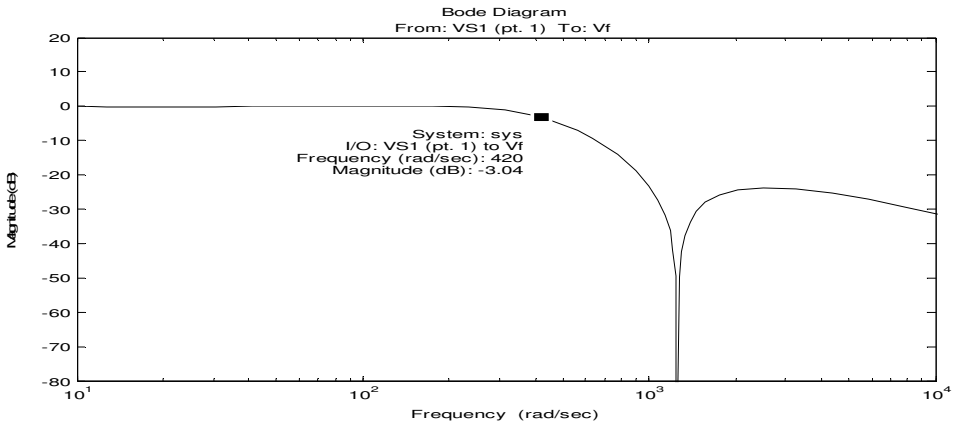



Figure 3.21 The closed-loop Bode diagram of $V_f/V_{S1}(s)$ (SPSAF-AVM).

As its is done for CM, by means of the low frequency closed-loop model, the responses of SPSAF with AVM under the circumstances of the sag by 35% and the load increase by 20% are reported conducting the simulations in MATLAB-Simulink. The load voltage responses of the system to the sag and the load increase, which are shown in Figure 3.22 and Figure 3.23, are better than the responses with CM such that the maximum voltage drops and the settling times are improved. The comparison between the SPSAF using CM and AVM is given in Table 3.4.

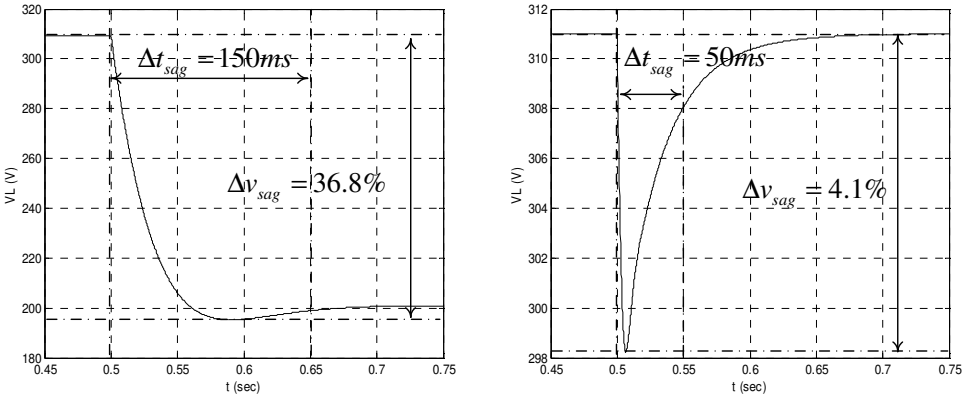



Figure 3.22 The load voltage responses to the voltage sag by 35% (a) without feedback and (b) with feedback (SPSAF-AVM).

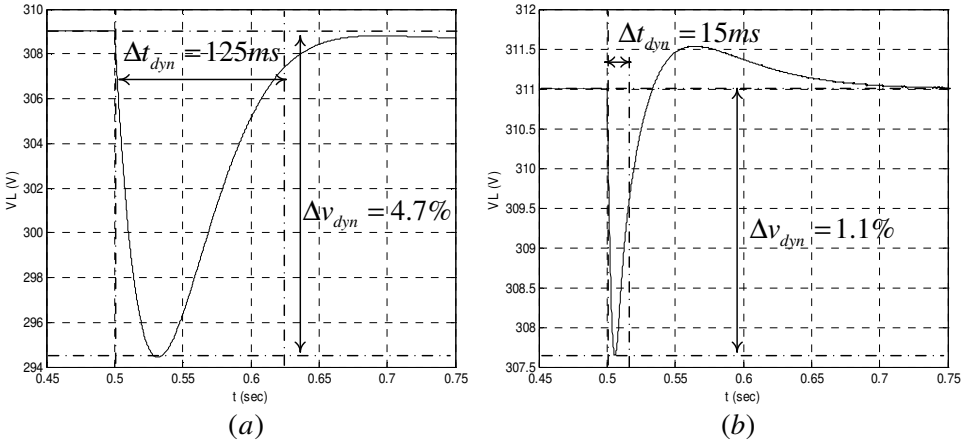



Figure 3.23 The load voltage responses to the load power increase by 20% (a) without feedback and (b) with feedback (SPSAF-AVM).

Table 3.4 The comparison of the load voltage regulation performances using CM and AVM (SPSAF)

| | CM | | AVM | |
|---|---|---|---|---|
| | No feedback | With feedback | No feedback | With feedback |
| $\Delta v_{sag}$ (%) | 54.1 | 12.9 | 36.8 | 4.1 |
| $\Delta t_{sag}$ (ms) | 300 | 200 | 150 | 50 |
| $\Delta v_{dyn}$ (%) | 7.6 | 2.9 | 4.7 | 1.1 |
| $\Delta t_{dyn}$ (ms) | 260 | 40 | 125 | 15 |

## 3.4 TPSAF

TPSAF parameters, which are used in the simulations and the experiments, are listed in Table 3.5. The same approach for SPSAF is pursued to determine the gains of HCI, RDC, and FCC.

### 3.4.1 High Frequency Model

The parameters derived from the Table 3.5 using the equations given for the high frequency model are listed in Table 3.6. With these derived parameters, the linear model at high frequency is built up in MATLAB-Simulink, as shown in Figure 3.24.

Table 3.5 The linear model parameters (TPSAF)

| | | |
|---|---|---|
| $V_S$ | Rated line-to-line utility voltage | 380 $V_{rms}$ |
| $L_S$ | Utility inductance | 200 μH |
| $R_S$ | Utility resistance | 100 mΩ |
| $C_L$ | Load capacitance | 2.2 mF |
| $R_L$ | Load resistance | 24 Ω |
| $L_f$ | SRF inductance | 2.2 mH |
| $C_f$ | SRF capacitance | 2.0 μF |
| $R_f$ | Resistance of the SRF inductance | 450 mΩ |
| $R_d$ | SRF damping resistance | 5.6 Ω |
| $L_1$ | Primary side leakage inductance of SIT | 250 μH |
| $L_2$ | Secondary side leakage inductance of SIT | 40 μH |
| $R_1$ | Primary side copper resistance of SIT | 550 mΩ |
| $R_2$ | Secondary side copper resistance of SIT | 90 mΩ |
| N | Turns-ratio of SIT ($N_1$:$N_2$) | 2.5 |
| $N_V$ | AC/DC transformation ratio ($\sqrt{6}/\pi$) | 0.78 |
| $f_{PWM}$ | PWM frequency | 20 kHz |
| $T_S$ | Sampling time (Double update) | 25 μs |

Table 3.6 The high frequency model parameters (TPSAF)

| | | |
|---|---|---|
| $L_{Seqf}$ | Equivalent line inductance | 280 μH |
| $R_{Seqf}$ | Equivalent line resistance | 278 mΩ |
| $L'_f$ | The referred SRF inductance | 352 μH |
| $C'_f$ | The referred SRF capacitance | 12.5 μF |
| $R'_f$ | The referred resistance of the SRF inductance | 72 mΩ |
| $R'_d$ | SIT damping resistance | 0.9 Ω |
| $T_d$ | Total delay time of inverter | 30 μs |

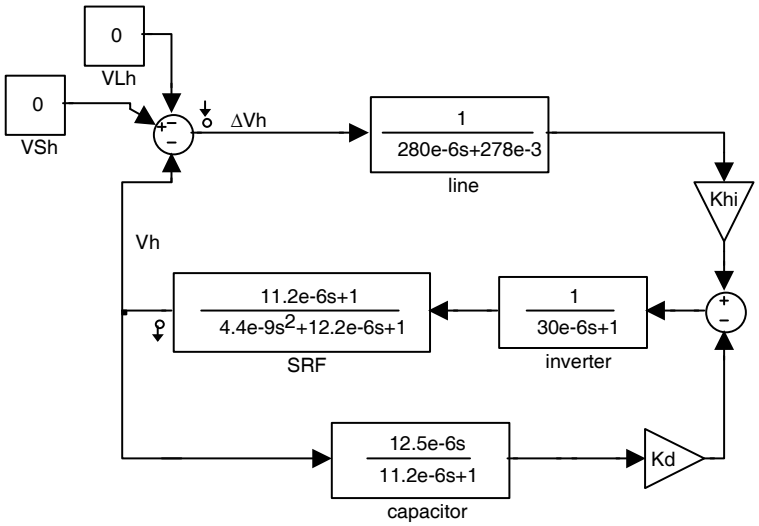



Figure 3.24 The control block diagram of the high frequency linear model in MATLAB-Simulink (TPSAF).

The same procedure for the determination of $K_{hi}$ and $K_d$ as the one for SPSAF is practiced such that the open-loop Bode diagram of $\Delta V_h/V_h(s)$ are analyzed in the frequency-domain. In order to optimize the stability margin and the good harmonic isolation performance (high $K_{hi}$), two cases are considered. The first case is for $K_d$ = 20 and $K_{hi}$ = 4, 6, 8, 10, and 12 and the second case is for $K_{hi}$ = 8 and $K_d$ = 10, 15, 20, 25, and 30 as given in Figure 3.25 and Figure 3.26, respectively. To avoid repetition of the single-phase case, the details of the figures are not discussed. With the given specifications of the minimum phase margin ($\varphi_M$) of 20˚ and the gain margin ($G_M$) larger than 6 dB, $K_{hi}$ and $K_d$ can be chosen as 10 and 20, respectively. In this condition, $G_M$ = 16 dB and $\varphi_M$ = 23˚.

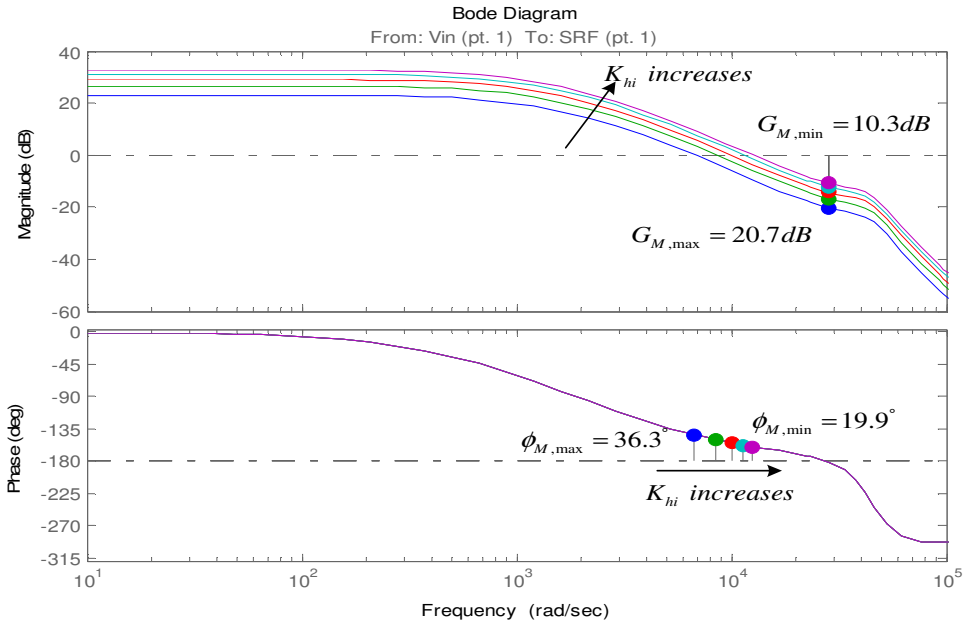



Figure 3.25 The open-loop Bode diagrams of $\Delta V_h/V_h(s)$ for $K_d = 20$ (TPSAF).

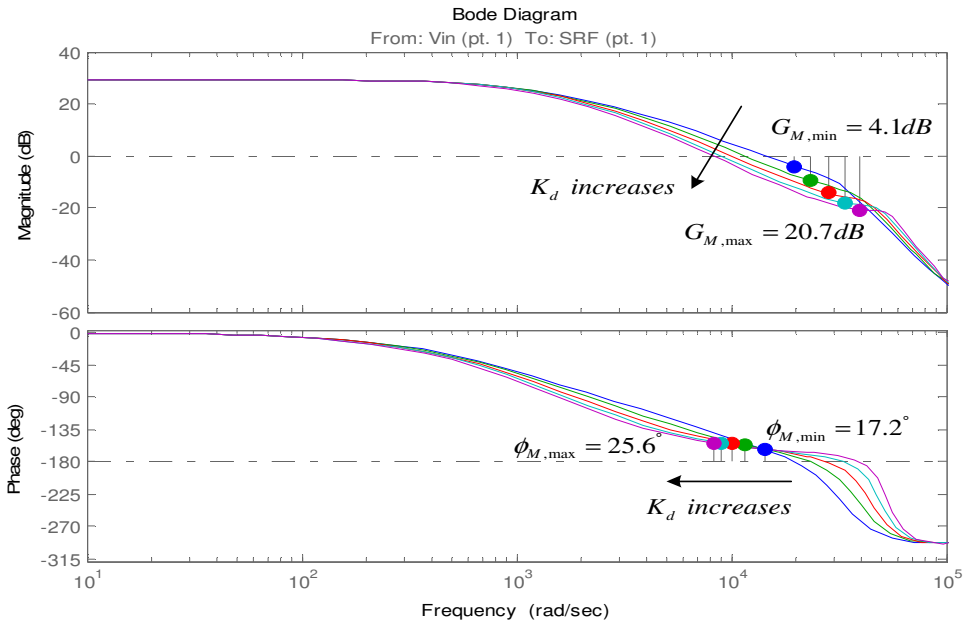



Figure 3.26 The open-loop Bode diagrams of $\Delta V_h/V_h(s)$ for $K_{hi} = 8$ (TPSAF).

In the closed loop system, $I_{Sh}/V_{Lh}(s)$ represents the admittance of the system. As shown in Figure 3.27, the Bode diagram of $I_{Sh}/V_{Lh}(s)$ shows low admittance for lower harmonic frequencies such that $I_{Sh}/V_{Lh} < 0.2$ for $f < 800$ Hz considering $K_{hi} = 10$ and the admittance of this value is 0.1 ideally. However, the admittance increase to 0.8 as f goes to the resonant frequency of the switching ripple filter ($f_o \approx 2.0$ kHz). Thus, the feedback controller of HIC is more effective at lower harmonic frequencies.

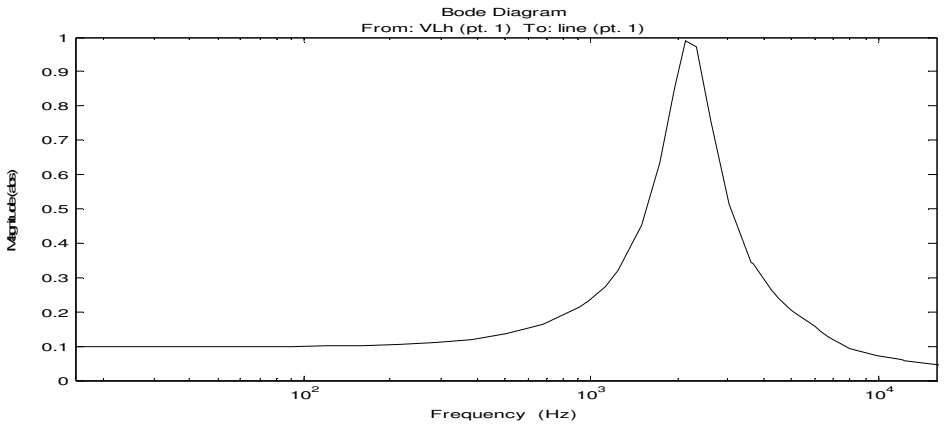



Figure 3.27 The closed -loop Bode diagram of $I_{Sh}/V_{Lh}(s)$ (TPSAF).

### 3.4.2 Low Frequency Model

The parameters used in the low frequency linear model are derived from the Table 3.5 and listed in Table 3.7. FCC is designed in the same manner given for SPSAF.

Table 3.7 The low frequency linear model parameters (TPSAF)

| | | |
|---|---|---|
| $V_{S1}$ | Rated equivalent fundamental utility voltage | 220√3 V |
| $L_{Seq1}$ | Equivalent line inductance | 632 μH |
| $R_{Seq1}$ | Equivalent line resistance | 350 mΩ |
| $C_{Leq}$ | Equivalent load capacitance | 3.62 mF |
| $R_{Leq}$ | Equivalent load resistance | 14.6 Ω |
| $N_V$ | AC/DC transformation ratio | 0.78 |
| $K_{hi,eq}$ | HIC gain for line current | 10 |
| $K_{hv}$ | HIC gain for load voltage (CM) | 0.9 |
| $K_{hv}$ | HIC gain for load voltage (AVM) | 1 |
| $f_{chi}$ | HIC HPF cutoff frequency for line current | 7.5 Hz |
| $f_{chv}$ | HIC HPF cutoff frequency for load voltage (CM) | 7.5 Hz |
| $f_{c1v}$ | FCC LPF cutoff frequency (CM) | 15 Hz |
| $f_{2nd}$ | AVM resonant filter frequency ($2^{nd}$) | 100 Hz |
| $f_{6th}$ | AVM resonant filter frequency ($6^{th}$) | 300 Hz |

### 3.4.2.1 CM

The low frequency linear model for CM is built up in MATLAB-Simulink, as shown in Figure 3.28. The feedback controller of TPSAF is designed using the same method utilized in SPSAF-CM. For $K_{Iv} = 0$ and $T_v = 0$, $K_{Pv}$ is chosen in order that $\varphi_M$ of the open-loop transfer function of $V_f/V_{S1}(s)$ is around 50˚ and $G_M$ is larger than 6 dB as a rule of thumb. For $K_{Pv} = 1.5$, $G_M = 49.7$ dB and $\varphi_M = 51.2$˚. With the usage of $K_{Iv}$ in order to eliminate the steady-state error of the system, $\varphi_M$ decreases such that $G_M = 45.6$ dB and $\varphi_M = 25.6$˚ for $K_{Pv} = 1.5$ and $K_{Iv} = 40$. In order to increase $\varphi_M$, the phase-lead compensator with $a_v = 4.6$ and $T_v = 10$ ms is suitable such that the stability margins of the compensated system are as follows; $G_M = 41.3$ dB and $\varphi_M =$

47.7˚. The open-loop Bode diagrams of $V_f/V_{S1}(s)$ during the design procedure of the PI controller and the phase-lead compensator are given in Figure 3.29. The step-responses of $V_f/V_{S1}(s)$ with and without the compensator are given in Figure 3.30, which shows that the compensator improves the step response such that it damps oscillations, enhances the settling time ($t_{ss}$ : 0.32 → 0.25 s), alleviates overshoot ($M_p$ : 0.27% → 14%). As seen in Figure 3.31, which is the closed-loop Bode diagram of $V_f/V_{S1}(s)$, the bandwidth of the system is 175 rad/s (28 Hz).

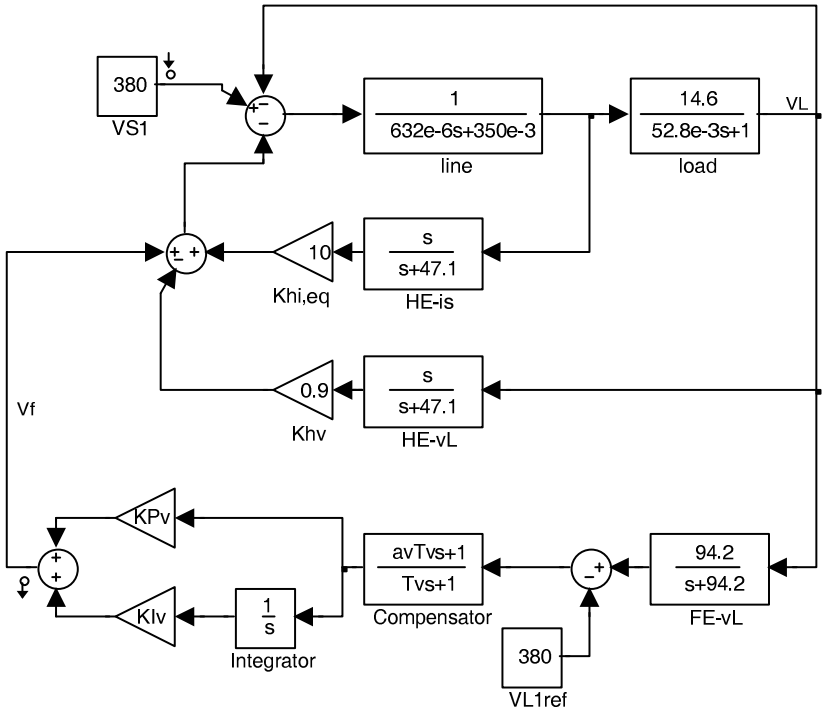



Figure 3.28 The control block diagram of the low frequency linear model in MATLAB-Simulink (TPSAF-CM).

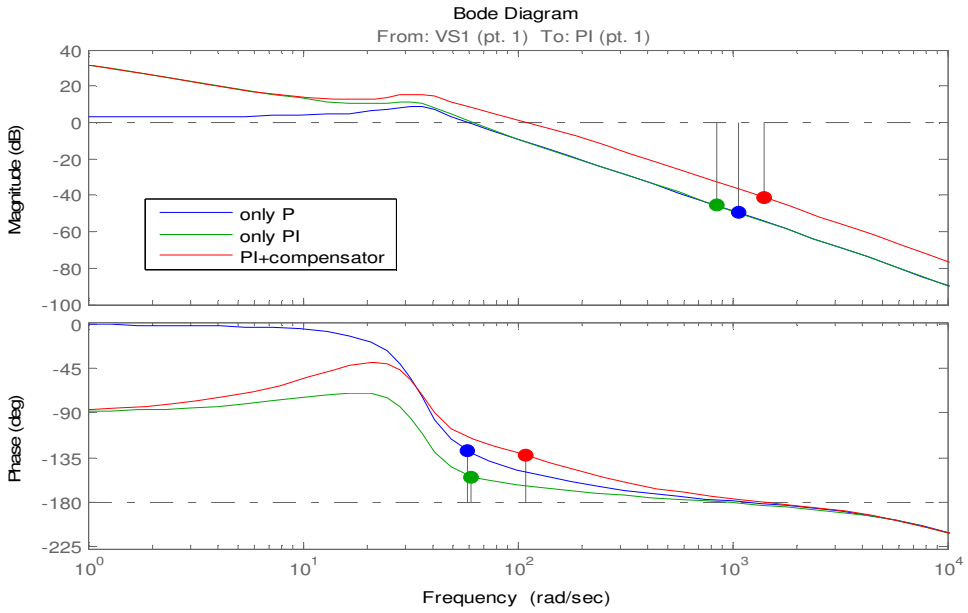



Figure 3.29 The open-loop Bode diagrams of $V_f/V_{S1}(s)$ during the controller design procedure (TPSAF-CM).

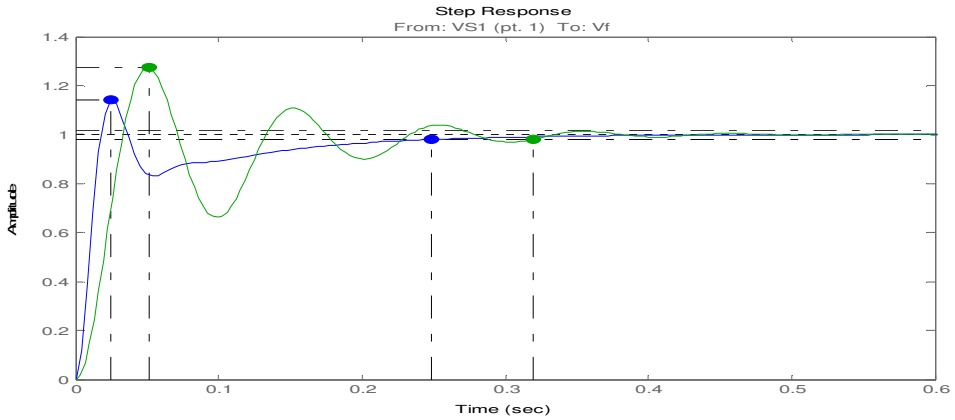



Figure 3.30 The step-response of $V_f/V_{S1}$ (s) for the uncompensated (green) and the compensated (blue) closed-loop systems (TPSAF-CM).

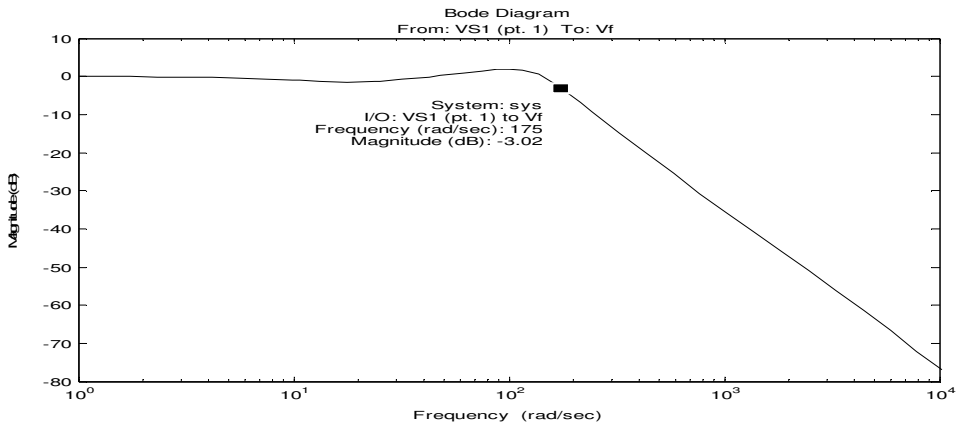



Figure 3.31 The closed-loop Bode diagram of $V_f/V_{S1}$ (s) of the compensated system (TPSAF-CM).

Using the low frequency closed-loop model, the simulations of the TPSAF system under the circumstances of the three-phase sag by 35% and the load increase by 20% can be conducted for the system with and without the feedback (the PI controller and the compensator) via MATLAB-Simulink. The load voltage response of the system to the sag is shown in Figure 3.32. In the figure, while the feedback regulates the load fundamental frequency voltage, the system without feedback cannot perform this job. The comparisons of the maximum voltage drop and the settling time due to the voltage sag ($\Delta v_{sag}$ and $\Delta t_{sag}$) for the controlled and the uncontrolled cases show the effectiveness of the controller. The feedback enhances the performance of the system against the load dynamics regarding the maximum voltage drop ($\Delta v_{dyn}$) and the time elapsed for steady-state condition ($\Delta t_{dyn}$) as shown in Figure 3.33.

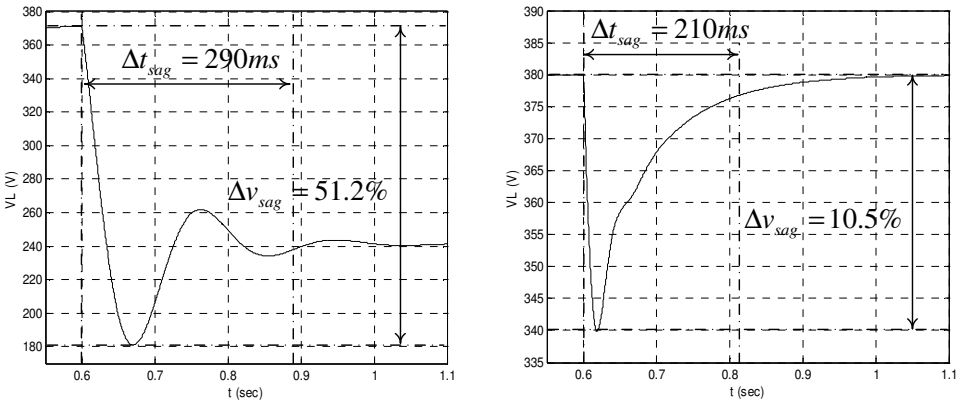



Figure 3.32 The load voltage responses to the voltage sag by 35% (a) without feedback and (b) with feedback (TPSAF-CM).

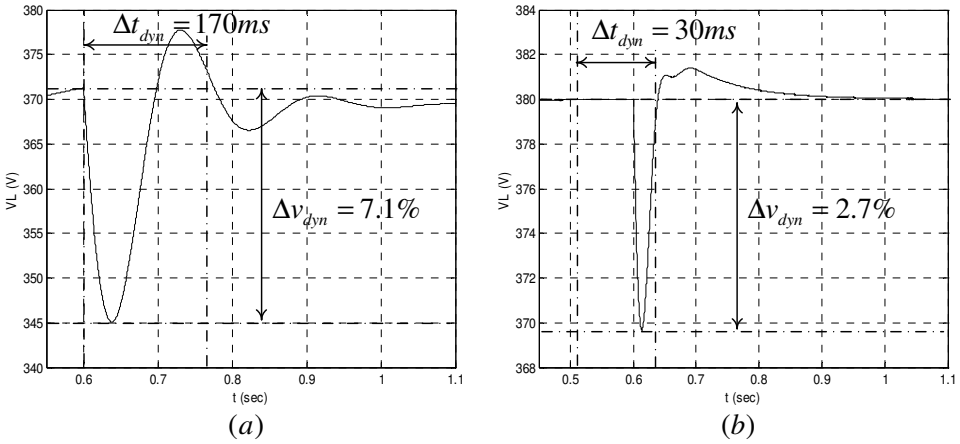



Figure 3.33 The load voltage responses to the load power increase by 20% (a) without feedback and (b) with feedback (TPSAF-CM).

For TPSAF, there are unbalanced sag disturbances unlike SPSAF. In this study, the single-phase sag by 35% of rated line voltage is used to analyze the response of TPSAF to the unbalanced sags. In the linear model on 'de' frame, the negative sequence component of the single phase sag of 35% is represented as a sine wave

with the peak magnitude of 11.7% (35%/3) at the frequency of $2f_e$ (100 Hz) and the voltage drop of 11.7% of the line voltage ($V_{S1}$) considering the symmetrical component transformation [34]. Via the simulations in Simulink, the responses of TPSAF to the single phase sag for no feedback and with feedback cases are shown in Figure 3.34. For the two cases, the voltage fluctuation percentages ($\Delta v_{neg}$) associated with the negative sequence component of the single-phase voltage sag are close to each other and low (1.0%) since the attenuation at 100 Hz is around 27 dB for each case, which shows that the feedback does not enhance the bandwidth of the system towards to 100 Hz. Nevertheless, the voltage drop ($\Delta v_{sag}$) associated with the positive sequence of the single-phase sag cannot be regulated for no feedback case unlike the case with feedback.

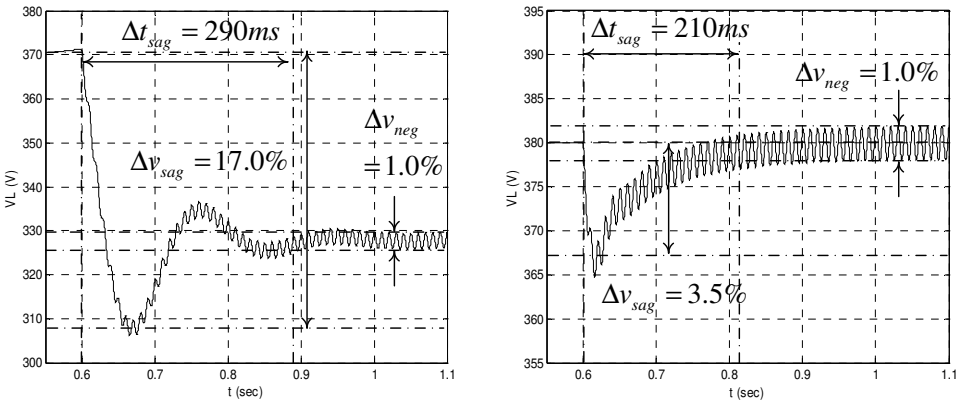



Figure 3.34 The load voltage responses to the single-phase voltage sag by 35% (a) without feedback and (b) with feedback (TPSAF-CM).

### 3.4.2.2 AVM

The low frequency linear model of TPSAF with AVM is shown in Figure 3.35. By means of the Bode diagrams of the open-loop transfer function of $V_f/V_{S1}(s)$, $K_{Pv}$ and $K_{Iv}$ are chosen as 5 and 175, respectively. As shown in Figure 3.36, $G_M$ = 14.9 dB

and $\varphi_M$ = 57.1˚, which are appropriate margins; therefore, there is no need for a phase-lead compensator as in the SPSAF-AVM. The unit step-response of $V_f/V_{S1}(s)$ shows both good transient and steady-state performances in Figure 3.37. The bandwidth of $V_f/V_{S1}(s)$ in the closed-loop system is 246 rad/s (39 Hz) as shown in Figure 3.38.

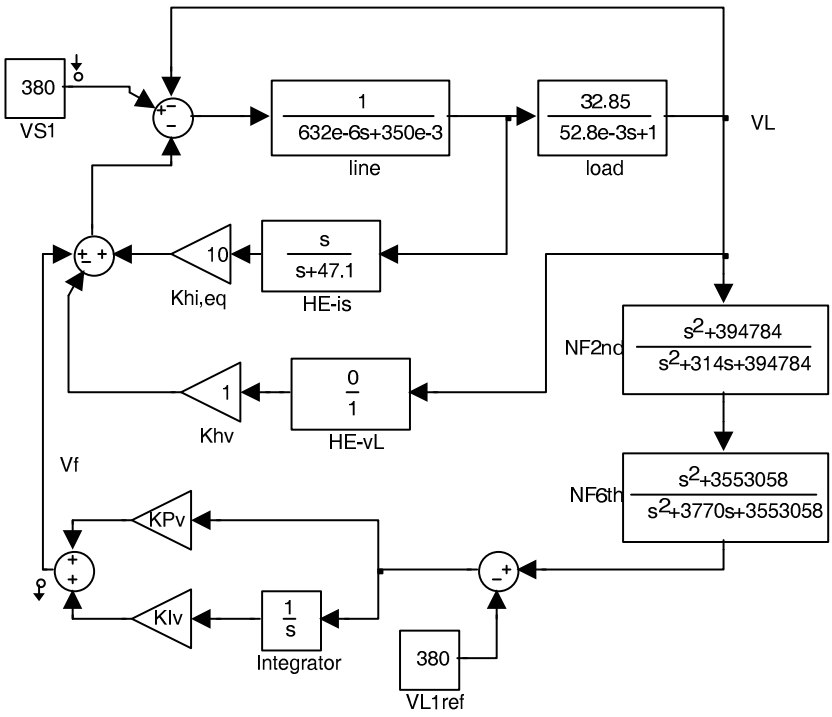



Figure 3.35 The control block diagram of the low frequency linear model system in MATLAB-Simulink (TPSAF-AVM).

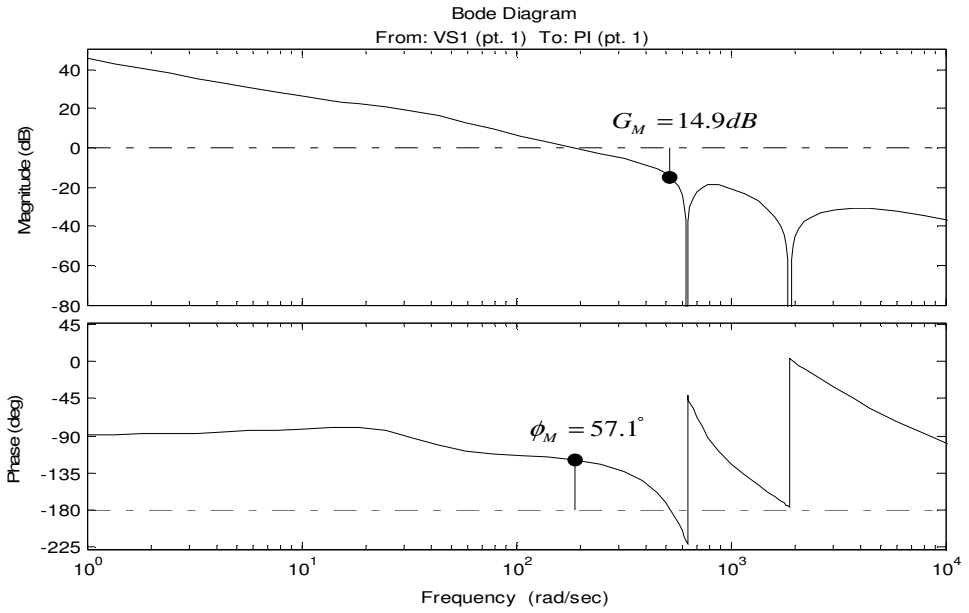



Figure 3.36 The open-loop Bode diagram of $V_f/V_{S1}(s)$ (TPSAF-AVM).

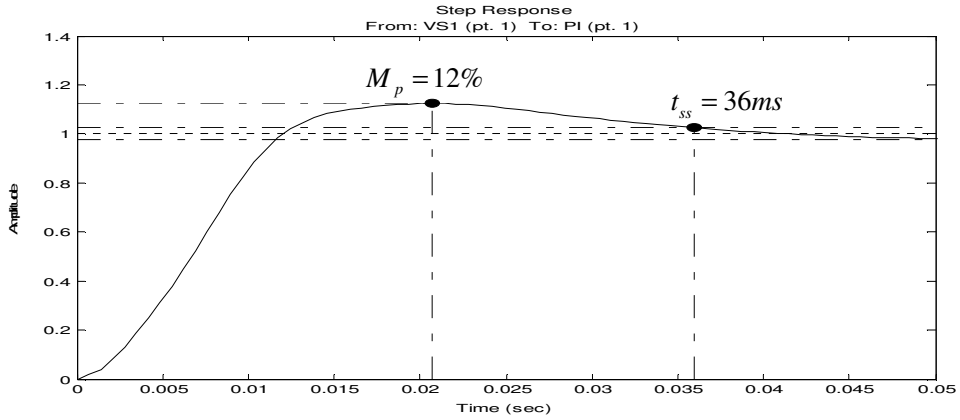



Figure 3.37 The closed-loop unit step-response of $V_f/V_{S1}(s)$ (TPSAF-AVM).

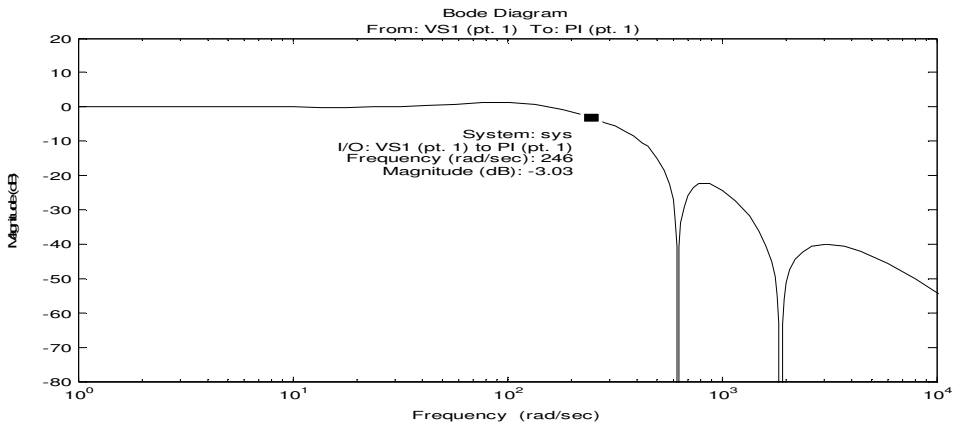
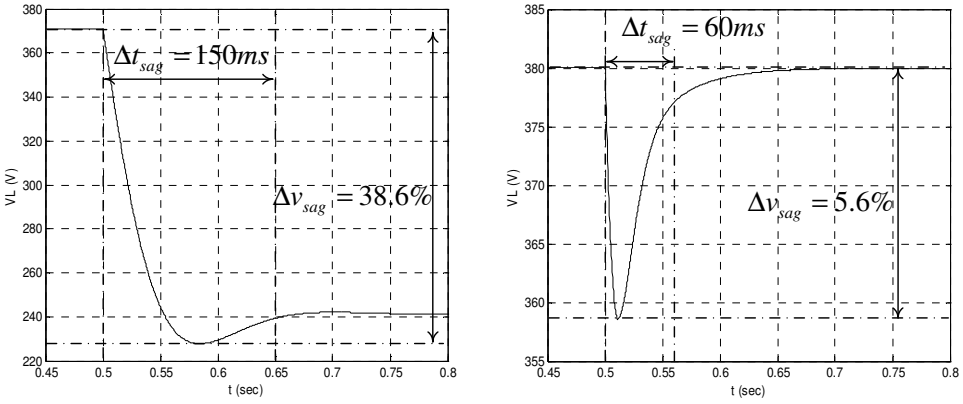



Figure 3.38 The closed-loop Bode diagram of $V_f/V_{S1}(s)$ (TPSAF-AVM).

Via the simulations, the responses of TPSAF to the three-phase sag by 35% and the load increase by 20% are conducted for the system with and without the feedback controller via MATLAB-Simulink. The load voltage responses of the system to the three-phase sag and the load power increase for no feedback and with feedback cases are shown in Figure 3.39 and Figure 3.40, respectively. These responses are better than those obtained using CM as shown in the comparison of the simulation results of the TPSAF systems using CM and AVM with respect to the voltage drops and the settling times in Table 3.8.




(*a*) (*b*)

Figure 3.39 The load voltage responses to the voltage sag by 35% (a) without feedback and (b) with feedback (TPSAF-AVM).

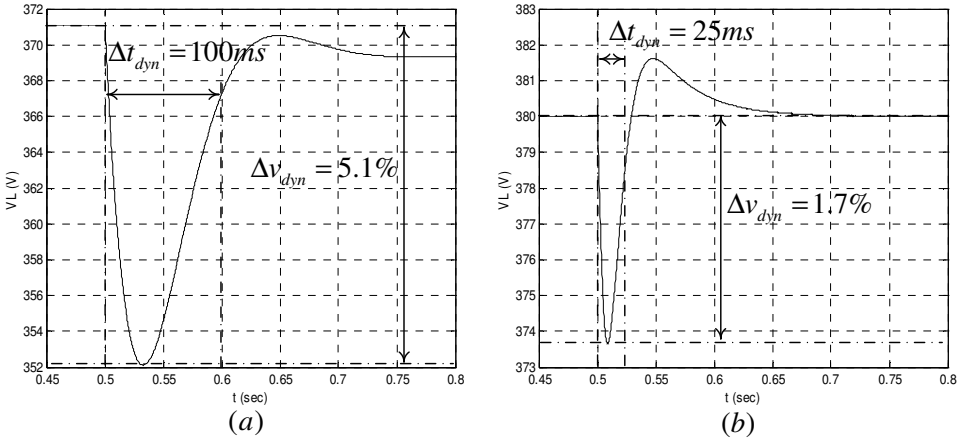



Figure 3.40 The load voltage responses to the load power increase by 20% (a) without feedback and (b) with feedback (TPSAF-AVM).

Table 3.8 The comparison of fundamental voltage regulation performances using CM and AVM (TPSAF)

| | CM | | AVM | |
|---|---|---|---|---|
| | No feedback | With feedback | No feedback | With feedback |
| $\Delta v_{sag}$ (%) | 51.2 | 10.5 | 38.6 | 5.6 |
| $\Delta t_{sag}$ (ms) | 290 | 210 | 150 | 60 |
| $\Delta v_{dyn}$ (%) | 7.1 | 2.7 | 5.1 | 1.7 |
| $\Delta t_{dyn}$ (ms) | 170 | 30 | 100 | 25 |

For the single-phase sag by 35%, the responses of TPSAF with no feedback and with feedback cases are shown in Figure 3.41. For the two cases, the voltage fluctuation percentages ($\Delta v_{neg}$) associated with the negative sequence component of the single-phase voltage sag are the same and low (1.0%) since the notch filter at 100 Hz

provides the attenuation of 27 dB. These results show that the TPSAF systems using CM and AVM have the same steady-state response to negative sequence components.

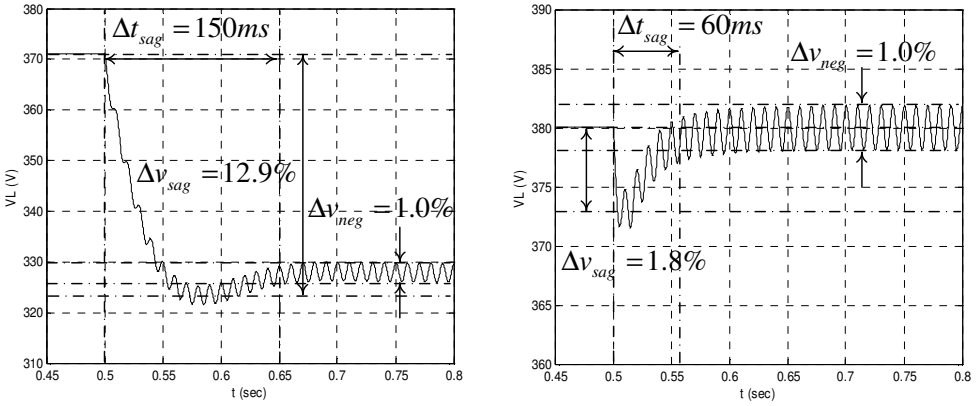



Figure 3.41 The load voltage responses to the single-phase voltage sag by 35% (a) without feedback and (b) with feedback (TPSAF-AVM).

### 3.5 Summary

In this chapter SPSAF and TPSAF compensated systems are modeled as a superposition of the simplified linear models at high frequency and low frequency. In each model, the power and the control units of SAF compensated system effective in the system behavior are taken into account. By analyzing these linear models using open-loop Bode diagrams and step-response tests, feedback controllers are designed. Via the simulations conducted through the low frequency models, the superior performance of the SAF systems using AVM to the performance of the SAF systems using CM are demonstrated in terms of the load voltage regulation under the conditions of balanced/unbalanced voltages sags and load power increase. The next chapter conveys the detailed computer simulations of the considered systems such that the theory and system level simulations are verified.

# CHAPTER 4

# THE PERFORMANCE ANALYSIS OF 2.5 kW SINGLE-PHASE AND 10 kW THREE-PHASE SERIES ACTIVE FILTER COMPENSATED SYSTEMS VIA COMPUTER SIMULATIONS

## 4.1 Introduction

In this chapter, the 2.5 kW single-phase and the 10 kW three-phase Series Active Filter (SPSAF and TPSAF) compensated system performances are analyzed by means of detailed computer simulations. First, the utility, the nonlinear load, the power circuits, and the controllers of the SAF systems are modeled in detail on the computer simulation software Ansoft-Simplorer V7.0 [35]. Next, the simulations are conducted through these system models. The simulation results are reported and the harmonic isolation and the load voltage regulation performances are evaluated. Finally, the performances of SAF with the Conventional Method (CM) and the novel Absolute Value Method (AVM), which are utilized as the harmonic/fundamental frequency component extraction methods for the load voltage, are compared and the latter's superiority is verified via simulations as it is asserted theoretically in Chapter 2 and confirmed by the linear analyses in Chapter 3. In the following, the computer simulation models and results are discussed for SPSAF and TPSAF compensated systems sequentially.

## 4.2 SPSAF

### 4.2.1 Simulation Model of The 2.5 kW SPSAF Compensated System

The SPSAF compensated system diagram used in the simulations is illustrated in Figure 4.1. As shown in the figure, the utility is modeled as an ideal voltage source with an equivalent inductance and an equivalent resistance. The load is a single-phase diode rectifier with a parallel RC load, i.e., V-type nonlinear load. The SPSAF is represented with a single-phase full-bridge VSI, a switching ripple filter, and a series injection transformer. In the circuit, IGBTs and diodes are modeled as ideal switches with on-state voltage drop. The components used in the SRF are ideal ones without any parasitics. The SIT is modeled using the Jiles-Atherton nonlinear model with respect to the design and the test data of the manufactured SIT (to be detailed in the next chapter) [36]. At the DC bus of the VSI, a three-phase diode bridge rectifier stands as an auxiliary DC power supply. Additionally, a thyristor by-pass circuit is placed across the output terminals of the SIT. The parameters used in the model of SPSAF are tabulated in Table 4.1. The controllers are also modeled in detail emulating a digital signal processor performing discrete time control.

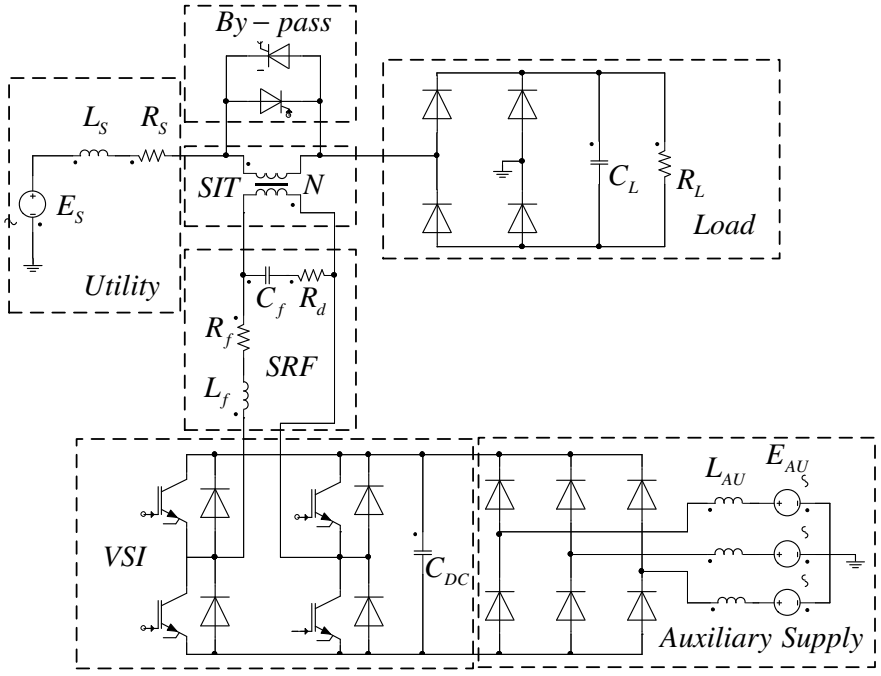



Figure 4.1 The simulation model of the SPSAF compensated system in Simplorer.

Table 4.1 The simulation model parameters (SPSAF)

| | | |
|---|---|---|
| $E_S$ | Utility voltage | 220 $V_{rms}$ (50 Hz) |
| $L_S$ | Utility inductance | 200 µH |
| $R_S$ | Utility resistance | 100 mΩ |
| $V_{L,DC}$ | Rated DC bus voltage of the compensated load | 245 V |
| $C_L$ | Load capacitance | 2.2 mF |
| $R_L$ | Load resistance | 24 Ω (2.5 kW) |
| $L_f$ | SRF inductance | 1.8 mH |
| $C_f$ | SRF capacitance | 2.35 µF |
| $R_f$ | Resistance of the SRF inductance | 300 mΩ |
| $R_d$ | SRF damping resistance | 5.6 Ω |
| $V_{DC}$ | Rated DC bus voltage of VSI | 520 V |
| $C_{DC}$ | DC bus capacitance of VSI | 2.2 mF |
| $E_{AU}$ | Supply voltage of auxiliary rectifier | 380 $V_{rms}$ (50 Hz) |
| $L_{AU}$ | Line inductance of auxiliary rectifier | 1.43 mH |
| $L_1$ | Primary side leakage inductance of SIT | 40 µH |
| $L_2$ | Secondary side leakage inductance of SIT | 10 µH |
| $R_1$ | Primary side copper resistance of SIT | 140 mΩ |
| $R_2$ | Secondary side copper resistance of SIT | 35 mΩ |
| N | Turns-ratio of SIT ($N_1$:$N_2$) | 2 |
| $f_{PWM}$ | PWM frequency | 20 kHz |
| $T_S$ | Sampling time (Double update) | 25 µs |

### 4.2.2 Simulation of The SPSAF Compensated System Using CM

With CM for the load voltage signal decomposition, simulation results are reported with respect to harmonic isolation and load voltage regulation. In investigating the SAF performance for the load voltage regulation, two types of disturbance are considered, which are voltage sag by 35% of rated utility voltage and an instantaneous load power increase by 20% of the rated power as used in Chapter 3.

The controller parameters used in the simulations for CM are given in the Table 4.2. The parameters of harmonic isolation controller (HIC), resonance damping controller (RDC), and fundamental component controller (FCC) are the same as found and utilized in Chapter 3.

Table 4.2 The controller parameters of the SPSAF using CM

| | | |
|---|---|---|
| $K_{hi}$ | HIC gain for line current | 10 |
| $K_{hv}$ | HIC gain for load voltage | 0.9 |
| $f_{cih}$ | HIC cut-off frequency for line current | 5 Hz |
| $f_{cvh}$ | HIC cut-off frequency for load voltage | 5 Hz |
| $K_d$ | RDC gain | 25 |
| $K_{Pv}$ | FCC proportional gain | 1.5 |
| $K_{Iv}$ | FCC integral gain | 40 |
| $f_{cv1}$ | FCC cut-off frequency for load voltage | 10 Hz |
| $f_{cvff}$ | FCC LPF cut-off frequency for line voltage | 500 Hz |
| $a_v$ | Constant of phase-lead compensator in FCC | 4.6 |
| $T_v$ | Time constant of phase-lead compensator in FCC | 10 ms |

#### 4.2.2.1 Harmonic Isolation

Before assessing the harmonic isolation performance of SPSAF, the harmonic distortion of the uncompensated single-phase V-type nonlinear load is shown by simulations for two modes. The first mode is the by-pass mode when SAF is by-passed using by-pass thyristors. The second mode is when SAF is in series with the utility-load pair but generates zero voltage by means of setting upper switches of VSI and resetting lower switches or vice versa (standby mode) [22]. Line voltage, load voltage, and line current waveforms for the two modes are given in Figure 4.2. In the standby mode, the filter inductance ($L_f$) of SPSAF smoothes the line current to the extent that the total harmonic distortion of the line current ($THD_I$) goes down to

97.01% from 125.91%. The THD of the line voltage ($THD_V$) also gets better with $L_f$ (3.69%→2.42%). Regardless of $L_f$, the harmonic distortion is very large, therefore, the power factor (PF) is very low for the two cases (0.6 and 0.7). Besides, as shown in Figure 4.3, load DC bus voltage ripple ($\Delta v_{dc}$) is very high for both cases (14.8% and 12.8%), which forces the load side to use bigger capacitors and/or bulky AC/DC inductors.

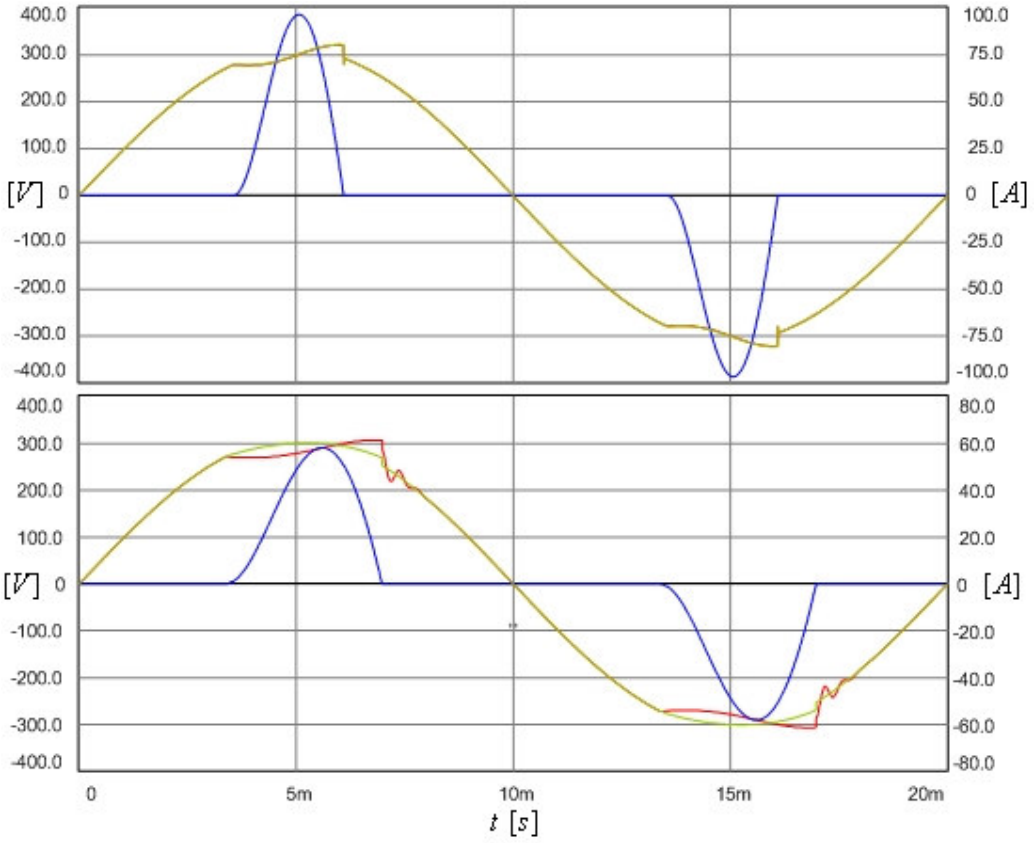



Figure 4.2 Uncompensated single-phase system line voltage (yellow), load voltage (red), and line current (blue) waveforms in by-pass mode (top) and standby mode (bottom).

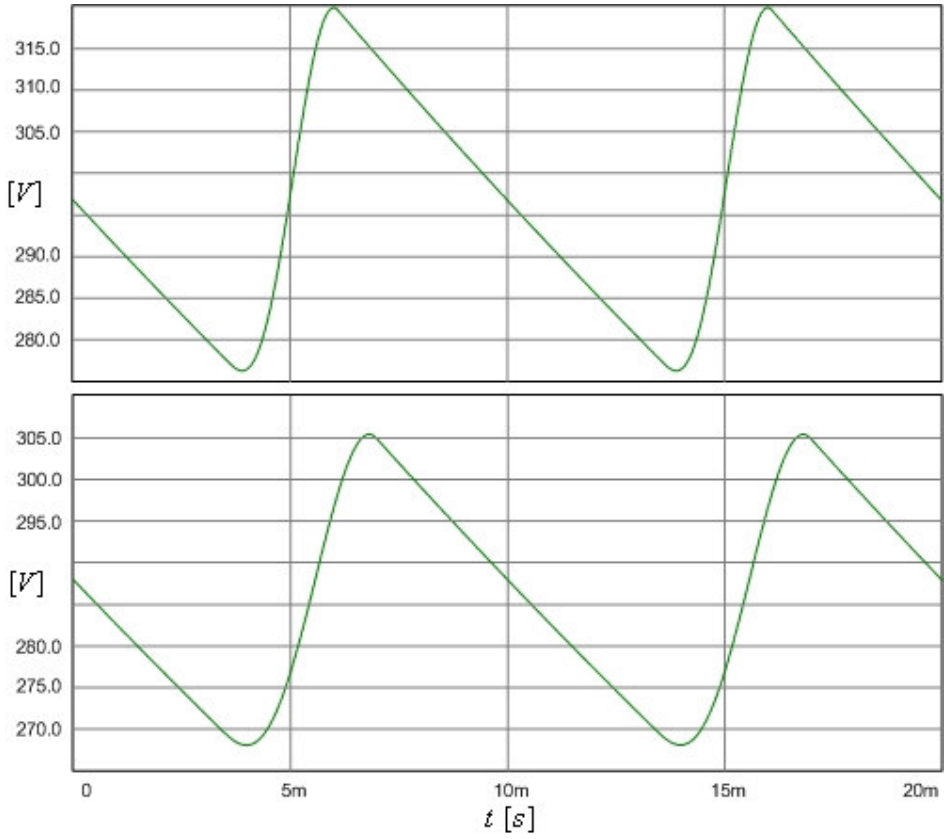



Figure 4.3 Uncompensated single-phase system load DC bus voltage waveforms in by-pass mode (top) and in standby mode (bottom).

With the injection of harmonic isolation voltage by SPSAF, the line current and voltage become less distorted ($THD_I$ = 13.75% and $THD_V$ = 0.86%) and PF improves (0.985) as shown in Figure 4.4. It should be noted that the ripple frequency of the line current waveform is around the resonance frequency of SRF, where the admittance of the system is higher as illustrated in Chapter 3. By means of the harmonic isolation, the load voltage resembles a square wave and $\Delta v_{dc}$ decreases to 5.5% as shown in Figure 4.5.

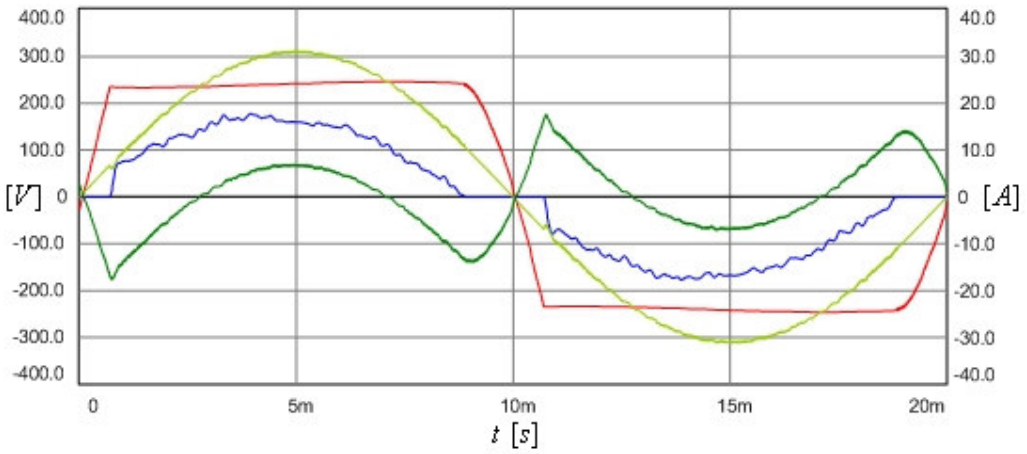



Figure 4.4 Line voltage (yellow), load voltage (red), SAF voltage (green), and line current (blue) waveforms (SPSAF-CM).

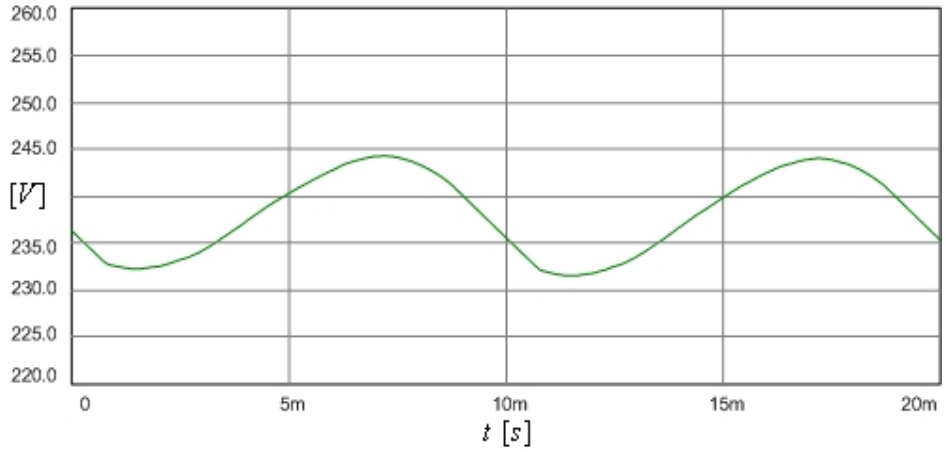



Figure 4.5 Load DC bus voltage waveform (SPSAF-CM).

#### 4.2.2.2 Load Voltage Regulation

The load voltage regulation performance of SPSAF is reported against two disturbance cases, which are utility voltage sag by 35% and load power increase by 20%. The responses of SPSAF to these disturbances are simulated under three conditions. The first condition is when FCC is not active, the second is when only the

feedback part of FCC is active, and the last case is when the feedback and the feedforward parts of FCC are both active.

When SPSAF operates just as a harmonic isolator (No FCC); the load DC bus, load, and line voltages during the voltage sag by 35% are shown in Figure 4.6. In the figure, the maximum voltage drop on the load DC bus voltage ($\Delta v_{sag}$) and the time elapsed for steady-state, i.e., settling time, ($\Delta t_{sag}$) are 53.7% and 300 ms. For the load power increase by 20%, the response of SAF is illustrated by the load DC bus voltage and the line current in Figure 4.7. In the figure, the maximum voltage drop and the settling time are $\Delta v_{dyn}$ = 6.7% and $\Delta t_{dyn}$ = 250 ms.

As shown in Figure 4.8 and Figure 4.9, the SPSAF with the feedback controller of FCC compensates for the line voltage sag and enhances the transient response of the system to the load power increase with respect to the previous case such that $\Delta v_{sag}$ = 12.2%, $\Delta t_{sag}$ = 200 ms, $\Delta v_{dyn}$ = 3.2%, and $\Delta t_{dyn}$ = 40 ms. In Table 4.3, maximum load voltage drops and settling times are listed along with those found for SPSAF without FCC and those found via simplified linear models with CM in Chapter 3. Through the comparison of the results obtained by detailed and simplified models, the simplified linear model is validated.

With the addition of the feedforward controller to the feedback controller, $\Delta v_{sag}$ and $\Delta t_{sag}$ improve to the extent that they can be neglected as shown in Figure 4.10 because the feedforward controller directly generates the compensation voltage for the line voltage sag meanwhile the feedback controller is based on the load voltage error. As expected, $\Delta v_{dyn}$ and $\Delta t_{dyn}$ remain the same as the feedback controller case because the line voltage drop due to the load power increase is negligible (due to voltage drop on the small line inductance) as shown in Figure 4.11.

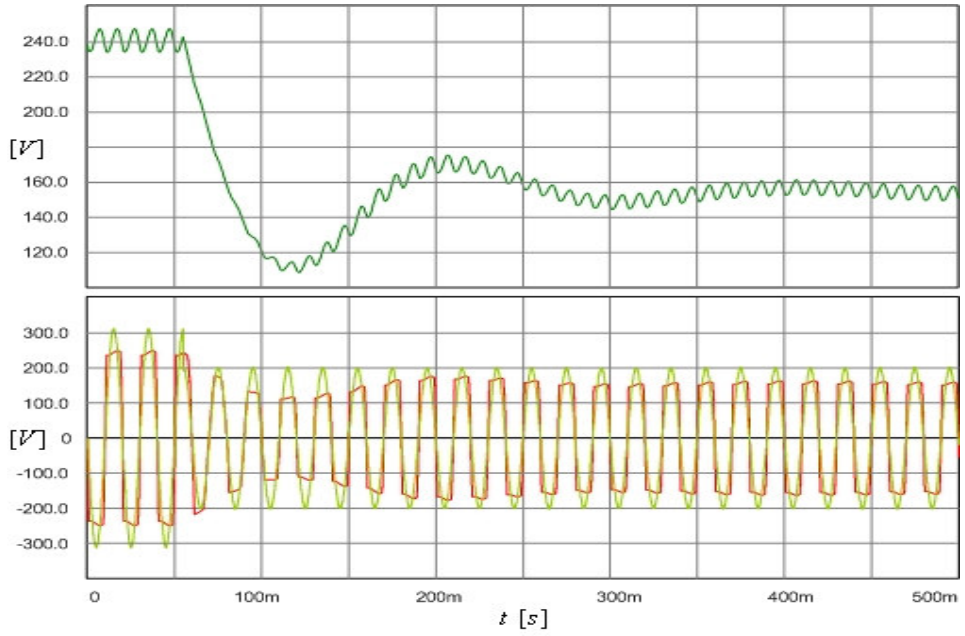



Figure 4.6 Load DC bus voltage (green), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-CM without FCC).

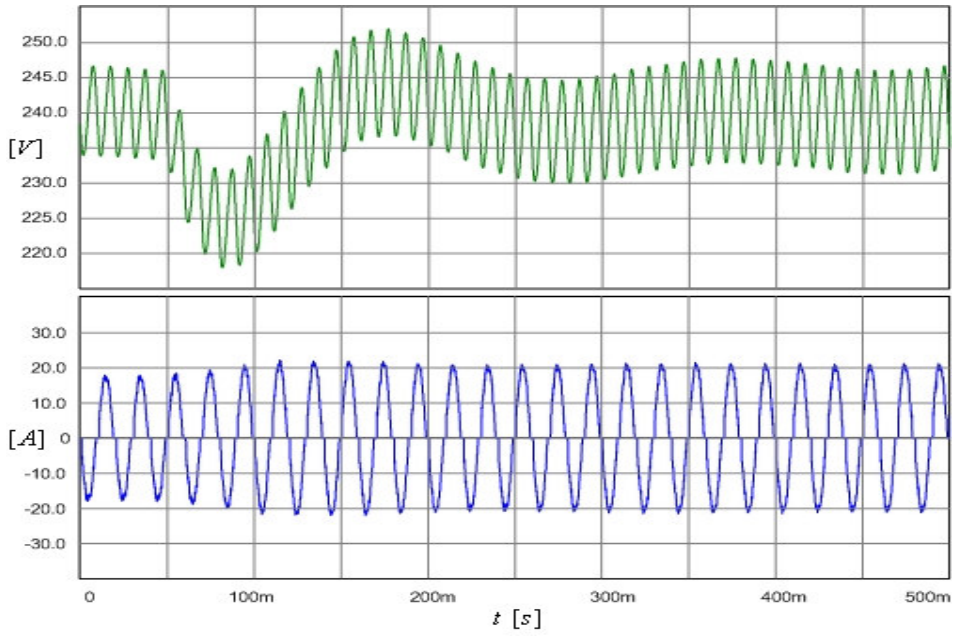



Figure 4.7 Load DC bus voltage (green) and line current (blue) waveforms for 20% load power increase (SPSAF-CM without FCC).

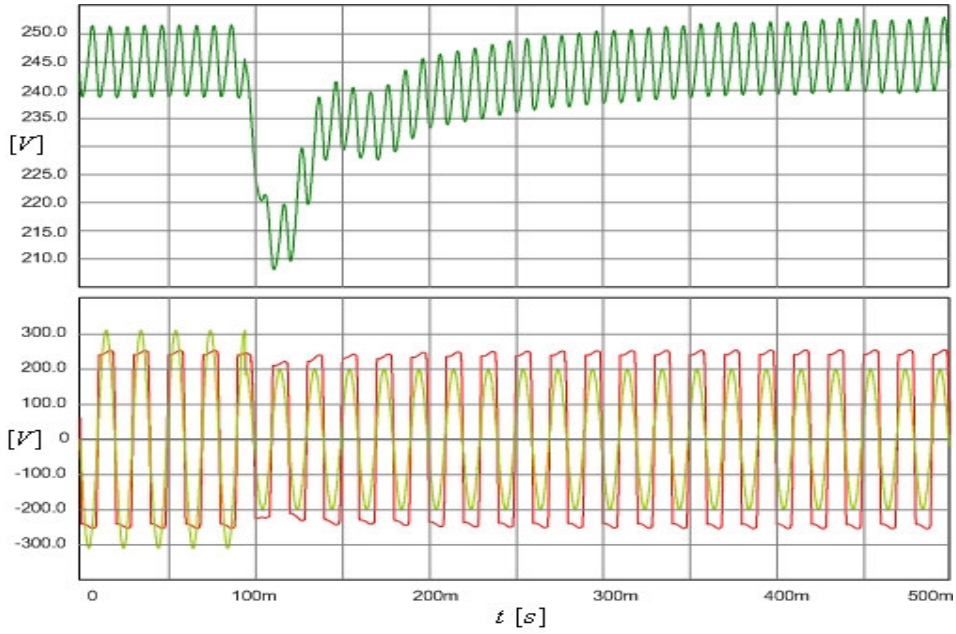



Figure 4.8 Load DC bus voltage (green), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-CM with only feedback).

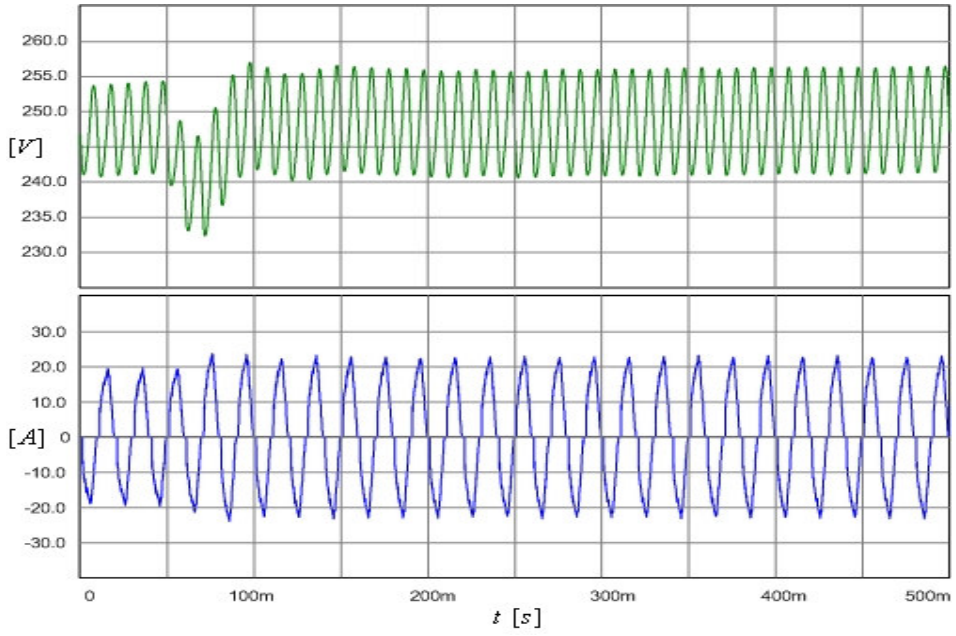



Figure 4.9 Load DC bus voltage (green) and line current (blue) waveforms for 20% load power increase (SPSAF-CM with only feedback).

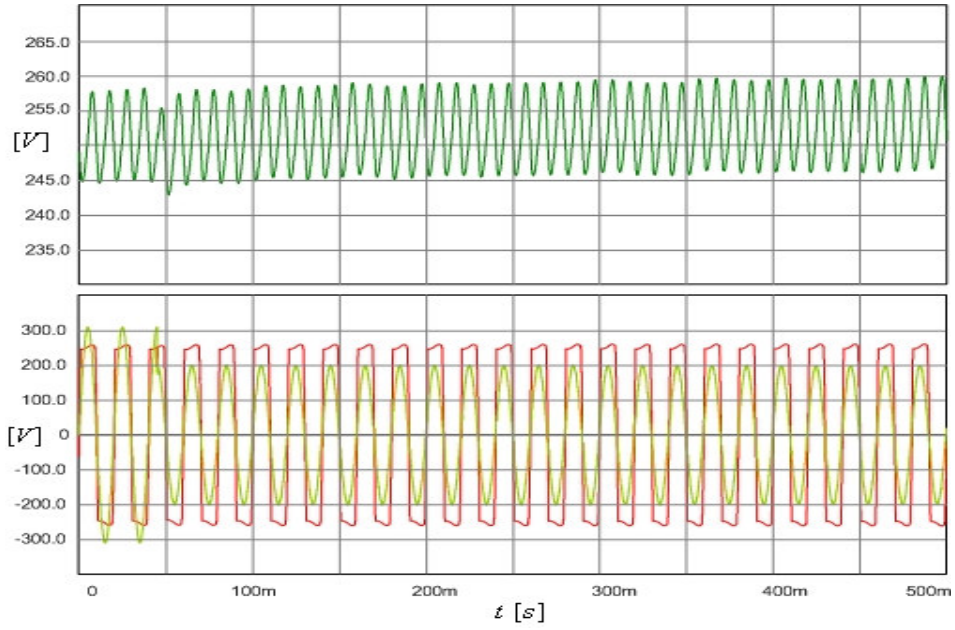



Figure 4.10 Load DC bus voltage (green), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-CM with feedback & feedforward).

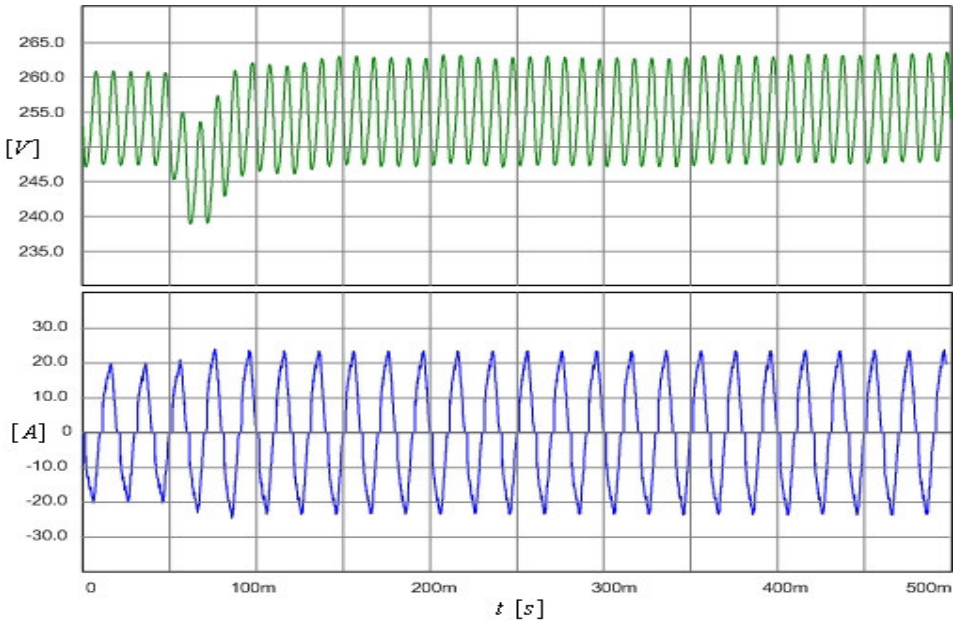



Figure 4.11 Load DC bus voltage (green) and line current (blue) waveforms for 20% load power increase (SPSAF-CM with feedback & feedforward).

Table 4.3 The comparison between the load voltage regulation performances of the linear model and the detailed model of the system (SPSAF-CM)

| | Linear Model | | Detailed Model | |
|---|---|---|---|---|
| | No FCC | Only Feedback | No FCC | Only Feedback |
| $\Delta v_{sag}$ (%) | 54.1 | 12.9 | 53.7 | 12.2 |
| $\Delta t_{sag}$ (ms) | 300 | 200 | 300 | 200 |
| $\Delta v_{dyn}$ (%) | 7.6 | 2.9 | 6.7 | 3.2 |
| $\Delta t_{dyn}$ (ms) | 260 | 40 | 250 | 40 |

### 4.2.3 Simulation of The SPSAF Compensated System Using AVM

The controller parameters used in the simulations of SPSAF using AVM are given in the Table 4.4. The simulations are conducted in the same manner as the CM case.

Table 4.4 The controller parameters of the SPSAF using AVM

| | | |
|---|---|---|
| $K_{hi}$ | HIC gain for line current | 10 |
| $K_{hv}$ | HIC gain for load voltage | 1 |
| $f_{cih}$ | HIC cut-off frequency for line current | 5 Hz |
| $K_d$ | RDC gain | 25 |
| $T_r$ | AVM rise time for load voltage synthesis | 0.4 ms |
| $T_\theta$ | AVM compensation time for phase angle delay | 200 µs |
| $K_{Pv}$ | FCC proportional gain | 1.5 |
| $K_{Iv}$ | FCC integral gain | 40 |
| $f_{cvff}$ | FCC LPF cut-off frequency for line voltage | 500 Hz |
| $f_{c4th}$ | AVM resonant filter frequency | 200 Hz |
| $f_{cvf}$ | AVM LPF cut-off frequency | 500 Hz |

#### 4.2.3.1 Harmonic Isolation

With the utilization of AVM, better harmonic isolation than the CM case is obtained as shown in Figure 4.12 such that $THD_I$ = 5.97%, $THD_V$ = 0.73%, and PF = 0.998 since the load harmonic voltage feedforward controller with AVM generates more accurate harmonic isolation reference voltage than the controller with CM. The improvement is primarily due to direct synthesis of the load harmonic voltage and the load voltage phase angle compensation in the controller using AVM. The controller using CM relies on the $K_{hi}$ and $K_{hv}$ gains strongly and due to the stability limitations $K_{hi}$ and $K_{hv}$ are quite bounded so that the controller using CM performance is limited. The phase delay of the CM method is also significant and its compensation is involved. Therefore, In the AVM case performance is significantly better than the CM case. Also, $\Delta v_{dc}$ becomes 4.0% as shown in Figure 4.13.

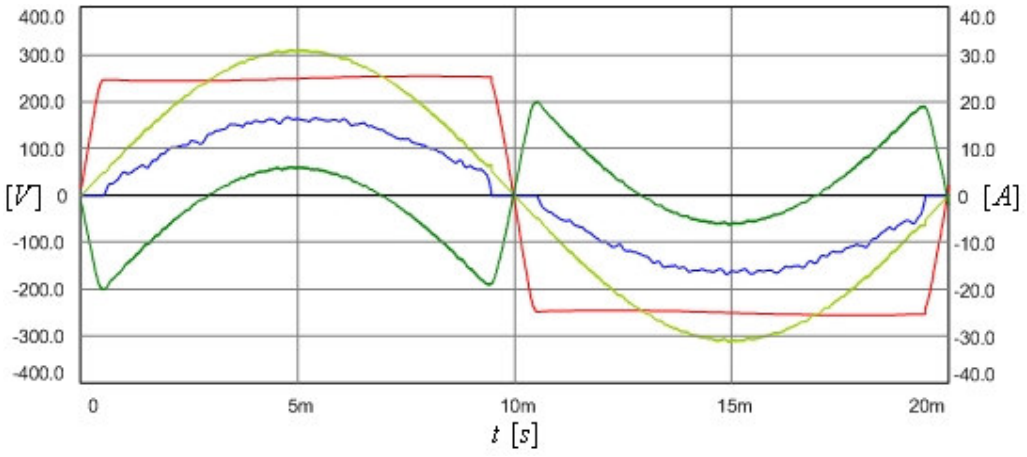



Figure 4.12 Line voltage (yellow), load voltage (red), SAF voltage (green), and line current (blue) waveforms (SPSAF-AVM).

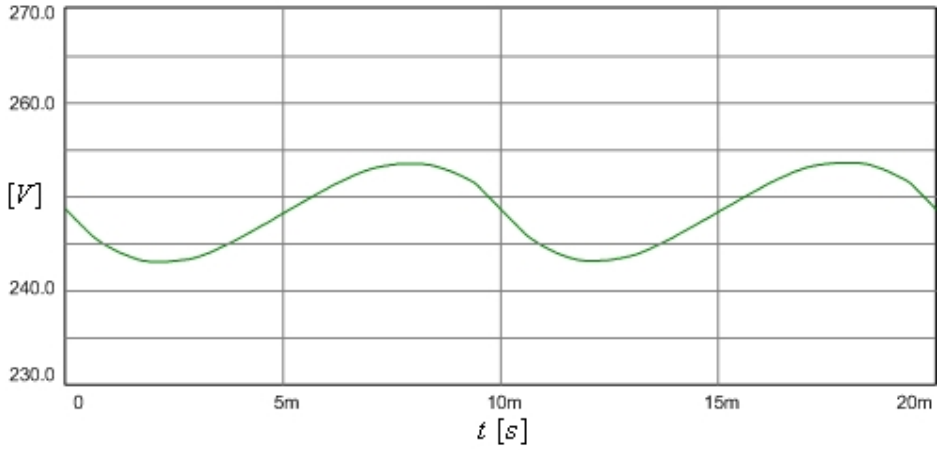



Figure 4.13 Load DC bus voltage waveform (SPSAF-AVM).

#### 4.2.3.2 Load Voltage Regulation

When FCC is inactive the responses of the SPSAF system using AVM to 35% voltage sag and 20% load power increase are shown in Figure 4.14 and Figure 4.15, respectively. In the former figure, $\Delta v_{sag}$ = 37.9% and $\Delta t_{sag}$ = 150 ms. In the latter figure, $\Delta v_{dyn}$ = 4.4% and $\Delta t_{dyn}$ = 125 ms. These results show that the feedforward controller of HIC with AVM does not affect the low frequency characteristic of the system as the feedforward controller with CM does. This implies that there is less interaction between the FCC and HIC controller of AVM based system than in the CM based system.

By means of the feedback controller of FCC, the responses of SPSAF to the same disturbances are improved as seen in Figure 4.16 and Figure 4.17. Maximum load voltage drops and settling times times are such that $\Delta v_{sag}$ = 4.4%, $\Delta t_{sag}$ = 40 ms, $\Delta v_{dyn}$ = 1.2%, and $\Delta t_{dyn}$ = 20 ms. In Table 4.5, maximum load voltage drops and settling times are listed along with those found for SPSAF without FCC and those found via simplified linear models with AVM in Chapter 3. Through the comparison of the results obtained by detailed and simplified models, the simplified linear model is validated.

With the addition of the feedforward controller of FCC, the response to the voltage sag is improved as shown in Figure 4.18 such that $\Delta v_{sag}$ and $\Delta t_{sag}$ are negligible. Expectedly, the response to the load power increase is not enhanced as shown in Figure 4.19 because the feedforward is only effective for the line voltage disturbances.

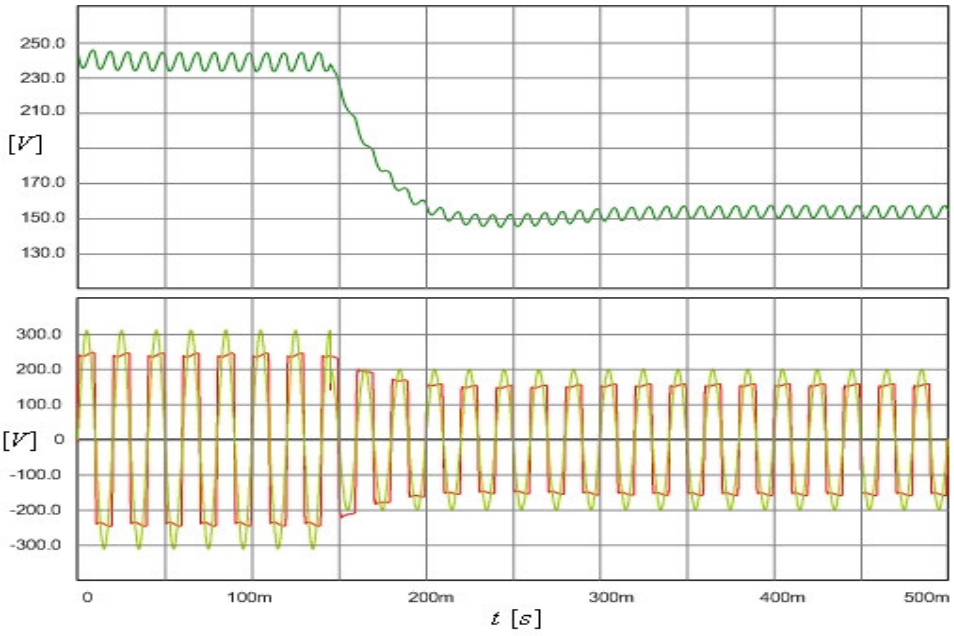



Figure 4.14 Load DC bus voltage (green), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-AVM without FCC).

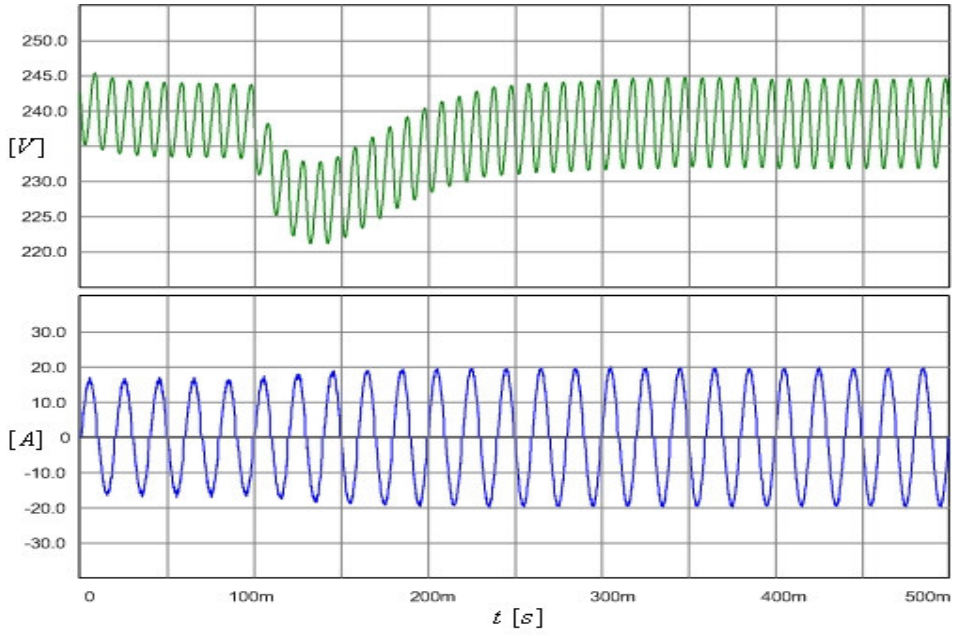



Figure 4.15 Load DC bus voltage (green) and line current (blue) waveforms for 20% load power increase (SPSAF-AVM without FCC).

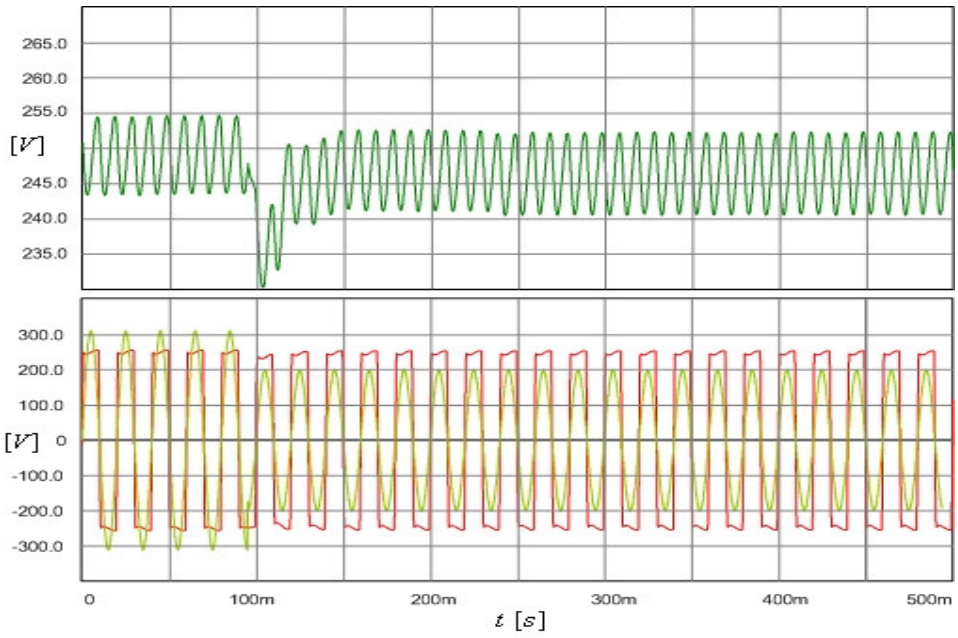



Figure 4.16 Load DC bus voltage (green), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-AVM with only feedback).

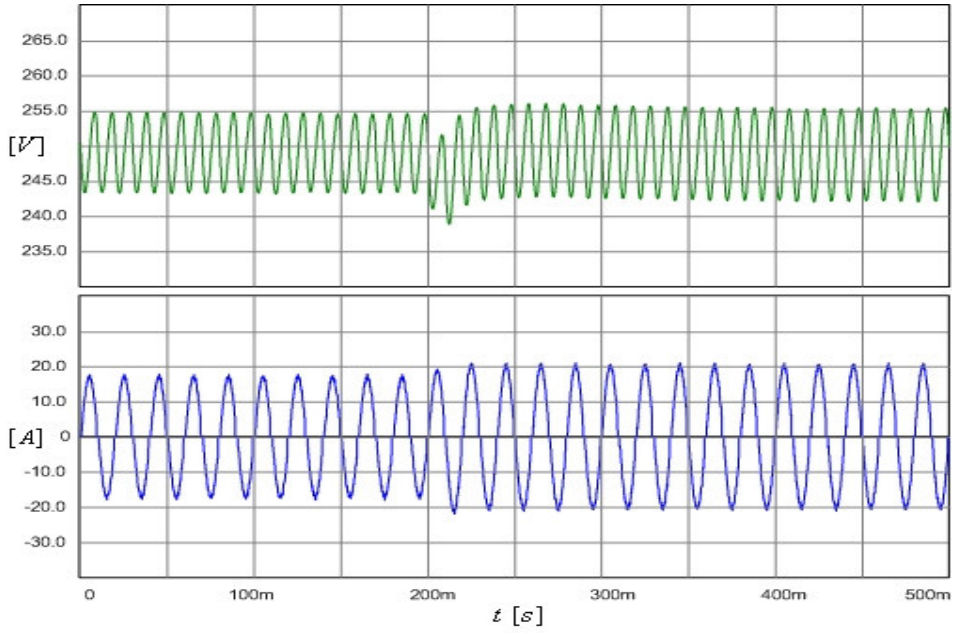



Figure 4.17 Load DC bus voltage (green) and line current (blue) waveforms for 20% load power increase (SPSAF-AVM with only feedback).

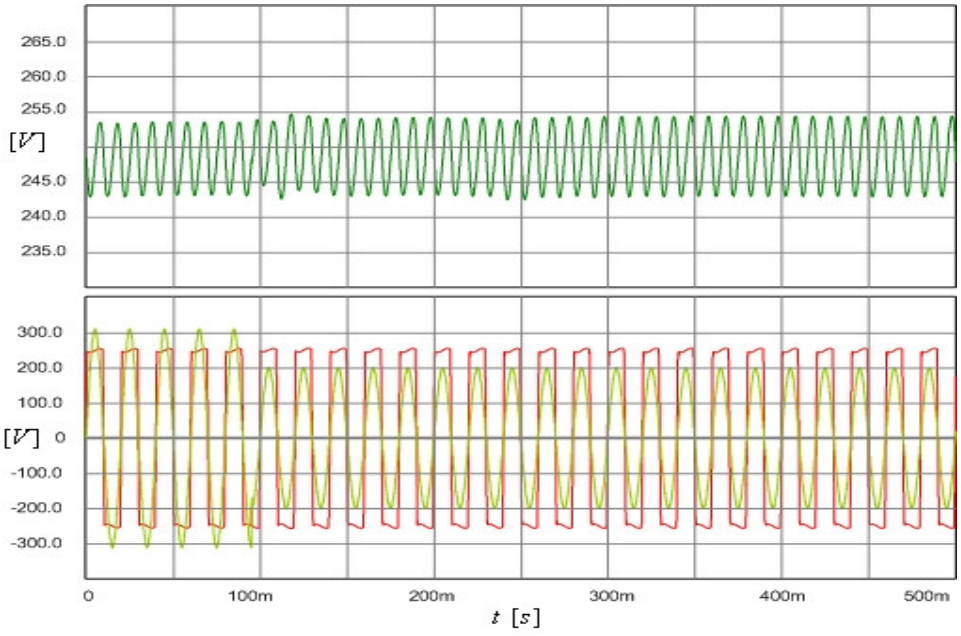



Figure 4.18 Load DC bus voltage (green), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-AVM with feedback & feedforward).

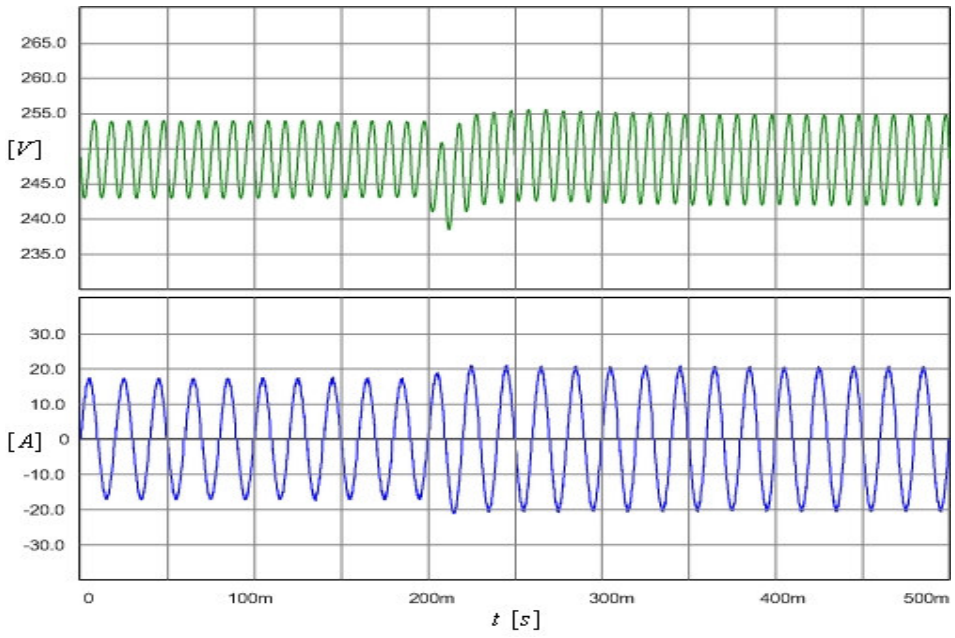



Figure 4.19 Load DC bus voltage (green) and line current (blue) waveforms for 20% load power increase (SPSAF-AVM with feedback & feedforward).

Table 4.5 The comparison between the load voltage regulation performances of the linear model and the detailed model of the system (SPSAF-AVM)

| | Linear Model | | Detailed Model | |
|---|---|---|---|---|
| | No FCC | Only Feedback | No FCC | Only Feedback |
| $\Delta v_{sag}$ (%) | 36.8 | 4.1 | 37.9 | 4.4 |
| $\Delta t_{sag}$ (ms) | 125 | 50 | 150 | 40 |
| $\Delta v_{dyn}$ (%) | 4.7 | 1.1 | 5.8 | 1.2 |
| $\Delta t_{dyn}$ (ms) | 125 | 15 | 125 | 20 |

### 4.2.4 Performance Comparison

As the criteria for harmonic mitigation, the IEEE 519 Recommendation is taken into account. In the recommendations, the limit for a specific harmonic component is proposed with respect to the short-circuit ratio ($I_{SC}/I_{L1}$) of the utility-load pair. The short circuit current of the utility is 1900 A ($L_S$ = 200 μH and $R_S$ = 100 mΩ) and the load current is 11.4 A (for 2.5 kW load). Then, the ratio is 167 and the IEEE 519 limits for this ratio are tabulated along with the simulation results in Table 4.6. Note that the load current is less than 16 A which implies that the harmonic standards do not apply directly. However, the simulation examples and laboratory prototypes are small rated due to infrastructure constraints. The small power rating however does not significantly change the circuit harmonic characteristics and the same harmonics can be directly applied to evaluate the power quality performance of the filter. Therefore, the small rated load will be considered with the same approach as the large power rating load that is required to meet the IEEE 519 limits. Considering the AVM and CM cases studied, although the harmonic limitations are satisfied by the two methods, the performance of the SPSAF using AVM is superior to the SPSAF using CM as Table 4.6 clearly illustrates.

In order to compare the load voltage regulation performances of SPSAF using CM and AVM for the voltage sag and the load power increase, the simulation results obtained under 35% voltage sag and 20% load power increase conditions are tabulated in Table 4.7. As seen in the table, the SPSAF using AVM is superior to the SPSAF using CM such that the former has less voltage drops and shorter response times. Moreover, it should be noticed in the table, the feedforward controller can improve the response of SPSAF to line voltage variations but not load dynamics as expected.

It is worthwhile to mention that the power rating of the load utilized in the simulation is relatively low compared to the modeled utility. The power line impedance modeled corresponds to several hundred kVA ratings and this is greater than the load by orders of magnitude. As a result the load current with or withour HIC does not

significantly influence the voltage THD at the PCC. Therefore, the line current THD is a better indicator of the power quality throughout the studies in this section and the upcoming three-phase system study.

Table 4.6 The performance comparison between the harmonic isolation provided by the SPSAF using CM and AVM

| | By-pass Mode | Standby Mode | SPSAF with CM | SPSAF with AVM | IEEE 519 Limits |
|---|---|---|---|---|---|
| $I_1$ (%) | 100.0 | 100.0 | 100.0 | 100.0 | 100.0 |
| $I_3$ (%) | 89.1 | 80.1 | 9.7 | 0.5 | 12.0 |
| $I_5$ (%) | 69.9 | 49.4 | 6.2 | 1.5 | 12.0 |
| $I_7$ (%) | 47.1 | 20.7 | 3.9 | 1.5 | 12.0 |
| $I_9$ (%) | 25.4 | 6.0 | 3.9 | 2.2 | 12.0 |
| $I_{11}$ (%) | 8.9 | 6.8 | 1.6 | 1.8 | 5.5 |
| $I_{13}$ (%) | 2.9 | 4.6 | 0.5 | 1.1 | 5.5 |
| $I_{15}$ (%) | 5.6 | 2.5 | 1.1 | 1.8 | 5.5 |
| $I_{17}$ (%) | 4.8 | 2.7 | 2.2 | 2.6 | 5.0 |
| $I_{19}$ (%) | 2.4 | 1.9 | 1.4 | 0.8 | 5.0 |
| $I_{21}$ (%) | 1.6 | 1.4 | 1.6 | 0.6 | 5.0 |
| $I_{23}$ (%) | 2.2 | 1.4 | 0.5 | 0.8 | 2.0 |
| $I_{25}$ (%) | 1.9 | 1.9 | 1.0 | 0.7 | 2.0 |
| $THD_I$ (%) | 125.91 | 97.01 | 13.75 | 5.97 | 15.0 |
| $THD_V$ (%) | 3.69 | 2.42 | 0.88 | 0.73 | 5.0 |
| PF | 0.605 | 0.700 | 0.984 | 0.998 | - |
| $\Delta v_{dc}$ (%) | 14.8 | 12.8 | 5.5 | 4.0 | - |

Table 4.7 The performance comparison between the load voltage regulation provided by the SPSAF using CM and AVM

| | CM | | AVM | |
|---|---|---|---|---|
| | Only Feedback | Feedback & Feedforward | Only Feedback | Feedback & Feedforward |
| $\Delta v_{sag}$ (%) | 12.2 | 0 | 4.4 | 0 |
| $\Delta t_{sag}$ (ms) | 200 | 0 | 40 | 0 |
| $\Delta v_{dyn}$ (%) | 3.2 | 3.2 | 1.2 | 1.2 |
| $\Delta t_{dyn}$ (ms) | 40 | 40 | 20 | 20 |

## 4.3 TPSAF

### 4.3.1 Simulation Model of The 10 kW TPSAF Compensated System

The three-phase system diagram used in the simulation study is illustrated in Figure 4.20. As shown in the figure, the utility is modeled as a three-phase ideal voltage source with an equivalent inductance and an equivalent resistance. The nonlinear load is a three-phase diode rectifier with a parallel resistor-capacitor (RC) load (V-type nonlinear load). With a full-bridge per phase VSI, a switching ripple filter per phase, and a series injection transformer per phase, TPSAF is constituted. At the DC bus of the VSI, a three-phase diode bridge rectifier stands as an auxiliary DC power supply. Additionally, a thyristor by-pass circuit is placed across the output terminals of each SIT. The parameters used in the simulation are listed in Table 4.8. The controllers are also modeled in detail emulating a digital signal processor. The simulations of TPSAF using CM and AVM are conducted and reported in the following.

### 4.3.2 Simulation of The TPSAF Compensated System Using CM

With CM, the simulation results are reported regarding harmonic isolation and load voltage regulation. In investigating the TPSAF performance for the load voltage regulation, three types of disturbance are considered, which are three-phase and single-phase voltage sags by 35% of rated utility voltage, and an instantaneous load power increase by 20% of rated load power. The controller parameters of the TPSAF using CM are given in the Table 4.9.

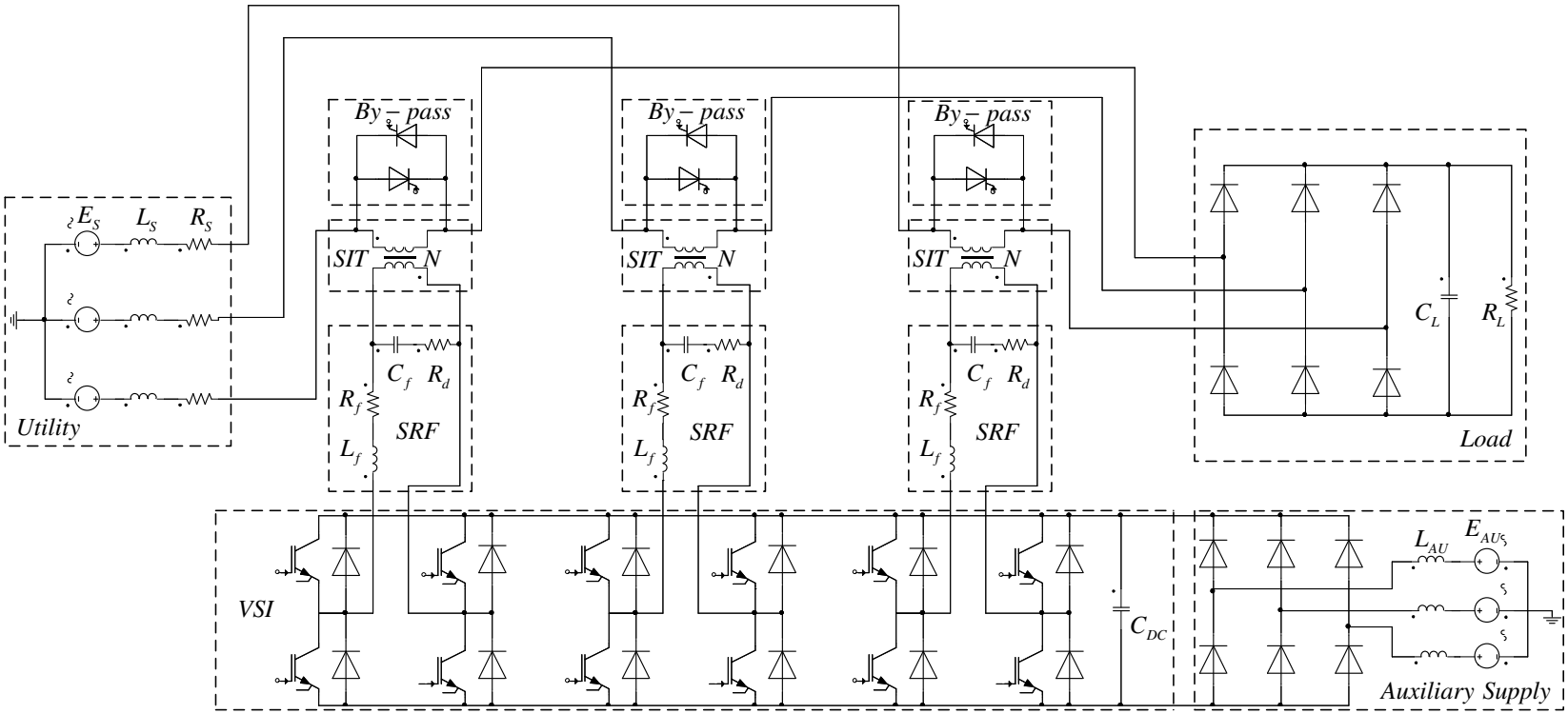



Figure 4.20 The simulation model of the TPSAF compensated system in Simplorer.

Table 4.8 The simulation model parameters (TPSAF)

| | | |
|---|---|---|
| $E_S$ | Utility voltage (per phase) | 220 $V_{rms}$ (50 Hz) |
| $L_S$ | Utility leakage inductance (per phase) | 200 µH |
| $R_S$ | Utility resistance (per phase) | 100 mΩ |
| $V_{L,DC}$ | Rated DC bus voltage of the compensated load | 488 V |
| $C_L$ | Load capacitance | 2.2 mF |
| $R_L$ | Load resistance | 24 Ω (10 kW) |
| $L_f$ | SRF inductance | 2.2 mH |
| $C_f$ | SRF capacitance | 2.0 µF |
| $R_f$ | Resistance of the SRF inductance | 450 mΩ |
| $R_d$ | SRF damping resistance | 5.6 Ω |
| $V_{DC}$ | Rated DC bus voltage of VSI | 520 V |
| $C_{DC}$ | DC bus capacitance of VSI | 4.95 mF |
| $E_{AU}$ | Supply voltage of auxiliary rectifier | 380 $V_{rms}$ (50 Hz) |
| $L_{AU}$ | Line inductance of auxiliary rectifier | 1.43 mH |
| $L_1$ | Primary side leakage inductance of SIT | 250 µH |
| $L_2$ | Secondary side leakage inductance of SIT | 40 µH |
| $R_1$ | Primary side copper resistance of SIT | 550 mΩ |
| $R_2$ | Secondary side copper resistance of SIT | 90 mΩ |
| N | Turns-ratio of SIT ($N_1$:$N_2$) | 2.5 |
| $f_{PWM}$ | PWM frequency | 20 kHz |
| $T_S$ | Sampling time (Double update) | 25 µs |

Table 4.9 The controller parameters of the TPSAF using CM

| | | |
|---|---|---|
| $K_{hi}$ | HIC gain for line current | 10 |
| $K_{hv}$ | HIC gain for load voltage | 0.9 |
| $f_{cih}$ | HIC cut-off frequency for line current | 7.5 Hz |
| $f_{cvh}$ | HIC cut-off frequency for load voltage | 7.5 Hz |
| $K_d$ | RDC gain | 20 |
| $K_{Pv}$ | FCC proportional gain | 1.5 |
| $K_{Iv}$ | FCC integral gain | 40 |
| $f_{cv1}$ | FCC cut-off frequency for load voltage | 15 Hz |
| $f_{cvff}$ | FCC LPF cut-off frequency for line voltage | 500 Hz |
| $a_v$ | Constant of phase-lead compensator in FCC | 4.6 |
| $T_v$ | Time constant of phase-lead compensator in FCC | 10 ms |

#### 4.3.2.1 Harmonic Isolation

As done in SPSAF, the harmonic distortion of the three-phase V-type nonlinear load is investigated for by-pass and standby modes before the harmonic isolation performance of TPSAF is observed; the line and load voltages, and line current waveforms for the two modes are given in Figure 4.21. The presence of the filter inductor improves the power quality to the extent that $THD_I$ decreases from 94.50% to 58.87%, $THD_V$ decreases from 3.21% to 1.73%, and PF increases from 0.713 to 0.845. Additionally, as shown in Figure 4.22, $\Delta v_{dc}$ for the two cases are 2.5% and 1.4%, respectively.

With the injection of the harmonic isolation voltage by TPSAF, line current and voltage waveforms, as shown in Figure 4.23, become less distorted ($THD_I$ = 9.91% and $THD_V$ = 0.93%). PF also improves and is near unity (0.991). As expected, the load voltage resembles a six-step rectangular waveform by the TPSAF harmonic isolation voltage. As a result, $\Delta v_{dc}$ decreases to 0.2% as shown in Figure 4.24.

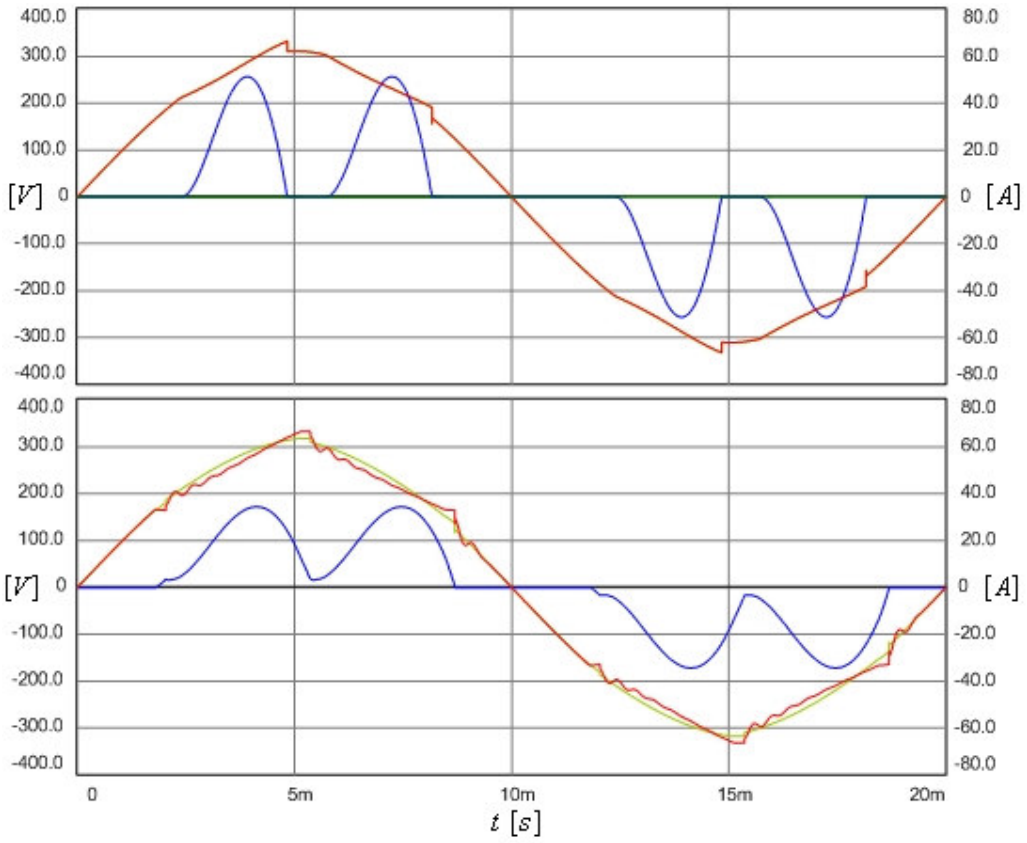



Figure 4.21 Uncompensated three-phase system line voltage (yellow), load voltage (red), and line current (blue) waveforms in by-pass mode (top) and standby mode (bottom).

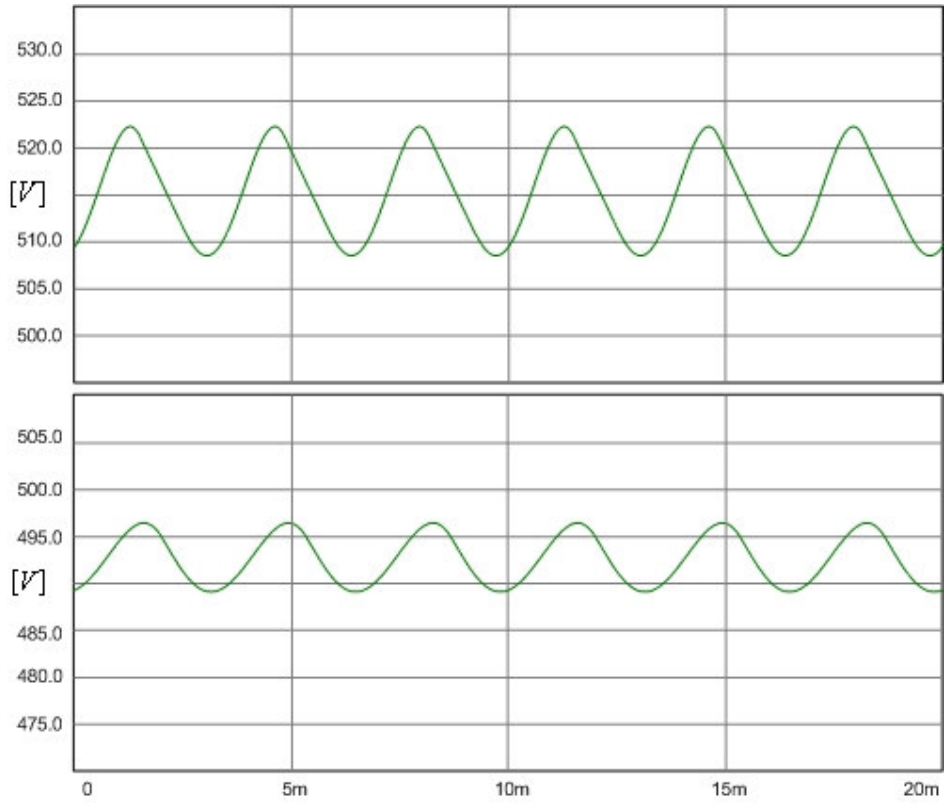



Figure 4.22 Uncompensated three-phase system load DC bus voltage waveforms in by-pass mode (top) and in standby mode (bottom) (TPSAF).

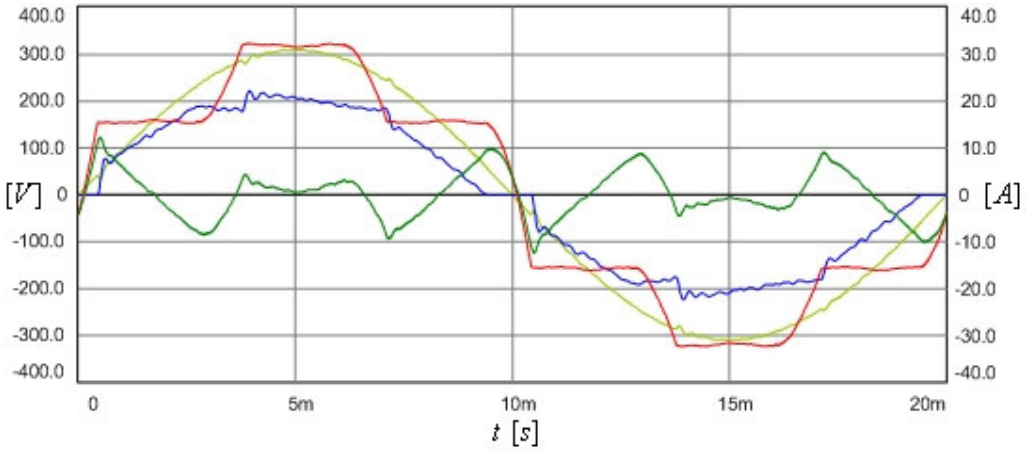



Figure 4.23 Line voltage (yellow), load voltage (red), SAF voltage (green), and line current (blue) waveforms (TPSAF-CM).

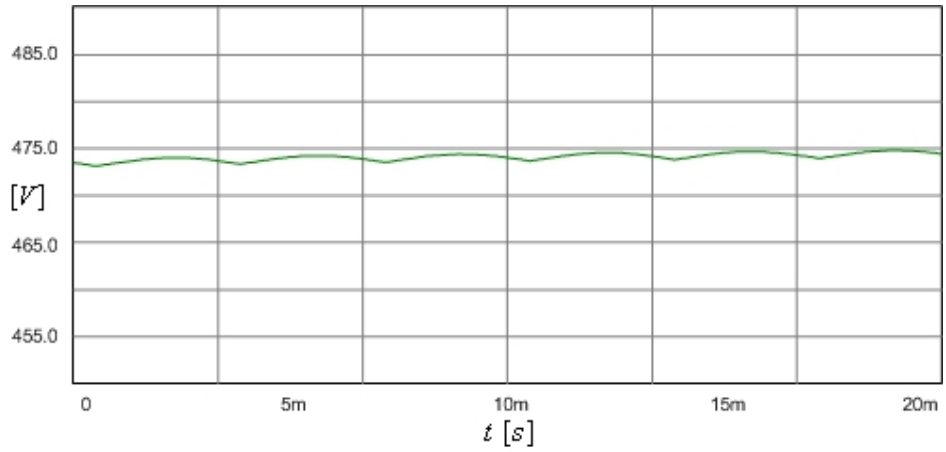



Figure 4.24 Load DC bus voltage waveform (TPSAF-CM).

#### 4.3.2.2 Load Voltage Regulation

The load voltage regulation performance of TPSAF is reported against three types of disturbances, which are three-phase balanced 35% utility voltage sag, single-phase 35% utility voltage sag, and load power increase by 20%.

When FCC of TPSAF does not operate (No FCC); the load DC bus, load, and line voltages during 35% three-phase voltage sag are shown in Figure 4.25. In the figure, the maximum voltage drop on the load DC bus voltage ($\Delta v_{sag}$) and the settling time ($\Delta t_{sag}$) are 52.4% and 300 ms. For 35% single-phase sag the response is shown in Figure 4.26. In the figure, the voltage ripple due to negative sequence ($\Delta v_{neg}$) appears 1.0% at steady-state. In the sag conditions, low frequency voltage fluctuations accompanied with decrease on the load voltage are due to the effect of HIC on the system characteristics as explained in Chapter 3. For the load power increase by 20%, the response is illustrated by the load DC bus voltage and line current in Figure 4.27. In the figure, the maximum voltage drop and the time elapsed for steady-state are $\Delta v_{dyn}$ = 7.0% and $\Delta t_{dyn}$ = 200 ms.

When the feedback controller of FCC is active, the responses of TPSAF to the same disturbances as above mentioned improves as shown in Figure 4.28, Figure 4.29, and Figure 4.30 except for $\Delta v_{neg}$, which remains the same as the case without FCC. In Table 4.10, the maximum load voltage drops, the settling times, and the negative sequence voltage ripples are listed along with those obtained in the simulations of TPSAF without FCC and those found in Chapter 3 for TPSAF using CM. In the table, the consistency between the simulation results obtained using the detailed model and the simplified linear model verifies the validity of the simplified linear models.

With the addition of the feedforward controller, the responses to the sag conditions are improved as shown in Figure 4.31 and Figure 4.32 such that $\Delta v_{sag}$, $\Delta v_{neg}$, and $\Delta t_{sag}$ (0.6%, 0.4%, and 0 ms) are smaller than those obtained by TPSAF with only feedback. However, the response to load power increase does not enhance as shown in Figure 4.33.

Table 4.10 The comparison between the load voltage regulation performances of the linear model and the detailed model of the system (TPSAF-CM)

| | Linear Model | | Detailed Model | |
|---|---|---|---|---|
| | No FCC | Only Feedback | No FCC | Only Feedback |
| $\Delta v_{sag}$ (%) | 51.2 | 10.5 | 52.4 | 10.5 |
| $\Delta t_{sag}$ (ms) | 290 | 210 | 300 | 200 |
| $\Delta v_{dyn}$ (%) | 7.1 | 2.7 | 7.0 | 2.9 |
| $\Delta t_{dyn}$ (ms) | 170 | 30 | 200 | 35 |
| $\Delta v_{neg}$ (%) | 1.0 | 1.0 | 1.0 | 1.2 |

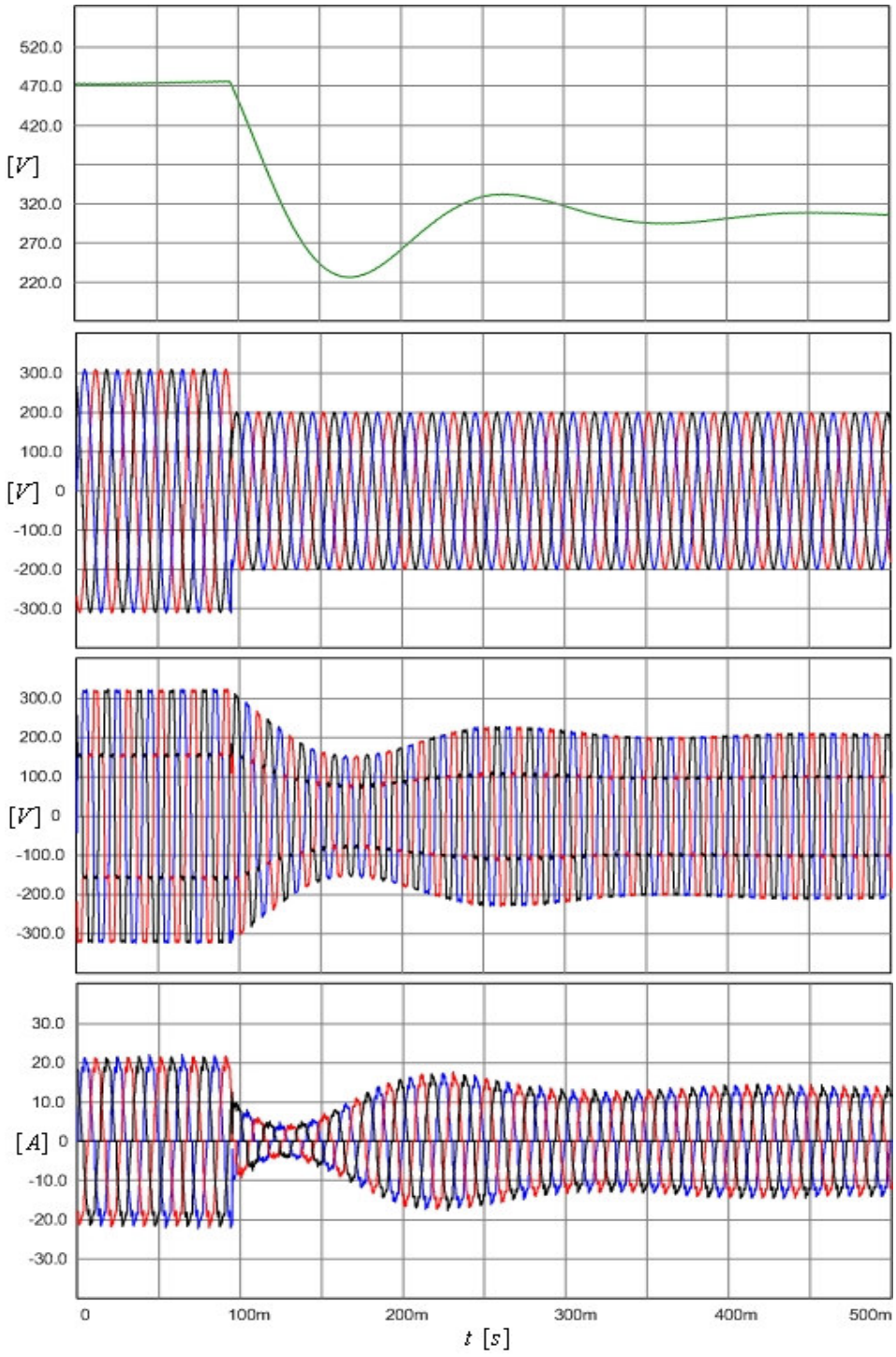



Figure 4.25 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-CM without FCC).

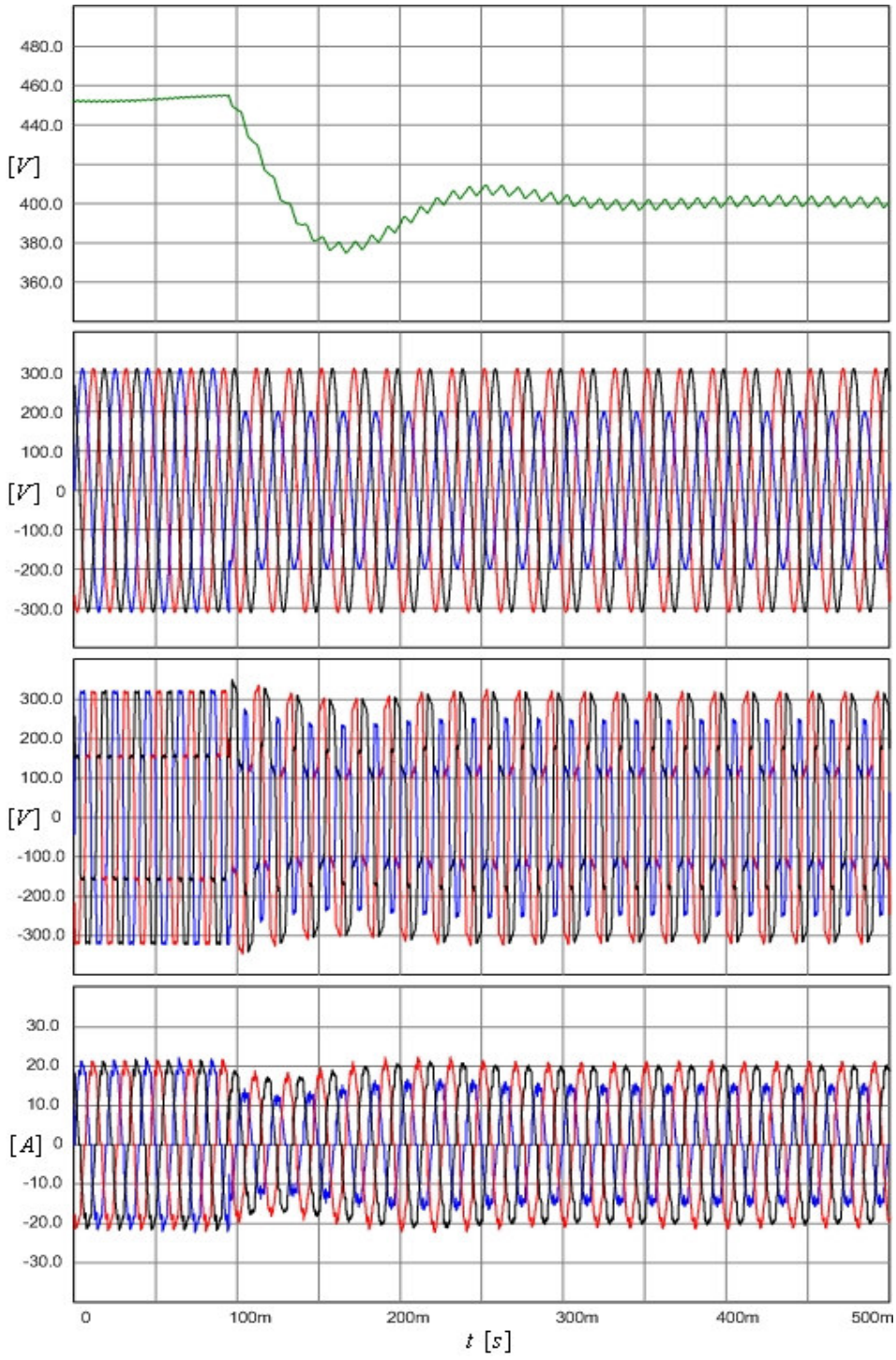



Figure 4.26 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-CM without FCC).

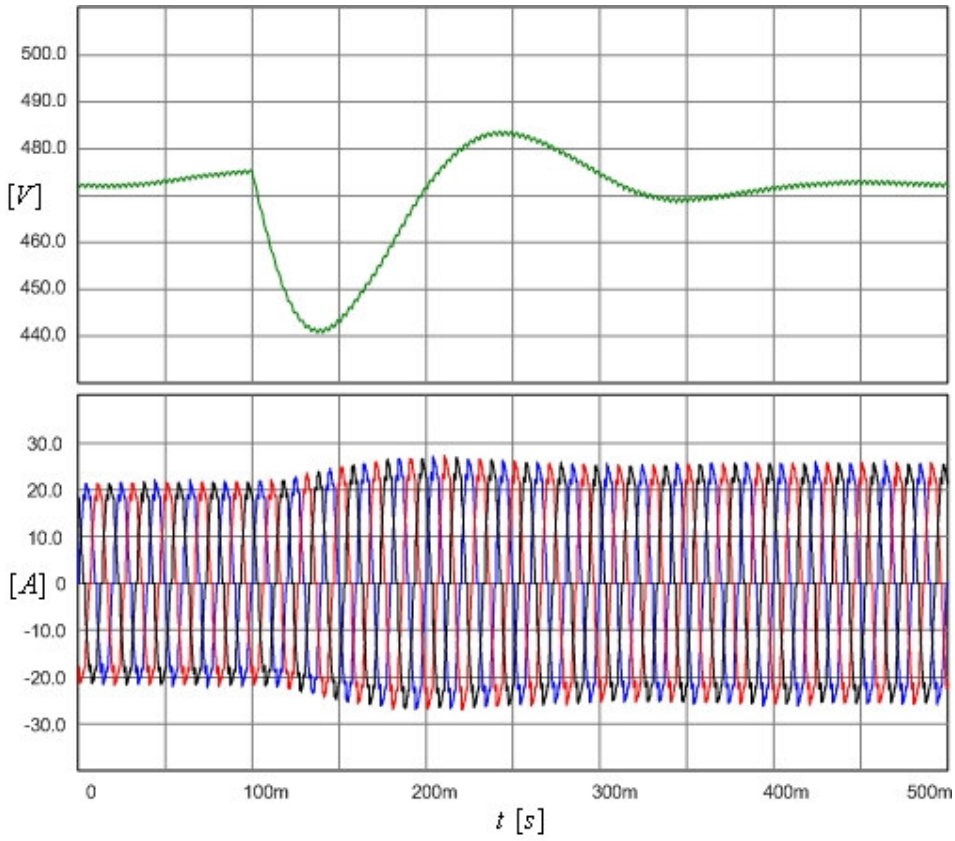



Figure 4.27 The load DC bus voltage (top) and three-phase line currents (bottom) waveforms for 20% load power increase (TPSAF-CM without FCC).

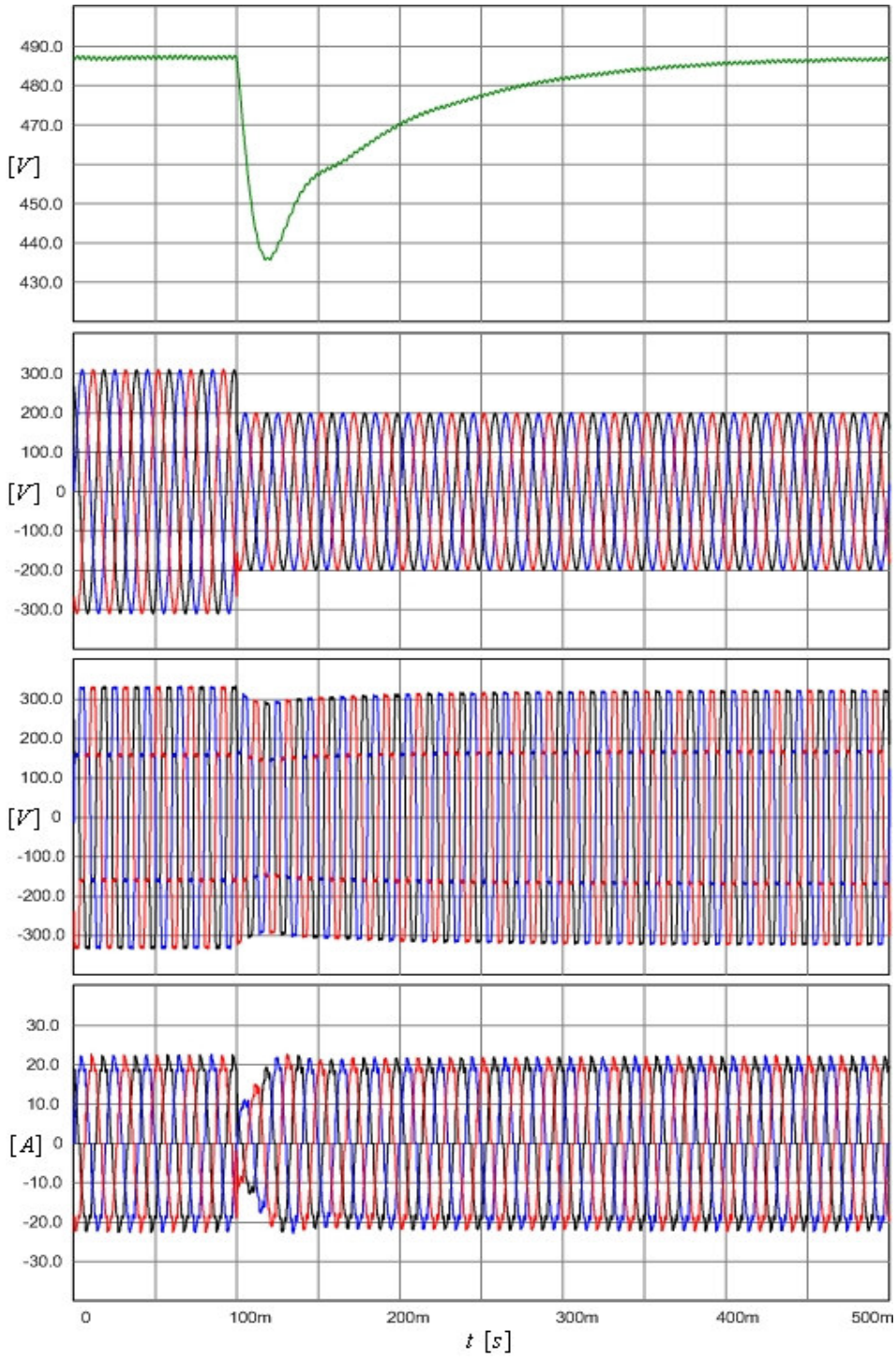



Figure 4.28 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-CM with only feedback).

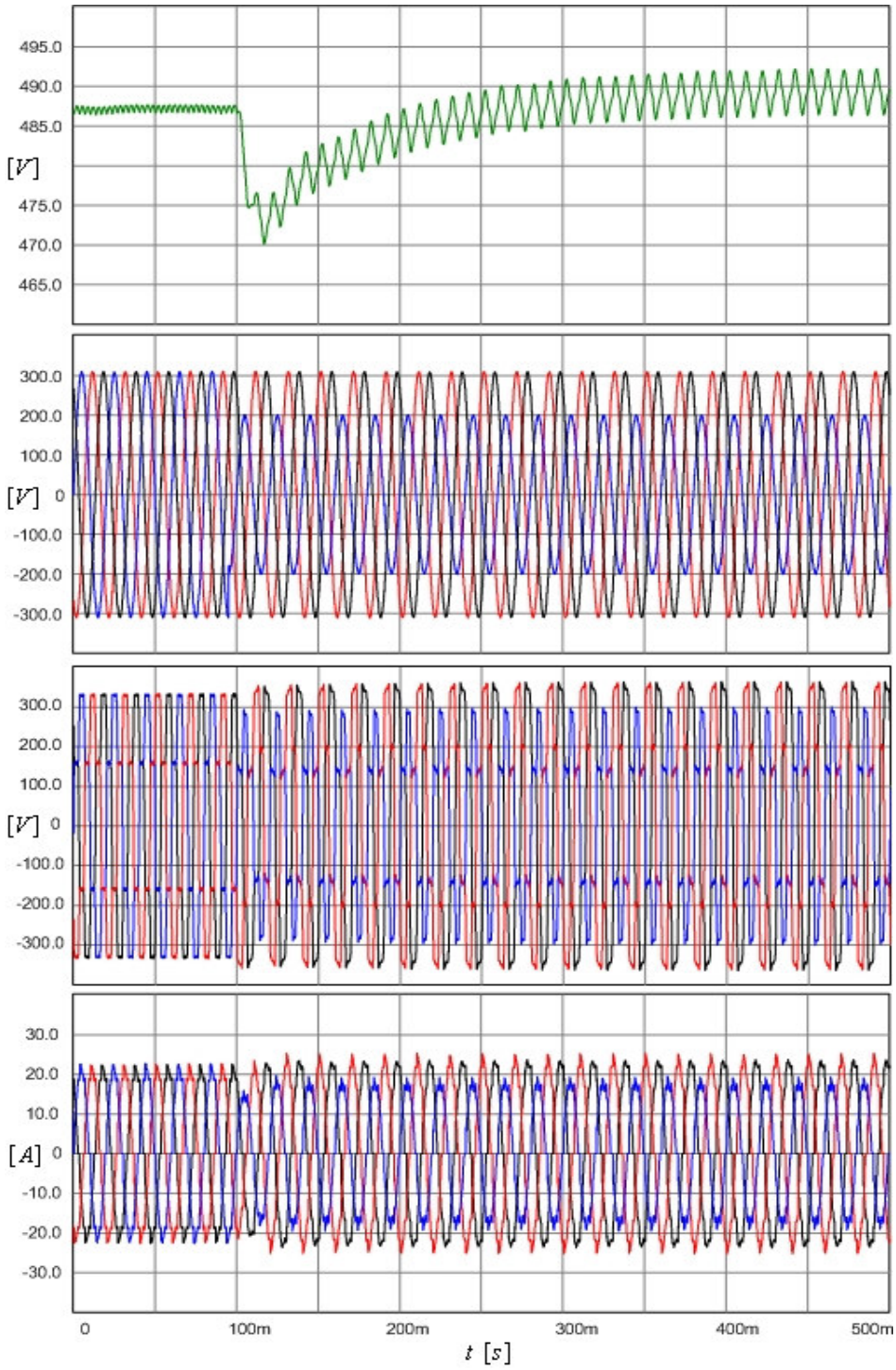



Figure 4.29 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-CM with only feedback).

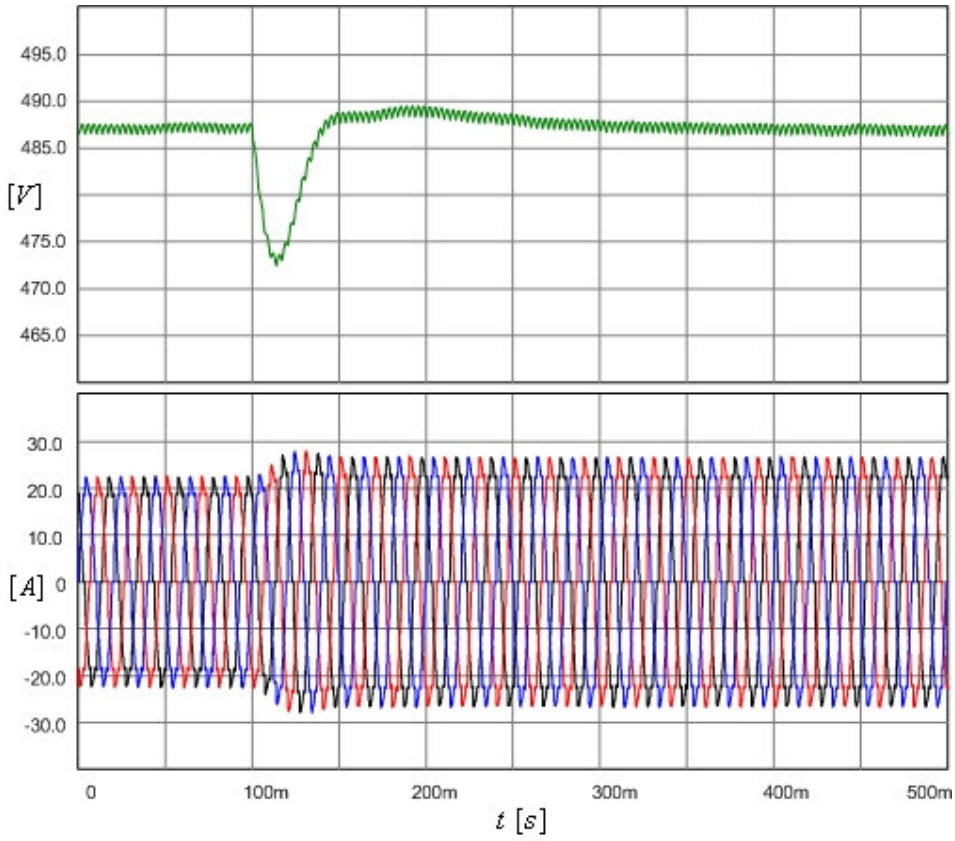



Figure 4.30 Load DC bus voltage (top) and three-phase line currents (bottom) waveforms for 20% load power increase (TPSAF-CM with only feedback).

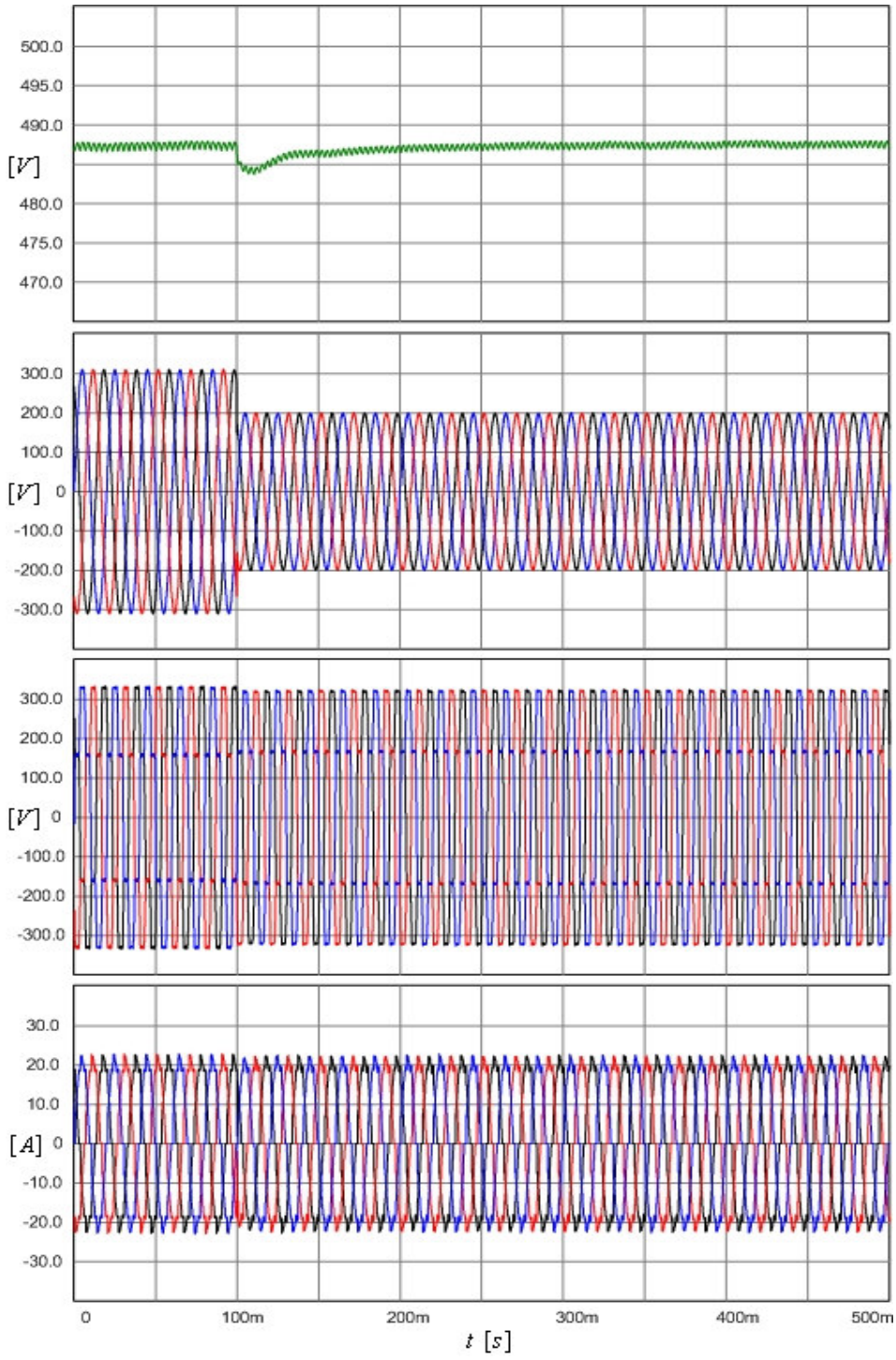



Figure 4.31 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-CM with feedback&feedforward).

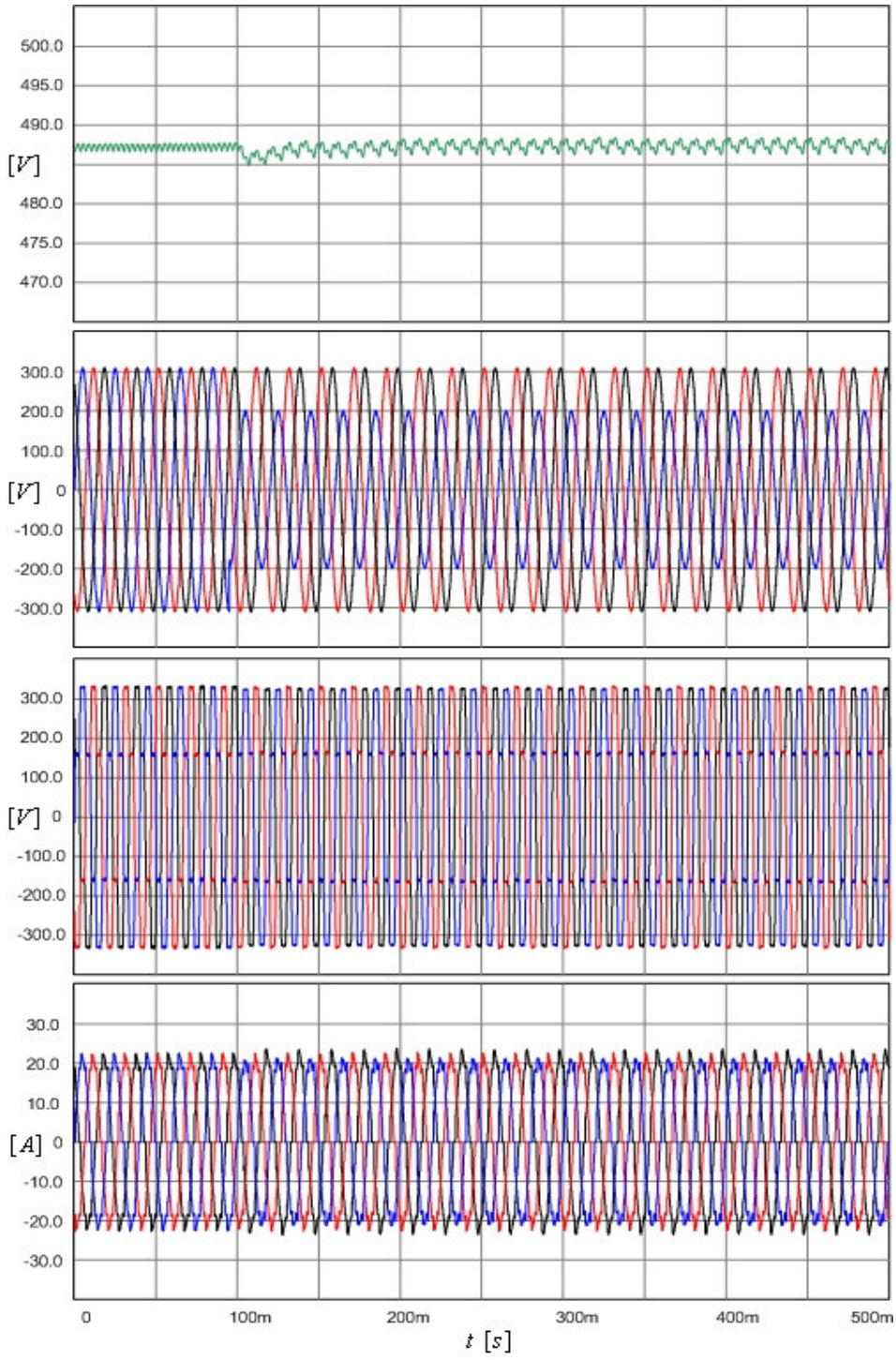



Figure 4.32 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-CM with feedback&feedforward).

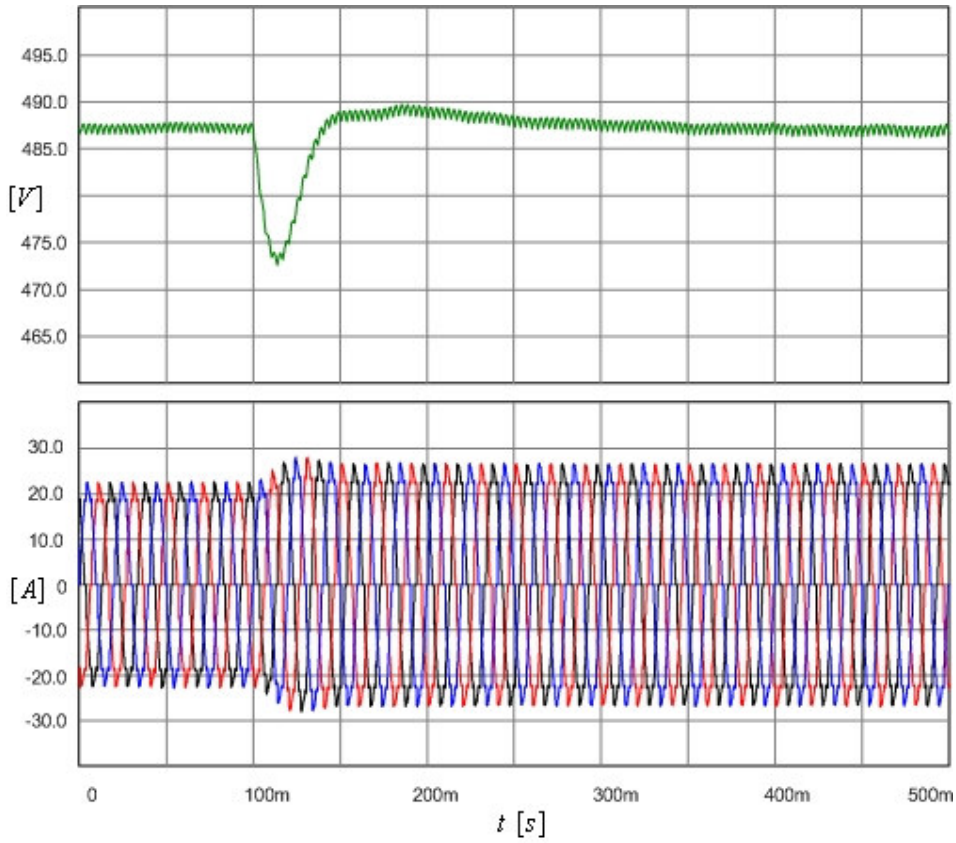



Figure 4.33 Load DC bus voltage (top) and three-phase line currents (bottom) waveforms for 20% load power increase (TPSAF-CM with feedback&feedforward).

### 4.3.3 Simulation of The TPSAF Compensated System Using AVM

The controller parameters used in the simulations for AVM are given in the Table 4.11.

#### 4.3.3.1 Harmonic Isolation

With the utilization of TPSAF using AVM, the harmonic isolation becomes better than the system with CM, as shown in Figure 4.34 such that $THD_I$ = 3.95% and $THD_V$ = 0.60% and PF approaches to the unity (0.998). Additionally, $\Delta v_{dc}$ becomes 0.1% as shown in Figure 4.35.

Table 4.11 The controller parameters of TPSAF using AVM

| | | |
|---|---|---|
| $K_{hi}$ | HIC gain for line current | 10 |
| $K_{hv}$ | HIC gain for load voltage | 1 |
| $f_{cih}$ | HIC cut-off frequency for line current | 7.5 Hz |
| $K_d$ | RDC gain | 20 |
| $T_r$ | AVM rise time for load voltage synthesis | 0.4 ms |
| $T_\theta$ | AVM compensation time for phase angle delay | 200 μs |
| $K_{Pv}$ | FCC proportional gain | 5 |
| $K_{Iv}$ | FCC integral gain | 175 |
| $f_{cvff}$ | FCC LPF cut-off frequency for line voltage | 500 Hz |
| $f_{c2th}$ | AVM resonant filter frequency ($2f_e$) | 100 Hz |
| $f_{c6th}$ | AVM resonant filter frequency ($6f_e$) | 300 Hz |
| $f_{cv}$ | AVM LPF cut-off frequency | 300 Hz |

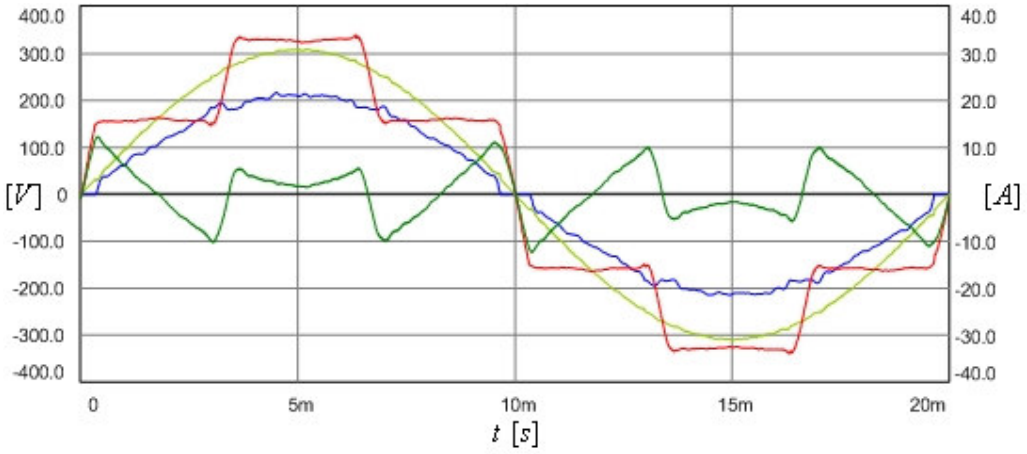



Figure 4.34 Line voltage (yellow), load voltage (red), SAF voltage (green), and line current (blue) waveforms (TPSAF-AVM).

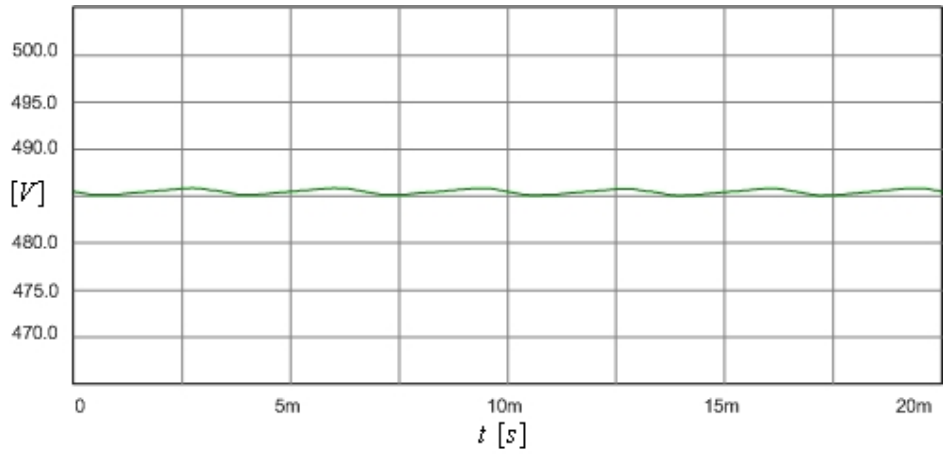



Figure 4.35 Load DC bus voltage waveform (TPSAF-AVM).

#### 4.3.3.2 Load Voltage Regulation

When TPSAF operates just as a harmonic isolator using AVM (without FCC), its response to the three-phase voltage sag is shown by the load DC bus, the load, and the line voltages in Figure 4.36. In the figure, $\Delta v_{sag}$ and $\Delta t_{sag}$ are 39.9% and 150 ms. It should be noted that the low frequency fluctuations present in the CM case do not appear due to the HIC employing AVM. In Figure 4.37, the response of TPSAF to the single-phase sag is illustrated. $\Delta v_{neg}$ appears 1.1% at steady-state in the figure, which shows that the system is immune to the negative sequence. For the load power increase, the response is such that $\Delta v_{dyn}$ and $\Delta t_{dyn}$ (5.1% and 100 ms) as shown in Figure 4.38.

When the feedback controller of FCC is active, the responses of TPSAF to the same disturbances as above mentioned improve such that $\Delta v_{sag}$ = 6.1%, $\Delta t_{sag}$ = 60 ms, $\Delta v_{dyn}$ = 1.8%, and $\Delta t_{dyn}$ = 25 ms, as shown in Figure 4.39, Figure 4.40, and Figure 4.41. Exceptionally, $\Delta v_{neg}$ remains almost the same. It is observed that these responses are better than those obtained in the CM case. In Table 4.12, the maximum load voltage drops, the settling times, and the negative sequence voltage ripples are listed along with those found in the simulations of TPSAF without FCC and those

found in Chapter 3 for AVM. In the table, the consistency between the simulation results obtained using the detailed model and the simplified linear model verifies the validity of the simplified linear models.

With the use of the feedforward controller in addition to the feedback controller, the response to the three-phase sag is improved as shown in Figure 4.42 such that $\Delta v_{sag}$ is 0.5% and $\Delta t_{sag}$ is nearly zero. The response to the single-phase sag enhances and $\Delta v_{neg}$ becomes 0.3% as shown in Figure 4.43. As expected, the response to the load power increase does not get enhanced as shown in Figure 4.44.

Table 4.12 The comparison between the load voltage regulation performances of the linear model and the detailed model of the system (TPSAF-AVM)

| | Linear Model | | Detailed Model | |
|---|---|---|---|---|
| | No FCC | Only Feedback | No FCC | Only Feedback |
| $\Delta v_{sag}$ (%) | 38.6 | 5.6 | 39.9 | 6.1 |
| $\Delta t_{sag}$ (ms) | 150 | 60 | 150 | 60 |
| $\Delta v_{dyn}$ (%) | 5.1 | 1.7 | 5.1 | 1.8 |
| $\Delta t_{dyn}$ (ms) | 100 | 25 | 100 | 25 |
| $\Delta v_{neg}$ (%) | 1.0 | 1.0 | 1.1 | 1.2 |

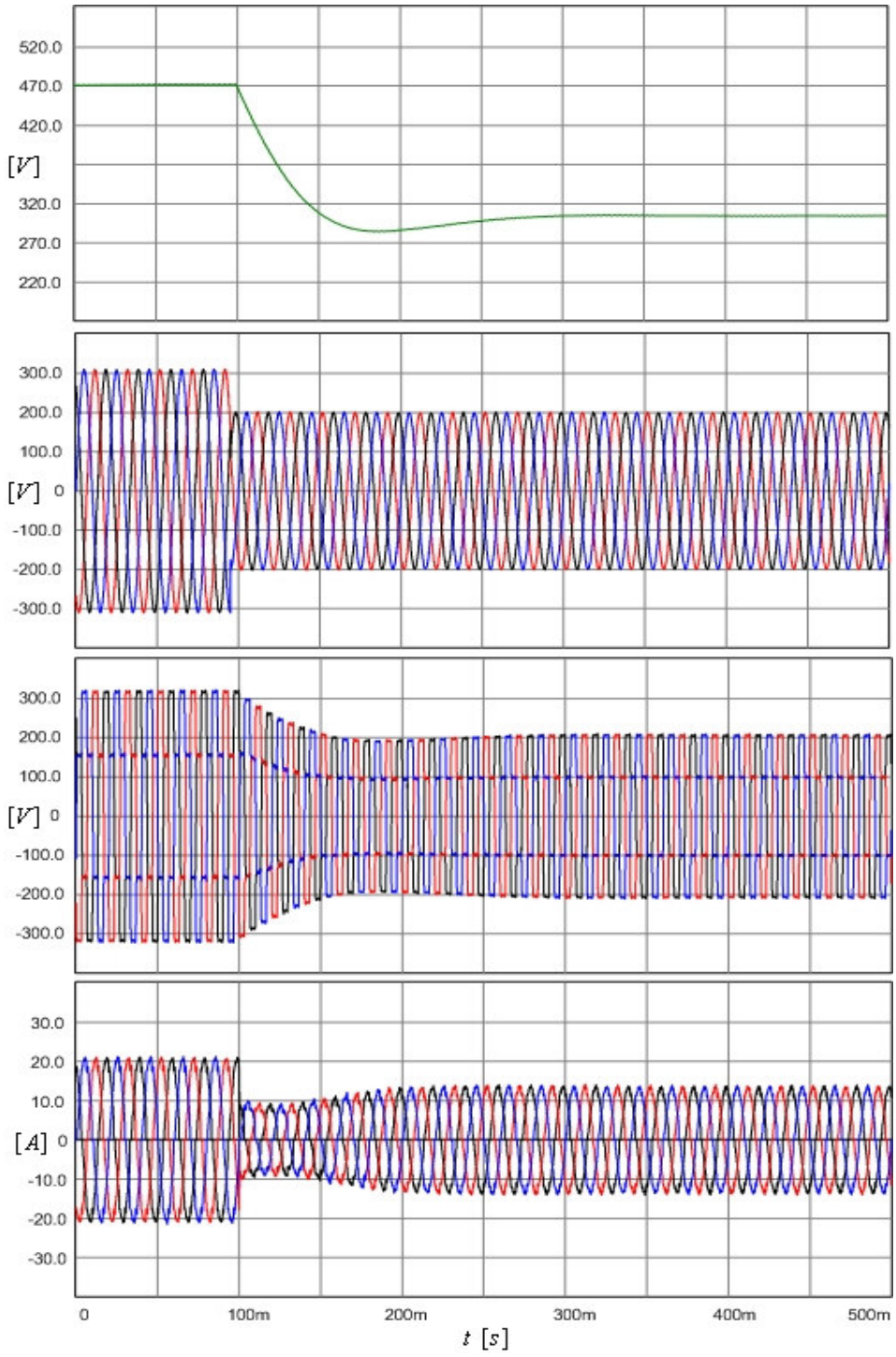



Figure 4.36 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-AVM without FCC).

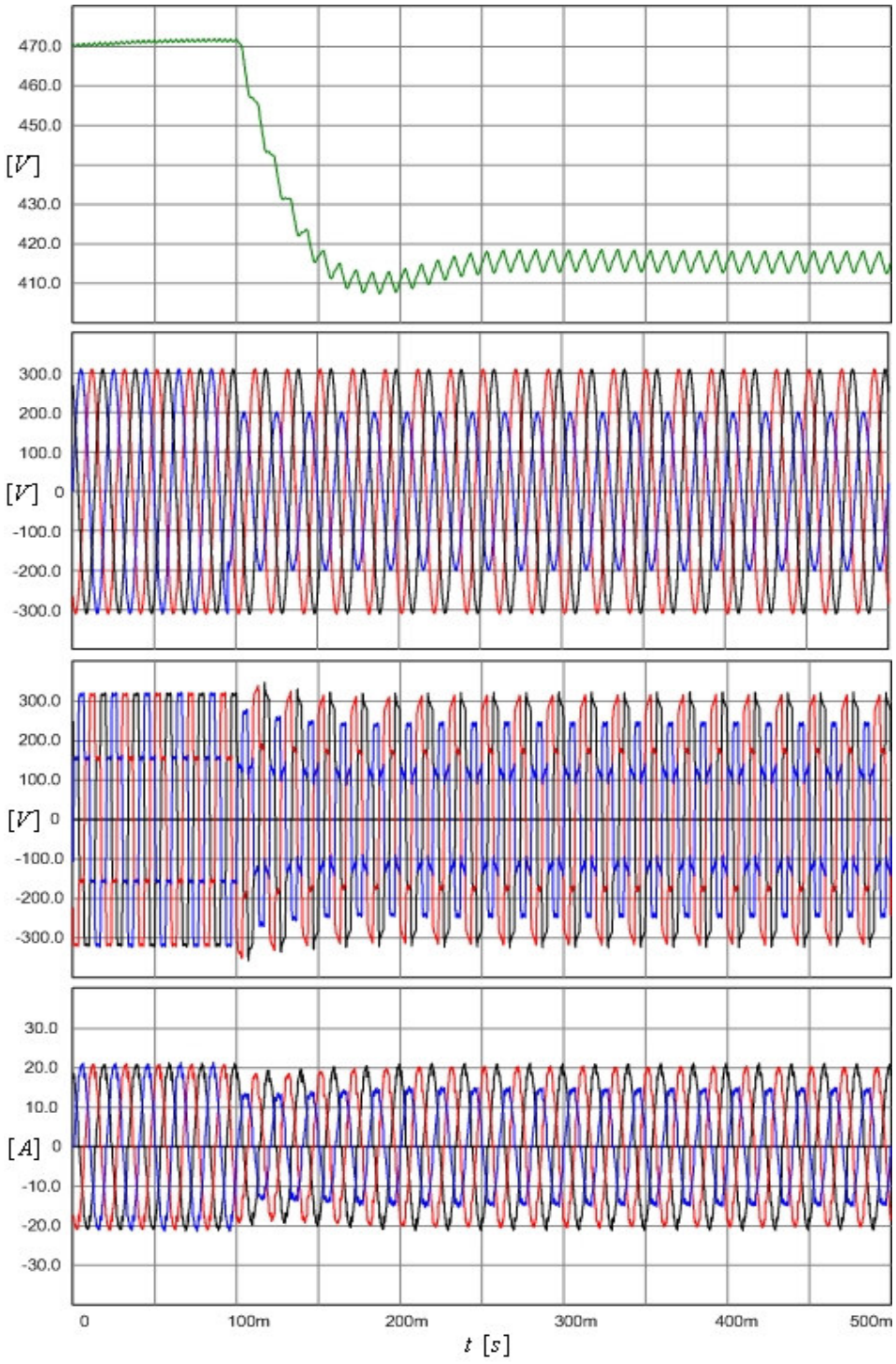



Figure 4.37 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-AVM without FCC).

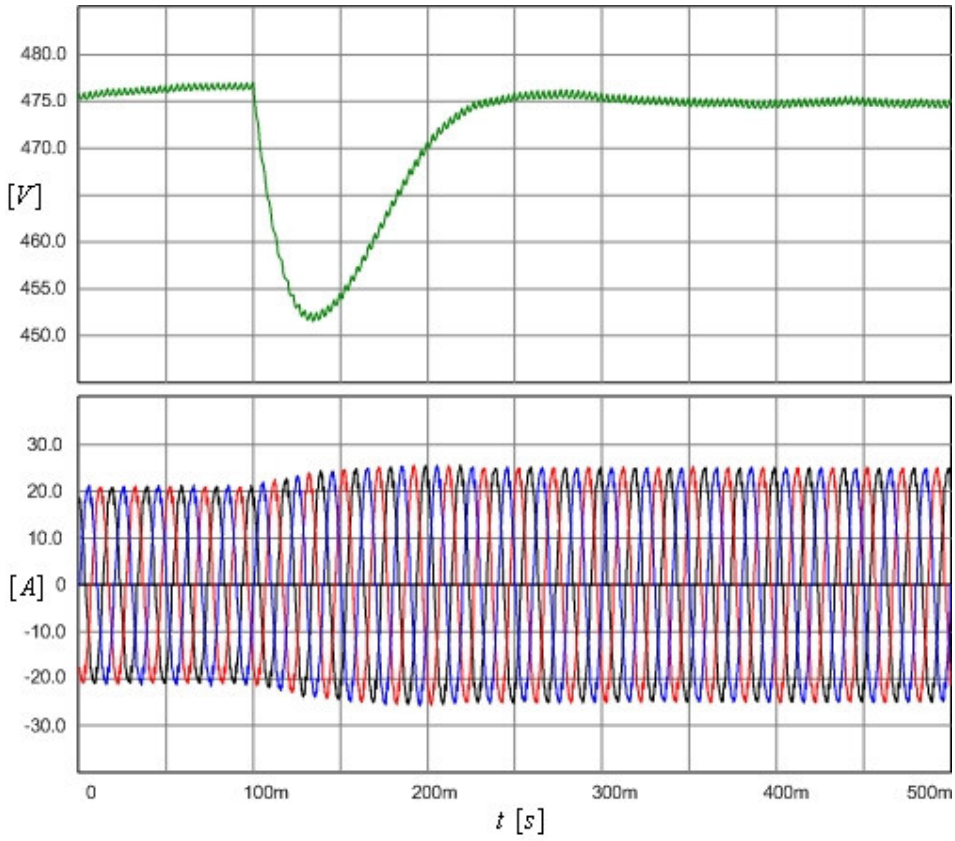



Figure 4.38 Load DC bus voltage (top) and three-phase line currents (bottom) waveforms for 20% load power increase (TPSAF-AVM without FCC).

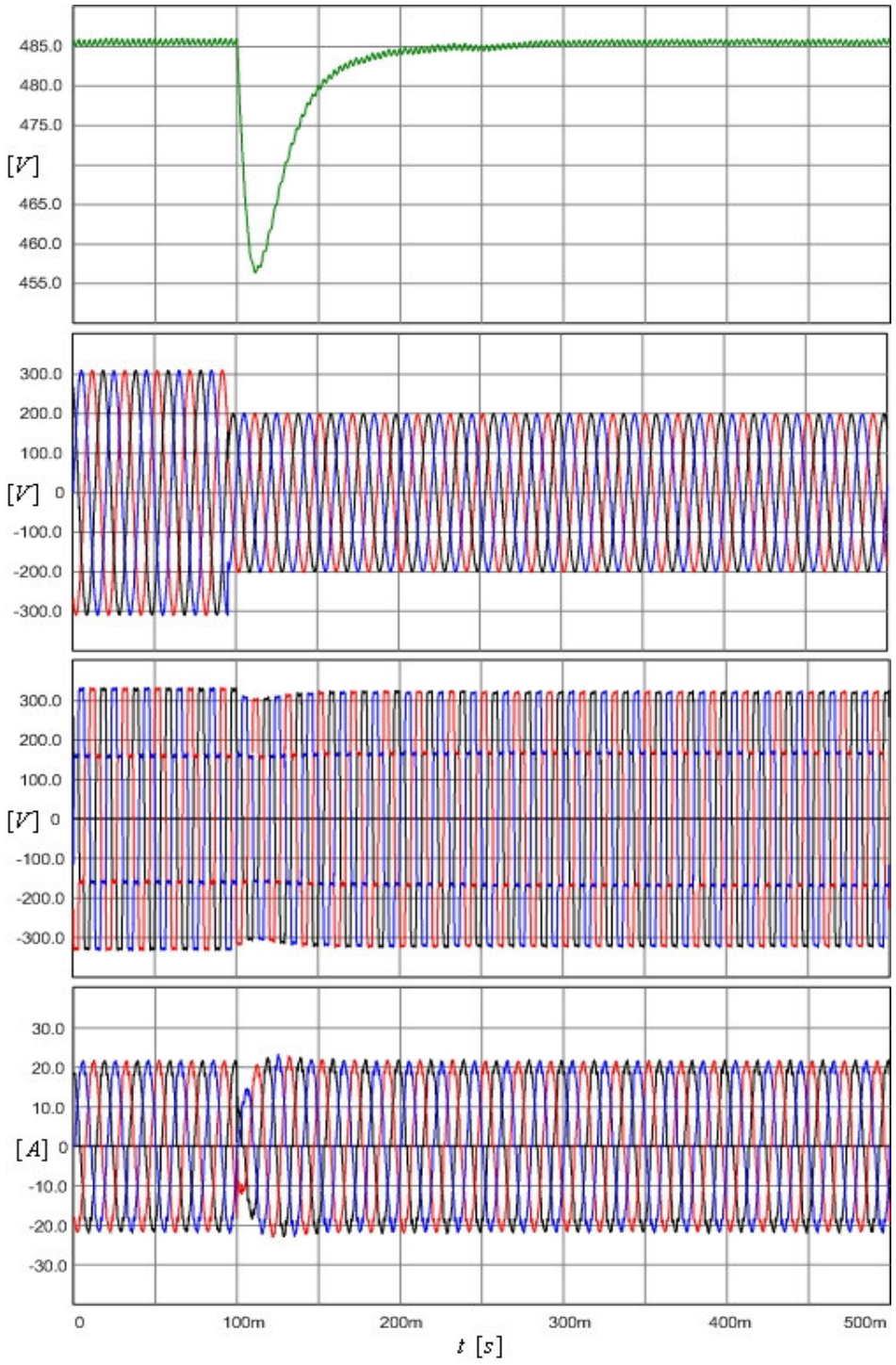



Figure 4.39 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-AVM with only feedback).

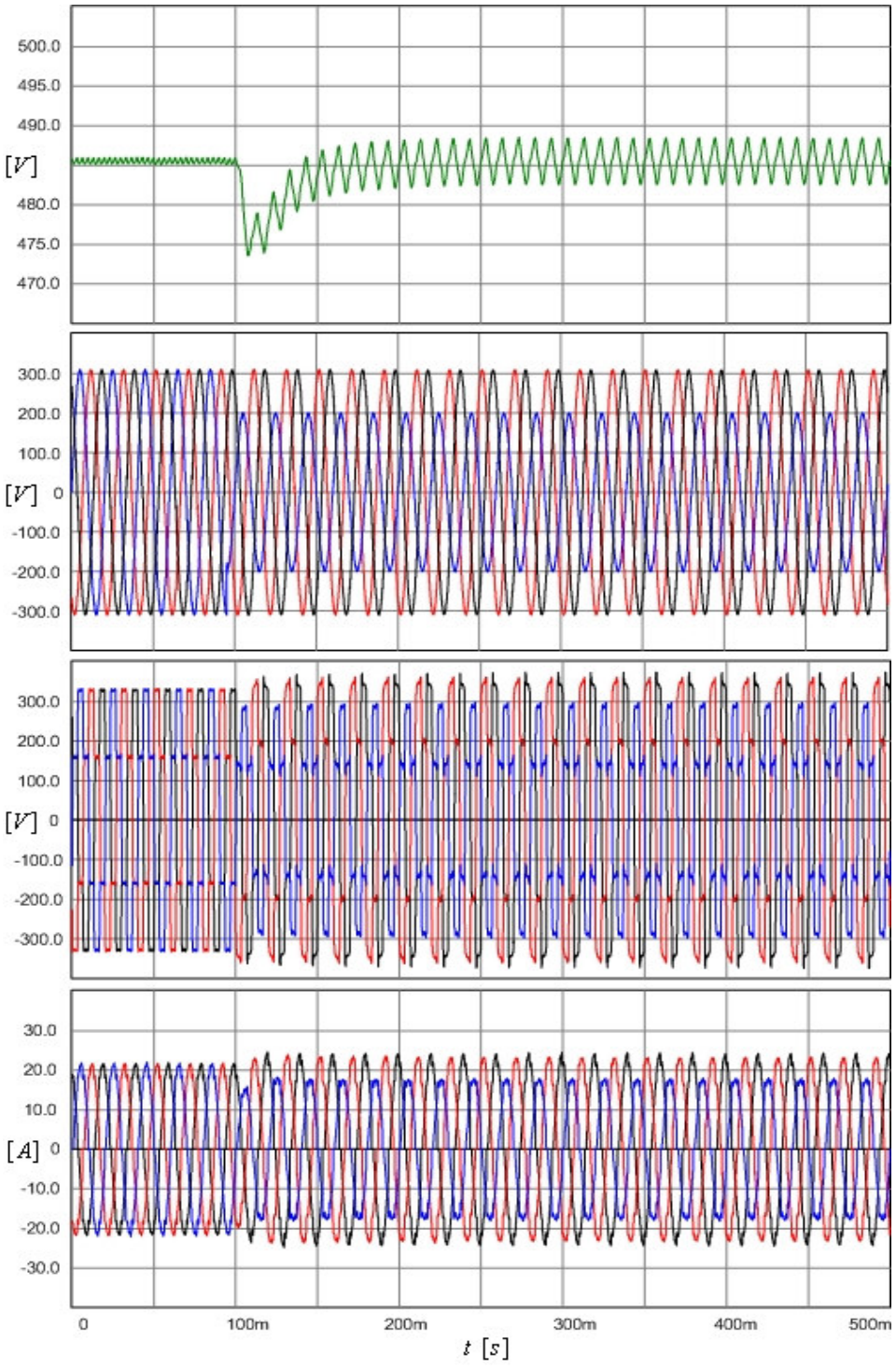



Figure 4.40 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-AVM with only feedback).

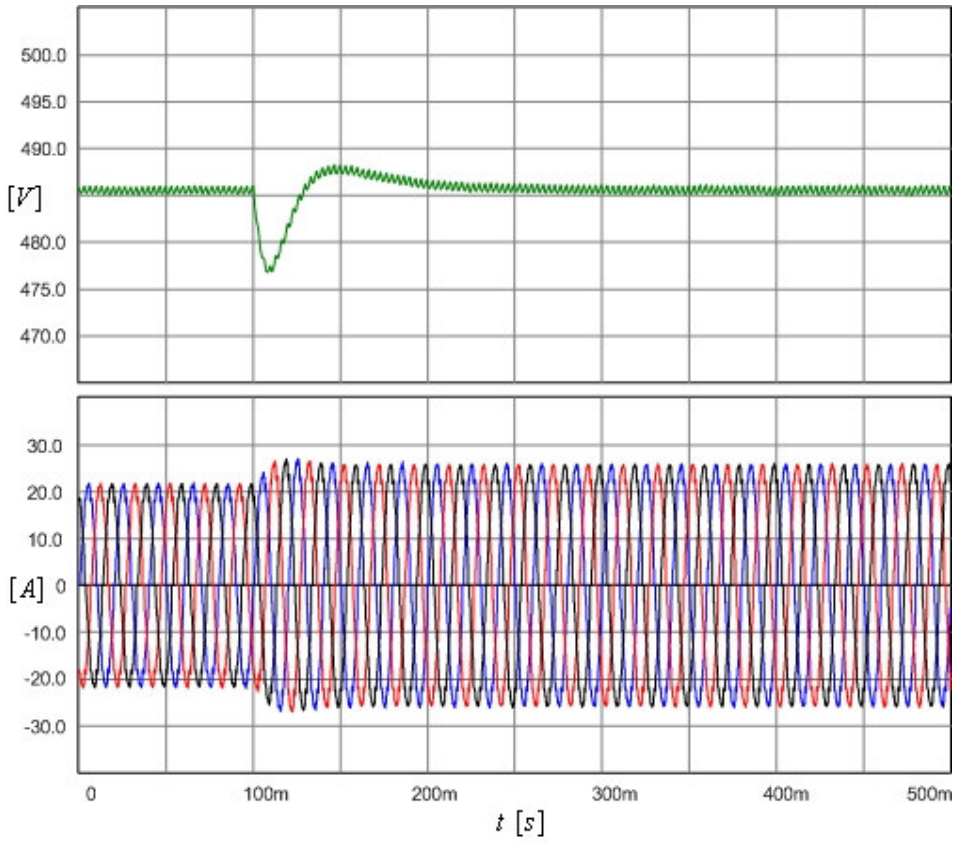



Figure 4.41 Load DC bus voltage (top) and three-phase line currents (bottom) waveforms for 20% load power increase (TPSAF-AVM with only feedback).

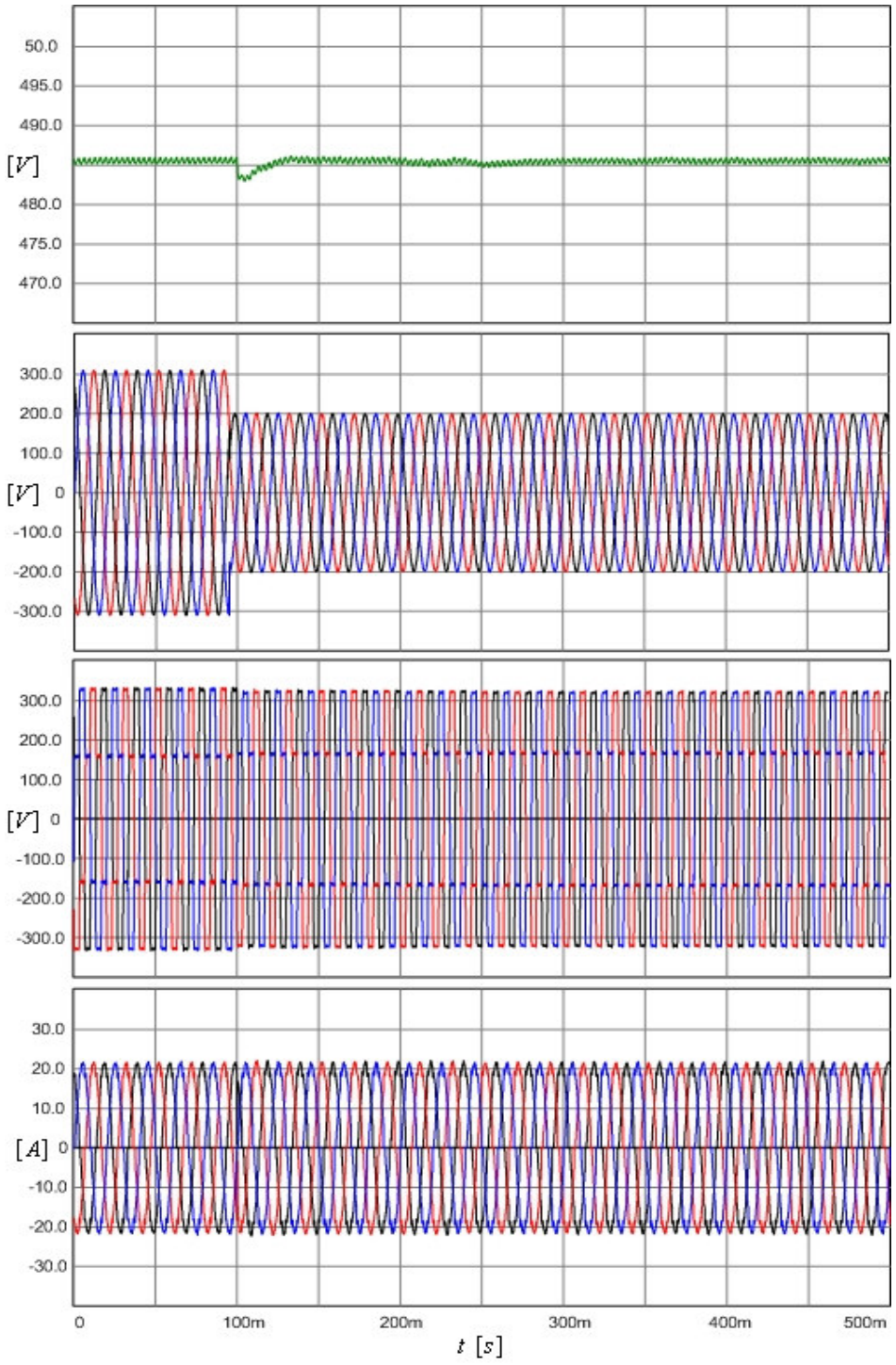



Figure 4.42 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-AVM with feedback & feedforward).

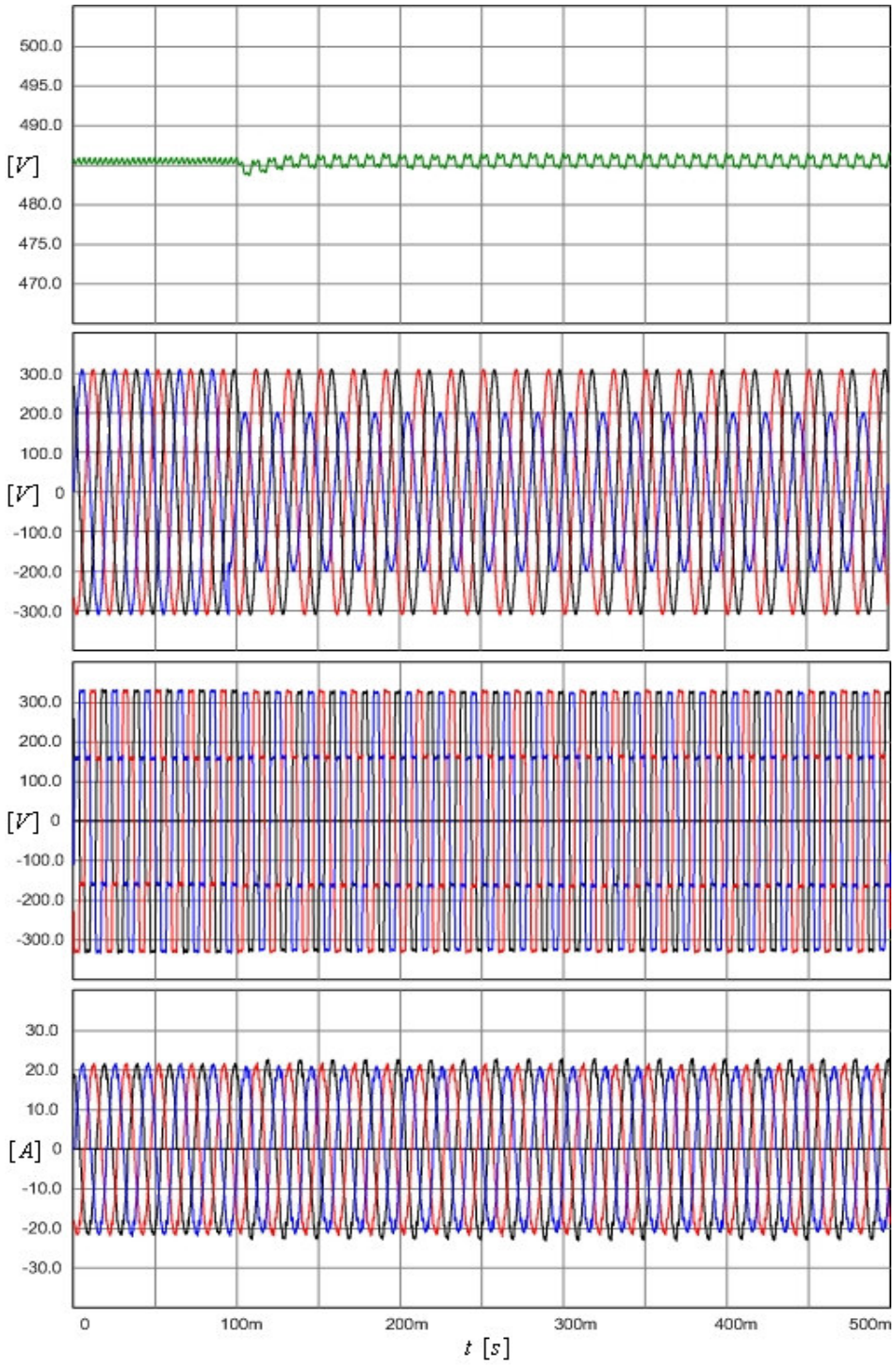



Figure 4.43 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, three-phase utility voltages, three-phase load voltages, and three-phase line currents (TPSAF-AVM with feedback & feedforward).

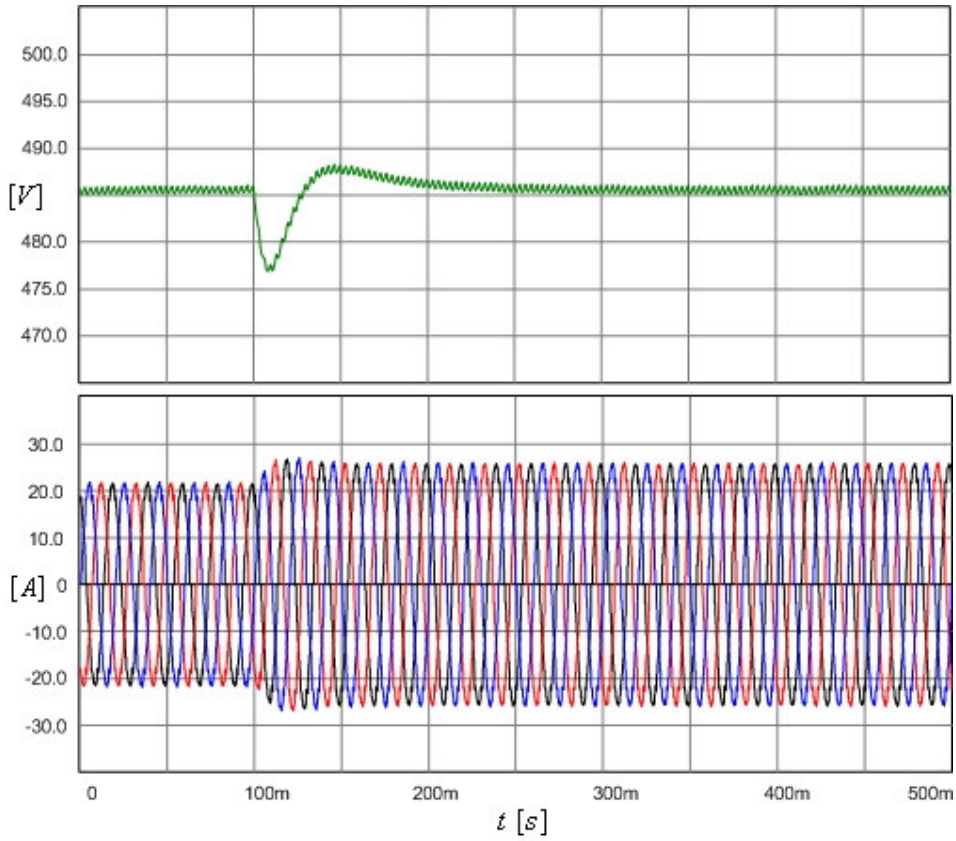



Figure 4.44 Load DC bus voltage (top) and three-phase line currents (bottom) waveforms for 20% load power increase (TPSAF-AVM with feedback & feedforward).

### 4.3.4 Performance Comparison

The harmonic isolation performances of TPSAF at steady-state are shown in Table 4.13. In the table, IEEE 519 limits for harmonic quantities are listed along with those obtained by the TPSAF simulations. The short circuit current of the utility is 1900 A and the load current is 15.1 A (for 10 kW load). Then, the short circuit ratio is 127, which determines the IEEE 519 limits applied. Note that the load current is less than 16 A therefore the same approach on the harmonic limits as discussed in Section 4.2.4 is valid. It is obvious that the performance of the TPSAF using AVM is significantly better than the performance of the TPSAF using CM. Specifically the

current THD improvement of AVM compared to CM is striking as it provides better than 100% improvement over CM. The dominant harmonics are more effectively suppressed with AVM compared to CM while the high frequency components are approximately equal.

In order to compare the dynamic responses of the SAF with the cases discussed, the simulation results are tabulated in Table 4.14. As seen in the table the TPSAF employing AVM is superior to the TPSAF employing CM. It should be also noted that the feedforward controller improves the response of the SAF for voltage sags but not the load dynamics.

Table 4.13 The performance comparison between the harmonic isolation provided by the TPSAF using CM and AVM

| | By-pass Mode | Standby Mode | TPSAF with CM | TPSAF with AVM | IEEE 519 Limits |
|---|---|---|---|---|---|
| $I_1$ (%) | 100.0 | 100.0 | 100.0 | 100.0 | 100.0 |
| $I_5$ (%) | 74.4 | 52.1 | 5.7 | 1.5 | 12.0 |
| $I_7$ (%) | 54.2 | 25.6 | 3.9 | 1.5 | 12.0 |
| $I_{11}$ (%) | 17.1 | 6.6 | 4.1 | 1.8 | 5.5 |
| $I_{13}$ (%) | 7.3 | 5.4 | 2.4 | 1.1 | 5.5 |
| $I_{17}$ (%) | 6.9 | 2.9 | 1.3 | 0.8 | 5.0 |
| $I_{19}$ (%) | 5.3 | 2.2 | 1.3 | 0.8 | 5.0 |
| $I_{23}$ (%) | 2.7 | 1.7 | 1.0 | 0.8 | 2.0 |
| $I_{25}$ (%) | 2.9 | 1.2 | 1.0 | 0.7 | 2.0 |
| $THD_I$ (%) | 94.50 | 58.87 | 9.91 | 3.95 | 15.0 |
| $THD_V$ (%) | 3.21 | 1.73 | 0.93 | 0.60 | 5.0 |
| PF | 0.713 | 0.845 | 0.991 | 0.998 | - |
| $\Delta v_{dc}$ (%) | 2.5 | 1.4 | 0.2 | 0.1 | - |

Table 4.14 The performance comparison between the load voltage regulation provided by the TPSAF using CM and AVM

| | CM | | AVM | |
|---|---|---|---|---|
| | Only Feedback | Feedback & Feedforward | Only Feedback | Feedback & Feedforward |
| $\Delta v_{sag}$ (%) | 10.5 | 0.6 | 6.1 | 0.5 |
| $\Delta t_{sag}$ (ms) | 200 | 0 | 60 | 0 |
| $\Delta v_{dyn}$ (%) | 2.9 | 2.9 | 1.8 | 1.8 |
| $\Delta t_{dyn}$ (ms) | 35 | 35 | 25 | 25 |
| $\Delta v_{neg}$ (%) | 1.2 | 0.4 | 1.2 | 0.3 |

## 4.4 Summary

By means of the simulation results of the detailed system models of the SPSAF and TPSAF compensated systems, it is verified that a SAF is capable of isolating harmonic voltage of V-type nonlinear loads from utility and regulating the load voltage of V-type nonlinear loads against line voltage and load current disturbances. The performance improvement in both harmonic isolation and load voltage regulation by means of the novel AVM instead of CM is demonstrated via the comparison between the simulation results obtained in the SPSAF and TPSAF compensated systems. The usage of AVM provides significant line current THD improvement specifically for the dominant harmonics such that the harmonic isolation of the SAF is nearly perfect. In this section, additionally, the validity of the simplified linear models introduced in Chapter 3 is verified through the comparison between the simulations results of the linear models and the detailed system models. In the next chapter experimental studies will be conducted for the purpose of further verifying the performance of the proposed AVM approach.

# CHAPTER 5

# THE PERFORMANCE ANALYSIS OF 2.5 kW SINGLE-PHASE AND 10 kW THREE-PHASE SERIES ACTIVE FILTER COMPENSATED SYSTEMS VIA EXPERIMENTS

## 5.1 Introduction

In this chapter, experimental studies of Series Active Filters (SAF) applied to single-phase and three-phase V-type nonlinear loads are conducted. The experimental setups of the single-phase and three-phase SAF compensated systems are described. Experiments are conducted in accordance with the cases investigated in Chapter 3 and Chapter 4. The experimental results of harmonic isolation and load voltage regulation performances of the 2.5 kW SPSAF and 10 kW TPSAF compensated systems are evaluated with respect to the two load voltage harmonic/fundamental extraction methods, the Conventional Method (CM) and the novel Absolute Value Method (AVM). Via the experiments, the theory and the simulations are validated. The experimental performance comparison between the SAF compensated systems using CM and AVM is done and the latter's superiority is proven.

## 5.2 Experimental Setup

The power circuits of the SAF systems are realized as single-phase and three-phase circuits in laboratory in accordance with the designs given in Chapter 2. The VSI unit is composed of intelligent power modules (IPM), which have embedded gate drive and protection circuits (optically isolated). In this study, Mitsubishi PM75DSA120

dual pack IPMs, which have IGBTs that are rated as 75 A 1200 V, 20 kHz are utilized. In order to power up the internal gate drive and protection circuits of the IPMs, a Powerex M57140-01 isolated DC/DC converter, which converts 20 V to 4-channel 15 V, is used per VSI.

These power circuits are controlled via a digital signal processor (DSP) platform and analog circuits as shown in Figure 5.1 in single-phase representation. The DSP platform, which is manufactured by Spectrum Digital under the eZdsp F2808 trademark, includes a TMS320F2808 DSP and its peripheral interface circuits. The DSP runs at 100 MHz, has a 16-channel 12-bit analog-to-digital converter (ADC) with the maximum conversion rate of 12.5 MHz per channel, and has a 12-channel PWM unit with programmable deadtime.

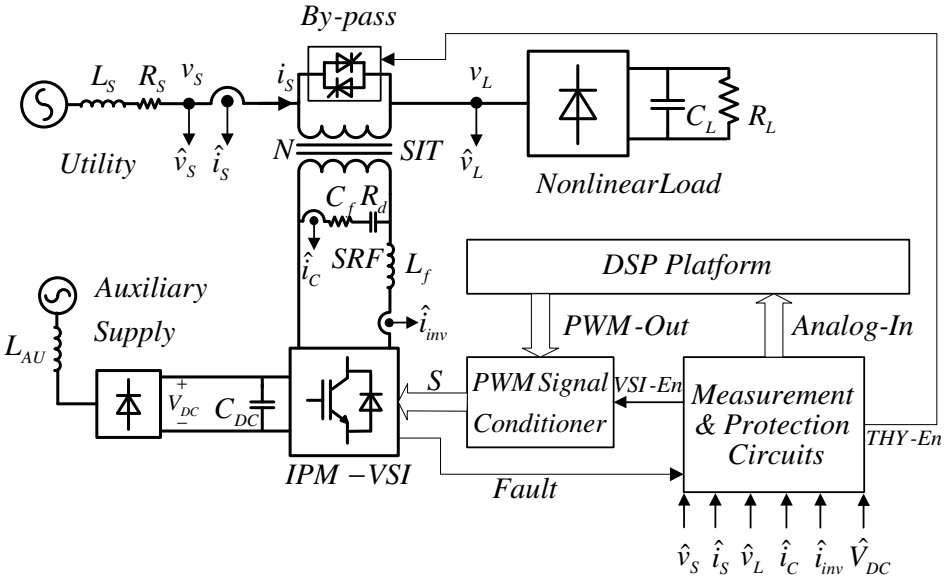



Figure 5.1 The experimental setup of the SAF compensated system in single-phase representation.

The analog circuits are for measurement, protection, and PWM signal conditioning, which are described as follows. First, the measurement circuits measure, scale, and condition the signals used in the control algorithm of SAF realized in the DSP platform, which are the line voltage ($v_S$), the line current ($i_S$), the load voltage ($v_L$), the capacitor current ($i_C$), and the VSI DC bus voltage ($V_{DC}$) and the signal used in the protection of SAF, which is the VSI current ($i_{inv}$). Next, the protection circuits detect the inverter overcurrent fault condition from $i_{inv}$ and IPM fault conditions from the fault signals generated by IPMs under the shortcircuit, overcurrent, overtemperature, low gate drive supply voltage conditions. After detection of any fault condition, the protection circuits disable the VSI(s) by means of forcing the IPMs to operate in stand-by mode and enable the by-pass thyristors in order to disconnect SAF from the utility-load pair. Lastly, the PWM logic output signals of the DSP are isolated and conditioned via the PWM signal conditioner circuit composed of level shifters and optoisolators such that these PWM signals are compatible with the IPM.

The control algorithm realized in the DSP platform is illustrated in the flow chart in Figure 5.2. The flow of the algorithm can be described as follows. After the initialization of the variables used in the DSP code, the counter of the PWM block of DSP is reset. Then, the signals used in the low bandwidth control loops (other than HIC and RDC) are read by the ADC block and these signals are used in their corresponding control method. In order to realize the near-next-state sampling by the nearness of $T_n$ (5μs), after the counter reaches the beginning of the last $T_n$ part of the sampling period $T_S$ (25μs), $i_S$ and $i_C$ are read via ADC and used in the HIC and RDC units. Hence, the delay time due to sampling of the signals is significantly reduced. Next, the reference voltage for each VSI is generated and the PWM block of DSP produces on/off signals with deadtime for each IPM. When the PWM counter reaches the $T_S$, the algorithm is restarted by the counter reset.

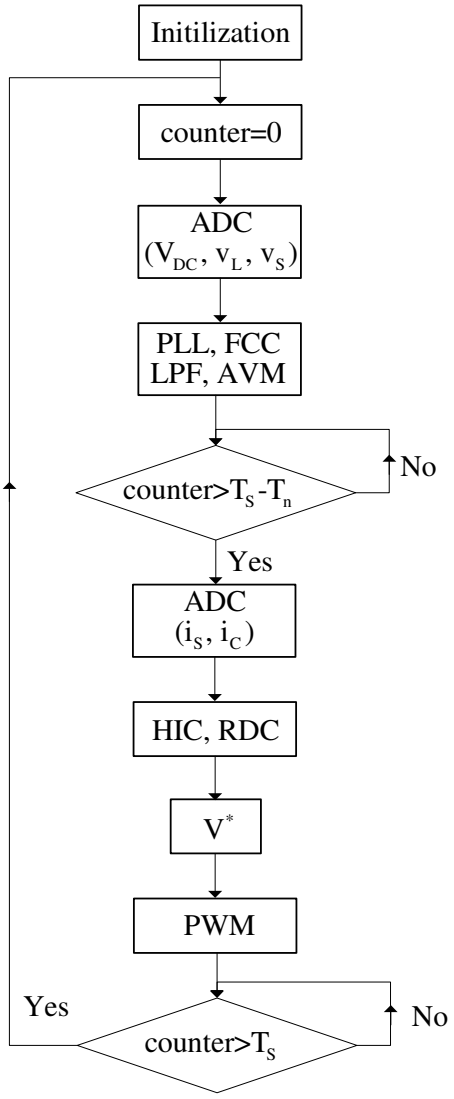



Figure 5.2 The control algorithm flow-chart utilized in the DSP platform.

The experimental performances in harmonic isolation and load voltage regulation of the SAF compensated systems using CM and AVM are reported under the voltage sag and the load power increase as done in Chapter 4. Nevertheless, instantaneous voltage sags could not be realized in the laboratory. Instead, voltage sags with approximately 200 ms fall time for 35% sag are used by means of a variac. Moreover, the load power increase, which is used as 20% of the rated load power, is realized as the increase of almost 25% due to the load increment restriction in the resistive load

bank available. The experimental waveforms are collected by LeCroy Waverunner 6050A oscilloscope and the harmonic analyses are done by Fluke 43 B harmonic analyzer.

### 5.3 SPSAF

The detailed power circuit of the SPSAF compensated system is illustrated in Figure 5.3 and the SPSAF laboratory setup is shown in Figure 5.4. The parameters of the power units are listed in Table 5.1. The short-circuit tests, in order to determine the parameters of SIT listed in the table, are conducted at 250 Hz in order to take more accurate measurements considering the leakage inductances of SIT is significantly low.

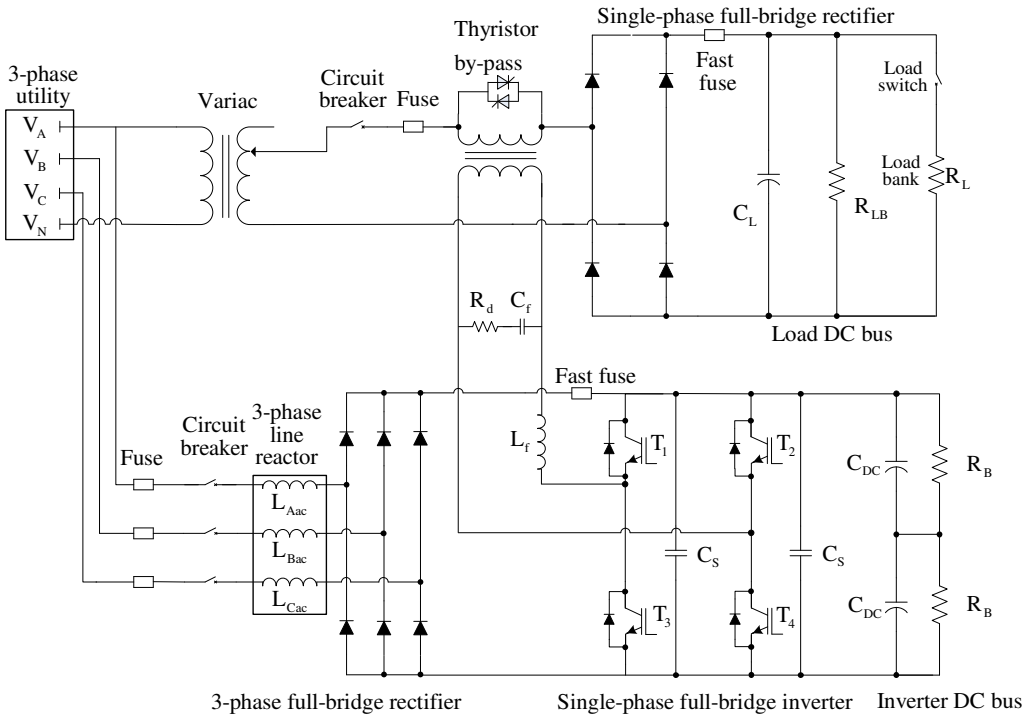



Figure 5.3 The detailed power circuit of the 2.5 kW SPSAF compensated system in the laboratory.

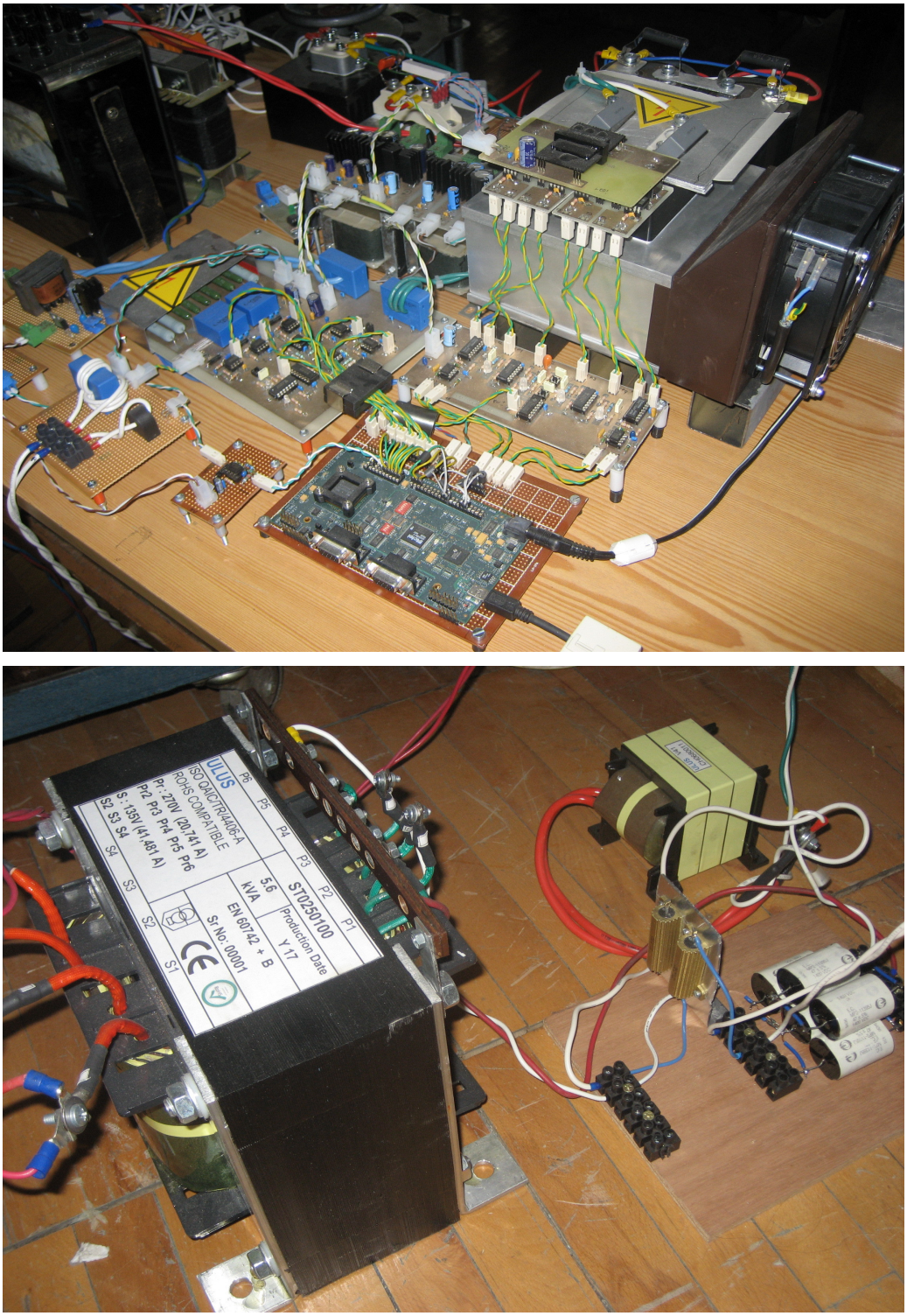



Figure 5.4 Laboratory setup of the SPSAF system; The VSI, the analog and digital circuits (top), the SIT and SRF (bottom).

Table 5.1 The experimental parameters of the SPSAF system

| | | |
|---|---|---|
| $E_S$ | Utility voltage | 220 $V_{rms}$ (50 Hz) |
| $L_S$ | Utility leakage inductance | 200 µH |
| $R_S$ | Utility resistance | 100 mΩ |
| $V_{L,DC}$ | Rated DC bus voltage of VSI | 245 V |
| $C_L$ | Load capacitance | 2.2 mF |
| $R_L$ | Load resistance | 24 Ω (2.5 kW) |
| $R_{LB}$ | Load DC bus bleeding resistance | 22 kΩ |
| $L_f$ | SRF inductance | 1.8 mH |
| $C_f$ | SRF capacitance | 2.35 µF |
| $R_f$ | Resistance of the SRF inductance | 300 mΩ |
| $R_d$ | SRF damping resistance | 5.6 Ω |
| $V_{DC}$ | Rated DC bus voltage of VSI | 520 V |
| $C_{DC}$ | DC bus capacitance of VSI | 4.7 mF |
| $C_S$ | DC bus snubber capacitance of VSI | 220 nF |
| $R_B$ | DC bus bleeding resistance of VSI | 30 kΩ |
| $E_{AU}$ | Supply voltage of auxiliary rectifier | 380 $V_{rms}$ (50 Hz) |
| $L_{AU}$ | Line inductance of auxiliary rectifier | 1.43 mH |
| $L_1$ | Primary side leakage inductance of SIT | 40 µH |
| $L_2$ | Secondary side leakage inductance of SIT | 10 µH |
| $R_1$ | Primary side copper resistance of SIT | 140 mΩ |
| $R_2$ | Secondary side copper resistance of SIT | 35 mΩ |
| N | Turns-ratio of SIT ($N_1$:$N_2$) | 2 |
| $f_{PWM}$ | PWM frequency | 20 kHz |
| $T_S$ | Sampling time (Double update) | 25 µs |
| $T_n$ | Near-next-state sampling time | 5 µs |
| $T_{dt}$ | Deadtime of the IGBT switches | 3.5 µs |

### 5.3.1 Experiment of The SPSAF Compensated System Using CM

With CM for the load voltage signal decomposition, experimental results are reported with respect to harmonic isolation and load voltage regulation. The

controller parameters used in the experiments are given in the Table 5.2. The parameters of harmonic isolation controller (HIC), resonance damping controller (RDC), and fundamental component controller (FCC) are the same as those found and utilized in Chapter 4.

Table 5.2 The experimental controller parameters of the SPSAF using CM

| | | |
|---|---|---|
| $K_{hi}$ | HIC gain for line current | 10 |
| $K_{hv}$ | HIC gain for load voltage | 0.9 |
| $f_{cih}$ | HIC cut-off frequency for line current | 5 Hz |
| $f_{cvh}$ | HIC cut-off frequency for load voltage | 5 Hz |
| $K_d$ | RDC gain | 25 |
| $K_{Pv}$ | FCC proportional gain | 1.5 |
| $K_{Iv}$ | FCC integral gain | 40 |
| $f_{cv1}$ | FCC cut-off frequency for load voltage | 10 Hz |
| $f_{cvff}$ | FCC LPF cut-off frequency for line voltage | 500 Hz |
| $a_v$ | Constant of phase-lead compensator in FCC | 4.6 |
| $T_v$ | Time constant of phase-lead compensator in FCC | 10 ms |

#### 5.3.1.1 Harmonic Isolation

When there is no harmonic isolation provided by SPSAF, the harmonic distortion of the V-type single-phase nonlinear load is investigated for the two modes as discussed in Chapter 4. In the by-pass mode and the standby mode, the waveforms of line voltage, load voltage, and line current are as shown in Figure 5.5 and Figure 5.6. The total harmonic distortions of line current ($THD_I$) are very large for both modes (85.7% and 79.4%). Consequently, the distortions of the line voltages are practically equal for both modes ($THD_V$ = 5.1%) and power factor (PF) is very low (0.727 and 0.757). The inconsistency between $THD_V$ values of the simulations and the experiments are due to the distorted utility voltage at the laboratory with $THD_V$ = 2-2.5% at no load (mostly $5^{th}$ harmonic frequency). The cause of the voltage distortion at the laboratory is partially the computer loads in the facility and partially the

insufficient power line cable capacity at the laboratory. Thus, throughout the experiments the source of voltage harmonic is not only the V-type load, but also the utility line. The SAF efficiency of isolating both is well tested in the laboratory environment.

The harmonic isolation provided by SPSAF alleviates the harmonic distortion on the line current and the voltage as seen in Figure 5.7 such that $THD_I$ = 15.8%, $THD_V$ = 2.6%, and PF = 0.965. However, the line current is still distorted and in order to improve the harmonic isolation either $K_{hi}$ should be increased (bounded by the stability of the system) or $K_{hv}$ should be increased using high accuracy load voltage harmonic extraction method (bounded with the performance of CM). As an additional effect of the harmonic isolation controller, the load DC bus voltage ripple ($\Delta v_{dc}$) decreases to 6.3% as seen in Figure 5.8 whereas $\Delta v_{dc}$ = 13.8% for the by-pass mode and $\Delta v_{dc}$ = 13.1% for the standby mode. This decrease is advantageous in the selection of DC bus capacitor.

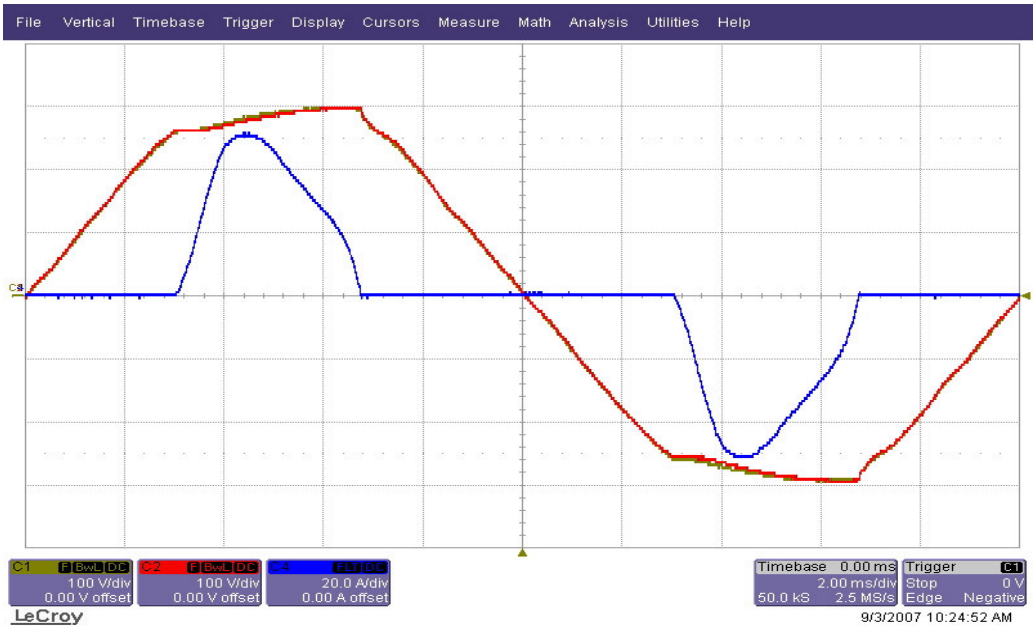



Figure 5.5 Uncompensated single-phase system line voltage (yellow), load voltage (red), and line current (blue) waveforms in by-pass mode.

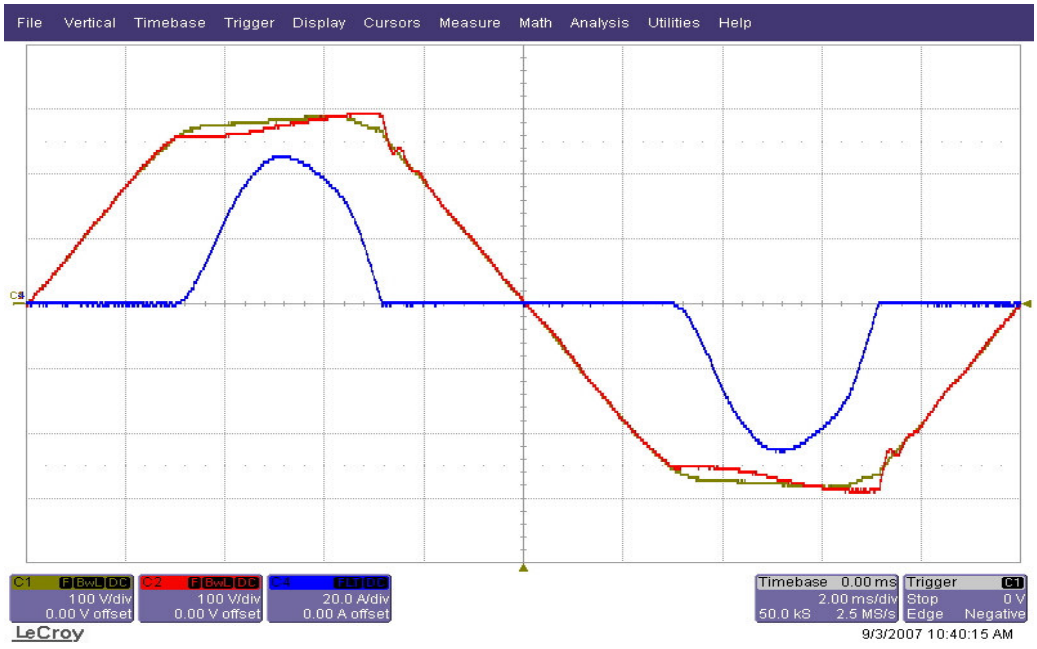



Figure 5.6 Uncompensated single-phase system line voltage (yellow), load voltage (red), and line current (blue) waveforms in standby mode.

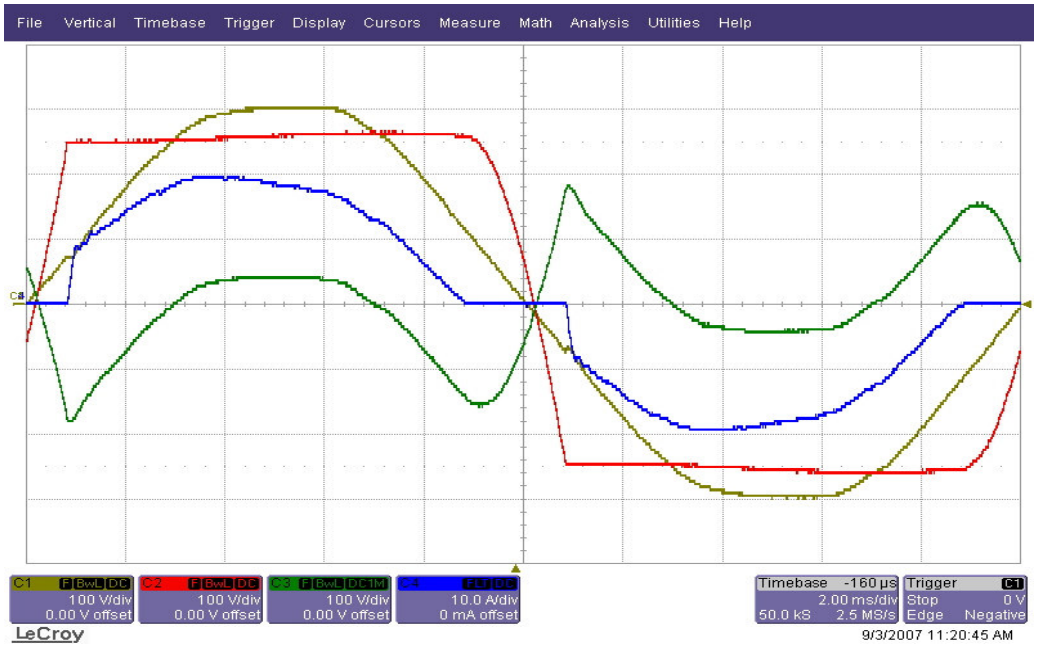



Figure 5.7 Line voltage (yellow), load voltage (red), SAF voltage (green), and line current (blue) waveforms (SPSAF-CM).

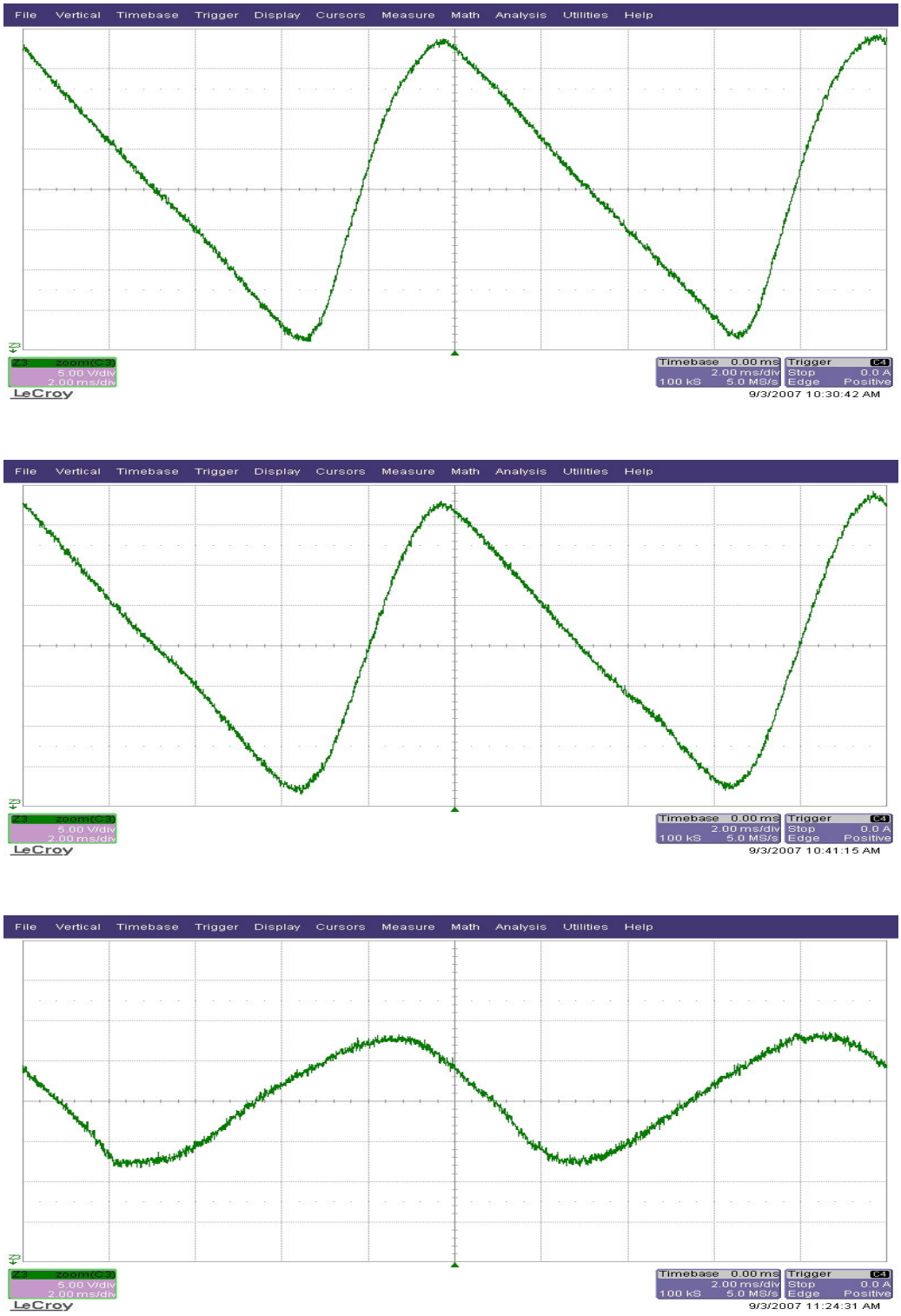



Figure 5.8 Load DC bus ripple voltage waveforms; (top) by-pass mode, (middle) standby mode, and (bottom) HIC (SPSAF-CM).

#### 5.3.1.2 Load Voltage Regulation

When the fundamental component controller (FCC) of SPSAF does not work, the responses of the SPSAF compensated system with only HIC to 35% voltage sag and 20% load power increase are shown in Figure 5.9 and Figure 5.10, respectively. In the first figure, load DC bus and load voltages drop along with the line voltage. In the second figure, the maximum voltage drop on the load DC bus voltage ($\Delta v_{dyn}$) is 10.5% and the settling time ($\Delta t_{dyn}$) is 150 ms.

The SPSAF compensated system responses to the disturbances discussed are improved by means of FCC as follows. With only feedback controller of FCC functioning (only feedback), the load DC bus voltage is regulated against the sag such that the maximum voltage drop of the load DC bus voltage during the sag ($\Delta v_{sag}$) is 3.1% and the settling time of the response to the sag ($\Delta t_{sag}$) is 300 ms as shown in Figure 5.11. The response to the load dynamic is improved as shown in Figure 5.12 such that $\Delta v_{dyn}$ = 4.1% and $\Delta t_{dyn}$ = 50 ms, which is better than the response without FCC.

The experimental results with the addition of the feedforward controller of FCC to the feedback controller under the disturbance conditions are given in Figure 5.13 and Figure 5.14. As seen in the figures, the immunity of the load voltage to the line voltage sag is increased such that $\Delta v_{sag}$ and $\Delta t_{sag}$ are negligibly small while the response of the SPSAF system to the load power increase is the same as the response in the feedback controller because the load power increase hardly affects the line voltage.

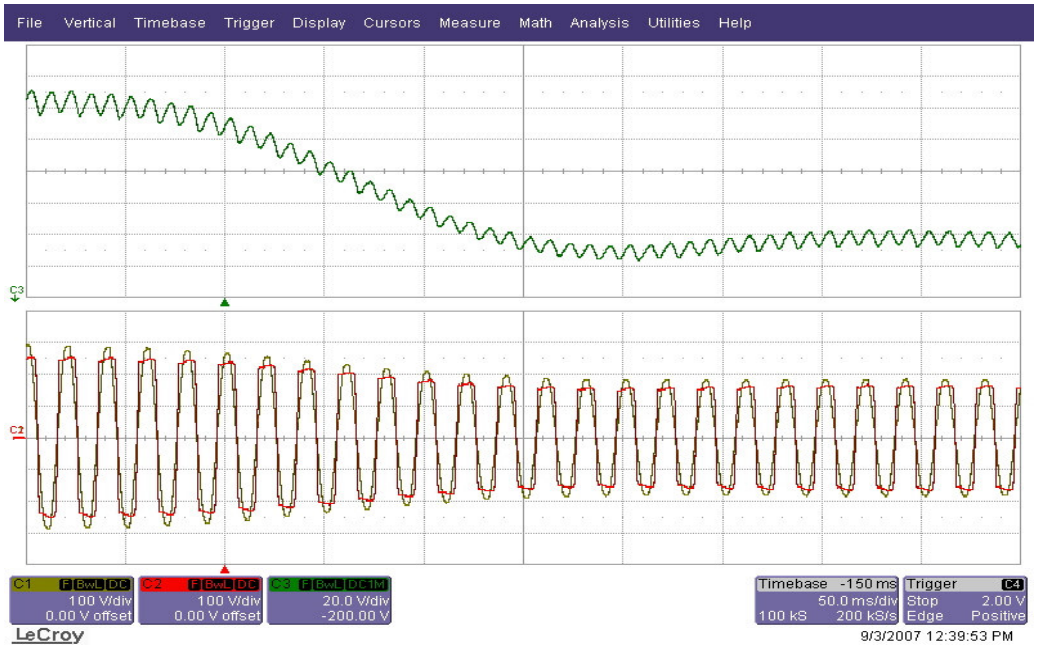



Figure 5.9 Load DC bus voltage (green, top), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-CM without FCC).

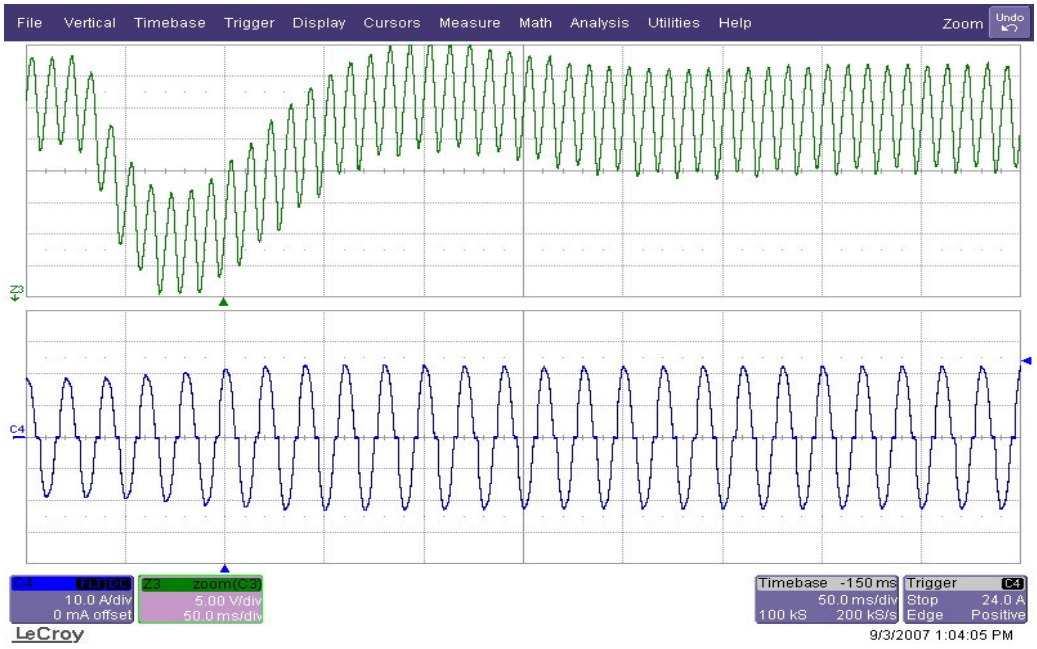



Figure 5.10 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (SPSAF-CM without FCC).

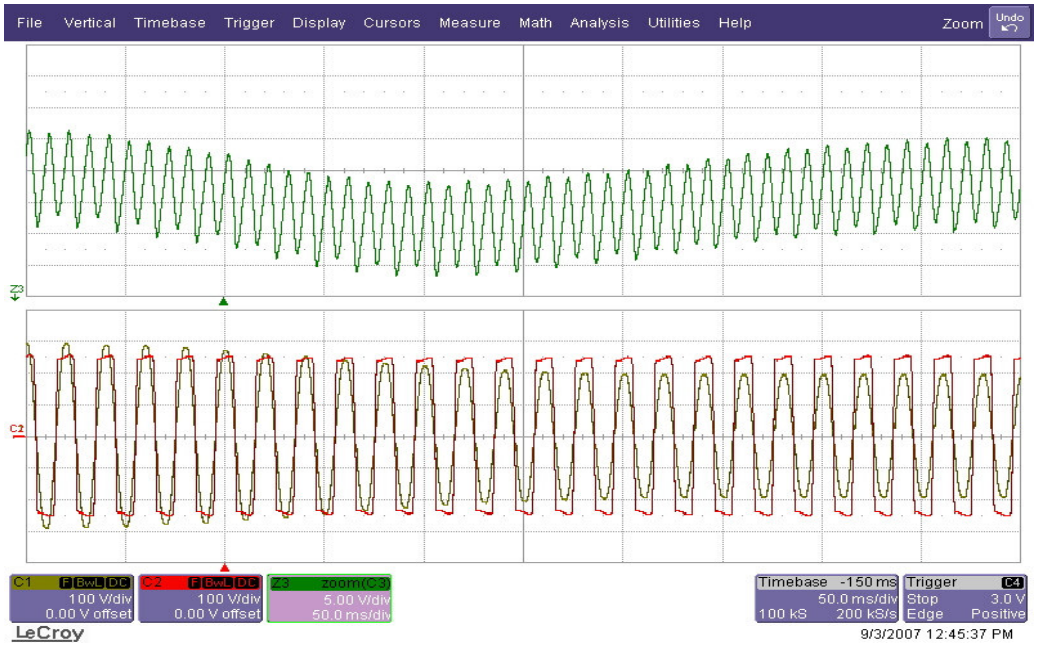



Figure 5.11 Load DC bus voltage (green, top), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-CM with feedback).

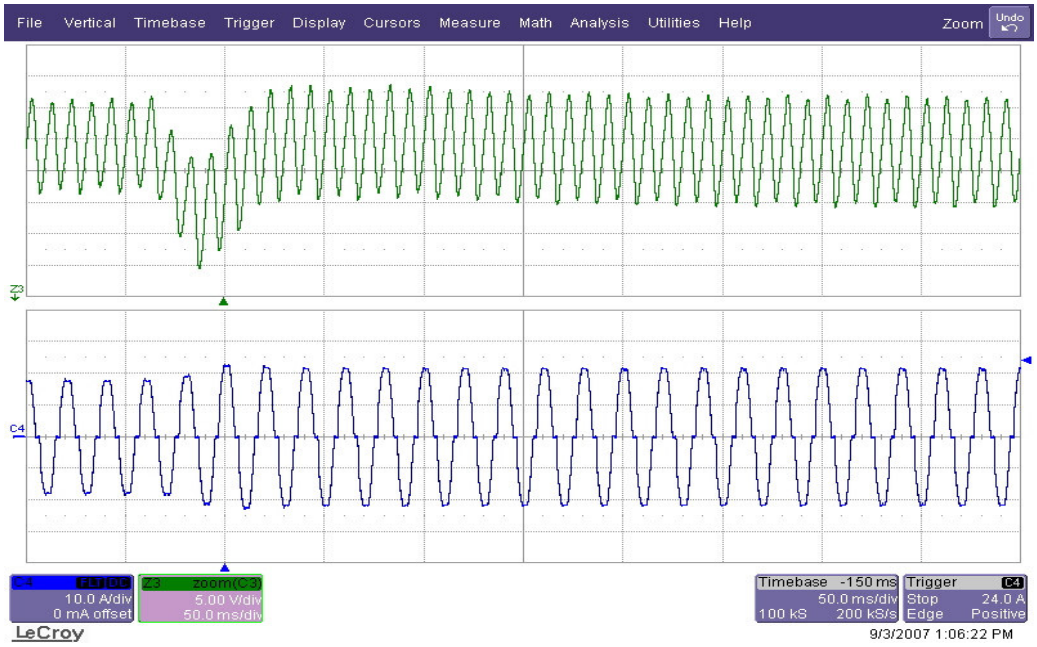



Figure 5.12 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (SPSAF-CM with feedback).

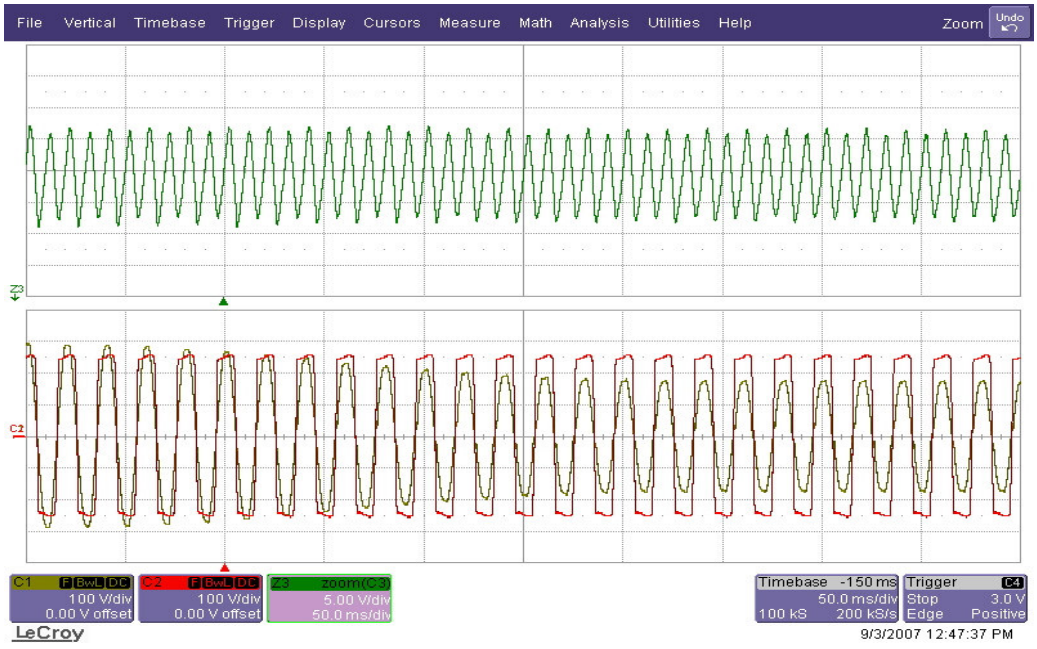



Figure 5.13 Load DC bus voltage (green, top), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-CM with feedback & feedforward).

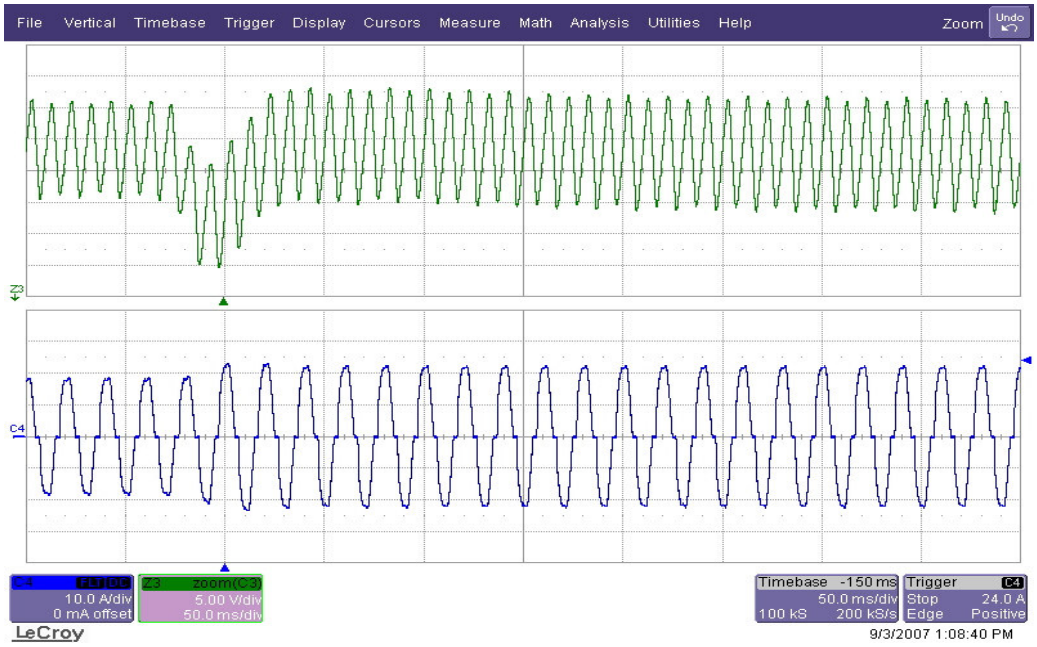



Figure 5.14 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (SPSAF-CM with feedback & feedforward).

### 5.3.2 Experiment of the SPSAF Compensated System Using AVM

The controller parameters used in the experiments of SPSAF using AVM are given in the Table 5.3. The experiments are conducted in the same manner as the CM case.

Table 5.3 The experimental controller parameters of the SPSAF using AVM

| | | |
|---|---|---|
| $K_{hi}$ | HIC gain for line current | 10 |
| $K_{hv}$ | HIC gain for load voltage | 1 |
| $f_{cih}$ | HIC cut-off frequency for line current | 5 Hz |
| $K_d$ | RDC gain | 25 |
| $T_r$ | AVM rise time for load voltage synthesis | 0.4 ms |
| $T_\theta$ | AVM compensation time for phase angle delay | 200 μs |
| $K_{Pv}$ | FCC proportional gain | 1.5 |
| $K_{Iv}$ | FCC integral gain | 40 |
| $f_{cvff}$ | FCC LPF cut-off frequency for line voltage | 500 Hz |
| $f_{c4th}$ | AVM resonant filter frequency | 200 Hz |
| $f_{cvf}$ | AVM LPF cut-off frequency | 500 Hz |

#### 5.3.2.1 Harmonic Isolation

The harmonic isolation performance by means of AVM is significantly improved with respect to the CM case as seen in Figure 5.15 such that AVM provides more accurate load voltage harmonic reference signal than CM does. The harmonic isolation performance is as follows; $THD_I$ = 6.6%, $THD_V$ = 2.5%, and PF = 0.998. Also, $\Delta v_{dc}$ becomes 5.2% as shown in Figure 5.16.

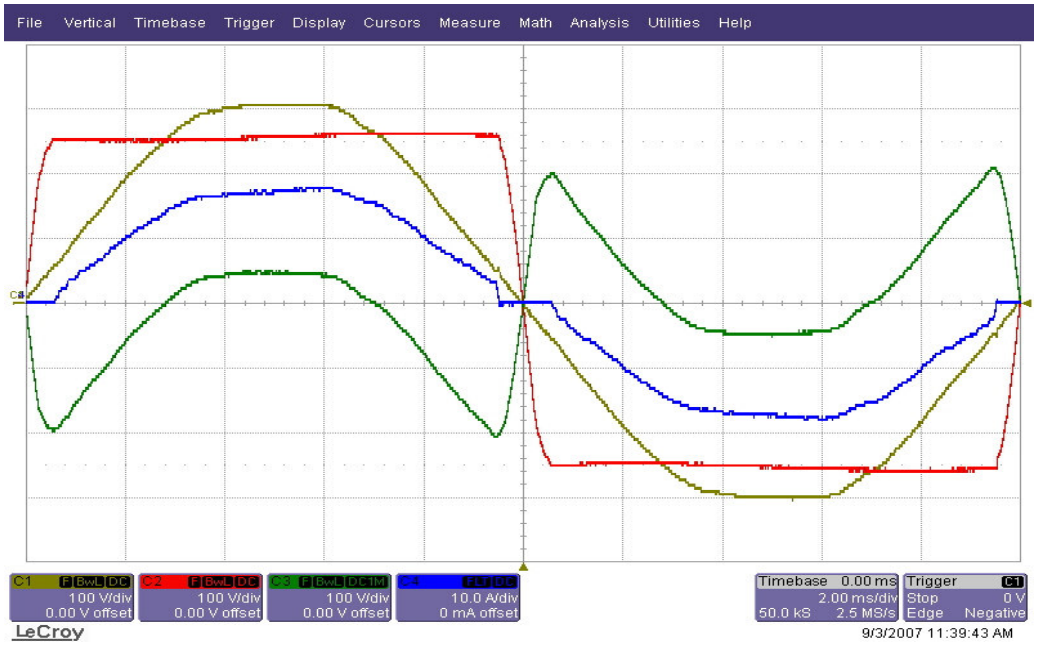



Figure 5.15 Line voltage (yellow), load voltage (red), SAF voltage (green), and line current (blue) waveforms (SPSAF-AVM).

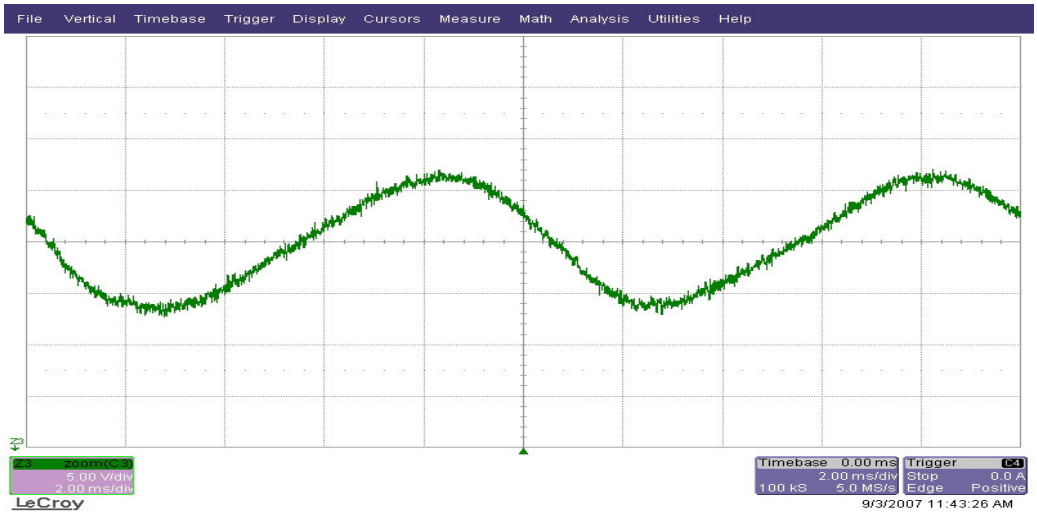



Figure 5.16 Load DC bus voltage ripple waveform (SPSAF-AVM).

#### 5.3.2.2 Load Voltage Regulation

Without FCC, the responses of the SPSAF system with only HIC to 35% voltage sag and 20% load power increase are shown in Figure 5.17 and Figure 5.18, respectively. In the first figure, there is no regulation such that load DC bus and load voltages drop along with line voltage. In the second figure, the response is such that $\Delta v_{dyn}$ is 7.3 % and $\Delta t_{dyn}$ is 125 ms.

The SPSAF system responses to the disturbances discussed are improved by means of FCC as follows. With only feedback controller of FCC functioning, the response to the voltage sag is such that $\Delta v_{sag}$ is 1.0% and $\Delta t_{sag}$ is practically zero as shown in Figure 5.19. The response to the load power increase improves such that $\Delta v_{dyn}$ = 2.0% and $\Delta t_{dyn}$ = 20 ms as shown in Figure 5.20.

The experimental results with the addition of the feedforward controller of FCC to the feedback controller are given in Figure 5.21 and Figure 5.22. As seen in the figures, the immunity of the load voltage to the line voltage sag is increased such that $\Delta v_{sag}$ and $\Delta t_{sag}$ are negligibly small while the response to the load power increase is the same as the response in the only feedback controller case.

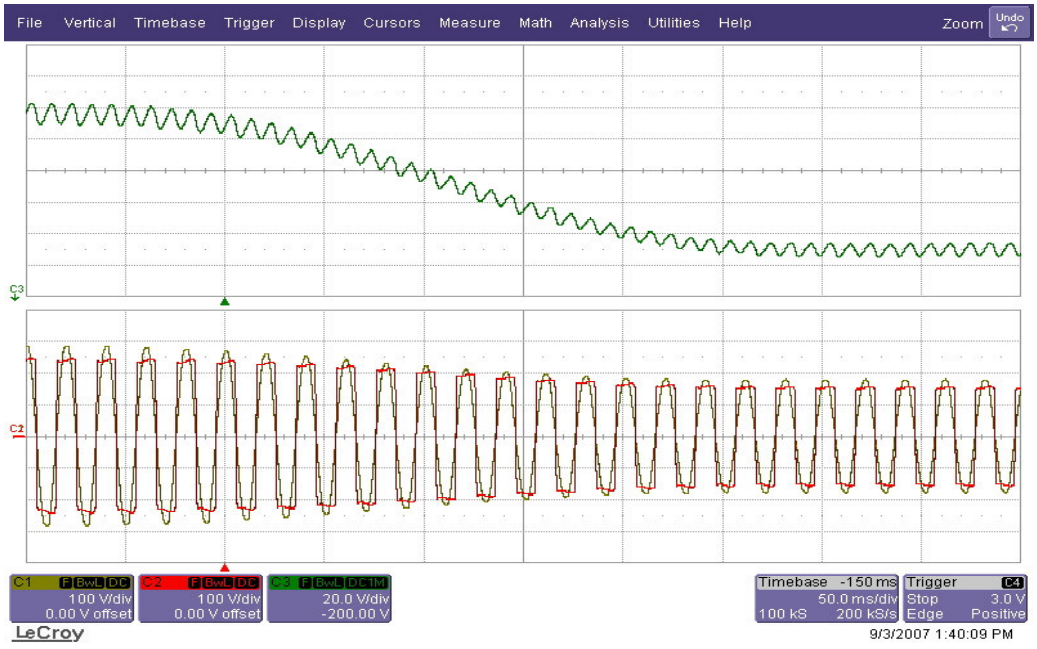



Figure 5.17 Load DC bus voltage (green, top), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-AVM without FCC).

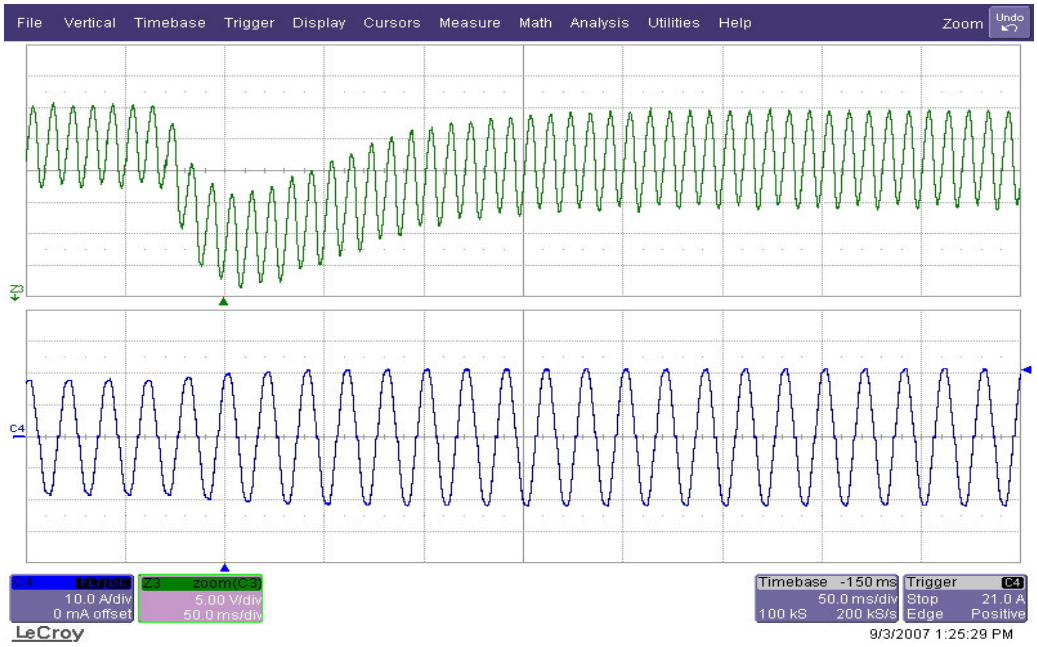



Figure 5.18 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (SPSAF-AVM without FCC).

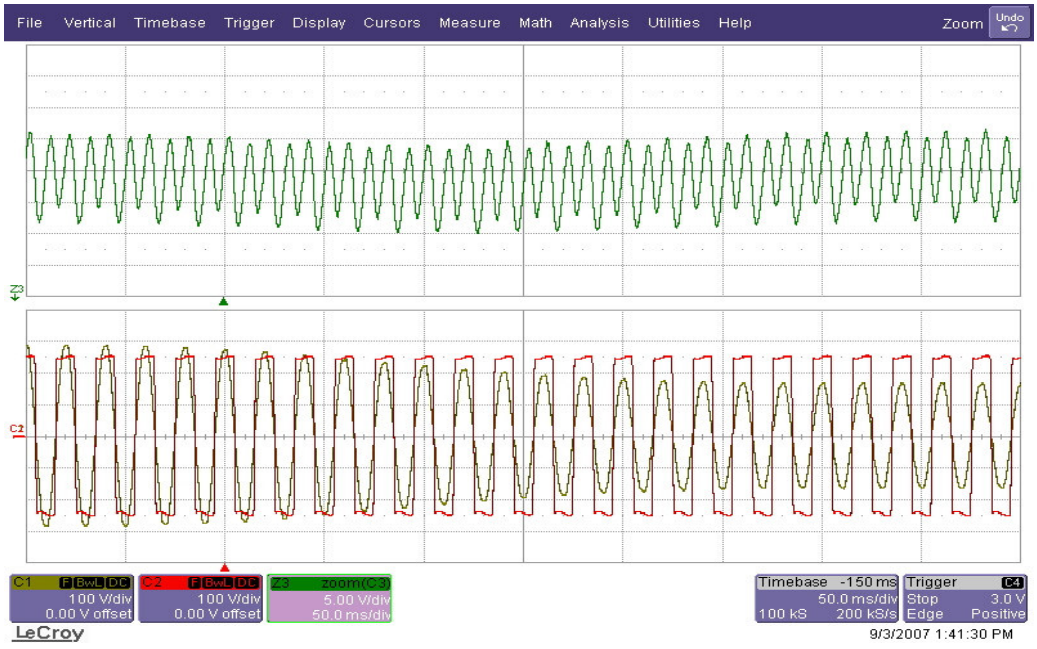



Figure 5.19 Load DC bus voltage (green, top), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-AVM with feedback).

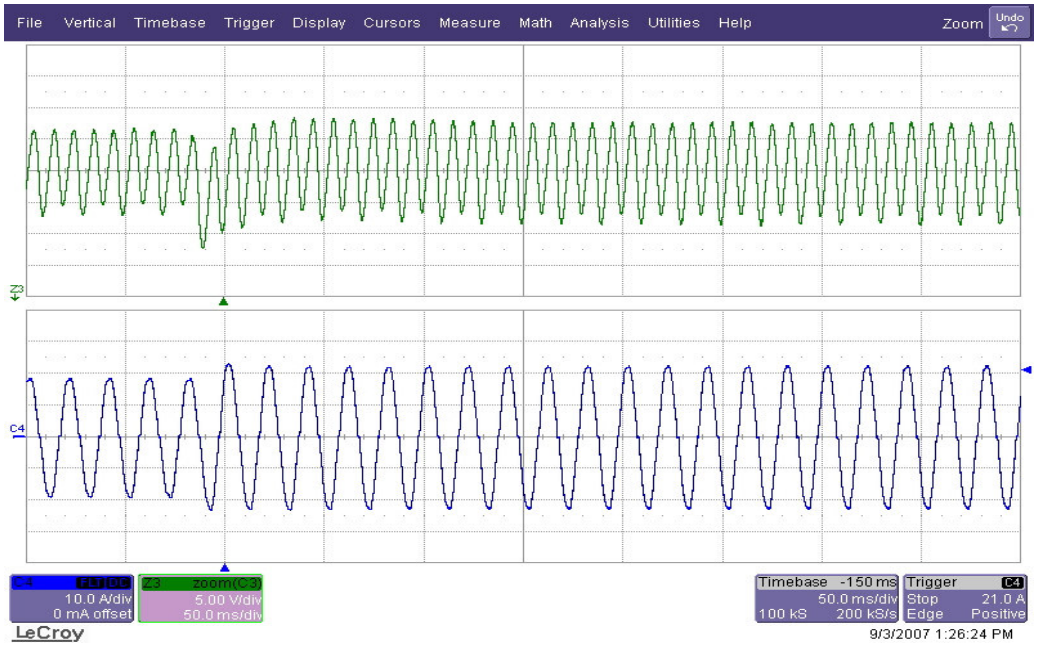



Figure 5.20 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (SPSAF-AVM with feedback).


Figure 5.21 Load DC bus voltage (green, top), load voltage (red), and line voltage (yellow) waveforms for 35% voltage sag (SPSAF-AVM with feedback & feedforward).

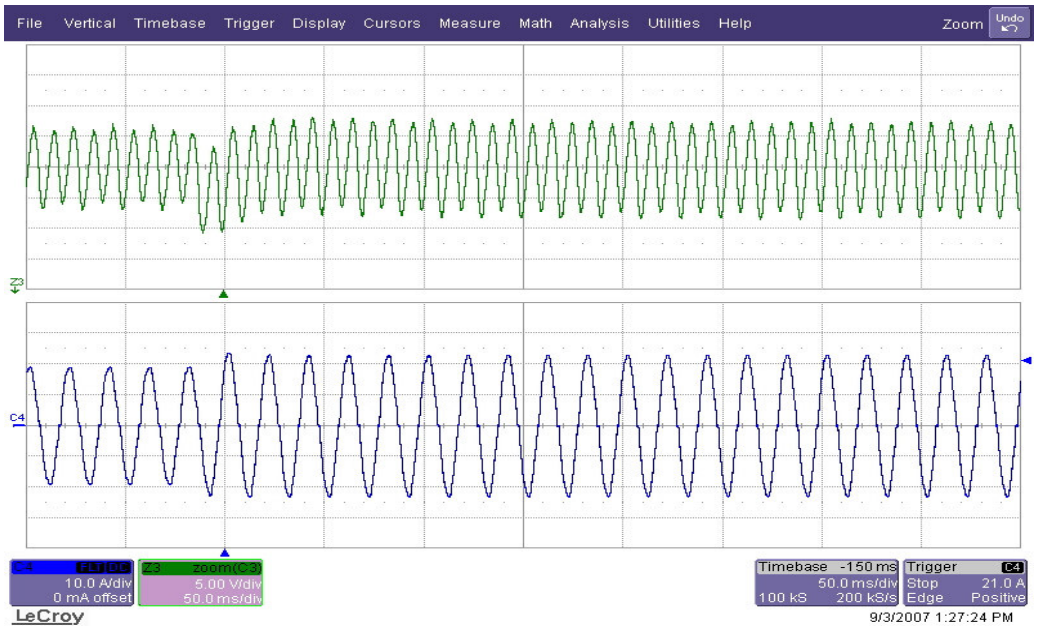



Figure 5.22 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (SPSAF-AVM with feedback & feedforward).

### 5.3.3 Performance Comparison

The harmonic isolation performance of the SPSAF compensated system is evaluated through Table 5.4 as done in Chapter 4. In the table, IEEE 519 limits for harmonic quantities are listed along with the harmonics obtained by the SPSAF experiments. It is obvious that the performance of the SPSAF using AVM is significantly better than the performance of the SPSAF using CM because AVM is less dependent on the line current harmonic feedback controller and yields more accurate load voltage harmonic signal (due to its load voltage geometric shape based algorithm) than CM.

In order to compare the dynamic responses of the SPSAF compensated system to the line and load disturbances considered, the experiment results are tabulated in Table 5.5. As seen in the table, the responses of the SPSAF system using AVM are superior to the responses of the SPSAF system using CM because AVM generates load voltage fundamental frequency component signal with wider bandwidth than CM.

The experimental results are compared to the simulation results in Table 5.6. In the table, $\Delta v_{sag}$ and $\Delta t_{sag}$ are not used because instantaneous voltage sags, which are considered in the simulations, could not be realized in the laboratory. In the table results are consistent except for $THD_V$ and $\Delta v_{dyn}$. As mentioned before, the inconsistency between $THD_V$ values obtained in simulations and the experiments arises from the distortion on the utility voltage. In the experiments, $\Delta v_{dyn}$ values are larger because the load power increase realized in the laboratory is larger than 20% (around 25%) due to the load increment restriction in the resistive load bank used in the experiments.

Table 5.4 The performance comparison between the harmonic isolation provided by the SPSAF using CM and AVM

| | By-pass Mode | Standby Mode | SPSAF with CM | SPSAF with AVM | IEEE 519 Limits |
|---|---|---|---|---|---|
| $I_1$ (%) | 100.0 | 100.0 | 100.0 | 100.0 | 100.0 |
| $I_3$ (%) | 74.4 | 71.4 | 9.8 | 2.3 | 12.0 |
| $I_5$ (%) | 37.2 | 31.8 | 10.1 | 5.1 | 12.0 |
| $I_7$ (%) | 11.2 | 8.0 | 4.9 | 1.2 | 12.0 |
| $I_9$ (%) | 12.3 | 8.6 | 3.3 | 1.5 | 12.0 |
| $I_{11}$ (%) | 9.0 | 5.4 | 1.5 | 1.3 | 5.5 |
| $I_{13}$ (%) | 0.8 | 2.5 | 2.0 | 1.7 | 5.5 |
| $I_{15}$ (%) | 4.0 | 3.5 | 1.5 | 1.2 | 5.5 |
| $I_{17}$ (%) | 3.2 | 1.6 | 1.7 | 0.9 | 5.0 |
| $I_{19}$ (%) | 0.4 | 1.3 | 1.4 | 0.7 | 5.0 |
| $I_{21}$ (%) | 1.5 | 1.3 | 0.9 | 0.3 | 5.0 |
| $I_{23}$ (%) | 1.1 | 0.6 | 1.0 | 0.1 | 2.0 |
| $I_{25}$ (%) | 0.8 | 0.7 | 0.6 | 0.1 | 2.0 |
| $THD_I$ (%) | 85.6 | 79.4 | 15.8 | 6.6 | 15.0 |
| $THD_V$ (%) | 5.1 | 5.1 | 2.6 | 2.5 | 5.0 |
| PF | 0.727 | 0.757 | 0.965 | 0.998 | - |
| $\Delta v_{dc}$ (%) | 13.8 | 13.1 | 6.3 | 5.2 | - |

Table 5.5 The performance comparison between the load voltage regulation provided by the SPSAF using CM and AVM

| | CM | | AVM | |
|---|---|---|---|---|
| | Only Feedback | Feedback & Feedforward | Only Feedback | Feedback & Feedforward |
| $\Delta v_{sag}$ (%) | 3.1 | 0 | 1.0 | 0 |
| $\Delta t_{sag}$ (ms) | 300 | 0 | 0 | 0 |
| $\Delta v_{dyn}$ (%) | 4.1 | 4.1 | 2.0 | 2.0 |
| $\Delta t_{dyn}$ (ms) | 50 | 50 | 20 | 20 |

Table 5.6 The comparison between the performances of SPSAF in the simulation and the experiment

| | Simulation | | Experiment | |
|---|---|---|---|---|
| | CM | AVM | CM | AVM |
| $THD_I$ (%) | 13.75 | 5.97 | 15.8 | 6.6 |
| $THD_V$ (%) | 0.88 | 0.73 | 2.6 | 2.5 |
| PF | 0.984 | 0.998 | 0.965 | 0.998 |
| $\Delta v_{dc}$ (%) | 5.5 | 4.0 | 6.3 | 5.2 |
| $\Delta v_{dyn}$ (%) | 3.2 | 1.2 | 4.1 | 2.0 |
| $\Delta t_{dyn}$ (ms) | 40 | 20 | 50 | 20 |

## 5.4 TPSAF

The detailed power circuit diagram of the TPSAF compensated system is illustrated in Figure 5.23 and its laboratory setup is shown in Figure 5.24. The parameters of the power units in the figure are listed in Table 5.7. In the figure, only the single-phase circuit of TPSAF (Module A) is given in detail and the others are represented as Module B and C with the same components as in Module A. All modules share the same DC bus.

### 5.4.1 Experiment of The TPSAF Compensated System Using CM

With CM, the experimental results are reported regarding harmonic isolation and load voltage regulation. In investigating the TPSAF performance for the load voltage regulation, three types of disturbance are considered, which are three-phase and single-phase voltage sags by 35% of rated utility voltage, and an instantaneous load power increase by 20% of rated load power. The controller parameters of the TPSAF using CM are given in the Table 5.8. In the table, $K_{hv}$ could not be realized as high as in the simulations (0.9) because the inaccuracy of the load voltage harmonic voltage gives rise to instability in the system.

Table 5.7 The experimental parameters of the TPSAF system

| | | |
|---|---|---|
| $E_S$ | Utility voltage | 380 $V_{rms}$ (50 Hz) |
| $L_S$ | Utility leakage inductance | 200 µH |
| $R_S$ | Utility resistance | 100 mΩ |
| $V_{L,DC}$ | Rated DC bus voltage of the compensated load | 488 V |
| $C_L$ | Load capacitance | 2.2 mF |
| $R_L$ | Load resistance | 24 Ω (10 kW) |
| $R_{LB}$ | Load bleeding resistance | 22 kΩ |
| $L_f$ | SRF inductance | 2.2 mH |
| $C_f$ | SRF capacitance | 2.0 µF |
| $R_f$ | Resistance of the SRF inductance | 450 mΩ |
| $R_d$ | SRF damping resistance | 5.6 Ω |
| $V_{DC}$ | Rated DC bus voltage of VSI | 520 V |
| $C_{DC}$ | DC bus capacitance of VSI | 3.3 mF |
| $C_S$ | DC bus snubber capacitance of VSI | 220 nF |
| $R_B$ | DC bus bleeding resistance of VSI | 30 kΩ |
| $E_{AU}$ | Supply voltage of auxiliary rectifier | 380 $V_{rms}$ (50 Hz) |
| $L_{AU}$ | Line inductance of auxiliary rectifier | 1.43 mH |
| $L_1$ | Primary side leakage inductance of SIT | 250 µH |
| $L_2$ | Secondary side leakage inductance of SIT | 40 µH |
| $R_1$ | Primary side copper resistance of SIT | 550 mΩ |
| $R_2$ | Secondary side copper resistance of SIT | 90 mΩ |
| N | Turns-ratio of SIT ($N_1$:$N_2$) | 2.5 |
| $f_{PWM}$ | PWM frequency | 20 kHz |
| $T_S$ | Sampling time (Double update) | 25 µs |
| $T_n$ | Near-next-state sampling time | 5 µs |
| $T_{dt}$ | Deadtime of the IGBT switches | 3.5 µs |

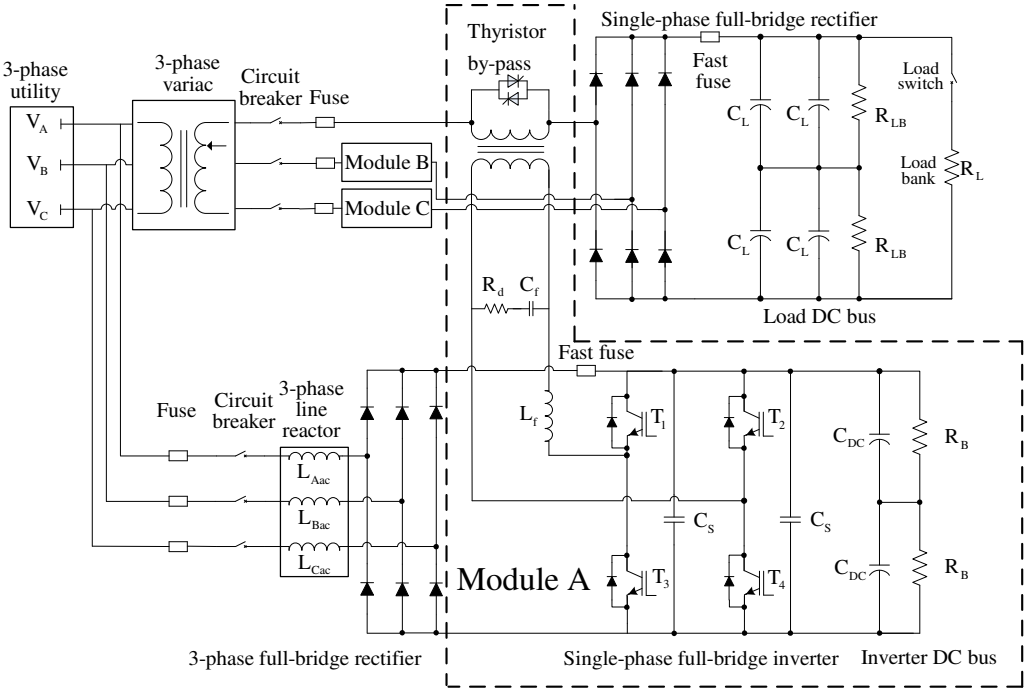



Figure 5.23 The detailed power circuit diagram of the 10 kW TPSAF compensated system in the laboratory.

Table 5.8 The experimental controller parameters of the TPSAF using CM

| | | |
|---|---|---|
| $K_{hi}$ | HIC gain for line current | 10 |
| $K_{hv}$ | HIC gain for load voltage | 0.6 |
| $f_{cih}$ | HIC cut-off frequency for line current | 7.5 Hz |
| $f_{cvh}$ | HIC cut-off frequency for load voltage | 7.5 Hz |
| $K_d$ | RDC gain | 20 |
| $K_{Pv}$ | FCC proportional gain | 1.5 |
| $K_{Iv}$ | FCC integral gain | 40 |
| $f_{cv1}$ | FCC cut-off frequency for load voltage | 15 Hz |
| $f_{cvff}$ | FCC LPF cut-off frequency for line voltage | 500 Hz |
| $a_v$ | Constant of phase-lead compensator in FCC | 4.6 |
| $T_v$ | Time constant of phase-lead compensator in FCC | 10 ms |

Figure 5.24 Laboratory setup of the TPSAF system (top), the power converter and electronic circuitry (bottom).

### 5.4.1.1 Harmonic Isolation

In the by-pass mode and the standby mode, the waveforms of line voltage, load voltage, and line current are as shown in Figure 5.25 and Figure 5.26. $THD_I$ values are very large for both modes (103.3% and 72.3%). Consequently, the line voltage is distorted ($THD_V$ = 2.0% and 1.4%) and PF is very low (0.702 and 0.796). The same reasoning in the SPSAF system is valid for the inconsistency between the experiment and the simulation results. However, the distortion is less in the three-phase system compared to the single-phase system due to the absence of the triplen harmonic currents in the former.

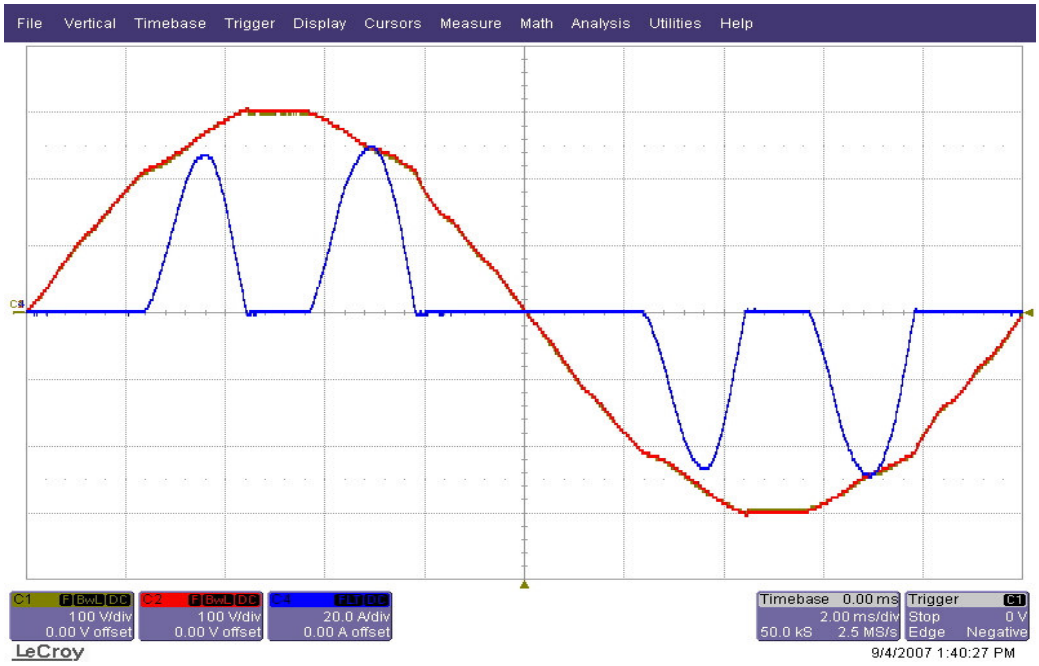



Figure 5.25 Uncompensated three-phase system line voltage (yellow), load voltage (red), and line current (blue) waveforms in by-pass mode.

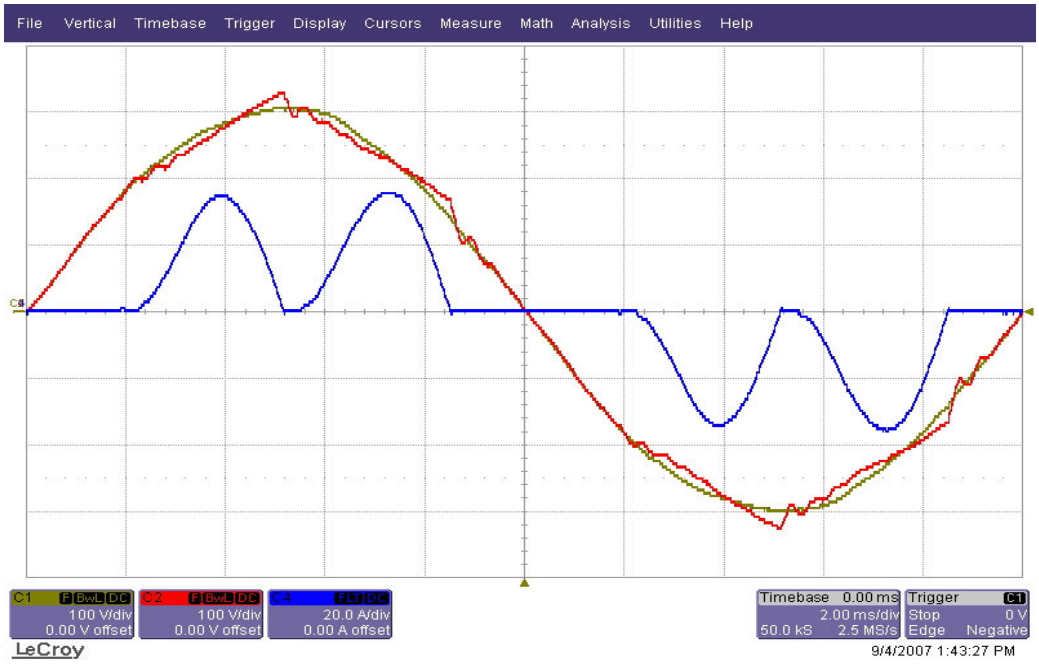



Figure 5.26 Uncompensated three-phase system line voltage (yellow), load voltage (red), and line current (blue) waveforms in standby mode.

When harmonic isolation is provided by TPSAF, the harmonic distortion is alleviated as seen in Figure 5.27. In the figure, the load voltage becomes a distorted six-step waveform by means of the series injection voltage and $THD_I$ = 11.1%, $THD_V$ = 1.5%, and PF = 0.987. Moreover, the correlation between $THD_V$ values found in the experiments and the ones found in simulation is not firm due to the interaction between the utility voltage distortion and the load voltage harmonics. As an additional effect of the harmonic isolation, $\Delta v_{dc}$ decreases to 0.5% as seen in Figure 5.28 where $\Delta v_{dc}$ = 3.0% for the by-pass mode and $\Delta v_{dc}$ = 2.0% for the standby mode. This decrease provides a minor advantage in the selection of DC bus capacitor.

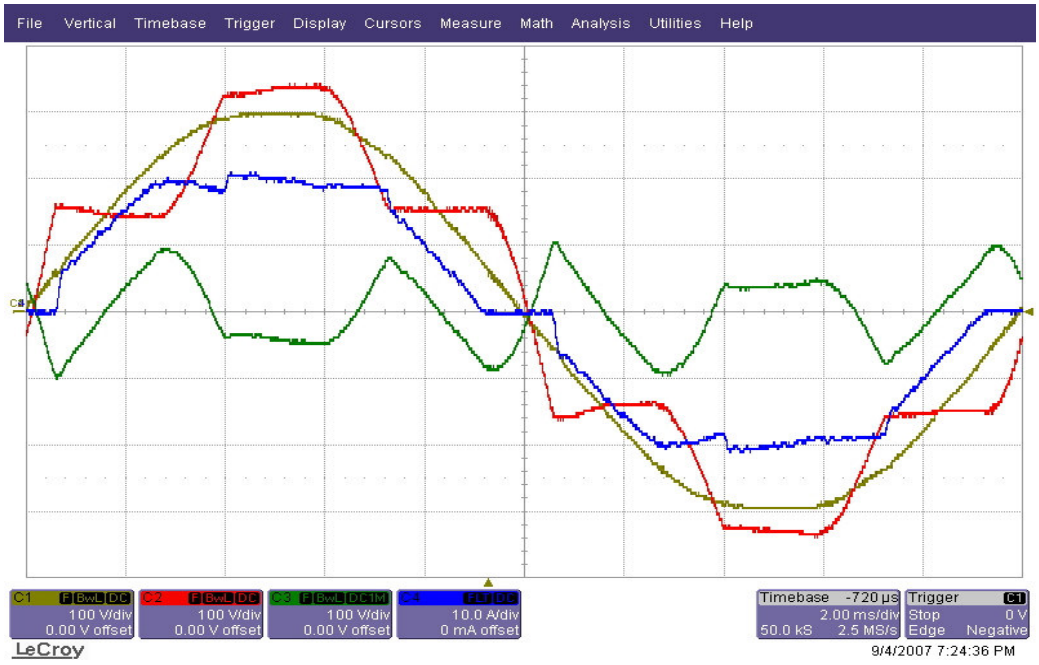



Figure 5.27 Line voltage (yellow), load voltage (red), TPSAF voltage (green), and line current (blue) waveforms (TPSAF-CM).

### 5.4.1.2 Load Voltage Regulation

The responses of the TPSAF system with only HIC to 35% single-phase and three-phase voltage sags, and 20% load power increase are shown in Figure 5.29, Figure 5.30, and Figure 5.31, respectively. For the three-phase balanced sag, load DC bus and load voltages drop along with line voltage. In the second figure, there are 100 Hz ripples on the load DC bus voltage accompanied with the decrease on it due to unbalanced behavior of the single-phase sag. The ripple percentage due to the negative sequence voltage ($\Delta v_{neg}$) is 1.1%. In the third figure, $\Delta v_{dyn}$ is 9.1 % and the $\Delta t_{dyn}$ is 200 ms approximately.

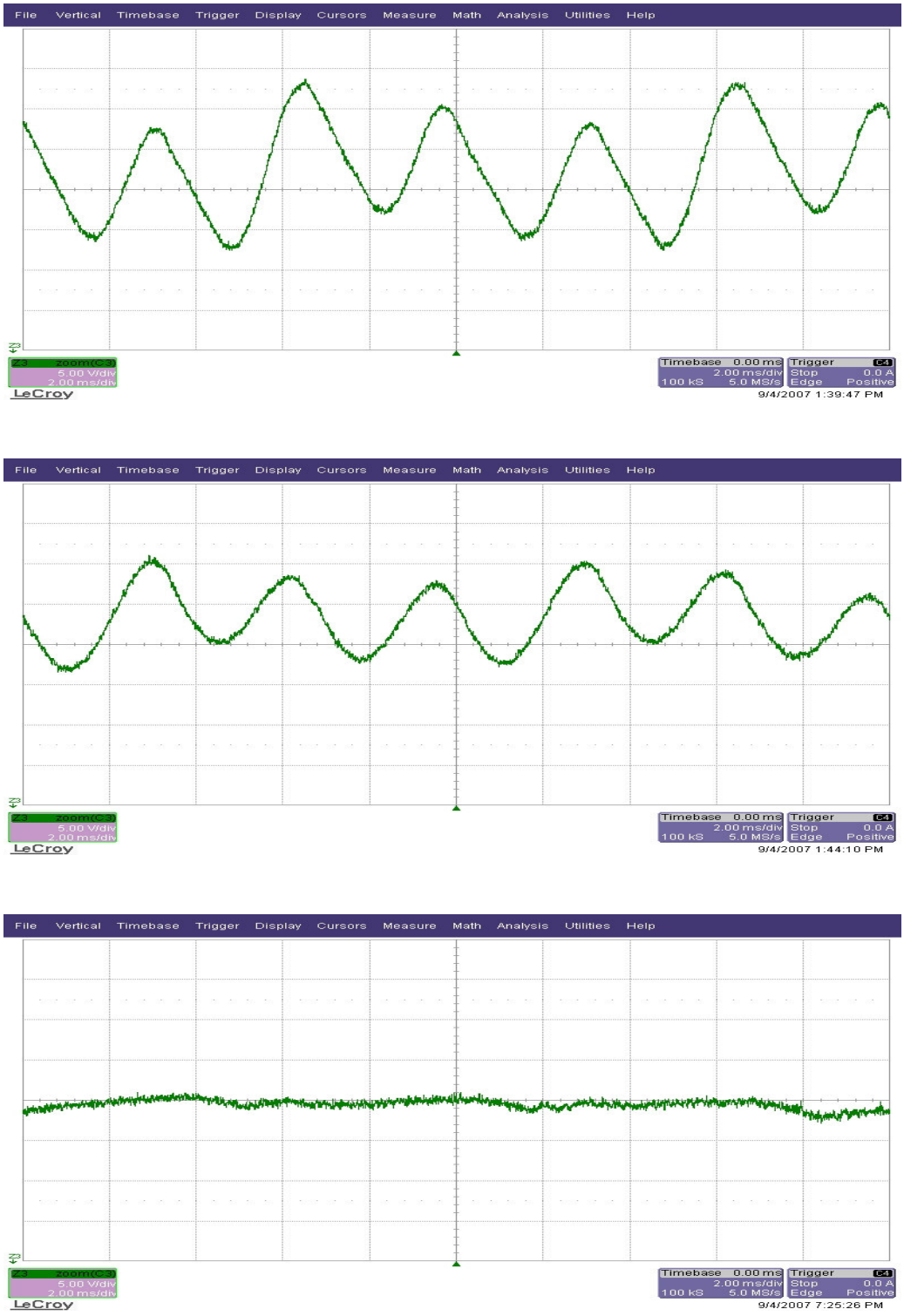



Figure 5.28 Load DC bus ripple voltage waveforms; (top) by-pass mode, (middle) standby mode, and (bottom) HIC (TPSAF-CM).

With only the feedback controller of FCC functioning, the load voltage is regulated against the three-phase voltage sag such that $\Delta v_{sag}$ = 2.5% and $\Delta t_{sag}$ = 200 ms as shown in Figure 5.32. For the single-phase sag, TPSAF regulates the load voltage against the single-phase voltage sag and $\Delta v_{neg}$ becomes 1.4% as shown in Figure 5.33. The response to the load dynamic is shown in Figure 5.34 such that $\Delta v_{dyn}$ = 3.1% and $\Delta t_{dyn}$ = 40 ms, which shows that the response of the system to the load power increase is improved.

The experimental results with the addition of the feedforward controller under the conditions discussed are given in Figure 5.35, Figure 5.36, and Figure 5.37. As seen in the figures, the immunity of the load voltage to the line voltage sags is increased such that $\Delta v_{sag}$, $\Delta v_{neg}$, and $\Delta t_{sag}$ are negligible while the response of TPSAF to the load power increase is the same as the response with the feedback controller.

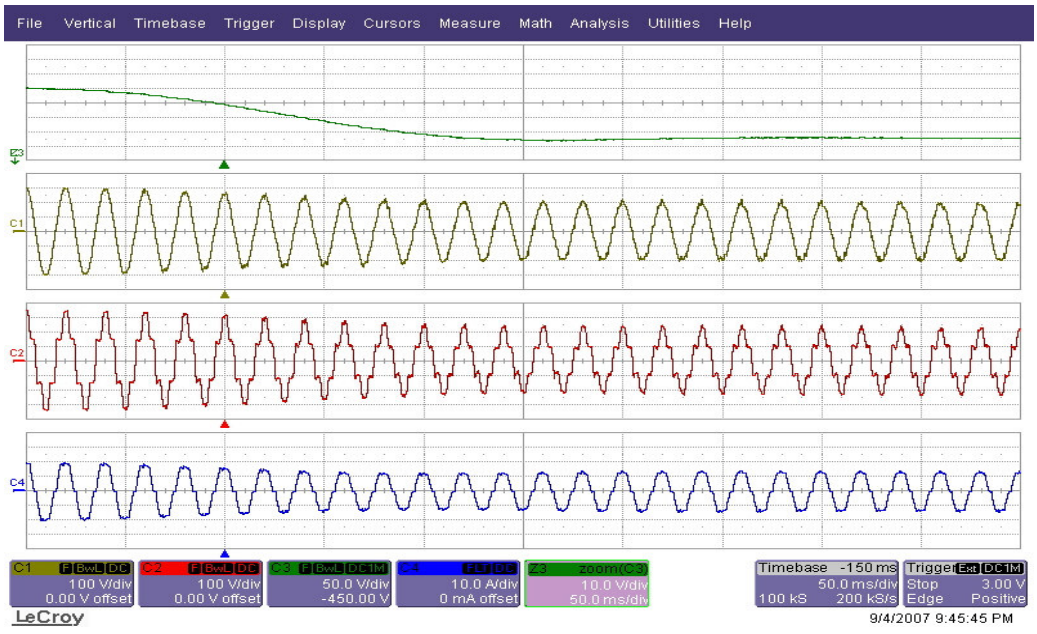



Figure 5.29 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-CM without FCC).

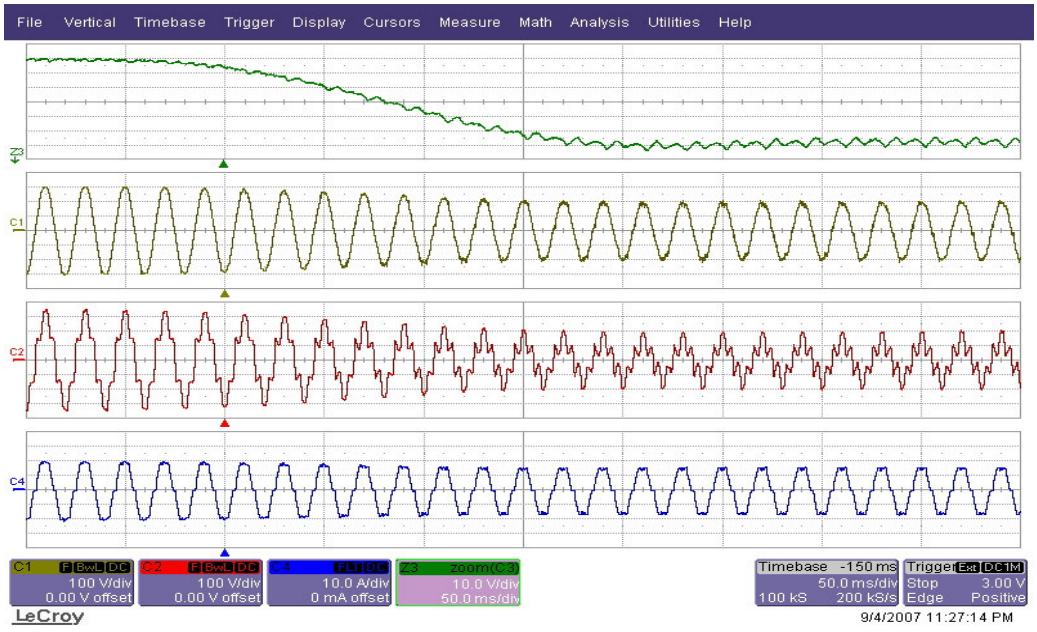



Figure 5.30 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-CM without FCC).

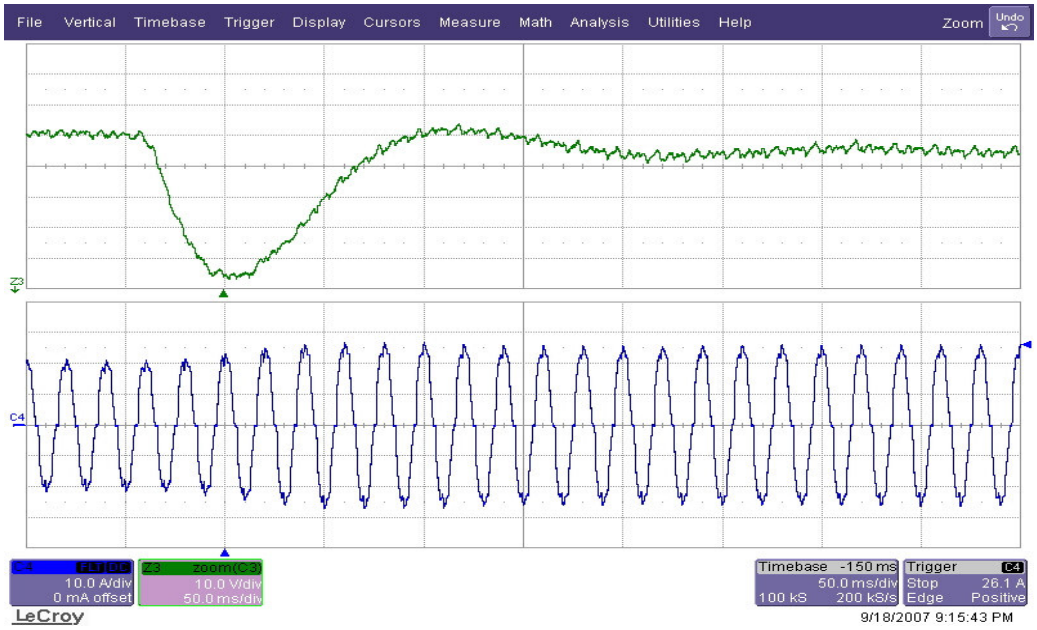



Figure 5.31 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (TPSAF-CM without FCC).

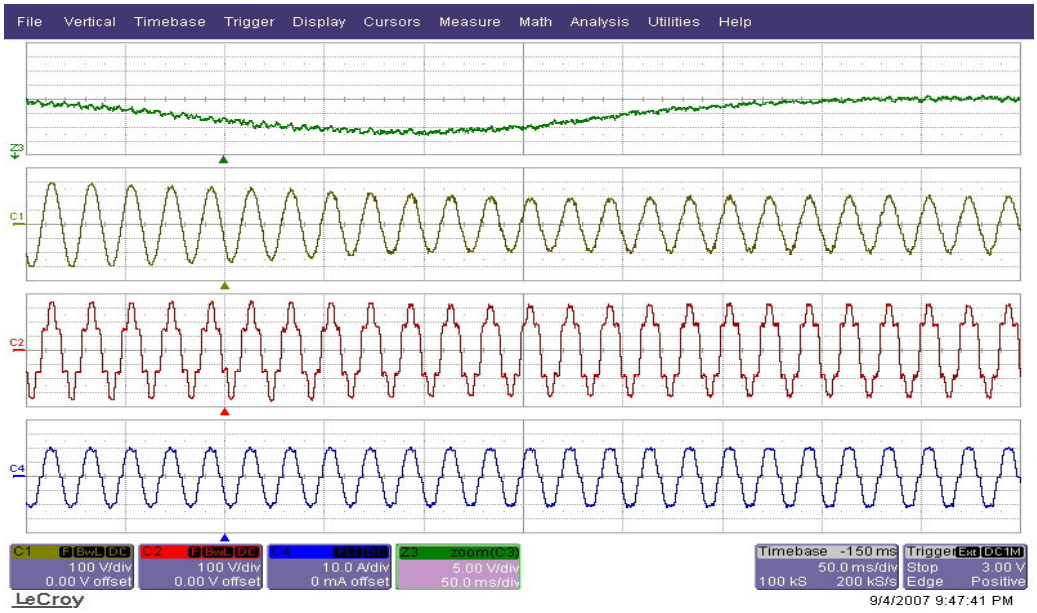



Figure 5.32 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-CM with feedback).

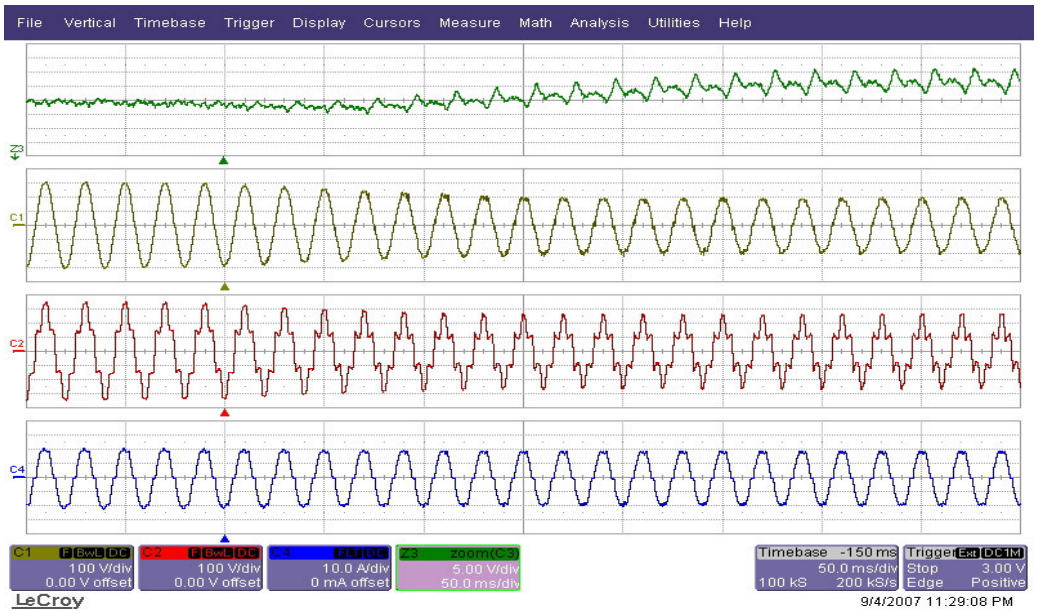



Figure 5.33 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-CM with feedback).

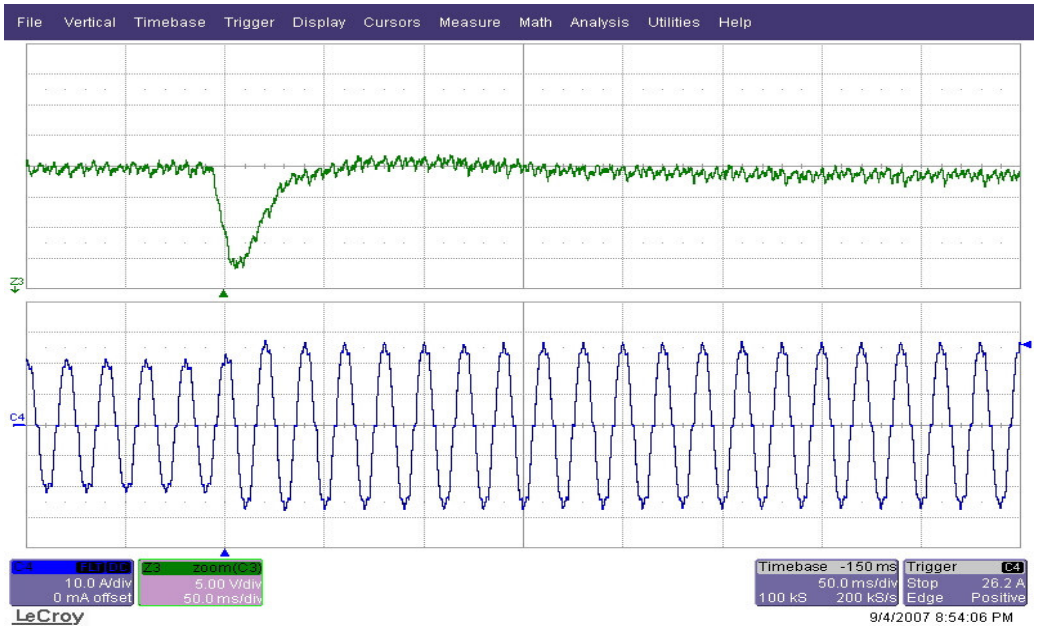



Figure 5.34 Load DC bus voltage (green, top) and line current (blue) waveforms for the load power increase (TPSAF-CM with feedback).

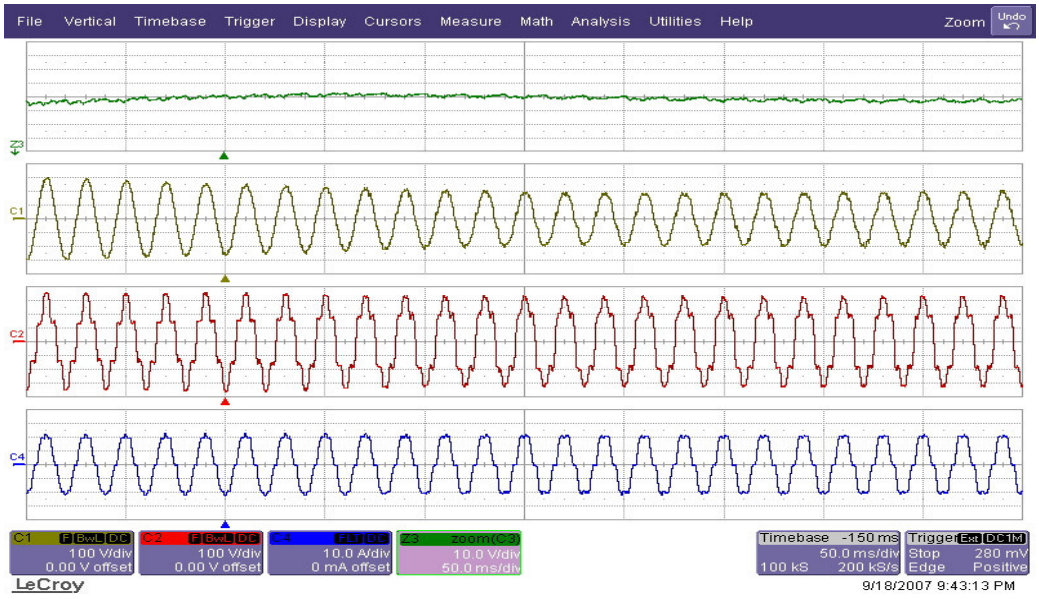



Figure 5.35 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-CM with feedback & feedforward).

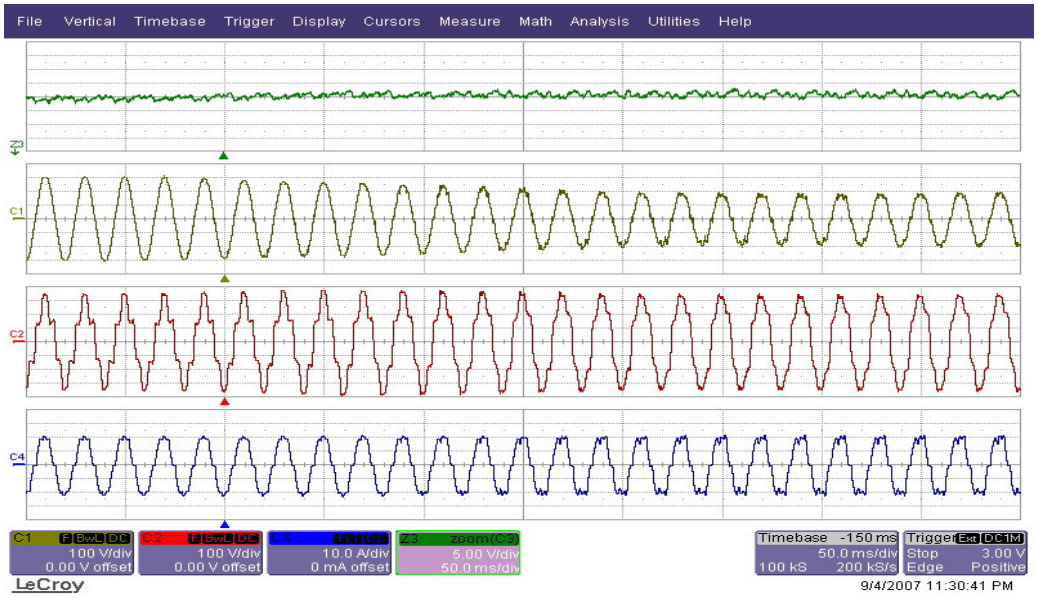



Figure 5.36 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-CM with feedback & feedforward).

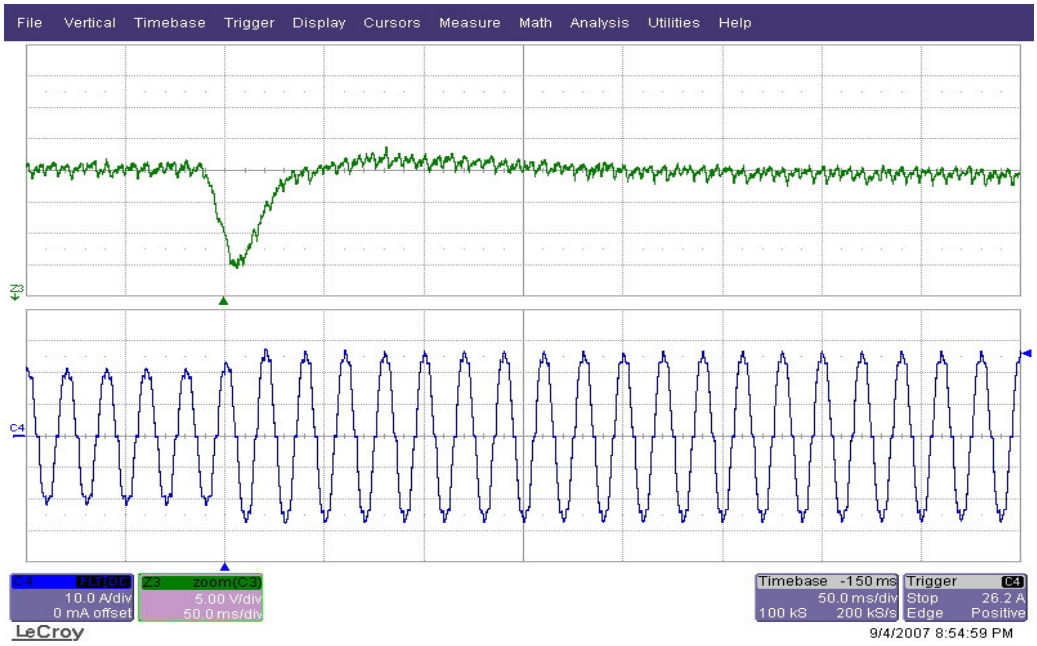



Figure 5.37 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (TPSAF-CM with feedback & feedforward).

### 5.4.2 Experiment of The TPSAF Compensated System Using AVM

The controller parameters for AVM used in the experiments are the same as the simulations given in the Table 5.9.

#### 5.4.2.1 Harmonic Isolation

By means of HIC using AVM, the harmonic isolation performance is improved with respect to the CM case as seen in Figure 5.38 such that $THD_I = 5.0\%$, $THD_V = 1.9\%$, and PF = 0.998. Beneath the improvement lies the accurate load voltage harmonic extraction by means of AVM. Besides, $\Delta v_{dc}$ becomes 0.3% as shown in Figure 5.39.

Table 5.9 The experimental controller parameters of TPSAF using AVM

| | | |
|---|---|---|
| $K_{hi}$ | HIC gain for line current | 10 |
| $K_{hv}$ | HIC gain for load voltage | 1 |
| $f_{cih}$ | HIC cut-off frequency for line current | 7.5 Hz |
| $K_d$ | RDC gain | 20 |
| $T_r$ | AVM rise time for load voltage synthesis | 0.4 ms |
| $T_\theta$ | AVM compensation time for phase angle delay | 200 μs |
| $K_{Pv}$ | FCC proportional gain | 5 |
| $K_{Iv}$ | FCC integral gain | 175 |
| $f_{cvff}$ | FCC LPF cut-off frequency for line voltage | 500 Hz |
| $f_{c2th}$ | AVM resonant filter frequency ($2f_e$) | 100 Hz |
| $f_{c6th}$ | AVM resonant filter frequency ($6f_e$) | 300 Hz |
| $f_{cv}$ | AVM LPF cut-off frequency | 300 Hz |

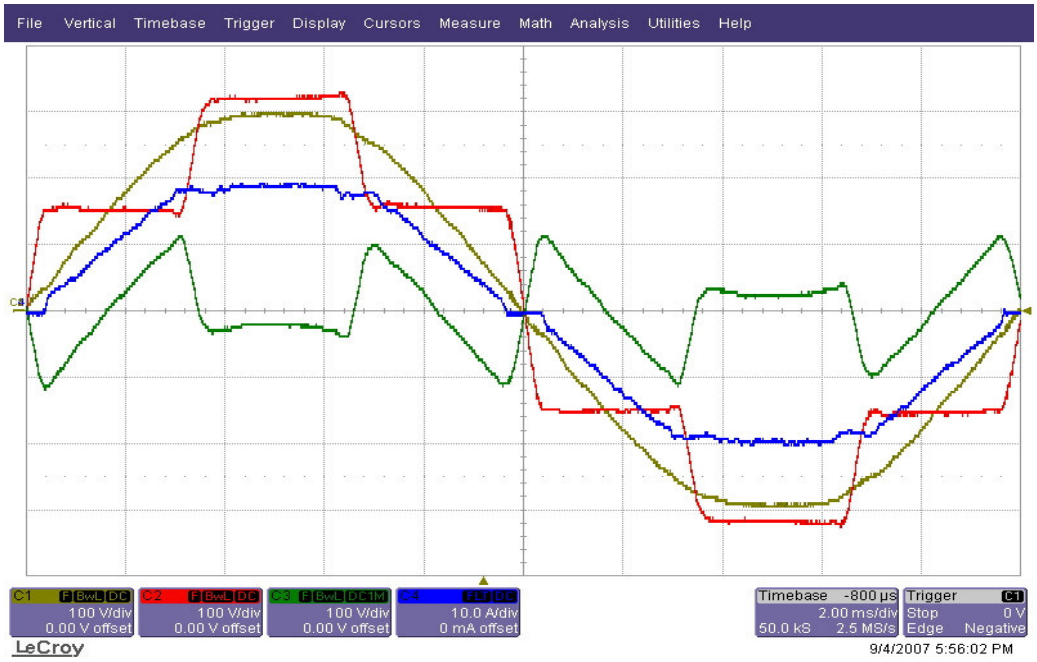



Figure 5.38 Line voltage (yellow), load voltage (red), TPSAF voltage (green), and line current (blue) waveforms (AVM).

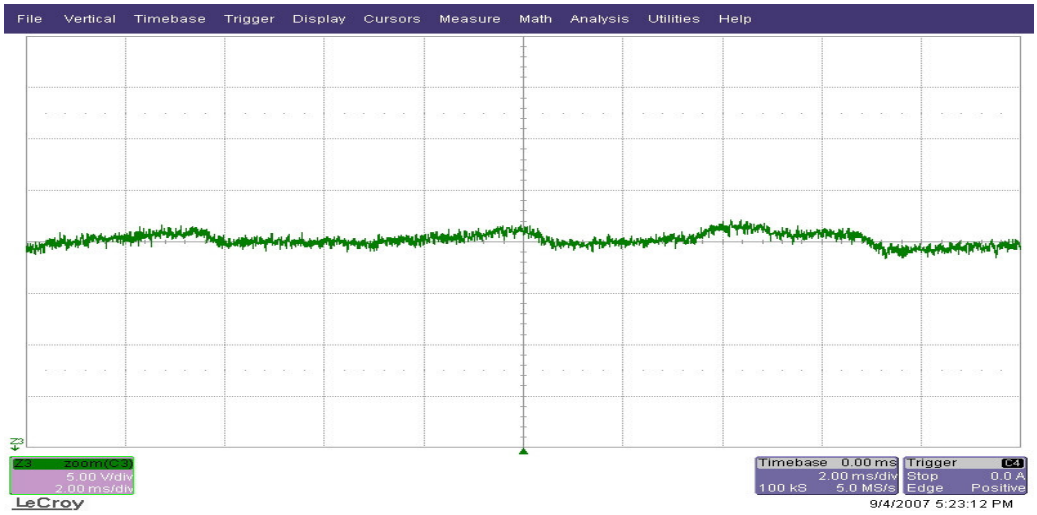



Figure 5.39 Load DC bus ripple voltage waveform (AVM).

#### 5.4.2.2 Load Voltage Regulation

The responses of the TPSAF system with only HIC to 35% single-phase and three-phase voltage sags, and 20% load power increase are shown in Figure 5.40, Figure 5.41, and Figure 5.42, respectively. In the first figure, load DC bus and load voltages are not regulated therefore they drop along with line voltage. In the second figure, load voltage is not regulated but the negative sequence of the single-phase sag is mostly suppressed such that $\Delta v_{neg}$ is 1.1%. As shown in the last figure, $\Delta v_{dyn}$ is 6.4% and $\Delta t_{dyn}$ is 150 ms, approximately. Another point worth noticing is that the harmonic isolation performance of the TPSAF using CM degrades but the one of TPSAF using AVM stays almost the same during the voltage sags.

With only feedback controller of FCC, TPSAF regulates the load voltage against the three-phase voltage sag such that $\Delta v_{sag}$ is 2.1% and $\Delta t_{sag}$ is 100 ms as shown in Figure 5.43. As shown in Figure 5.44, the load voltage is regulated and $\Delta v_{neg}$ is 1.2% for the single-phase voltage sag. The response to the load dynamic is improved with respect to the TPSAF without FCC as shown in Figure 5.45 such that $\Delta v_{dyn}$ = 2.1% and $\Delta t_{dyn}$ = 50 ms. In the figures, it is observed that the load DC voltage has low frequency fluctuations and the reasoning of this problem will be given later in the next section.

The experimental results with the addition of the feedforward controller of FCC are given in Figure 5.46, Figure 5.47, and Figure 5.48 under the same conditions discussed. As seen in the figures, the immunity of the load voltage to the voltage sags is increased such that $\Delta v_{sag}$, $\Delta t_{sag}$, and $\Delta v_{neg}$ are improved such that they can be neglected while the response of TPSAF to the load power increase is the same as the one in FB.

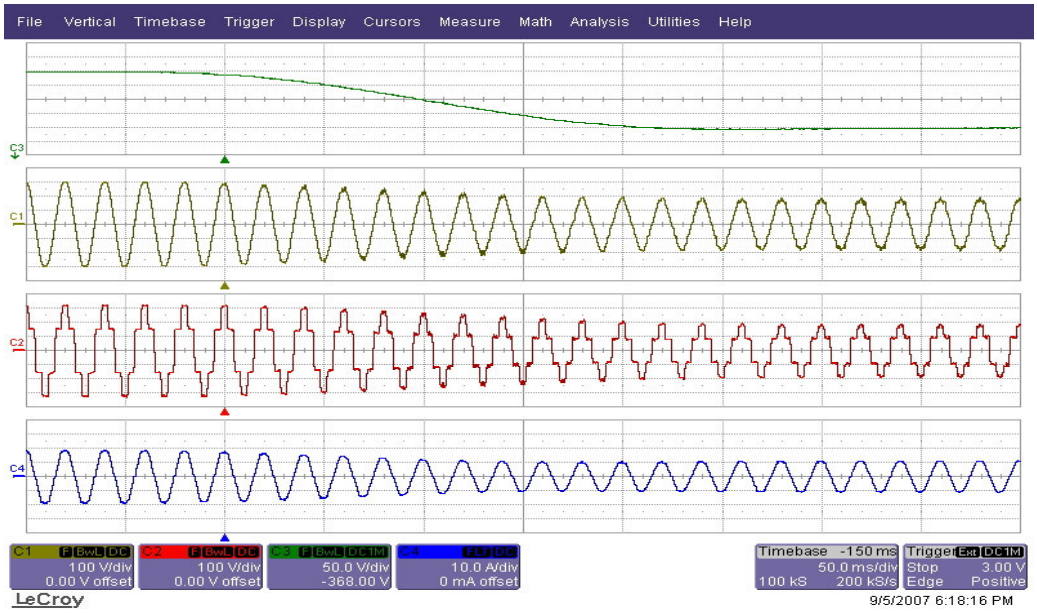



Figure 5.40 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-AVM without FCC).

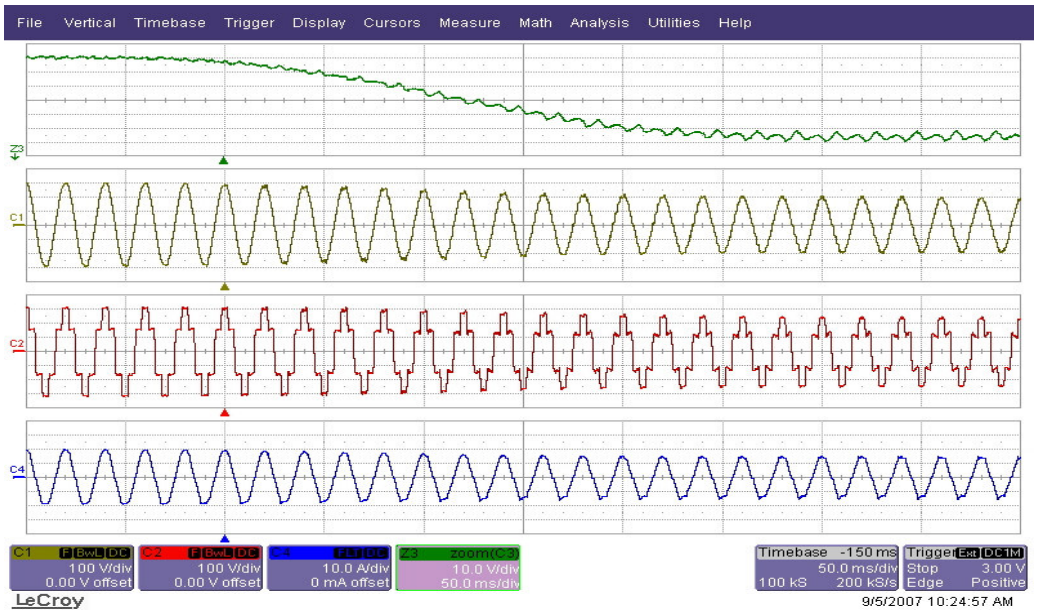



Figure 5.41 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-AVM without FCC).

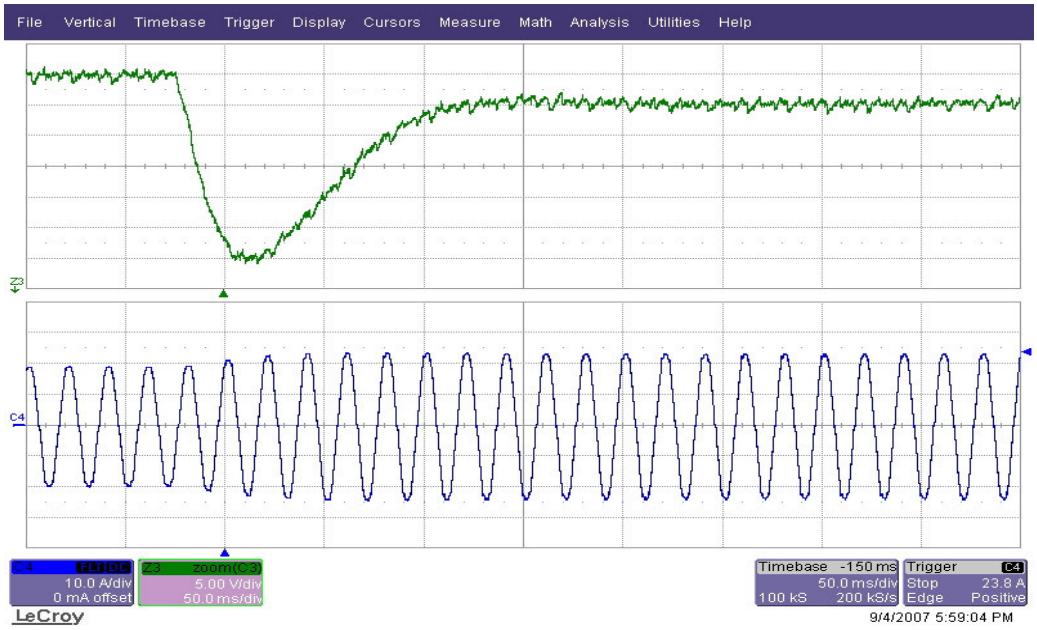



Figure 5.42 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (TPSAF-AVM without FCC).

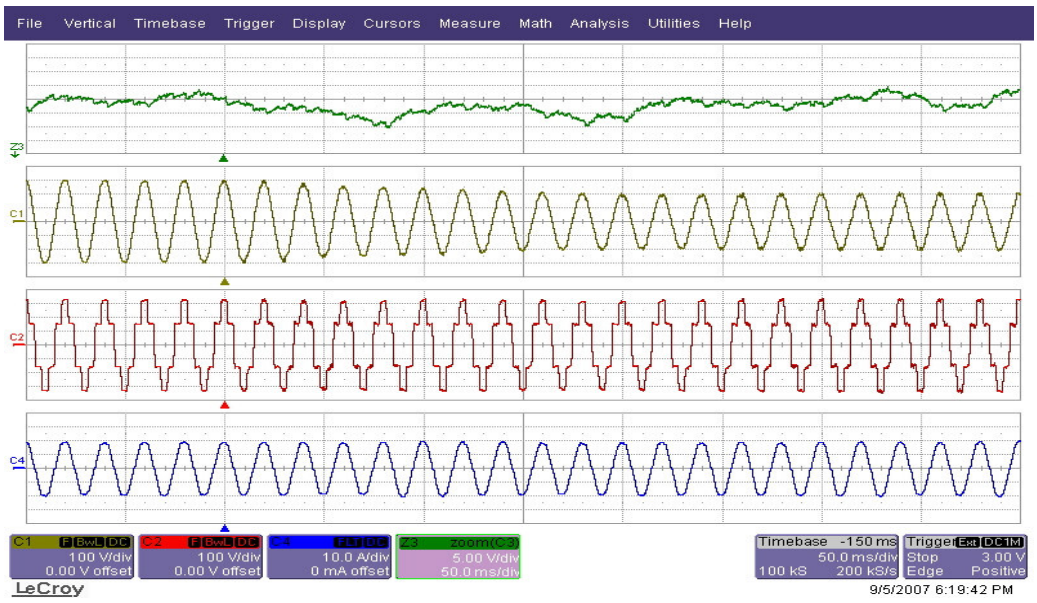



Figure 5.43 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-AVM with feedback).

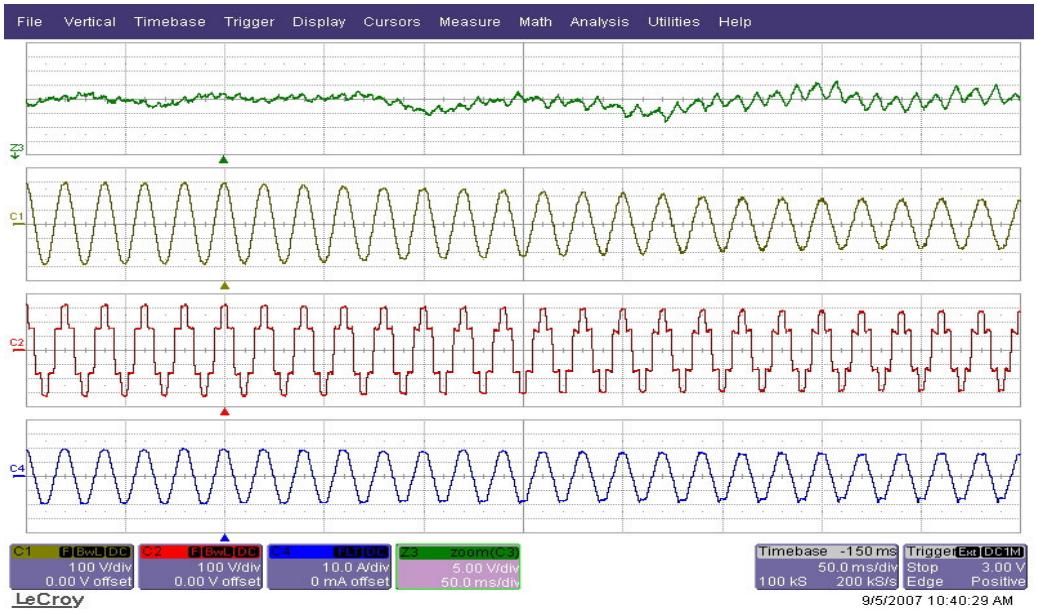



Figure 5.44 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-AVM with feedback).

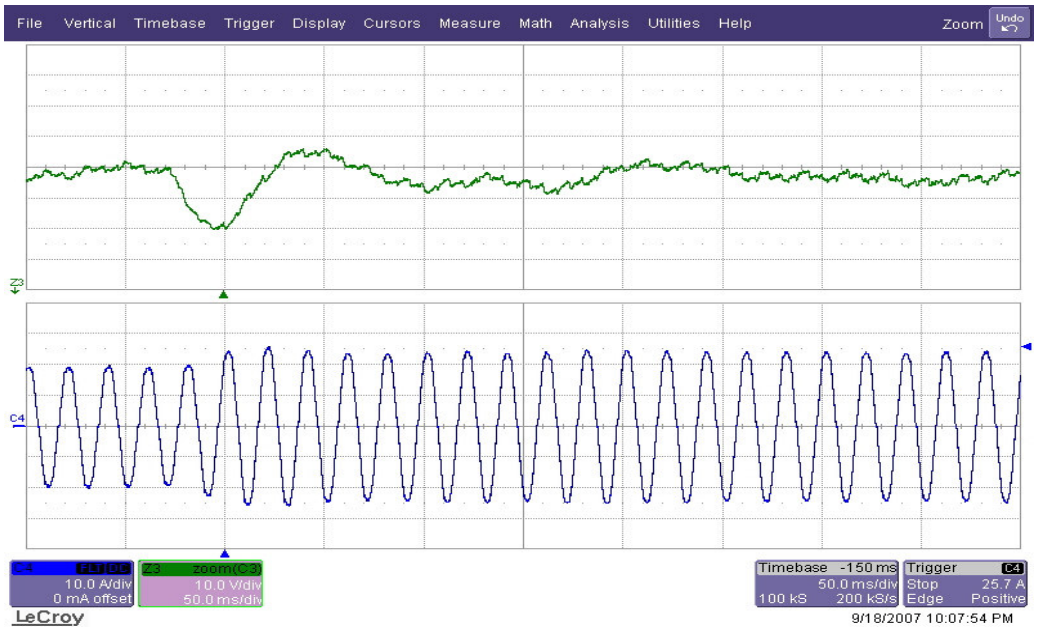



Figure 5.45 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (SPSAF-AVM with feedback).

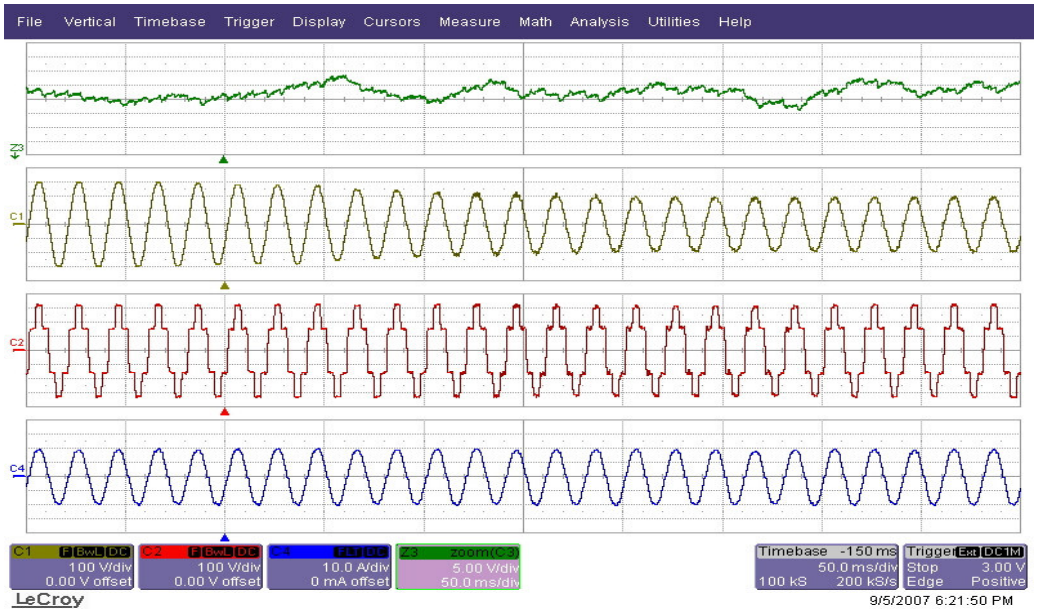



Figure 5.46 Waveforms for 35% balanced three-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-AVM with feedback & feedforward).

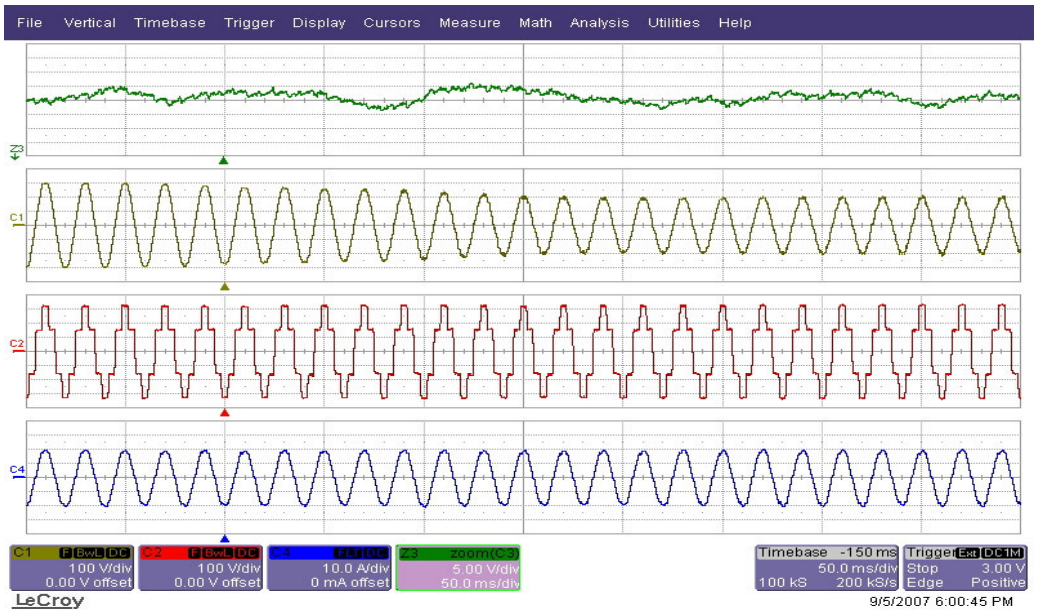



Figure 5.47 Waveforms for 35% single-phase voltage sag. Top to bottom: Load DC bus voltage, utility voltage, load voltage, and line current (TPSAF-AVM with feedback & feedforward).

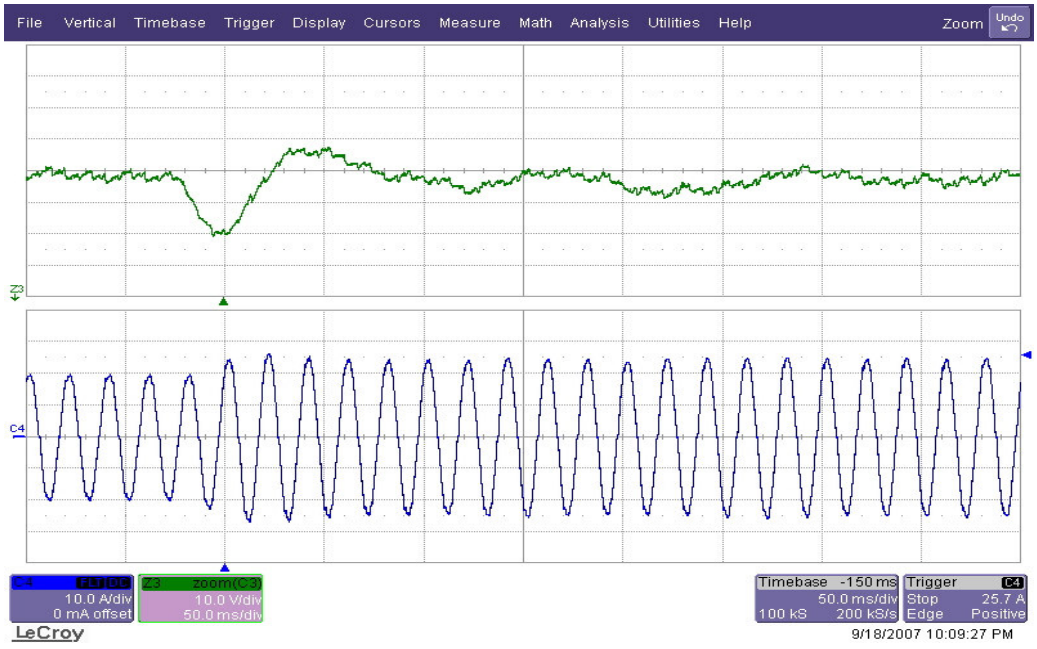



Figure 5.48 Load DC bus voltage (green, top) and line current (blue) waveforms for 20% load power increase (TPSAF-AVM with feedback & feedforward).

### 5.4.3 Performance Comparison

The harmonic isolation performance of TPSAF is tabulated along with the IEEE 519 limits in Table 5.10. It is obvious that the performance of TPSAF using AVM is significantly better than the one of TPSAF using CM because AVM generates high accuracy load voltage harmonic signal.

In order to compare the responses of TPSAF to the line and load disturbances discussed, the experiment results are tabulated in Table 5.11. As seen in the table, the TPSAF using AVM is superior to the TPSAF using CM because AVM generates high bandwidth load fundamental frequency voltage signal. It should be also noted that the feedforward controller improves the response of TPSAF for voltage sags but not load dynamics because the load current increase hardly affects the line current.

Table 5.10 The performance comparison between the harmonic isolation provided by the TPSAF using CM and AVM

| | By-pass Mode | Standby Mode | TPSAF with CM | TPSAF with AVM | IEEE 519 Limits |
|---|---|---|---|---|---|
| $I_1$ (%) | 100.0 | 100.0 | 100.0 | 100.0 | 100.0 |
| $I_5$ (%) | 77.9 | 62.2 | 9.0 | 4.4 | 12.0 |
| $I_7$ (%) | 60.6 | 35.8 | 4.8 | 0.3 | 12.0 |
| $I_{11}$ (%) | 25.2 | 5.3 | 3.1 | 1.2 | 5.5 |
| $I_{13}$ (%) | 11.3 | 5.3 | 1.9 | 1.3 | 5.5 |
| $I_{17}$ (%) | 5.7 | 2.3 | 0.9 | 0.8 | 5.0 |
| $I_{19}$ (%) | 5.2 | 2.2 | 0.8 | 0.7 | 5.0 |
| $I_{23}$ (%) | 2.6 | 1.8 | 1.2 | 0.5 | 2.0 |
| $I_{25}$ (%) | 0.6 | 1.3 | 0.8 | 0.6 | 2.0 |
| $THD_I$ (%) | 103.3 | 72.3 | 11.1 | 5.0 | 15.0 |
| $THD_V$ (%) | 2.0 | 1.4 | 1.5 | 1.9 | 5.0 |
| PF | 0.702 | 0.796 | 0.987 | 0.998 | - |
| $\Delta v_{dc}$ (%) | 3.0 | 2.0 | 0.5 | 0.3 | - |

Table 5.11 The performance comparison between the load voltage regulation provided by the TPSAF using CM and AVM

| | CM | | AVM | |
|---|---|---|---|---|
| | Only Feedback | Feedback & Feedforward | Only Feedback | Feedback & Feedforward |
| $\Delta v_{sag}$ (%) | 2.5 | 0 | 2.1 | 0 |
| $\Delta t_{sag}$ (ms) | 200 | 0 | 100 | 0 |
| $\Delta v_{dyn}$ (%) | 3.1 | 3.1 | 2.1 | 2.1 |
| $\Delta t_{dyn}$ (ms) | 40 | 40 | 50 | 50 |
| $\Delta v_{neg}$ (%) | 1.4 | 0 | 1.2 | 0 |

The experimental results are compared to the simulation results in Table 5.12. In the table, $\Delta v_{sag}$ and $\Delta t_{sag}$ are not used because instantaneous voltage sags, which are considered in the simulations, could not be realized in the laboratory. In the table the results are consistent except for $THD_V$, $\Delta v_{dyn}$, and $\Delta t_{dyn}$. The reasoning for the two inconsistencies is the same explained in the SPSAF section. As for $\Delta t_{dyn}$, TPAVM is

susceptible to the low frequency signals generated by not identical analog measurement circuits for the three-phase load voltages. Therefore, the feedback controller for load voltage regulation using the load voltage magnitude information from TPAVM with high gains results in low frequency oscillation in the load voltage, which is shown in the load voltage regulation waveforms of the TPSAF using AVM, hence the response of the TPSAF to the line and load disturbances worsens.

### 5.5 Summary

By means of the experimental results obtained from the SPSAF and TPSAF prototypes, it is verified that SAF is capable of isolating harmonic voltage of V-type nonlinear loads from utility and regulating fundamental load voltage of V-type nonlinear load against line voltage and load power disturbances. The performance improvement in both harmonic isolation and load voltage regulation by means of the novel AVM with respect to CM is proven except for TPSAF, of which problem with AVM is identified. The experimental results are compared to the simulation results and inconsistencies are explained.

Table 5.12 The comparison between the performances of TPSAF in the simulation and the experiment

| | Simulation | | Experiment | |
|---|---|---|---|---|
| | CM | AVM | CM | AVM |
| $THD_I$ (%) | 9.91 | 3.95 | 11.1 | 5.0 |
| $THD_V$ (%) | 0.93 | 0.60 | 1.5 | 1.9 |
| PF | 0.991 | 0.998 | 0.987 | 0.998 |
| $\Delta v_{dc}$ (%) | 0.2 | 0.1 | 0.5 | 0.3 |
| $\Delta v_{dyn}$ (%) | 2.9 | 1.8 | 3.1 | 2.1 |
| $\Delta t_{dyn}$ (ms) | 35 | 25 | 40 | 50 |
| $\Delta v_{neg}$ (%) | 0.4 | 0.3 | 0 | 0 |

# CHAPTER 6

# CONCLUSIONS

The Series Active Filter (SAF) is an active power quality conditioner for both utility and load related power quality problems such that it isolates the harmonic voltage of the load from the utility and regulates the load voltage against the line voltage disturbances. One of its advantageous features is that it is directly applicable to the voltage harmonic source type nonlinear loads without changing the load type to the harmonic current source type by adding extra inductances. The other major advantage is that in addition to harmonic isolation, it provides load voltage regulation against line voltage disturbances such as unbalances and sags which are common. Single-phase SAF (SPSAF) and three-phase SAF (TPSAF) are the types of SAF which are utilized for single-phase and three-phase diode bridge rectifiers loads with DC bus capacitor and resistor (V-type loads), respectively.

The power circuit of SAF per phase is composed of a voltage source inverter (VSI), a switching ripple filter (SRF), and a series injection transformer (SIT). These main units are used to inject the SAF voltage for harmonic isolation and load voltage regulation between the utility and the load with galvanic isolation. Additionally, by-pass thyristors are used for protection and maintenance purposes and an auxiliary three-phase diode bridge rectifier is utilized to keep the DC bus of the VSI(s) constant when the real power transfer occurs between SAF and the load in order to regulate the load voltage.

The control of SAF is realized by Harmonic Isolation Controller (HIC), Fundamental Component Controller (FCC), Resonance Damping Controller (RDC), Pulse Width

Modulator (PWM), Phase Locked Loop (PLL), and Harmonic/Fundamental Extractor (HFE) in order to provide harmonic isolation and load voltage regulation stably. Among the controller units, HFE is vital because the proper operations of HIC and FCC strongly depend on the accurate and rapid extracted harmonic and fundamental components of the measured signals.

The main contribution of this thesis involves the development of the novel Absolute Value Method (AVM), which utilizes the geometric properties of rectangular voltage waveforms to extract both the harmonic and fundamental components of the load voltage fast and accurately for the single-phase and three-phase diode rectifiers with RC load. Utilizing this method in the HFE instead of using the Conventional Method (CM), which depends on low/high-pass filtering of the signals in 'de-qe' frame, higher overall power quality is obtained. AVM does not use very low frequency cut-off filters for harmonic extraction. Instead it utilizes the mathematical relations between the fundamental component and the rectangular load voltage waveform to extract the harmonics. The additional filtering elements utilized in the AVM extractor are to enhance its performance; however their dynamic responses are much faster than the CM case such that AVM provides a higher bandwidth harmonic extraction. The end result is that the whole system has higher steady-state performance and faster dynamic response yielding superior power quality compared to the CM case.

For the purpose of easy analysis and controller design, easy to use SAF compensated system models are developed. The simplified linear models of the SPSAF and the TPSAF compensated systems are derived at low frequency and high frequency. HIC and RDC can be designed by means of the linear analysis of the high frequency model whereas FCC could be designed by means of the linear analysis of the low frequency model in MATLAB-Simulink. Using the 2.5 kW SPSAF and 10 kW TPSAF compensated system parameters in these simplified models, the controller gains could be easily determined and the approximate controller performances could be predicted without time consuming simulations and costly experiments.

Via simulating the detailed models of the 2.5 kW SPSAF and 10 kW TPSAF compensated systems in Ansoft-Simplorer, the harmonic isolation and the load voltage regulation performances are thoroughly evaluated. It is observed that the performances of the SAF compensated systems using AVM are superior to the SAF systems using CM regarding both harmonic isolation and load voltage regulation as explained below. For SPSAF, the harmonic voltage of the V-type load, which results the harmonic distortion on the line current of $THD_I$ = 97.01, is isolated to the extent that $THD_I$ = 13.75% for the CM case and $THD_I$ = 5.97% for the AVM case. Against 35% line voltage sag, the response of the SPSAF system using the only feedback controller of FCC is such that the maximum load voltage drop ($\Delta v_{sag}$) is 12.2% with the settling time ($\Delta t_{sag}$) of 200 ms for the CM case and $\Delta v_{sag}$ = 4.4% and $\Delta t_{sag}$ = 40 ms for the AVM case. For TPSAF, $THD_I$ falls to 9.91% for the CM case and to 3.95% for the AVM case from 58.87%. Against 35% three-phase line voltage sag, the response of the TPSAF system using the only feedback controller of FCC is such that $\Delta v_{sag}$ = 10.5% and $\Delta t_{sag}$ = 200 ms for the CM case and $\Delta v_{sag}$ = 6.1% and $\Delta t_{sag}$ = 60 ms for the AVM case. Hence, AVM provides better than 100% harmonic isolation performance enhancement and approximately 100% load voltage regulation performance enhancement over CM.

To verify the theory and simulations, laboratory SPSAF and TPSAF systems were built and tested thoroughly. By means of the experimental setups of the SAF compensated systems, the harmonic isolation and the load voltage regulation performances are reported to prove the theory of SAF and verify the simulation results. The validity of AVM and the superior performance of AVM to CM are also proved via these experiments. In the experiments, when SPSAF is in standby mode $THD_I$ = 79.4 and this harmonic distortion decreases to 15.8% for the CM case and to 6.6% for the AVM case. For TPSAF, $THD_I$ falls to 11.1% for the CM case and to 5.0% for the AVM case from 72.3%. Hence, AVM provides higher than 100% harmonic isolation performance enhancement as deduced from the simulation results. Although the load voltage regulation is maintained against the line voltage and load power disturbances as in the simulations, the experimental results cannot be compared to the simulation results since voltage sags could not be realized as in the

simulations with zero fall time. Fortunately, it is obvious from the experimental results that the load voltage regulation performance is better for the AVM case than the CM case except that there is load voltage regulation performance degradation in three-phase AVM case due to improper analog measurement circuits.

Overall, this thesis covers the design, control, and implementation of SPSAF and TPSAF with a novel load voltage harmonic extraction method. With the innovation of AVM, the harmonic isolation and load voltage regulation performances of the SPSAF and TPSAF compensated systems are significantly improved.

As future work, improvements in the load voltage regulation of TPSAF with AVM should be considered. The diode rectifier which has been utilizied throughtout this work as auxiliary power supply for the SAF should be replaced with PWM rectifier to provide better performance. The load voltage regulation of the SAF systems against other utility power quality problems such as voltage swell and flicker should also be investigated.

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