OUTPUT VOLTAGE CONTROL OF A FOUR-LEG INVERTER BASED THREE-PHASE UPS BY MEANS OF STATIONARY FRAME RESONANT FILTER BANKS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

EYYUP DEMİRKUTLU

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
THE DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

DECEMBER 2006

Approval of the Graduate School of Natural and Applied Sciences

_____
Prof. Dr. Canan Özgen
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

_____
Prof. Dr. İsmet Erkmen
Head of Department

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

_____
Asst. Prof. Dr. Ahmet M. Hava
Supervisor

Examining Committee Members

Prof. Dr. Aydın Ersak	(METU, EE)	_____
Asst. Prof. Dr. Ahmet M. Hava	(METU, EE)	_____
Prof. Dr. Yıldırım Üçtuğ	(METU, EE)	_____
Prof. Dr. Kemal Leblebicioğlu	(METU, EE)	_____
Dr. Recep Görür	(ELSİS Co.)	_____

I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Name, Last name : Eyyup Demirkutlu

Signature :

ABSTRACT

OUTPUT VOLTAGE CONTROL
OF A FOUR-LEG INVERTER BASED THREE-PHASE UPS
BY MEANS OF STATIONARY FRAME RESONANT FILTER BANKS

Demirkutlu, Eyyup
M.S., Department of Electrical and Electronics Engineering
Supervisor: Asst. Prof. Dr. Ahmet M. Hava

December 2006, 258 pages

A method for high performance output voltage control of a four-leg inverter based three-phase transformerless UPS is proposed. Voltage control loop is employed and the method employs stationary frame resonant filter controllers for the fundamental and harmonic frequency components. A capacitor current feedback loop provides active damping and enhances the output voltage dynamic performance. The controller design and implementation details are given. Linear and nonlinear loads for balanced and unbalanced load operating conditions are considered. The steady-state and dynamic performance of the UPS are investigated in detail. A scalar PWM method with implementation simplicity and high performance is proposed and implemented. The control and PWM methods are proven by means of theory, simulations, and experiments.

Keywords: Three-phase, four-leg, four-wire, inverter, PWM, space vector, resonant filter, stationary frame, voltage control, THD, UPS, rectifier, active damping, switching loss, SVPWM

ÖZ

DURAĞAN KOORDİNATLARDA REZONANS SÜZGEÇ BANKASI KULLANARAK DÖRT BACAKLI EVİRİCİ TABANLI ÜÇ FAZLI KGK´NIN ÇIKIŞ GERİLİM DENETİMİ

Demirkutlu, Eyyup
Yüksek Lisans, Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi: Yrd. Doç. Dr. Ahmet M. Hava

Aralık 2006, 258 sayfa

Dört bacaklı eviricili, üç-fazlı, transformatörsüz bir kesintisiz güç kaynağının (KGK) çıkış gerilimini yüksek başarımla denetleyen bir yöntem geliştirilmiştir. Yöntemde gerilim çevrimi kullanılmakta ve çıkış gerilimi, durağan eksen takımında temel bileşen ve harmonik rezonans süzgeçleri ile denetlenmektedir. Kondansatör akımı geribeslemesi kullanılarak etkin sönüm oluşturulmakta ve çıkış gerilimi dinamik başarımı iyileştirilmektedir. Doğrusal ve doğrusal olmayan yükler, dengeli ve dengesiz yükleme koşulları incelenmiştir. KGKnın kararlı hal ve dinamik başarımı ayrıntılı incelenmiştir. Basit ve yüksek başarımlı skaler bir darbe genişlik modülasyon (DGM) yöntemi geliştirilip uygulanmıştır. Denetim ve DGM yöntemlerinin başarımı teori, bilgisayarla benzetim ve deneysel çalışmalarla doğrulanmıştır.

Anahtar Kelimeler: Üç faz, dört bacak, dört iletken, evirici, darbe genişlik modülasyonu (PWM), uzay vektörü, rezonans süzgeç, durağan koordinatlar, gerilim denetimi, THD, KGK, doğrultucu, etkin sönümlendirme, anahtarlama kayıpları, SVPWM

To My Parents, Bahattin and Şengül,
To My Niece, Ayşe İrem,
To My Nephew, Kerem,
And to all members of my family

for their patience and support
in all aspects of my life

ACKNOWLEDGMENTS

I would like to express my sincerest thanks to Asst. Prof. Dr. Ahmet M. Hava for his guidance, support, encouragement and valuable contributions during my graduate studies. His impressive knowledge and technical skills have been a model for me to follow.

I express my deepest gratitude to my family, my father Bahattin, my mother Şengül, my sister Kadriye, my brother Yakup, my sister-in-law Betül, my niece Ayşe İrem, and my nephew Kerem for their support throughout. Without their endless love and encouragements, I would not complete this thesis.

I would like to acknowledge TÜBİTAK for the scholarship and financial support for the hardware through the EEEAG research project grant number 104E009. Also partial funding for the hardware in this project was supplied by METU Graduate School of Natural and Applied Sciences project number BAP-2004-07-02-00-121.

Special appreciation goes to Süleyman Çetinkaya, Hasan Özkaya, and Mutlu Uslu for sharing their knowledge and valuable times with me during experimental studies. I also would like to thank my officemates Ömer Göksu, Mehmet Can Kaya, Ersin Küçükparmak, Osman Selçuk Şentürk, Emre Ün, Bülent Üstüntepe, Hazem Zubi and all my friends for their help and support.

I am grateful to my dear friends Mehmet Deniz and Tolga Keskin for their encouragements and support.

I wish to thank to Middle East Technical University Department of Electrical and Electronics Engineering faculty and staff for their help throughout my graduate studies.

TABLE OF CONTENTS

LIST OF FIGURES

FIGURES

LIST OF TABLES

TABLES

CHAPTER 1

INTRODUCTION

1.1. Electric Power Quality

The modern era involves electric power utilization in most aspects of life. From computers to house appliances, from railway systems to hospitals, from offices to industrial plants, all modern era technology equipment and devices require electrical energy. Most of the electrical energy demand is supplied by the AC utility grid. In residential areas as single-phase and in large infrastructures and industrial plants as three-phase, the AC power is widely utilized by the modern society.

As the modern society is strongly dependent on the AC electric power, its continuity and high quality become important. A clean sinusoidal voltage with constant magnitude and frequency is demanded by the customer (50 Hz, 220V rms per phase in most of the world). For three-phase systems also perfect balance among the phase voltages is demanded. Furthermore, the power must be continuous (uninterrupted). However, meeting these demands is impossible as contingencies and power quality problems such as harmonics, notching, surges and sags are frequent and well reported [1]. While some of the problems are due to natural causes such as lightning, and some others due to poor/inadequate power line infrastructure, some other problems have been created as side products of modern technology. In fact, power quality problems have increased over years as the modern power electronic equipments such as motor drives, switch mode power supplies were introduced to the society for their superior load side performance. Such loads have distorted the AC line voltage due to their non-sinusoidal input currents and as such nonlinear loads

increased in size and quantity the resulting negative impact on the power line quality has become alarming. On the one hand, power electronics has been beneficial to the society as it has improved the performance of the equipment using this technology. On the other hand, negative impact on the power line has been made. As the benefits have overwhelmed the disadvantages, the surge of the power electronics technology has become unavoidable. Today most of the electrical energy is processed through power electronics equipment while it travels from the AC grid to the final load. Thus, the power electronics device based AC utility line power quality problems have become challenging for electrical engineers. Considering the significant amount of power electronics related, natural phenomena related, and power system infrastructure related power quality problems, some critical loads requiring continuous and clean power can not be directly fed from the AC power line.

1.2. General Introduction to Uninterruptible Power Supplies

As a result of the significant power quality problems at the AC utility grid, there has been a growing demand for clean, reliable AC power supplies and power conditioning equipment to keep electrical and electronic equipment operating under all circumstances. Critical loads such as computer systems, security systems, communication systems, hospital equipment, critical process control equipment and on-line management systems require clean and reliable AC electric power. Uninterruptible Power Supply (UPS) systems provide uninterrupted, reliable and high quality power for such critical loads. UPS systems not only protect sensitive loads against power interruption, overvoltage (surge) and undervoltage (sag) conditions, but also suppress AC power line transients and harmonic disturbances.

Generally, an ideal UPS should be able to deliver uninterrupted power, and at the same time provide the necessary power conditioning for the particular application. Therefore, an ideal UPS should provide the following features to the customer [2]; regulated sinusoidal output voltage with low Total Harmonic Distortion (THD_v) independent from the changes in the input voltage or in the load, on-line operation

that means zero switching (transitioning) time from normal to back-up mode and vice versa, high efficiency, high reliability, low Electro-Magnetic Interference (EMI) and low acoustic noise, low maintenance, and low cost, weight, and size. In some applications galvanic isolation between the input and output is also necessary. The UPS should also be AC utility grid friendly. While it draws power from the AC grid, the UPS should not disturb or pollute the AC line. The input current should be sinusoidal and with low THD_v. The input power factor should be unity. It should also not emit EMI to the AC line. In the following, the output performance index definitions and their standard values for modern UPS systems will be summarized.

1.3. UPS Output Performance Criteria

The steady-state and dynamic output voltage characteristics of a UPS determine its output performance. For steady-state, the output voltage performance characteristics are defined for nonlinear and unbalanced loads as such loads provide the most challenging operating conditions. Since a nonlinear load draws a current waveform with high harmonic content, it results in large UPS output voltage distortion. The shape of the current waveform (specifically the current waveform peak value) is a determining factor in defining the load type and therefore the distortion in the output voltage. For this purpose the load current crest factor is defined in the following.

Crest Factor: The ratio of the current waveform peak value to its RMS value is defined as the Crest Factor (CF) as given in (1.1). For a linear load, when the voltage supply is an ideal sinusoidal waveform, the load current becomes a pure sine wave and therefore the peak to the RMS ratio of the load current takes the $\sqrt{2}$ value. However, for non-sinusoidal voltage source and/or nonlinear load case, the CF value increases. For the diode rectifier with capacitive filter at the DC bus, the CF value can be large (3 to 5). For UPS applications the typical worst case is a CF of 3 with the RMS value of the load current being equal to the rated RMS value. When the voltage supply is an ideal sinusoidal supply with zero internal impedance and no distortion, the nonlinear load may draw a current with high CF. However, if the

supply has a finite impedance and is not a pure sinusoid, and then the CF typically can not be increased to high values such as 3. Thus, the CF achievable in a UPS system also depends on the UPS design parameters and control methods involved.

$$CF = \frac{I_{peak}}{I_{rms}} \tag{1.1}$$

For a three-phase UPS, the load can be balanced three-phase load, a single-phase load, a load connected line-to-line, or any combination of these. Also, the loads connected could be linear or nonlinear. Such loads may cause an output voltage unbalance which will be discussed shortly. However, the prime UPS output voltage performance characteristics which are the voltage regulation and the voltage total harmonic distortion shall be discussed first.

Voltage Regulation: At steady-state the output voltage of a UPS should be maintained at the rated value regardless the operating condition. Specifically, the output voltage fundamental component RMS value should be within a defined tolerance band. Since the output voltage variation is mainly loading dependent, the two extreme cases for loading define the two extremes in terms of output voltage RMS value. While the no-load operating condition usually provides the highest UPS output voltage, the rated load defines the lowest output voltage. In a high performance UPS system, the output voltage is regulated well such that the output voltage at full-load does not deviate from the no-load value noticeably. Indicating the output voltage variation in terms of the rated output voltage, the voltage regulation (VR) is the percent variation of output voltage fundamental component from no-load to full-load and is given in (1.2). In the equation V_{nlrms1} is the no-load output voltage fundamental component RMS value and $V_{ratedrms1}$ (full-load) is the full-load output voltage fundamental component RMS value. Based on this definition, an ideal UPS has zero VR and in a practical UPS a small VR is required. Typically, a UPS with a VR of 1% or less is accepted as a high quality UPS in terms of output voltage regulation. Acceptable limits of VR in standard UPS systems are listed in Table 1.1.

Since an unbalanced load poses significant deviations in the output voltage fundamental component, the unbalanced load case VR is less constrained and as the table indicates a value of 3% is acceptable under extreme unbalance [3].

$$VR(\%) = \frac{V_{nlrms1} - V_{ratedrms1}}{V_{ratedrms1}} \times 100 \tag{1.2}$$

Table 1.1 Maximum limits of the voltage regulation

Balanced load	Unbalanced load
2%	3%

Output Voltage Total Harmonic Distortion: A UPS system employs a voltage source inverter that generates high frequency output voltage pulses that are filtered by an LC filter so that the UPS output voltage is free of the so called switching frequency harmonics. As the LC filters can only partially suppress the inverter harmonics, the output voltage may contain a small amount of distortion. When loaded by linear and nonlinear loads the output voltage may further degrade. In particular, nonlinear loads draw distorted current waveforms from UPS systems. The harmonic currents result in an output voltage distortion due to the finite output impedance of the UPS. The steady-state output voltage distortion is quantified with the total harmonic distortion (THD_v) given in (1.3) where V_{rms} is the rms value of the output voltage and V_{1rms} is the rms value of the fundamental frequency component of the output voltage. This value is defined for the full-load operating condition. In state of the art UPS systems, the output voltage THD_v limits are summarized in Table 1.2. While standard UPS products provide better than 3% THD_v for linear loads and 5% for nonlinear loads, the high performance UPS systems provide a cleaner output voltage with smaller THD_v values.

$$THD_V(\%) = \sqrt{\frac{V_{rms}^2 - V_{1rms}^2}{V_{1rms}^2}} \times 100 \tag{1.3}$$

Table 1.2 Maximum allowable THD_V values

$THD_v(\%)$	Linear load	Nonlinear load
Standard UPS	3	5
High performance UPS	2	3

Voltage Imbalance: In three-phase UPS systems the output phases may not be loaded equally and load imbalance may exist among the phases. In such cases the output voltages may be affected differently due to different loading conditions. If a proper compensation mechanism is not implemented in the control algorithm, the output voltages may become unbalanced resulting in performance problems both at the load side and in the UPS. The steady-state output voltage imbalance is defined in various forms. According to the NEMA definition given in (1.4) the output voltage imbalance is defined in terms of UPS output line-to-line voltages [4], [5].

$$V_{unbalance}(\%) = \frac{Maximum\ deviation\ from\ the\ mean\ of\ \{V_{ab}, V_{bc}, V_{ca}\}}{Mean\ of\ \{V_{ab}, V_{bc}, V_{ca}\}} \times 100 \tag{1.4}$$

The more standard and comprehensive definition of voltage imbalance [6], [7], [8] is based on symmetrical components approach. In this approach the output voltage is decomposed to its positive, negative, and zero sequence components. The steady-state output voltage imbalance is defined for the negative and zero sequence components in percentage of the positive sequence component of the output voltage as given in (1.5) and (1.6). In this thesis, this symmetrical component decomposition based approach will be employed to quantify the output voltage imbalance. In state

of the art UPS systems the output voltage imbalance for both components is typically less than 1% under the worst case load imbalances.

$$V_{unbalance\_negative}(\%) = \frac{V_{negative\_sequence}}{V_{positive\_sequence}} \times 100 \tag{1.5}$$

$$V_{unbalance\_zero}(\%) = \frac{V_{zero\_sequence}}{V_{positive\_sequence}} \times 100 \tag{1.6}$$

Dynamic Response: In addition to the steady-state performance characteristics given above, the dynamic performance of a UPS is also a determining factor of the UPS power quality. Specifically the loading transients may be too strong for a UPS that deep output voltage sags followed by oscillatory response may result. Likewise, rapid load reduction may have similar effect on the output voltage performance. Such dynamics may degrade the UPS performance and cause nuisances to other loads fed from the same UPS or even result in failure or shutdown of the UPS system disabling all the loads. Therefore, the dynamic performance of the UPS is critical in many applications and it is a measure for the overall acceptance of a UPS. In a UPS with good dynamic performance the loading and unloading transients are manipulated rapidly and with minimal output voltage deviation from the ideal output voltage waveform. For this purpose the output voltage maximum deviation from the rated value is given as the measure of UPS dynamic performance. Described with the aid of Figure 1.1, the maximum output voltage deviation from the rated value, which is more frequently a lost voltage (corresponding to a sag during a loading transient) than a surge, is given in (1.7) in percentage of the rated output rms voltage.

In this equation, ΔV is the difference between the initial voltage value given as $V_{initial}$ and the dip point of the voltage. For this purpose as the worst case loading transient, the peak of the sinusoidal voltage is considered as the initial voltage and typically the voltage dip percentage should be less than 20% in a high dynamic performance UPS.

$$V_{dip}(\%) = \frac{\Delta V}{V_{initial}} \times 100 = \frac{\left|V_{initial} - V_{dip}\right|}{\left|V_{initial}\right|} \times 100 \tag{1.7}$$

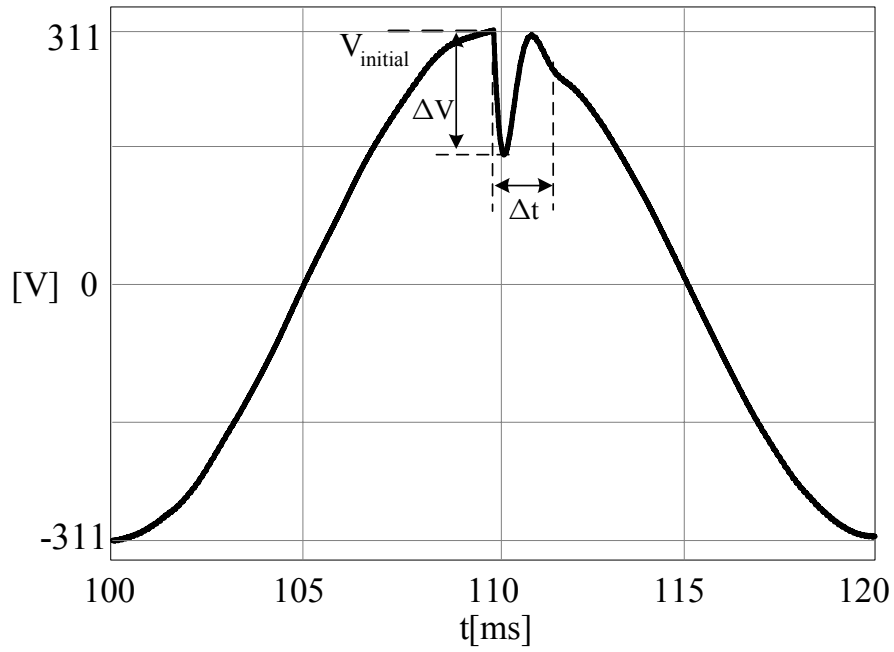


Figure 1.1 Dynamic response of a UPS to impact loading.

In addition to the dip, the duration of the sag (shown in Figure 1.1 as Δt) is also an important factor determining the dynamic performance. If the duration of the sag is small, the voltage dip percentage may not be too harmful to many loads involving energy storage elements (such as power supplies with diode rectifier front end involving large electrolytic capacitors in the DC bus). Thus, a dip larger than 20% may be tolerated provided that the time interval involved remains in several

milliseconds. For this purpose the lost volt-seconds could be considered as another (and perhaps the most meaningful) measure to define the UPS dynamic performance.

1.4. UPS Types

There are two types of UPS systems known as rotary UPS and static UPS. The rotary UPS uses a motor-generator set for isolation, energy conversion, and energy storage. The inertia of the rotating mass provides the energy source for the load during short time power line interruptions and disturbances. Thus, the rotary UPS is capable of providing a continuous, well-regulated power to the load irrespective of the normal mains supply disturbances. Main drawbacks of this type of UPS system are more maintenance and longer transition time (start-up, shut-down times measured in tens of seconds). Rotary UPS systems are larger, heavier, and have lower efficiency when compared to static UPS systems. Rotary UPS systems are less common than the static UPS systems and not subject study of this thesis. Therefore, from here on the focus will be on the static UPS systems and the name UPS will imply static UPS throughout.

Static UPS systems are power electronics based and employ solid-state power semiconductor switches. They have no moving parts. Hence the name static UPS. Static UPS systems consist of a rectifier/charger, a battery set, an inverter, and a static switch. Today, the vast majority of UPS inverters employ Insulated Gate Bipolar Transistor (IGBT) or Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices. And they are of the Voltage Source Inverter (VSI) type, with a DC link supplying voltage to the inverter. Static UPS systems can be classified into three categories: off-line UPS, line-interactive UPS, and on-line UPS systems.

Off-line UPS: Block diagram of an off-line UPS is shown in Figure 1.2. The static switch is on during the normal operation mode, thus the load is supplied from the AC utility line directly. The AC/DC rectifier charges the battery set. When there is a disturbance in the power line the UPS is activated and the load is supplied from the

inverter through the battery bank and the static switch disconnects the AC line. Advantages of the off-line UPS are lower cost, smaller size and weight, and higher efficiency. Switching from the by-pass state to the inverter operating mode and back involves a delay of tens of milliseconds. During this time interval, there is no voltage at the load terminals. During the by-pass mode, the output voltage quality is limited to what the line provides plus some simple disturbance suppressors such as transient overvoltage suppressors. The topology does not provide high output voltage quality and frequency regulation. Therefore, the off-line UPS technology is typically utilized in low power; low degree of criticality applications such as home PC's and typically not employed in critical applications.

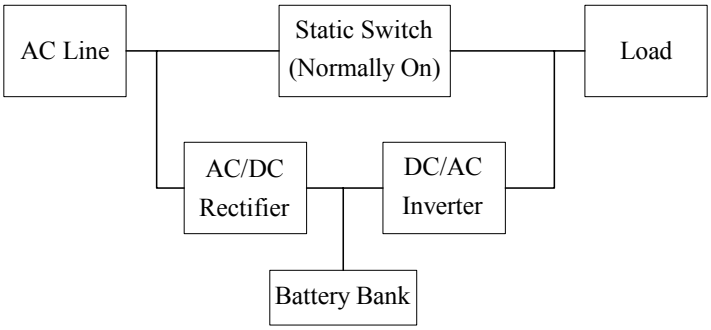


Figure 1.2 System block diagram of an off-line UPS.

Line-Interactive UPS: Line interactive UPS systems consist of a static switch, a series inductor, a bidirectional converter, and a battery bank. In the structure shown in Figure 1.3, a bi-directional AC/DC converter is connected in parallel with the load and operates as a rectifier and it charges the battery during the normal-line periods. When the AC line fails (here failure implies a significant voltage sag, interruption etc.), the bi-directional converter operates as an inverter and supplies the load from the battery set. The static switch disconnects the AC line. The line-interactive UPS has better performance than the off-line UPS. One major advantage of the line-interactive UPS systems is their high energy efficiency typically above 95% rated load efficiency is considered normal while 98% is not unusual. However, the line-interactive UPS does not provide frequency regulation and under line voltage sag

conditions the performance totally relies on the energy storage of the batteries. Therefore, its utilization and performance is limited. The improved version of the line-interactive UPS, the delta-conversion UPS involves a transformer instead of the series inductor. In that case, as shown in Figure 1.4, the transformer primary is fed from the bi-directional converter such that it provides regulation while the power line is available and during the power line failure the transformer is disconnected from the power line via a static switch and the bi-directional converter operates as an inverter and provides all the load power [2].

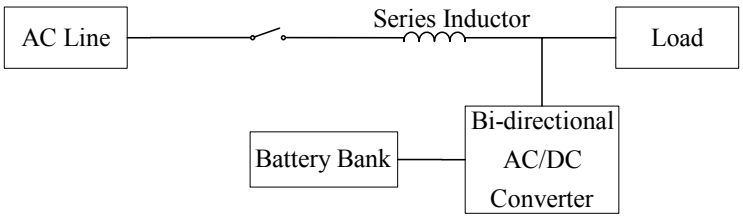


Figure 1.3 System block diagram of a line-interactive UPS.

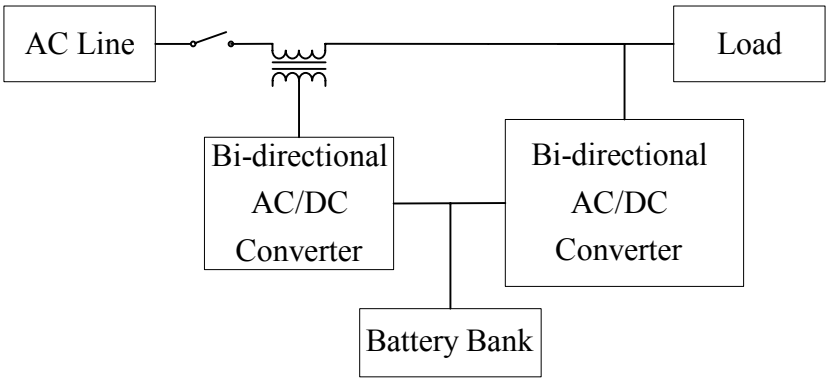


Figure 1.4 System block diagram of a line-interactive delta-conversion UPS.

On-line UPS: Figure 1.5 shows the block diagram of a typical on-line UPS. It is the most commonly used UPS system. The rectifier/charger converts the AC input line voltage to DC voltage, continuously supplies the DC bus, and charges the battery set. The inverter is connected in series with both the AC line and the load. So energy need of the load is delivered through the inverter, continuously. In case of failure

(interruption) in the AC utility line, the charger stops the operation and the inverter draws power from the battery without any discontinuity in the output power, since the inverter is continuously operating. The UPS effectively isolates the load from the main utility power disturbances. Thus the load is not affected from any disturbances (spikes, sags, swells, etc.) on the input AC power line. The UPS generates a clean, well-regulated and stable AC output. At steady-state and transients, it has an excellent performance. When the input voltage is out of pre-defined limits, the inverter is fed from battery and transitions from normal mode to back-up mode or back to normal mode do not cause any interruptions on the output voltage of the UPS. This is the main advantage of the on-line UPS systems. The on-line UPS systems have very wide tolerance to input voltage and frequency variation. The output voltage and frequency regulation is precise regardless the input conditions. Since the inverter is connected in series with the load, power loss on the inverter results in lower energy efficiency compared to line-interactive UPSs. This is the main drawback of this type of UPS system. When the rectifier is of thyristor rectifier circuit type, another disadvantage of using an on-line UPS is lower power factor and higher THD_v at the input. The rectifier that supplies DC bus voltage for the inverter draws current harmonics from the AC line. This problem can be overcome by using a Power Factor Correction (PFC) circuit or a Pulse Width Modulation (PWM) rectifier at the expense of significant increase in the total UPS system cost. However, with decreasing power semiconductor device prices, the on-line UPS technology has become economical for most critical application and gained wide acceptance.

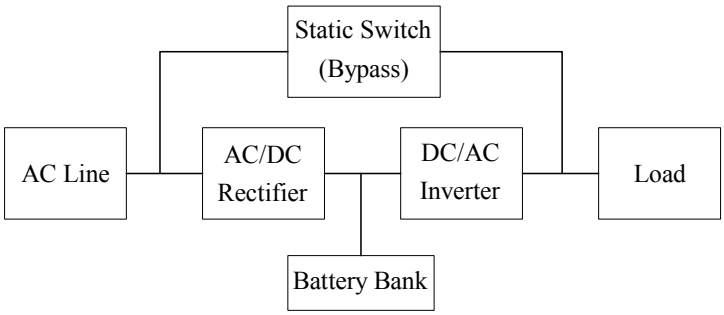


Figure 1.5 System block diagram of an on-line UPS.

1.5. State of the Art On-Line UPS Systems

This thesis involves the on-line UPS systems. Therefore, in the following the state of the art in power converter topologies, PWM methods and control methods for modern on-line UPS systems will be summarized.

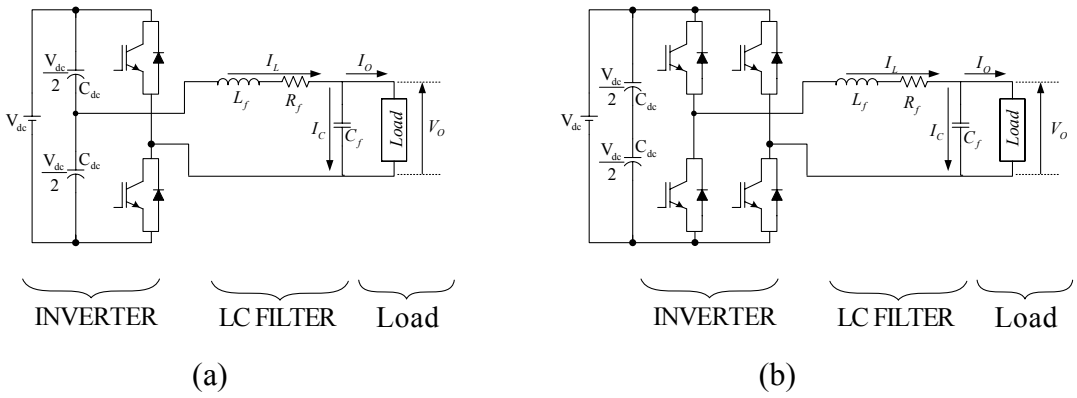
1.5.1. Power Converter Topologies

Power converter topologies used in on-line type UPS systems are classified based on the number of phases, power ratings, and application fields. Today, exclusively voltage source inverters are utilized in UPS systems as DC/AC power conversion units.

Single-phase inverters are used in low power (up to several kVA ratings) UPS applications. Shown in Figure 1.6, for lower cost applications the half-bridge inverter and at higher performance applications the full-bridge inverter is utilized. As shown in Figure 1.6, in the half-bridge topology, the midpoint of the DC bus capacitors is used as load terminal. As a result, the load current charges the DC bus capacitors and causes DC bus voltage fluctuation. Therefore, these capacitors should be chosen as large as possible to minimize the voltage ripple and associated performance degradation at the UPS output. In the half-bridge inverter, the output voltage can be obtained in range of positive and negative values of half of the DC bus voltage ($-V_{dc}/2 \sim V_{dc}/2$). The full-bridge inverter is shown in Figure 1.6.b. In this topology, two legs are utilized to control the output voltage. The midpoint of the DC bus is not used in this topology, thus the DC bus capacitors can be much smaller than those used in the half-bridge inverter. The output voltage is confined to the range of positive and negative values of the DC bus voltage ($-V_{dc} \sim V_{dc}$). Full-bridge inverters are employed in high performance and typically high power UPS applications.

In the half-bridge inverter topology based UPS, unless an isolation transformer is utilized at the UPS output for the purpose of stepping up the voltage, the required DC

bus voltage typically becomes high (800V for the 220Vrms utility grid application). Power semiconductor devices with blocking voltages of 1200V or higher become necessary for such applications. At this voltage level, due to the relatively low conduction losses, IGBTs are the devices of choice. When an isolation transformer is utilized the DC bus can be typically reduced to 60V or less so that the UPS energy storage batteries can be directly connected to the DC bus. In this case, the device to be utilized becomes a power MOSFET. The inverter output voltage is stepped up via the isolation transformer. At increasing power ratings the 800V DC bus approach is preferred as the transformer cost, size, and weight pose a problem.



(a) (b)

Figure 1.6 Single-phase UPS system inverter topologies:
(a) half-bridge inverter, (b) full-bridge inverter.

Three-phase inverters are generally utilized in high power (typically above 10 kVA) and three-phase output applications. There are three popular three-phase inverter topologies employed in state of the art UPS systems.

The first type involves an inverter accompanied with a transformer. Traditionally, three-phase inverters have employed the three-wire three-leg structure. However, three-wire three-phase inverters do not allow for the flow of zero sequence current which is an inevitable fact in three-phase UPS systems due to unbalanced loading. To establish a path for the zero sequence current, the inverter must be complemented with a Δ/Y or Δ/Z transformer such that the secondary of the transformer becomes an

artificial neutral point and the zero sequence current of the load flows through this path. The circuit diagram of the three-phase three-wire inverter with Δ/Y transformer is shown in Figure 1.7. The neutral wire at the output is provided by utilizing a Δ/Y transformer and the star point of the transformer secondary is utilized as the neutral wire. Since this topology requires a large transformer, the UPS size is large and the system energy efficiency is low. The slow response, acoustic noise, and high cost are the other disadvantages of the topology.

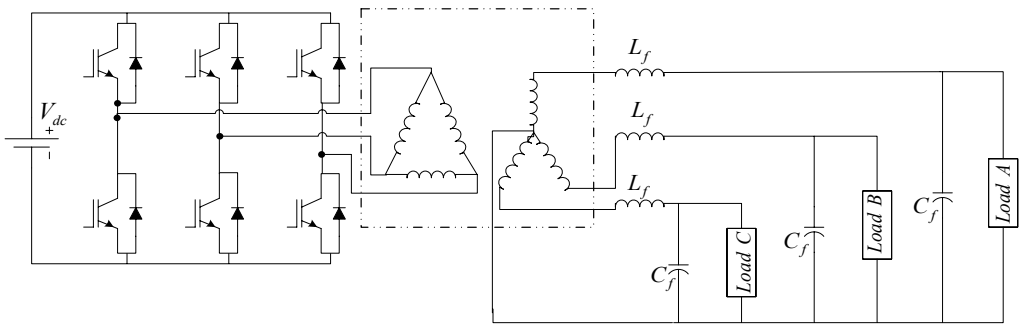


Figure 1.7 Circuit diagram of the three-phase UPS with three-phase inverter with Δ/Y transformer.

The second topology is the three-leg four-wire inverter topology which is based on the half-bridge single-phase inverter topology. In the three-leg four-wire inverter topology, the neutral point of the load is connected to the midpoint of the DC bus as shown in Figure 1.8. This topology can be modeled as three independent single-phase half-bridge inverters. Maximum achievable peak value of the line-to-neutral voltage at the output is half of the DC bus voltage ($V_{dc}/2$). Thus, in order to obtain 220Vrms per phase a large DC bus voltage (typically 800V) is required. As a result the switching and conduction losses of the necessary high voltage blocking devices become significant. This corresponds to limited energy efficiency of the topology (typically much less than 95%) and higher cost of the IGBT devices. In the topology, the neutral wire current flows through the midpoint connection to the DC bus

capacitors and this causes fluctuation on the DC bus voltage. Therefore, large size capacitors should be utilized. Thus the cost increases and the system becomes bulky.

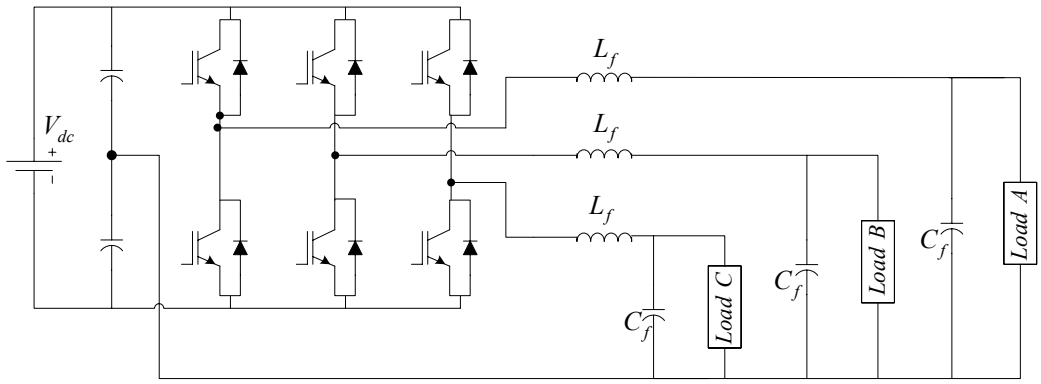


Figure 1.8 Circuit diagram of the three-phase UPS with three-leg four-wire inverter.

The third topology is the three-phase four-leg inverter shown in Figure 1.9. In this topology the fourth leg controls the neutral point potential and provides a path for the zero sequence current flow. The DC bus capacitors are utilized only to remove the ripple on the DC bus (the DC bus midpoint is not utilized; hence there is no capacitor voltage unbalance issue in this converter). Thus the DC bus capacitors employed are relatively small. The maximum achievable peak value of the line-to-neutral output voltage is higher than the value of three-leg four-wire topology ($V_{dc}/\sqrt{3} \approx 0.577V_{dc}$ as compared to $0.5V_{dc}$). As a result, the DC bus voltage level requirement becomes less than the half-bridge inverter based system and the switching and conduction losses decrease, leading to a higher efficiency UPS system. Compared to the three-leg inverter, there are two additional switches. The two additional power switches increase the number of the possible switching states from 8 (=2^3) to 16 (=2^4). Therefore, the PWM methodology and control of the inverter becomes more complex. Due to its topological and control complexity, the four-leg inverter is rarely employed in UPS applications. This thesis focuses on the three-phase four-leg UPS systems. Primarily the PWM methods and the control methods of

this UPS system are the focus of this thesis. Therefore, a discussion on these subjects follows.

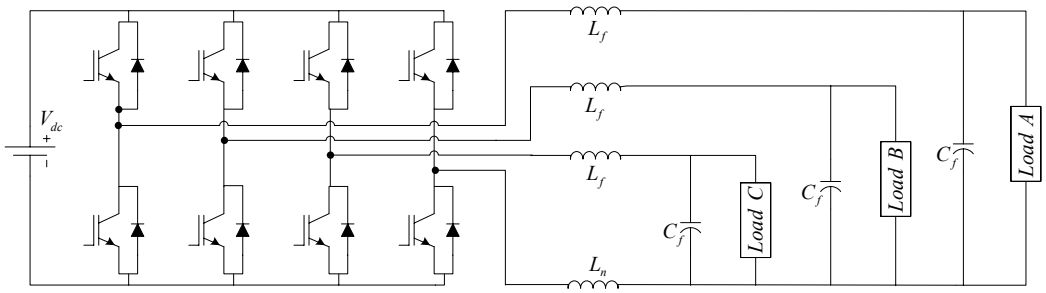


Figure 1.9 Circuit diagram of the three-phase UPS with three-phase four-leg inverter.

1.5.2. PWM Methods

Voltage source inverters are DC/AC converters that synthesize AC output voltages with rectangular pulses from a fixed DC voltage source. By controlling the width of the rectangular DC voltage pulses and their polarity via manipulating the VSI switches the inverter output voltage can be controlled. When the frequency of these pulses is fixed (this is called the carrier or switching frequency) and the width of the pulses is controlled, this approach is called the carrier based Pulse Width Modulation (PWM) technique. There are two methods, namely the scalar PWM and vector PWM methods. In the scalar PWM technique the inverter reference voltage (the modulation wave) is compared with a triangular carrier wave and the intersections define the switching instants. Within a carrier cycle, the output volt-seconds equal the reference volt-seconds. This implies that the output voltage average value over the PWM cycle is equal to the reference voltage. This is called the volt-seconds balance rule. In the space vector PWM method, complex variables are involved and phase quantities are transformed to the complex plane (the vector space). Therefore, the inverter output voltage vectors and their duration define the vector volt-seconds that should be equal to the reference volt-seconds defined in terms of the reference vector and carrier cycle. In either method, since the output voltages consist of pulses, a passive filter is

required to filter out the high frequency output voltage ripple components such that the filtered output voltage will contain signal only at the demanded frequencies. The VSI switches are typically manipulated at high switching frequencies (in UPS applications for power ratings above several hundred kilowatts up to 8-10 kHz, for power ratings below several kilowatts up to 20-30 kHz) in order to keep the filter size and the ripple current small. When utilizing the carrier based scalar or vector PWM methods and maintaining the switching frequency high, the output voltage THD_v becomes low. Whether scalar or vector PWM is utilized, there are various PWM patterns that yield the same output voltage but the other characteristics may not be the same. The switch conduction and switching losses, the voltage linearity, the DC bus and AC output current ripple, common mode voltage, etc. properties are all modulator type (pulse pattern type) dependent. Continuous PWM (CPWM), discontinuous PWM (DPWM), common mode voltage reducing PWM etc. many methods exist. In the three-leg three-wire three-phase standard inverter (the two level inverter), this variety stems from the fact that in a three wire system neutral current can not flow and therefore a zero sequence voltage can be added to the phase reference voltages. As a result, the choice of zero sequence signals and therefore the modulation wave types become infinite. In CPWM methods all inverter legs are switched within each PWM cycle. In DPWM methods, one of the inverter legs is locked to the positive or negative DC rail of the VSI for a full PWM cycle. Hence, this method is called discontinuous PWM. A large number of CPWM and DPWM methods are reported. Additionally, common mode voltage reduction PWM methods have been reported. Although the variety of PWM methods is large, only a few methods are widely employed. Of these, the sinusoidal PWM, DPWM1, and SVPWM methods are the most popular [9], [10].

In conventional three-phase three-leg inverters, the above discussed scalar and vector PWM methods are well established and their implementation is a trivial task. However, applying the same concept to the three-phase four-leg inverter involves difficulties as the number of inverter legs increase by one and the number of possible inverter states double. For the four-leg inverter, first, the three-dimensional (3-D) space vector PWM approach was reported [6], [11]. In this method, the reference

voltage vector has three complex variable components, thus 3-D space vector prism shown in Figure 1.10 is utilized to obtain duty cycles of the voltage vector and thus the duty cycles of the switches. In Figure 1.10, “on” state of the top switch of each leg is symbolized as “1” and “off” state of the top switches is symbolized as “0.” In Figure 1.10, the states are defined in the a-b-c-n sequence. There are two zero (“0000” and “1111”) vectors and fourteen non-zero vectors in 3-D SVPWM. 3-D SVPWM has seven layers as shown in Figure 1.10, and each layer has the same structure utilized in 2-D SVPWM for the three-leg standard three-phase inverter. The reference vector volt-seconds are matched by the three adjacent non-zero voltage vectors and two zero vectors of the four-leg inverter. The determination procedure of the three adjacent vectors is complicated. It involves identifying sectors of the hexagon prism, then the tetrahedrons of each sector and finally the sequence and duty cycle values of the inverter voltage vectors. Although high performance pulse patterns can be programmed with this approach, this procedure is highly complex and computationally involved. Thus, the approach is not favorable and simpler scalar PWM methods have been developed.

The four-leg inverter pulse pattern can also be programmed via scalar PWM methods. The scalar PWM approach involves defining appropriate modulation signals for each leg of the four-leg inverter. Thus modulation waves and triangular carrier waves can be compared to easily generate the inverter switch pulse pattern. This approach has been recently investigated and detailed study for the SVPWM implementation has been reported in [12], [13]. In this case the modulation signal for the fourth leg is generated from the phase reference voltages for the three-phases of the inverter. In the study, the modulation signal of the fourth-leg is termed as the “offset signal” and it is utilized to modulate the fourth-leg switches and at the same time this signal is added to the phase reference voltages to obtain the DC bus center-point referred modulation signals of the associated phases. Thus, the offset signal moves all the phase voltage references (modulation waves) simultaneously upwards or downwards (gives them an offset) to gain certain properties. With this approach, the offset signal can be utilized to reduce the PWM ripple, increase the voltage linearity, reduce the switching losses of the inverter etc. Thus, the offset signal is the

degree of freedom comparable to the zero sequence signal of the three-leg, three wire three-phase inverter. However, in [12], [13] the work is mainly confined to SVPWM and detailed performance attributes are not included in the study. Neither is the approach broad and easy to understand. Thus, further work is required on the scalar PWM approach for the four-leg inverter. One of the two main study subjects and contributions of this thesis involves the scalar PWM methods for the four-leg inverter.

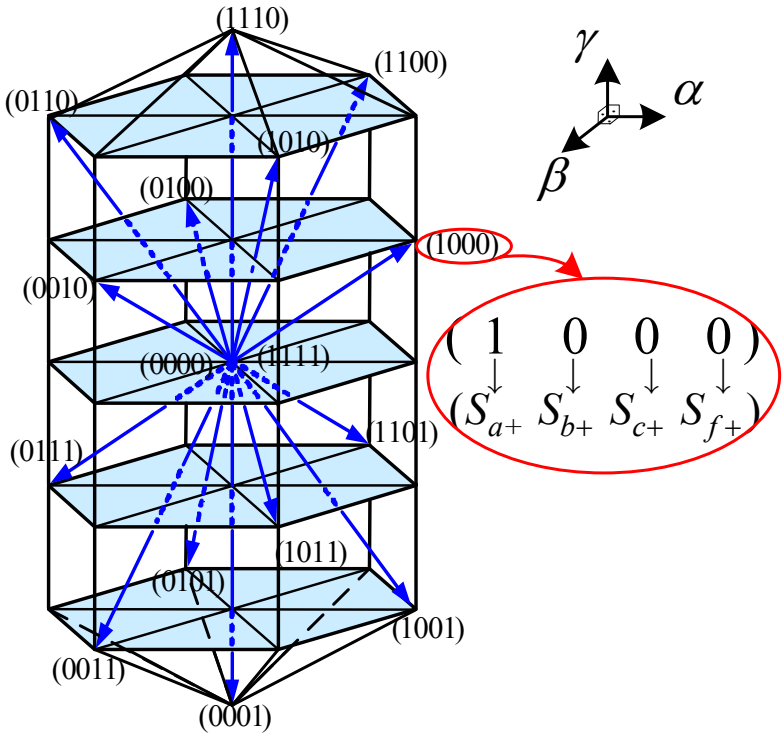


Figure 1.10 3-D Space vector diagram of the four-leg inverter.

1.5.3. Control Methods

Because of the need for high dynamic performance and excellent regulation of the output voltage and frequency, UPS systems must employ feedback control mechanisms. Quite significant variety of control methods for UPS output voltage

control are reported in the literature. Of these, the most popular methods will be discussed in this section.

In UPS systems, a second order LC filter is utilized to eliminate high frequency harmonics created by the inverter via PWM. However, the LC filter is typically small and under open-loop operating condition the UPS may become unstable for nonlinear loads and during load disturbances. The inverter itself can be a source of disturbance. The inverter non-idealities such as dead-time and switch non-ideal characteristics may excite resonance in the LC filter at light and no-load as there is no sufficient damping in the system. Under changing DC bus and load conditions the output voltage is likely to be significantly varying. Moreover, the filter may resonate with the load and as a consequence failure of the UPS and the loads is inevitable. Therefore, open-loop operation of on-line UPS systems is not preferable and closed-loop control with feedback signals is employed as shown in Figure 1.11.

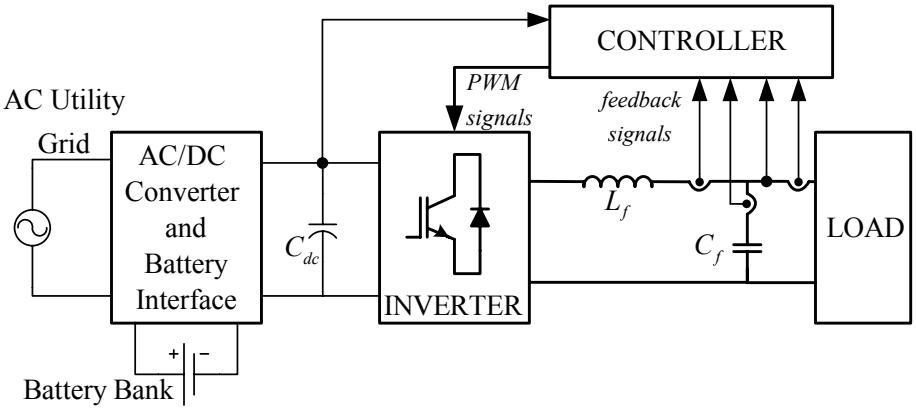


Figure 1.11 General single-phase block diagram of

a closed-loop UPS control system.

An ideal UPS should provide fast dynamic response, well-regulated output voltage and frequency, low output voltage Total Harmonic Distortion (THD_v), stable output waveforms at steady-state, and balanced output voltages. The performance of a UPS

can be tested under the following load conditions: no-load operation, rated loading (resistive, inductive, capacitive, etc.), unbalanced load operation, and nonlinear load operation. First, at no-load operation, the UPS system has the lowest damping. If a controller does not provide high bandwidth and sufficient damping, the system becomes unstable and oscillatory output voltages result. Secondly, when it is loaded, the UPS output voltage should not sag significantly and it should settle at the rated steady-state value rapidly. This defines the system dynamic response. Third, in a three-phase UPS, when the load is unbalanced, the output currents can have positive, negative, and zero sequence components. However, the output voltage should have only a positive sequence component. Therefore, the controller should eliminate the negative and zero sequence components of the output voltage. Finally, nonlinear loads draw current harmonics; these harmonics distort the output voltage. The controller should compensate the output voltage harmonics to have a high quality output voltage. Most commonly applied control methods are reviewed below. In all these controllers except the output voltage rms value controller, instantaneous values of the output voltages are controlled.

1.5.3.1. Output Voltage RMS Value Controller

The RMS value controller is based on controlling of the rms value of the output voltage. This controller has been widely used in most simple UPS applications. The RMS value controller can be utilized for both single-phase and three-phase UPS systems. Typically, in a few fundamental periods (for 50 Hz applications, 20 ms period), it drives the error to zero. If this controller is used in nonlinear load applications, output voltage harmonics can not be eliminated.

1.5.3.2. Output Voltage Instantaneous Value Controllers

1.5.3.2.1. Voltage Loop Controller

Single voltage control loop employs only the output voltage feedback. When this control method is utilized in single-phase applications, the controller manipulates AC signals. Since the output voltage lags the inverter output voltage, controller should compensate this lag with a leading term (derivative) in the regulator. Therefore, Proportional + Derivative (PD) type regulator should be implemented in the single-phase voltage loop controller. Theoretically, the single voltage loop with PD regulator operates excellently. However, the derivative control term in practice can not be made large due to noise sensitivity (due to noise and limited resolution in the measurement). High precision voltage sensors and A/D converters can be used to prevent this type problem, however this increases the cost. Thus, derivative control is rarely used in industry.

1.5.3.2.2. Multi-loop Controller

Due to the problems of obtaining the derivative term of the PD regulator in the single voltage loop controller, the capacitor current feedback can be utilized as a derivative term. The capacitor current is proportional to the derivative of the output voltage ($i_c = C \cdot dv/dt$). Therefore, the derivative term can be obtained from the capacitor current feedback with low cost current sensors (such as current transformer (CT)). In this controller the output voltage controller is a PI controller (typically only a significant P controller for tracking and steady-state response and a very small I controller to remove the very low frequency errors). The capacitor current feedback signal is scaled with a gain and added to the voltage controller output to generate the inverter reference voltage signal. Thus, in this method multi-loop controllers are in parallel structure. The capacitor current feedback term increases the damping, enhances the dynamic performance and reduces the output voltage harmonics [14].

1.5.3.2.3. Cascade Controller

Cascade control is applicable to systems with inner and outer loops where the time constants of the inner and outer systems differ by an order of magnitude or larger. In such a case, the outer loop is the slower loop while the inner loop is the faster loop. In a UPS such a control method can only be applied if the capacitor is relatively large and the inductor small. In this case, the current loop dynamics can be manipulated rapidly. The outer loop is not responsible from harmonic compensation as it is small. The inner loop is responsible from the dynamic performance. Thus, in a UPS, when employing the cascade control principle, the method must be complimented with load current and/or capacitor current feedforward. The capacitor rated current can be calculated from the reference voltage and the capacitance value and fed to the current controller. Likewise, the load current can be measured and fed back to the current controller as a load current disturbance compensation term. Also, the capacitor voltage could be utilized as a decoupling term in the outer controller. In both controllers Proportional Integral (PI) type regulators could be employed, although the integral gain is quite small [15]. Cascade control is not widely utilized due to the fact that in most UPS systems the filter components are of comparable size and the associated time constants are not separable by an order of magnitude. This controller is not favored also due to and the large number of feedback signals needed.

1.5.3.2.4. Deadbeat Controller

The deadbeat control method is unique to discrete time control systems. Hence, only digital implementation is possible. In the method, the system mathematical model must be given. Using the reference and feedback signals, and employing the system model, the control signal (the inverter voltage) that forces the output voltage error to zero in finite number of sampling cycles (of the discrete time system) is calculated and applied to the output. When the system model is exactly known, the error due to changes in the state variables is driven to zero in ideally one step and practically two steps. Thus, the deadbeat controller has a very high bandwidth. However, the

deadbeat control method, which is dynamically very stable for a well defined system, has a drawback that is the dependence on the parameters of the filter. An error in the parameters can make the system unstable. This is the major weakness of the method. In practical applications, the computational delays reduce the performance and measurement delay and errors make the system unstable. The computational delays can be compensated digitally [16], [17], [18]. In order to avoid the measurement delay and error, high precision sensors could be utilized. However, the system cost becomes economically infeasible.

1.5.3.2.5. Repetitive Controller

The repetitive controller is utilized for nonlinear load operation. Since the desired output voltage has only the fundamental component, harmonic components should be suppressed. The harmonic current, which is drawn from the nonlinear load, causes periodical distortion on the output voltage. The repetitive controller learns the periodical errors due to nonlinear load effects, in a few fundamental periods. After learning the error, it compensates the distortion [19], [20], [21]. The repetitive controller is installed as an outer loop to the voltage loop controller to improve the harmonic performance. It is a discrete time linear filter in structure. The main disadvantage involves the slow dynamic response. Additionally, in applications where the AC line frequency varies in a wide range and the output voltage must be synchronized with the AC line, the period (the frequency) of the controller varies and this creates a problem in terms of the performance of the discrete time filter structure.

1.5.3.2.6. Synchronous Reference Frame Based Controller

All the above controllers applied in single-phase UPS applications can also be implemented in three-phase applications via utilizing the complex variable transformations. In the stationary frame, the three-phase three-leg UPS can be controlled as two independent single-phase UPSs (α-β components), and the three-

phase four-leg UPS can be controlled as three independent single-phase UPS systems (α-β-0 components). Further via Synchronous Reference Frame (SRF) transformations the AC quantities can be transformed to DC. Thus control becomes easier with DC signals. The controller methods, reviewed above, can be utilized in conjunction with the SRF transformations.

In the SRF based controllers, when a signal is transformed to a coordinate frame that rotates synchronously with the signal, the signal in this frame becomes a DC signal. A PI regulator can provide zero steady-state error as the integral term has infinite gain at zero frequency [22]. Thus, implementing a controller in this frame becomes an easy task. However, transformation of the system model to the synchronous frame results in cross-coupling terms between the d and q channels which should be cancelled by means of the cross-coupling de-coupling controller. If no such action is taken, the dynamic performance of the SRF controlled system degrades. Also the controller regulates the output only at the synchronous frequency and has no effect on the disturbances. Thus, the negative sequence (which rotates at $-2\omega_e$ at the synchronous frame), and the dominant harmonics such as the 5^{th} and 7^{th} harmonics (which rotate at $6\omega_e$ at the synchronous frame) are not regulated to zero. Further, the d-q model does not include the zero sequence component of the phase voltages and the synchronous frame can not compensate for the effect of the load current zero sequence. Thus, when a single SRF controller is employed, only the positive sequence fundamental component of the output voltage is regulated and all other disturbances degrade the system performance as there is no countermeasure taken. Establishing synchronous frame controllers for each disturbing component is a complex procedure which is laborious. Further, the zero sequence component can not be compensated for with the SRF approach. Thus, a feasible method with high performance is required to realize a four-leg inverter based UPS system.

1.5.3.2.7. Resonant Filter Bank Controller

The resonant filter bank controller approach is closely related to the SRF based approach, but does not require coordinate transformations and it is utilized per phase. The method is based on compensator assignment for each frequency of interest. Thus, the controller has a parallel structure. Various compensator types are possible; however the type shown in the following equation is most widely utilized [23], [24], [25], [26], [27], [28], [29].

$$G_c(s) = \frac{2K_{im} \cdot s}{s^2 + (m\omega_e)^2} \tag{1.8}$$

In the resonant filter compensator of (1.8), K_{im} is the integral gain, ω_e is the angular fundamental frequency, and m is the frequency of interest where infinite gain is demanded. For example, if the resonant filter controller is tuned at the fundamental frequency (m=1), due to infinite gain (and zero phase) at the fundamental frequency, the steady-state error will be zero at fundamental frequency. As the controller has zero gain at all other frequencies, the controller does not influence other frequency components. Thus, for each frequency of interest a resonant filter at that frequency should be utilized. Thus, a parallel control structure results. As this approach has been recently developing, in this thesis the method will be applied to the four-leg inverter based UPS and its feasibility will be shown. As the method does not require positive, negative, zero sequence separation and it is easy to implement, it has been found favorable over other methods briefly discussed above. Thus, the second main contribution of this thesis involves the implementation of the resonant filter bank controller for the four-leg inverter based UPS.

1.6. Scope and The Organization of The Thesis

In this thesis, the three-phase four-leg inverter based UPS system, which is a high efficiency and low stress system is investigated. With proper control and PWM algorithms, such a UPS system can perform satisfactorily overall. While the energy efficiency can be maintained high due to reduced switching losses via discontinuous PWM of the four-leg inverter, the reduced DC bus voltage provides further loss reduction, yielding high energy efficiency. With the path for the load current zero sequence component being provided via the fourth leg and not via the DC bus center point, the voltage ripple and current ripple stress on the DC bus is further reduced. Thus this topology is a favorable three-phase transformerless UPS topology and forms the focus of this thesis.

The thesis has two main contributions to the four-leg inverter based UPS. One of the main contributions involves the simplification and generalization of the scalar PWM methods for the four-leg inverter. Via methodical and detailed study, the scalar PWM approach that has recently been found favourable over the space vector implementation in the standard three-leg inverters has also been applied to the four-leg inverter. The basic approach yields a zero state partitioning function based PWM signal generation. With this approach superior PWM patterns with various optimization criteria can be developed. The SVPWM and DPWM1 are the special cases of this general approach. A PWM algorithm which reduces the switching losses to a possible minimum value has been developed. The minimum loss DPWM (MLDPWM) method specifically provides advantage over the standard DPWM1 method for unbalanced load.

The second main contribution of this thesis involves the control structure of the four-leg inverter based UPS. Utilizing the voltage loop controller supplemented with the capacitor current feedback as active damping loop, a multi-loop structure has been established. While for the capacitor current feedback a proportional gain is utilized, for the voltage loop a resonant filter bank is favored. Designing the resonant filter bank with proper resonant filter components such as the fundamental component

filter, third harmonic filter, 5^{th}, 7^{th}, 9^{th}, 11^{th}, etc. the fundamental component output voltage can be precisely regulated while all the harmonic disturbances are rejected. Thus UPS system with high control performance could be realized. The PWM and control algorithms have been implemented on a 5-kVA UPS and the theory has been verified experimentally.

The organization of the thesis is given in the following.

In the second chapter, PWM techniques are analyzed in detail. The historically earlier developed 3-D space vector PWM method and the easier to implement scalar PWM methods are investigated. The 3-D space vector PWM method is summarized and the vector volt-seconds principle and the choice of the voltage vectors and the proper vector sequence discussed. The implementation difficulties are demonstrated. The scalar PWM method is summarized and a zero state partitioning function based generalization for the scalar PWM methods is developed. With the partitioning function being the degree of freedom in establishing a PWM pattern type, several scalar PWM methods with various optimization criterion are developed from this function. The SVPWM method which yields low PWM voltage/current ripple, the DPWM method which yields reduced switching losses are derived as a function of the partitioning function. The MLDPWM method, which yields minimum switching losses even under unbalanced, inductive (lagging) and capacitive (leading) load conditions, is developed and its performance is discussed in detail. The voltage linearity range and limitations of the approach are discussed in detail in this chapter.

The third chapter of the thesis addresses the output voltage control issues of the four-leg inverter based UPS. Various control methods are discussed and then the resonant filter bank based control approach which is the second main contribution of this thesis has been studied in depth. In this chapter the UPS system S domain model is established and via derivations and block diagrams the input to output and disturbance to output transfer functions are shown. A capacitor current feedback based active damping is included to improve the system stability and the effect of

this compensator on the system behaviour is demonstrated via analytical investigation.

In the fourth chapter, the detailed modelling and computer simulation of a 5-kVA, 50-Hz, 120-Vrms output four-leg inverter based UPS is provided. Following the establishment of the simulation model, the controller tuning procedure is described. Then the UPS control performance is investigated for steady-state and dynamic operating condition for various loading conditions such as linear, nonlinear, balanced, unbalanced loads. The superior steady-state and dynamic performance of the proposed control method is illustrated by means of computer simulations involving steady-state and dynamic loading conditions. The chapter concludes with the study of the steady-state performance of the scalar PWM methods.

The fifth chapter of the thesis covers the experimental studies of the 5-kVA system studied in the fourth chapter. In this chapter the experimental system hardware and software are discussed in detail. The steady-state performance under various load conditions and dynamic performance under loading transient conditions is shown via laboratory experiments. Correlation with the theory and computer simulation study results is provided.

The sixth chapter summarizes the research results, recommends future work on the study subject of this thesis, and concludes the thesis.

CHAPTER 2

PULSE WIDTH MODULATION TECHNIQUES FOR FOUR-LEG INVERTER BASED THREE-PHASE UPS SYSTEMS

2.1. Introduction

Voltage Source Inverters (VSI) are utilized to convert a fixed DC voltage source to a controllable AC output voltage. Since the DC voltage is fixed, to generate an output voltage with controllable frequency and magnitude, the switches should be manipulated in a manner to generate rectangular output voltage pulses that meet the output voltage requirement. One method involves manipulating the switches at a frequency that is equal or close to the intended output frequency. For example, for the three-phase three-leg standard inverter, one such method is the six step operating mode which involves operating the switches at the fundamental frequency of the desired output. However, in such a case the low frequency harmonics on the output voltage (odd harmonics such as the third, fifth, etc.) become significant and in the UPS application, the passive filtering requirement becomes prohibitive in terms of filter size and cost. Therefore, the switches are operated at a frequency significantly higher than the output voltage fundamental frequency. Since modern IGBT switches are highly efficient and their switching losses can be highly tolerable at the kHz range, the high frequency operation of the inverter switches is a standard approach.

One standard approach to operate the inverter switches is the pulse width modulation (PWM) approach. In the PWM approach, a fixed switching frequency and associated cycle are defined and the inverter switches are manipulated in each such cycle (the PWM cycle) once on and off. Since the DC bus voltage is fixed, to control the output

voltage the polarities and the width of these rectangular pulses are controlled. Further, the switch state positions for each inverter leg within a PWM cycle are coordinated such that the output voltage pattern in each PWM cycle results in specific performance attributes.

The basic principle of generating the switch logic signals and thus the transistor gate drive signals is the volt-seconds balance principle. Since an inverter is considered a voltage amplifier, a reference voltage must be provided. Given the reference voltage, the inverter switches should be manipulated such that the reference volt-seconds and output volt-seconds must be equal over each PWM cycle. Methods to generate the switching signals for the inverter switches operate based on this principle. Since the inverter output voltages are rectangular pulses with varying width, their harmonic spectrum includes terms in the switching frequency range and its multiples. Thus, passive filters are required to filter the output voltages and obtain sinusoidal currents. Since the switching frequency is quite higher than the output voltage fundamental frequency, the passive filter size becomes small and economical. Thus, the standard approach to manipulating the switches of modern VSIs is the PWM approach.

One standard approach to generate the switch gate logic signals is the scalar PWM approach where a triangular wave (the carrier wave) is compared with the scaled reference voltage waveform (the modulation wave) and the intersection points of the modulation wave (typically a sinusoidal signal) and triangle define the switching instants. For the upper switch of an inverter leg, if the modulation wave is greater than the triangular wave, the switch signal is set high (ON) and otherwise it is set low (OFF). The lower switch is operated with complementary logic to the upper leg and a blanking time is inserted between the two switch signals such that a DC bus shoot-through is avoided. Since in this approach the width of the switch on signals and thus the output voltage rectangular pulses is modulated, the process is termed as pulse width modulation. The reference voltage waveform is called the modulation wave. Since a triangular carrier wave is utilized, the reference and output voltage average value have a linear relations such that the volt-seconds rule is adhered for each PWM cycle. As will be discussed in detail shortly, in three-phase two-level inverters with

no DC bus center-point connection (full-bridge configurations), the choice of modulation signals is not unique (due to the existing degree of freedom) and each modulation wave results in different performance characteristics regarding the output voltage ripple, voltage linearity range, DC bus capacitor current ripple, etc. As a result there exists variety of PWM methods and their performance characteristics vary significantly. Before further investigations, it is necessary to define the modulation index definition which involves the main performance evaluation variable in a PWM method.

The performance of a modulation method depends on voltage utilization level. In order to quantify the voltage utilization level, modulation index term is used. The modulation index (M_i) can be defined as given in (2.1). The definition is made for the three-phase, two-level, three-leg inverter. However, it equally holds for the four-leg inverter. In the equation, V_{1m} is the fundamental component magnitude of the line to neutral inverter output voltage and $V_{1m6step}$ is the fundamental component magnitude of the six-step mode voltage. $V_{1m6step}$ can be calculated by utilizing (2.2) where V_{dc} is the DC bus voltage of the inverter.

$$M_i = \frac{V_{1m}}{V_{1m6step}} \tag{2.1}$$

$$V_{1m6step} = \frac{2V_{dc}}{\pi} \tag{2.2}$$

As shown in Figure 2.1, in the four-leg inverter, the UPS output voltage controller generates the three-phase reference voltages that the inverter must match. These signals are fed to the PWM block to generate the inverter switch logic signals. The logic signals are converted to the gate drive signals to operate the power transistors such that the output volt-seconds become to the reference volt-seconds over each PWM cycle. In the following, the above briefly discussed scalar PWM method and the space vector PWM method will be detailed for the four-leg inverter with the UPS application being the focus.

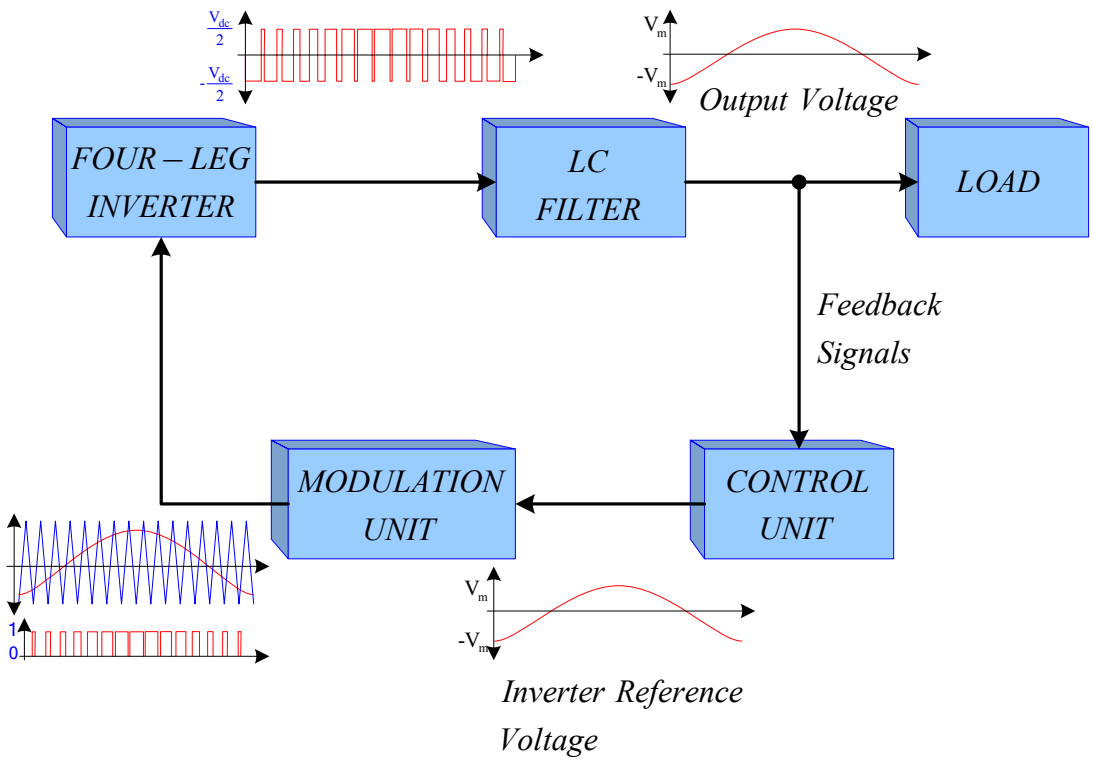


Figure 2.1 The general block diagram of the four-leg inverter based UPS system.

2.2. Scalar and Space Vector PWM Methods

PWM methods can be classified mainly according to the implementation technique employed as space vector PWM and scalar PWM. In this thesis, in contradiction to the traditional approach, the space vector PWM approach is reviewed first. Because for the four-leg inverter, historically, the space vector PWM method was developed prior to the scalar PWM method.

2.2.1. Space Vector PWM

In the space vector PWM approach, the three-phase inverter output voltages are transformed to complex variables. Thus, the output voltages are transformed to a

vector in the complex variable space. Hence, the name space vector. The duty cycles of the inverter switches are generated by means of the complex variable volt-seconds balance rule. The inverter output voltage vectors and their duration define the vector volt-seconds that should be equal to the reference volt-seconds defined in terms of the reference voltage vector and carrier cycle. When the zero voltage vectors are selected equal and pulse sequence is set symmetric, the pulse pattern is assigned the name space vector PWM (SVPWM) method. The SVPWM method generates less harmonic distortion in the output voltage in comparison with the Sinusoidal PWM (SPWM) method. Moreover, SVPWM provides more efficient use of DC bus voltage than SPWM [10], [30]. In the space vector PWM approach, the number of the complex variables defines the dimension of the reference vector. While for the three-phase three-leg inverter with no DC bus center-point connection the two dimensional space vector approach is sufficient, for the three-phase four-leg inverter the three-dimensional space vector PWM approach is required. In the following these methods are reviewed.

2.2.1.1. Space Vector PWM in Three-Leg Inverter

Since in the three-phase three-leg (thus, three wire output) VSI the load neutral point is floating, there is no path for the neutral wire current flow. Thus, a voltage common to all the phase outputs can be disregarded in terms of effect on the load current. Extracting this common component from the phase voltages, the remaining voltages meet the condition defined in (2.3). In other words, any three-phase variable set (voltages or currents) without zero sequence components can be expressed as in (2.3). This implies the third variable is a function of the other two (exactly the negative of their sum). Thus, in this system there are only two independent variables. Thus, in such a system the variables can be represented in the two dimensional complex coordinates. That is why the two-dimensional (2-D) space vector approach is utilized for the three-phase three-leg inverter.

$$X_a + X_b + X_c = 0 \tag{2.3}$$

The inverter reference voltages are transformed to complex variables by utilizing (2.4). Figure 2.2 shows the relationship between the a-b-c coordinate system and two-dimensional α-β coordinate system. The reference voltage vector can be expressed in the complex coordinates as in (2.5). In the equation (2.5), v_{ref} is the reference voltage vector, the vector v_α is the projection of the reference vector on the α axis and the vector v_β is the projection of the reference voltage vector on the β axis as in the Figure 2.2. In (2.5), "*j*" represents the imaginary unity vector.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.4}$$

$$v_{ref} = v_\alpha + jv_\beta \tag{2.5}$$

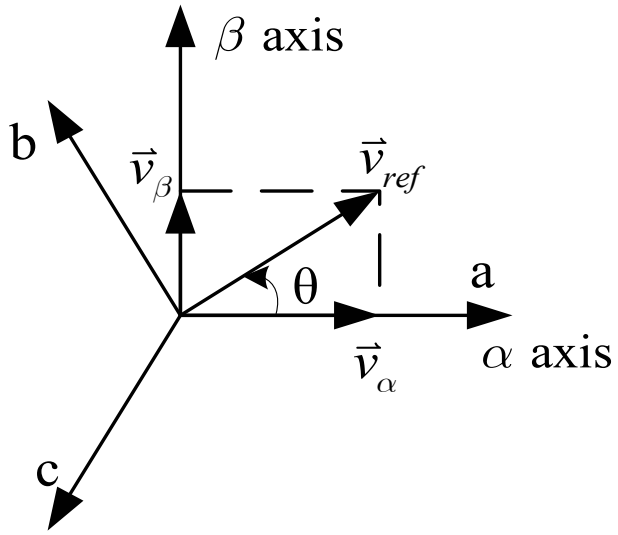


Figure 2.2 The relation between the a-b-c and α-β coordinates.

The number of the switch states of the inverter defines the number of vectors to be utilized in the space vector PWM approach. There are eight (2^3=8) voltage vectors in 2-D space vector PWM, since eight switch states exist in the three-phase three-leg

VSI. Table 2.1 shows the inverter voltage vectors in the complex coordinates which correspond to the switch states. In this table, on state of the top switch of each leg is symbolized as "1" and off state of the top switches is symbolized as "0". The states are defined in the a-b-c sequence. The voltage vectors form a hexagon in the α-β plane as shown in Figure 2.3. The states "000" and "111" define the two zero voltage vectors. These vectors are symbolized as V_0 and V_7, respectively. The zero voltage vectors are located at the origin of the space vector hexagon. Other vectors are called as nonzero voltage vectors. There are six identical triangles in the space vector hexagon. Each nonzero voltage vector has a length of $2V_{dc}/3$. In the 2-D space vector PWM method the adjacent nonzero voltage vectors are utilized in order to obtain low current ripple at the output of the inverter.

Table 2.1 The three-leg inverter switch states and corresponding inverter voltages

S_{a+} S_{b+} S_{c+}	Vector	V_{an}	V_{bn}	V_{cn}	V_α	V_β	Vector Length
0 0 0	V_0	0	0	0	0	0	0
1 0 0	V_1	$\frac{2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	0	$\frac{2V_{dc}}{3}$
1 1 0	V_2	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{-2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{3}}$	$\frac{2V_{dc}}{3}$
0 1 0	V_3	$\frac{-V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{3}}$	$\frac{2V_{dc}}{3}$
0 1 1	V_4	$\frac{-2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{-2V_{dc}}{3}$	0	$\frac{2V_{dc}}{3}$
0 0 1	V_5	$\frac{-V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{2V_{dc}}{3}$	$\frac{-V_{dc}}{3}$	$\frac{-V_{dc}}{\sqrt{3}}$	$\frac{2V_{dc}}{3}$
1 0 1	V_6	$\frac{V_{dc}}{3}$	$\frac{-2V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{3}$	$\frac{-V_{dc}}{\sqrt{3}}$	$\frac{2V_{dc}}{3}$
1 1 1	V_7	0	0	0	0	0	0

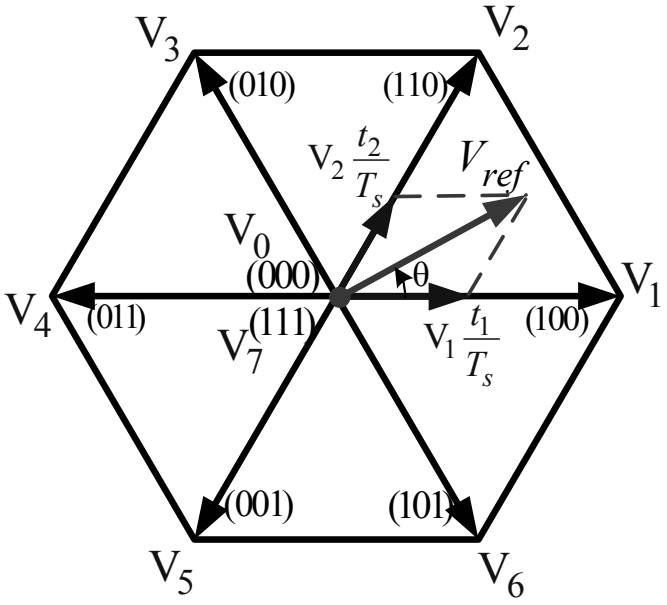


Figure 2.3 The two-dimensional space vector hexagon.

In the complex variable volt-second balancing approach, the inverter reference voltage vector is formed from two adjacent nonzero voltage vectors and two zero voltage vectors in the 2-D vector space. The choice of the adjacent vectors depends on the region in which the reference voltage vector exists. The region can be defined by utilizing the angle (θ) between the vectors v_1 and v_{ref}. By utilizing the volt-seconds balance equation (2.6), time lengths of the adjacent nonzero voltage vectors of the reference voltage vector are obtained. In this equation, v_{ref} and T_s represent the reference voltage vector and the switching period, respectively. v_k and v_{k+1} are the adjacent voltage vectors, and t_k and t_{k+1} are time lengths of the adjacent voltage vectors, respectively. When the region (r) is 6, then (r+1) becomes 1 (k=6 ➔ k+1=1). After obtaining the time lengths of the two nonzero voltage vectors, the total zero voltage vector time t_0+t_7 (of V_0 and V_7) is calculated with (2.7).

$$v_{ref}T_s = v_k t_k + v_{k+1}t_{k+1} \qquad \text{where } k \in \{1,2,3,4,5,6\} \tag{2.6}$$

$$t_0 + t_7 = T_s - (t_k + t_{k+1}) \qquad \text{where } k \in \{1,2,3,4,5,6\} \tag{2.7}$$

The total zero voltage vector time can be shared by the two zero states at various partitioning rates. When the zero voltage vector time is equally split among the two zero states, the output voltage ripple becomes minimum [10]. Considering minimum number of switchings and minimum output current ripple constraints, the optimal switching sequence is chosen as shown in Figure 2.4. In the figure, the time length values calculated from (2.6) and (2.7) are also illustrated. Also in the figure, S_{a+}, S_{b+}, S_{c+} represent the top switch signals for the inverter legs a, b, and c, respectively.

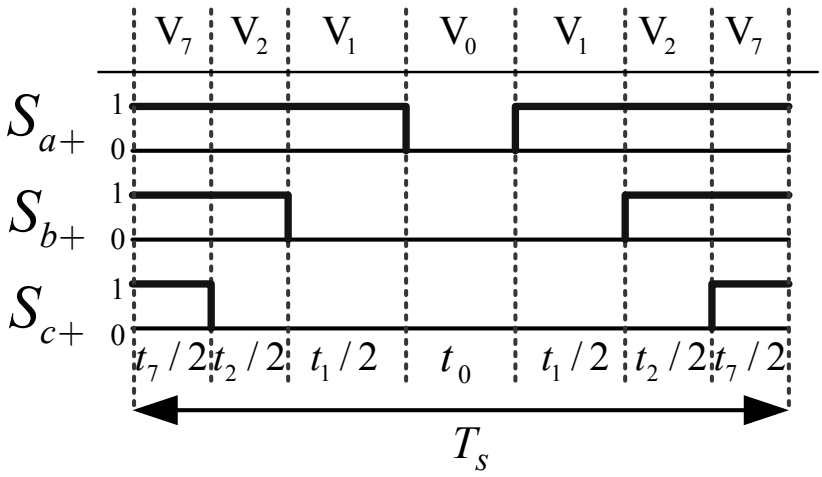


Figure 2.4 The switch pulse pattern of SVPWM in the first region of the hexagon.

2.2.1.2. Space Vector PWM in Four-Leg Inverter

Adding the fourth leg to the conventional three-phase three-leg inverter, not only provides a path for the load neutral wire current flow but also allows for control of the load neutral point potential. In Figure 2.5, the four-leg inverter is shown with the leg terminals a-b-c-f, where "f" represents the additional leg. The terminal of the additional leg "f" is taken as the reference point when defining the potentials of the inverter terminals a, b, and c. Thus, v_{af}, v_{bf}, v_{cf} are the phase voltages relative to the fourth leg potential. These voltages are the three independent voltages in the four-leg

inverter. In order to control the output voltages, the control unit of the UPS system must generate these reference voltages which include the zero sequence component.

Equation (2.3) is valid for the three-phase variables without zero-sequence components. However, it is not valid for the three-phase variables with a zero-sequence component, since the degree of freedom is increased from two to three with the additional leg. To represent the three independent variables of the four-leg inverter, three dimensional (3-D) vector space must be considered [6], [11]. The three phase-to-neutral reference voltages of the three-phase four-leg inverter are transformed to complex variables in the 3-D space. The components of the transformation are obtained from (2.8). The 3-D vector can be defined in terms of its components as in (2.9). In equation (2.9), V is the 3-D voltage vector and the vectors v_α, v_β and v_γ are the projections of the voltage vector on the α-β-γ axes, respectively. While α corresponds to the real axis, β and γ are the imaginary axes coordinate variables. The imaginary axes β and γ have the unit complex numbers of "j" and "k," respectively. The vector v_γ, which is absent in the three-leg inverter reference vector, corresponds to the zero sequence component in the four-leg inverter.

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_\gamma \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_{af} \\ v_{bf} \\ v_{cf} \end{bmatrix} \tag{2.8}$$

$$V = v_\alpha + jv_\beta + kv_\gamma \tag{2.9}$$

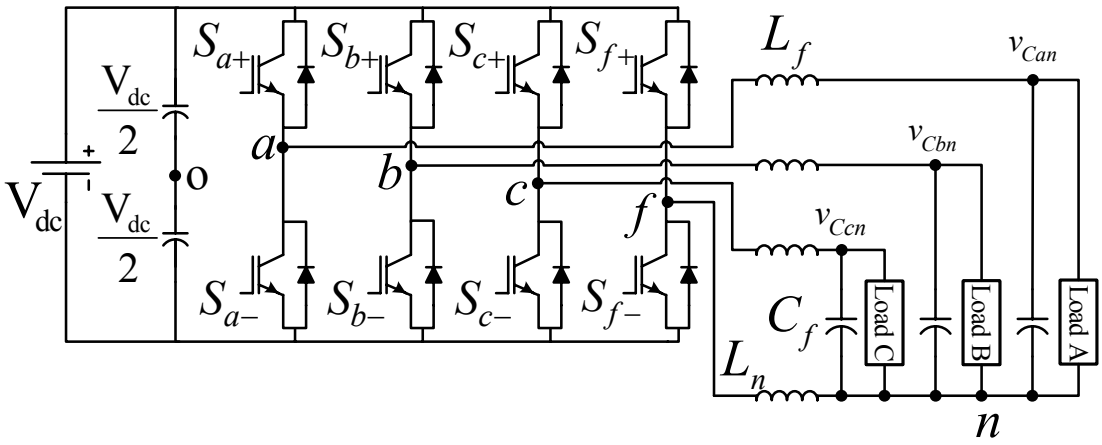


Figure 2.5 Three-phase four-leg UPS system basic circuit configuration.

The four-leg inverter differs from the three-leg inverter by one additional leg and thus two additional switches. There are sixteen (2^4=16) inverter states corresponding to the possible switch states in the three-phase four-leg inverter. The switch state combinations are given in Figure 2.6. In this figure, on state of the top switch of each leg is symbolized as “1” and off state of the top switches is symbolized as “0”. The switch states are defined in the a-b-c-n sequence. Table 2.2 shows the inverter voltages and 3-D space vector components which correspond to the 16 inverter switch states.

Table 2.2 The four-leg inverter switch states and the corresponding inverter voltages

$S_{a+}\ S_{b+}\ S_{c+}\ S_{f+}$	Vector	v_{af}	v_{bf}	v_{cf}	v_{α}	v_{β}	v_{γ}	Vector Length
0 0 0 0	V_0	0	0	0	0	0	0	0
0 0 0 1	V_1	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	0	$-V_{dc}$	$-V_{dc}$
1 0 0 0	V_2	V_{dc}	0	0	$\frac{2V_{dc}}{3}$	0	$\frac{V_{dc}}{3}$	$\frac{\sqrt{5}V_{dc}}{3}$
1 0 0 1	V_3	0	$-V_{dc}$	$-V_{dc}$	$\frac{2V_{dc}}{3}$	0	$\frac{-2V_{dc}}{3}$	$\frac{2\sqrt{2}V_{dc}}{3}$
1 1 0 0	V_4	V_{dc}	V_{dc}	0	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{3}}$	$\frac{2V_{dc}}{3}$	$\frac{2\sqrt{2}V_{dc}}{3}$
1 1 0 1	V_5	0	0	$-V_{dc}$	$\frac{V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{3}}$	$\frac{-V_{dc}}{3}$	$\frac{\sqrt{5}V_{dc}}{3}$
0 1 0 0	V_6	0	V_{dc}	0	$\frac{-V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{3}}$	$\frac{V_{dc}}{3}$	$\frac{\sqrt{5}V_{dc}}{3}$
0 1 0 1	V_7	$-V_{dc}$	0	$-V_{dc}$	$\frac{-V_{dc}}{3}$	$\frac{V_{dc}}{\sqrt{3}}$	$\frac{-2V_{dc}}{3}$	$\frac{2\sqrt{2}V_{dc}}{3}$
0 1 1 0	V_8	0	V_{dc}	V_{dc}	$\frac{-2V_{dc}}{3}$	0	$\frac{2V_{dc}}{3}$	$\frac{2\sqrt{2}V_{dc}}{3}$
0 1 1 1	V_9	$-V_{dc}$	0	0	$\frac{-2V_{dc}}{3}$	0	$\frac{-V_{dc}}{3}$	$\frac{\sqrt{5}V_{dc}}{3}$
0 0 1 0	V_{10}	0	0	V_{dc}	$\frac{-V_{dc}}{3}$	$\frac{-V_{dc}}{\sqrt{3}}$	$\frac{V_{dc}}{3}$	$\frac{\sqrt{5}V_{dc}}{3}$
0 0 1 1	V_{11}	$-V_{dc}$	$-V_{dc}$	0	$\frac{-V_{dc}}{3}$	$\frac{-V_{dc}}{\sqrt{3}}$	$\frac{-2V_{dc}}{3}$	$\frac{2\sqrt{2}V_{dc}}{3}$
1 0 1 0	V_{12}	V_{dc}	0	V_{dc}	$\frac{V_{dc}}{3}$	$\frac{-V_{dc}}{\sqrt{3}}$	$\frac{2V_{dc}}{3}$	$\frac{2\sqrt{2}V_{dc}}{3}$
1 0 1 1	V_{13}	0	$-V_{dc}$	0	$\frac{V_{dc}}{3}$	$\frac{-V_{dc}}{\sqrt{3}}$	$\frac{-V_{dc}}{3}$	$\frac{\sqrt{5}V_{dc}}{3}$
1 1 1 0	V_{14}	V_{dc}	V_{dc}	V_{dc}	0	0	V_{dc}	V_{dc}
1 1 1 1	V_{15}	0	0	0	0	0	0	0

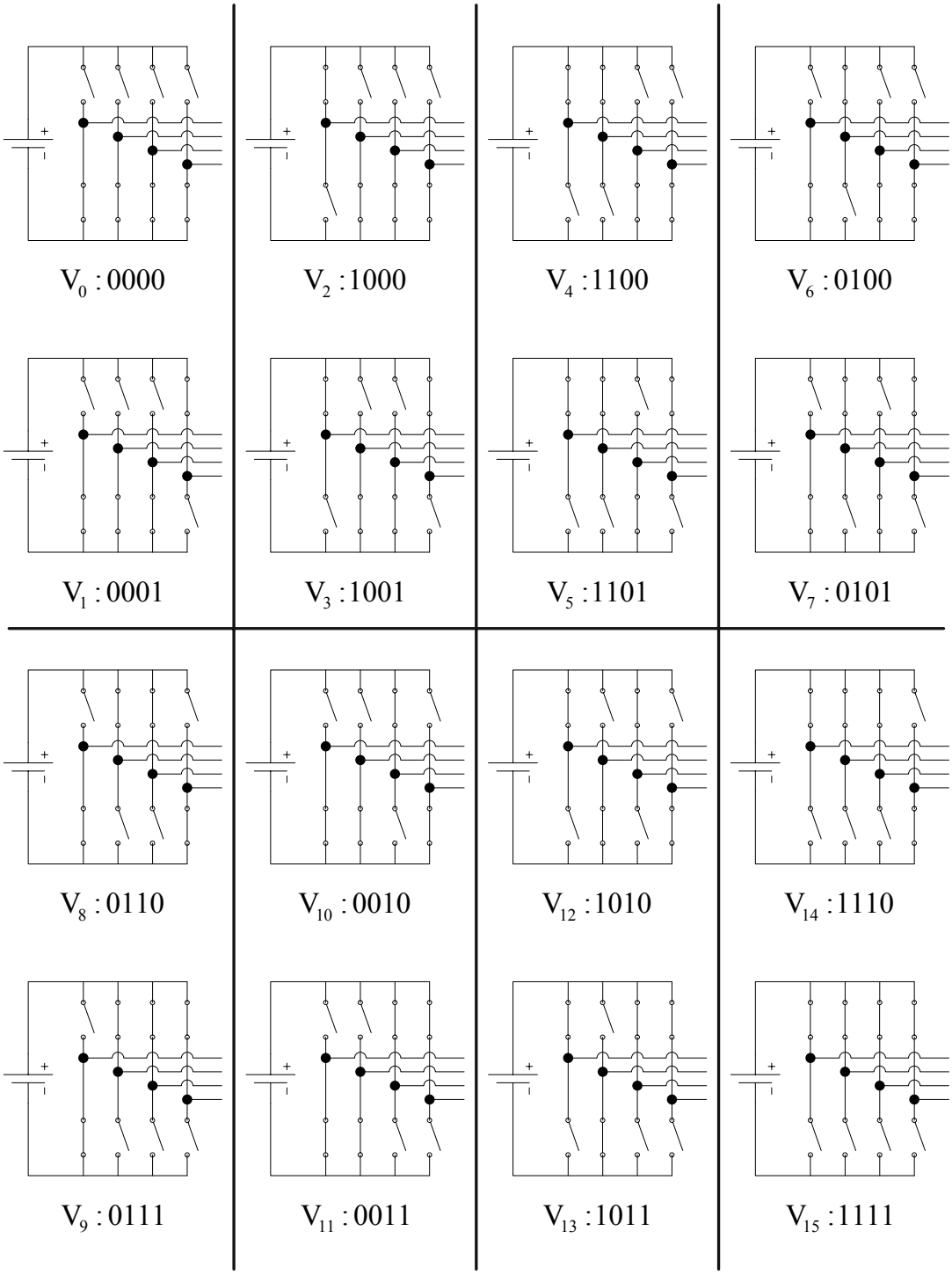


Figure 2.6 The 16 possible switch states of the four-leg inverter.

The inverter output voltages for the possible 16 inverter states shown in Table 2.2 are mapped to the 3-D vector space by utilizing (2.8) and (2.9) and the resulting space vector components are listed in Table 2.2. When these voltage vectors are represented in the 3-D vector space, their tip points define a hexagonal prism that has a hexagonal shaped pyramid roof that is shown in Figure 2.7. The states "0000" and "1111" define the zero voltage vectors that are located at the origin of the 3-D vector space and can be symbolized as V_0 and V_{15}, respectively. The other fourteen vectors are active vectors with nonzero magnitude value. When the active voltage vectors are projected on the α-β plane, the magnitude of the projected vectors becomes equal to $2V_{dc}/3$ which is the three-leg inverter voltage vector magnitude. The active voltage vectors of the four-leg inverter have a larger magnitude than the three-leg inverter and those belonging to the internal layers of the prism have a magnitude of $\sqrt{5}V_{dc}/3$ and those belonging to the external layers have the magnitude of $2\sqrt{2}V_{dc}/3$. The two extreme vectors corresponding to states 1110 and 0001 have a magnitude of V_{dc} each. Thus, it becomes clear that the hexagonal prism has seven layers based on the length of the zero sequence vector v_γ as shown in Figure 2.5. Each layer, except the top one and the bottom ones, has the same structure with the space vector hexagon utilized in 2-D space vector PWM. The middle layer ($v_\gamma=0$) has only two zero voltage vectors.

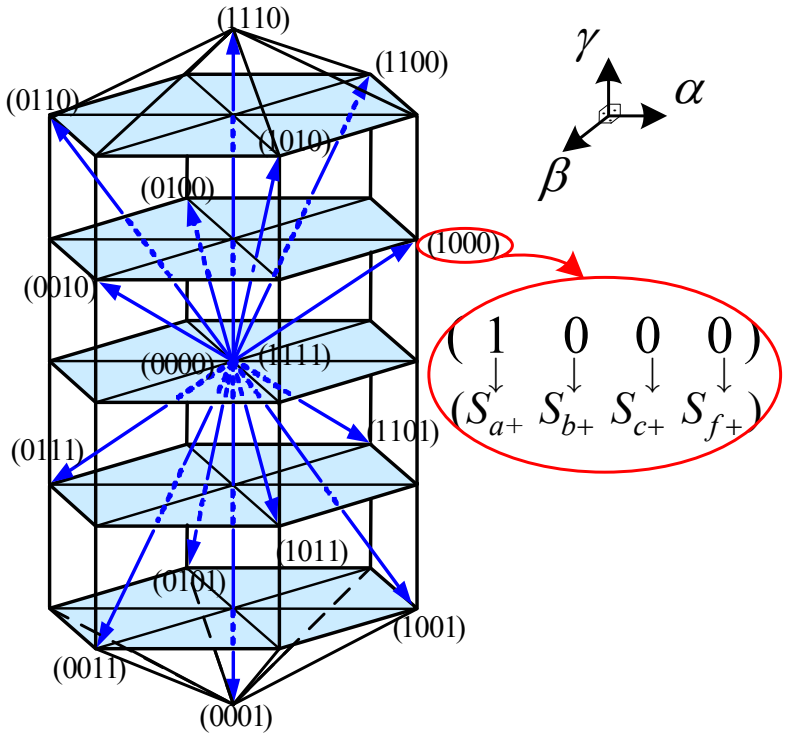


Figure 2.7 The voltage vectors of the four-leg inverter in the 3-D vector space.

There are six triangular prisms in the hexagonal prism as shown in Figure 2.9. Each triangular prism consists of six active voltage vectors, each of which is located at one of the hexagonal prism layers. Every triangular prism has four tetrahedrons. The tetrahedrons of the first triangular prism are shown in Figure 2.10. Each tetrahedron has three active voltage vectors and two zero voltage vectors. When utilizing space vector PWM, the reference voltage vector is formed from three adjacent active voltage vectors and the two zero voltage vectors in the 3-D vector space. In order to obtain low output current ripple, adjacent active voltage vectors are chosen. The determination procedure of the three adjacent active voltage vectors is complicated in the 3-D space vector PWM implementation. The adjacent voltage vectors are identified in two steps. Prism identification is the first step and tetrahedron identification is the second step. Using the projection of the reference vector on the α-β plane, prism identification can be done as in 2-D space vector PWM. There exist

twenty four (6x4=24) possible tetrahedrons, which the reference voltage vector can be in. This is the main complexity of 3-D space vector PWM method [6], [12].

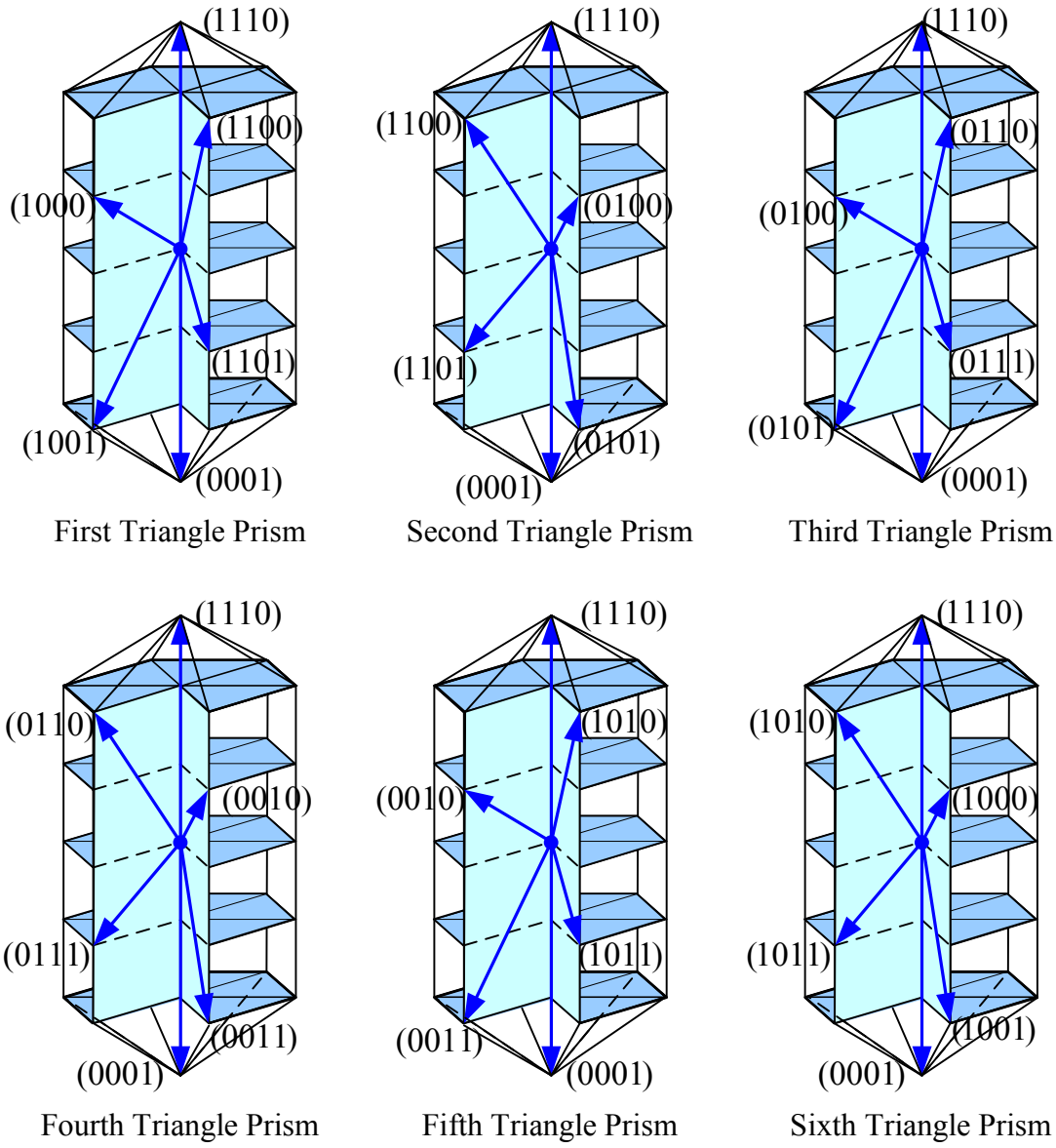


Figure 2.8 Triangular prisms of the four-leg inverter in the 3-D vector space.

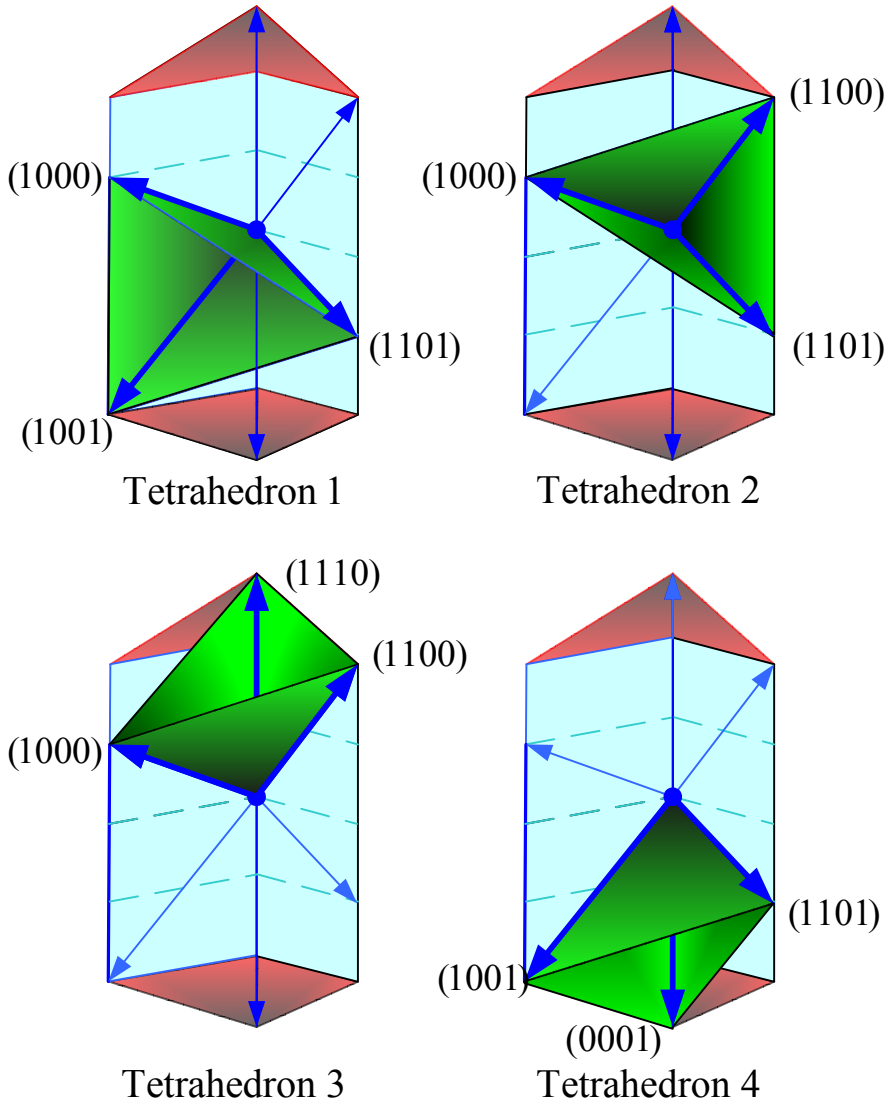


Figure 2.9 Tetrahedrons in the first triangular prism.

The operating time lengths of the voltage vectors that form the reference voltage vector are obtained from the volt-seconds balance equation as in (2.10). In equation (2.10) v_{ref} and T_s represent the reference voltage vector and PWM period respectively. v_x, v_y, v_z represent the adjacent active voltage vectors and the operating time lengths are symbolized as t_x, t_y, t_z. In this equation, the integers x, y, and z are in the range of 1 to 14. Since a total of 16 voltage vectors exist and only 14 of them are active voltage vectors. As shown in Table 2.2, the remaining two vectors are the zero

voltage vectors of V_0 and V_{15}. The integers x, y, and z are not ordered in the same manner as the conventional 2-D space vector PWM approach used for the three-leg inverter (k, k+1). This is due to the numbering system used in the four-leg inverter. The time lengths of the voltage vectors should be complemented to the PWM cycle T_s with the zero voltage vector time lengths. Thus, the operating time lengths (t_0+t_{15}) of the zero voltage vectors are calculated from (2.11).

$$v_{ref}T_s = v_x t_x + v_y t_y + v_z t_z \qquad x, y, z \in \{1,2,3,....,13,14\} \tag{2.10}$$

$$t_0 + t_{15} = T_s - (t_x + t_y + t_z) \tag{2.11}$$

Figure 2.11 shows the switch pulse pattern in the first tetrahedron of the first triangular prism. As in the 2-D space vector PWM, the total zero voltage vector time can be shared at any rate by the two zero states (0000 or 1111). In the SVPWM approach, they are shared equally in order to obtain low output voltage/current ripple. Alternatively, one of them can be eliminated in favor of reduced switching losses.

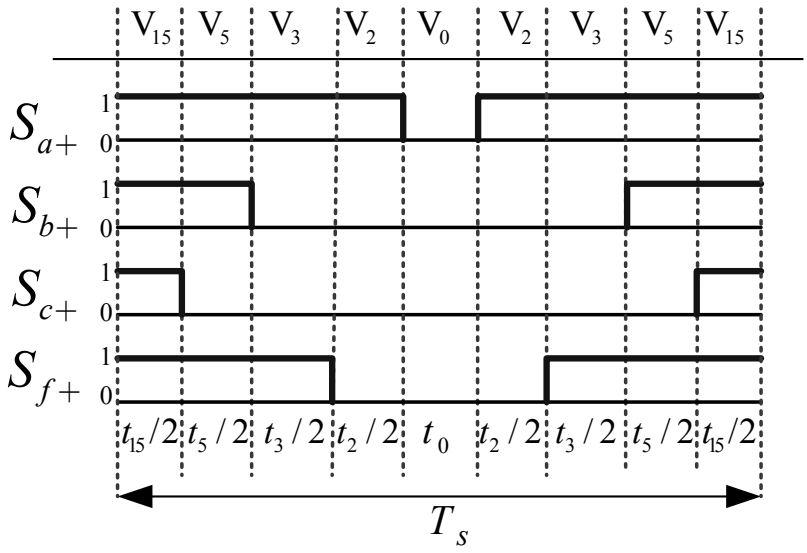


Figure 2.10 The switch pulse patterns in the first tetrahedron of the first triangular prism.

In the space vector PWM approach, the determination procedure of the three adjacent voltage vectors is complicated. It involves identifying sectors of the hexagonal prism, tetrahedrons of each triangular prism and finally the sequence and duty cycle values of the inverter voltage vectors. Although high performance pulse patterns can be programmed with this approach, this procedure is highly complex and computationally involved. Thus, the approach is not favorable and simpler scalar PWM methods have been developed. In the next section, simple scalar PWM methods, which can be utilized for four-leg inverters, are discussed into length.

2.2.2. Scalar PWM

In the scalar PWM technique, the switching logic signals of the switches are determined by intersecting the carrier signal which is a triangular wave and the modulation signal. In order to generate the switching signal, the modulation signal and carrier signal are compared. When the modulation signal is greater than the carrier signal, instantaneously, the top switch of the respective leg turns on and remains in the same state as long as the condition is valid. When the carrier signal is greater than the modulation signal, then the switch turns off and remains so as long as this condition is valid. Figure 2.11 illustrates the switch logic signal generation procedure. The module which performs this procedure is termed as the “modulator” or the “PWM unit.” The input to the modulator is the modulation signal and the output is the switch logic signal.

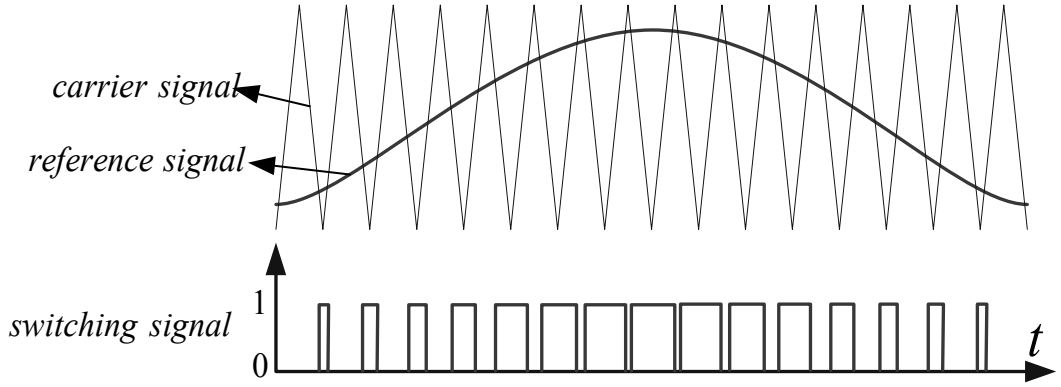


Figure 2.11 The switching signal generation method in scalar PWM.

In three-phase systems, the PWM block consists of multi-channels. One channel per inverter leg is utilized. Generally, all the channels are synchronized and one triangular carrier signal is utilized for all. The inputs to the PWM channels are the three reference voltages v_{ax}^*, v_{bx}^*, v_{cx}^* that are generated by the power converter control unit external to this block. If the inverter is a three-leg inverter, the point "x" (which is a reference potential point) is the virtual DC bus center point (point "O" in Figure 2.5). Thus, the phase reference voltages are defined with respect to the virtual center point of the DC bus. Since the neutral point of the load is floating with respect to the inverter DC bus, a signal may be added to or subtracted from all these reference voltages simultaneously and the additional signal is termed as the "zero sequence signal." Following the injection of the zero sequence signal, the three modulation signals are compared with the carrier signal and the intersection of each modulation signal with the carrier defines the switching signals for the associated inverter leg. Since the reference voltages are defined with respect to the virtual center point of the DC bus voltage, the triangular carrier signal has a magnitude of $\pm 0.5V_{dc}$. In an analog implementation, the modulation and triangular carrier signals are scaled down to an acceptable level for the electronic circuits. In the digital PWM implementation a counter and comparator are utilized and the signals are properly scaled and converted to binary signals then processed in the counter and comparator for high resolution PWM output signals.

In the four-leg inverter case, the point "x" is the center point of the fourth leg "f." Thus, for the four-leg inverter PWM block input voltages are v_{af}^{*}, v_{bf}^{*}, v_{cf}^{*} and since these signals are relative to the center point of the fourth leg, it is required to define the fourth leg reference voltage and then all the inverter output terminal reference voltages (v_{ao}^{**}, v_{bo}^{**}, v_{co}^{**}, v_{fo}^{*}) with respect to the virtual DC bus center point are defined. The next step is to generate the PWM output signals similar to the three-leg inverter case. Then, the modulation signals for all the inverter legs can be calculated as in (2.12). Since the center point of the DC bus voltage is isolated and there is no path for current flow from the "*f*" point to the "o" point (see Figure 2.5), there exists a degree of freedom in the choice of v_{fo}^{*} value. Thus, this degree of freedom can be utilized to the advantage of the inverter in terms of performance optimization. As it is added to the v_{af}^{*}, v_{bf}^{*}, v_{cf}^{*} to obtain the inverter leg modulation signals, this signal is called the offset or injection signal. Output current ripple minimization, voltage linearity range maximization, switching loss minimization, etc. criteria can be utilized for optimization of the offset signal. However, there are constraints on the choice of the fourth leg modulation signal as will be discussed in the following.

$$v_{xo}^{**} = v_{xf}^{*} + v_{fo}^{*} , \qquad x \in \{a,b,c\} \tag{2.12}$$

Similar to the three-leg inverter case, the triangular carrier wave is represented with V_{dc} peak-to-peak value as shown in Figure 2.12. In this case, the output voltages v_{ao}, v_{bo}, v_{co}, v_{fo} are bounded as in (2.13). This implies, that to retain voltage linearity in the modulator, the reference voltages v_{ao}^{**}, v_{bo}^{**}, v_{co}^{**}, v_{fo}^{*} should also be bounded as in (2.13). Since as a consequence of (2.13) the output voltage between any two terminals of the inverter is bounded by (2.14), its reference should also comply with (2.14) in order to maintain voltage linearity.

$$-\frac{V_{dc}}{2} \le v_{xo} \le \frac{V_{dc}}{2} \qquad x \in \{a,b,c,f\} \tag{2.13}$$

$$-V_{dc} \le v_{xy} \le V_{dc} \qquad x,y \in \{a,b,c,f\} \tag{2.14}$$

Although (2.13) defines the maximum theoretical range for the offset signal which is the fourth leg potential, there is a further constraint on the practical range. Of the three reference signals v_{af}^*, v_{bf}^*, v_{cf}^*, let's assume that the two extreme signals are $v^*_{\max}$ and $v^*_{\min}$, as defined in (2.15) and (2.16), respectively. The largest possible v_{fo}^* that retains the system linearity is a function of the absolute value of $v^*_{max} - v^*_{min}$. If $v^*_{max} - v^*_{min}$ is smaller than V_{dc}, this implies that (2.14) is satisfied and there is a room for injecting a v_{fo}^* signal. The available range for the injection depends on the sign and magnitude of the $v^*_{\max}$ and $v^*_{\min}$ signals. The top and bottom limits of the injection signal are given in (2.17) ve (2.18). If $v^*_{\max}$ is positive, then the top limit of the injection signal is the difference between the positive DC rail voltage and the $v^*_{\max}$. If $v^*_{\max}$ is negative, the injection signal will be limited to $V_{dc}/2$ due to the constraint (2.13). Thus, the injection signal top limit can be defined in (2.17). Likewise, the bottom limit of the injection signal is determined. If $v^*_{\min}$ is negative, then the bottom limit of the injection signal is the difference between the negative DC rail voltage and the $v^*_{\min}$. If $v^*_{\min}$ is positive, the injection signal will be limited to $-V_{dc}/2$ due to the constraint (2.13). Thus, the injection signal bottom limit can be defined in (2.18). Depending on the top and bottom limit values of the injection signal, a wide range may exist for the purpose of performance optimization. This will be benefited from in the following sections.

$$v^*_{\max} = \max(v^*_{af}, v^*_{bf}, v^*_{cf}) \tag{2.15}$$

$$v^*_{\min} = \min(v^*_{af}, v^*_{bf}, v^*_{cf}) \tag{2.16}$$

$$v^*_{fo\_top} = \begin{cases} \dfrac{V_{dc}}{2} & v^*_{\max} < 0 \\ \dfrac{V_{dc}}{2} - v^*_{\max} & \text{elsewhere} \end{cases} \tag{2.17}$$

$$v^*_{fo\_bottom} = \begin{cases} -\dfrac{V_{dc}}{2} & v^*_{\min} > 0 \\ -\dfrac{V_{dc}}{2} - v^*_{\min} & \text{elsewhere} \end{cases} \tag{2.18}$$

If no offset signal is injected, this implies that the v_{no} signal has zero value, the v_{af}^* signals define the v_{ao}^{**} etc. signals as shown in Figure 2.12 and the intersections of the reference signals with the triangular wave define the switching instants for each phase. Since its modulation signal is zero, the fourth leg is operated at 50% duty cycle yielding zero average value. If an offset signal that is within the boundaries of (2.17) and (2.18) is selected for v_{fo}^*, then as shown in Figure 2.13, all the original modulation signals simultaneously shift upwards or downwards depending on the injection signal polarity. Thus, the intersection points of the triangular carrier wave and the modulation signals and therefore the switching instants change. However, the original signals v_{af}^*, v_{bf}^*, v_{cf}^* remain relatively at the same distance from each other. Thus, their relative values remain the same. This means the rectangular line-to-line voltage pulses remain at the same width, although the distances between them remain the same. In the figure, this can be seen as the variation of the partitioning rate of the inverter zero states (the 0000 and 1111 states). This implies that the average value characteristics of the line to line voltages remain the same. The PWM characteristics, on the other hand, change and the output voltage/current ripple depends on the injection signal. Further, if the injection signal is exactly equal to one of the boundary values, the switching characteristics also change. Thus, the influence of the injection signal on the inverter performance is significant and various algorithms that optimize certain performance characteristics are developed. With such algorithms determining the offset signal, the PWM block diagram of the four-leg inverter becomes as shown in Figure 2.14. In the following the most popular PWM methods are discussed in detail.

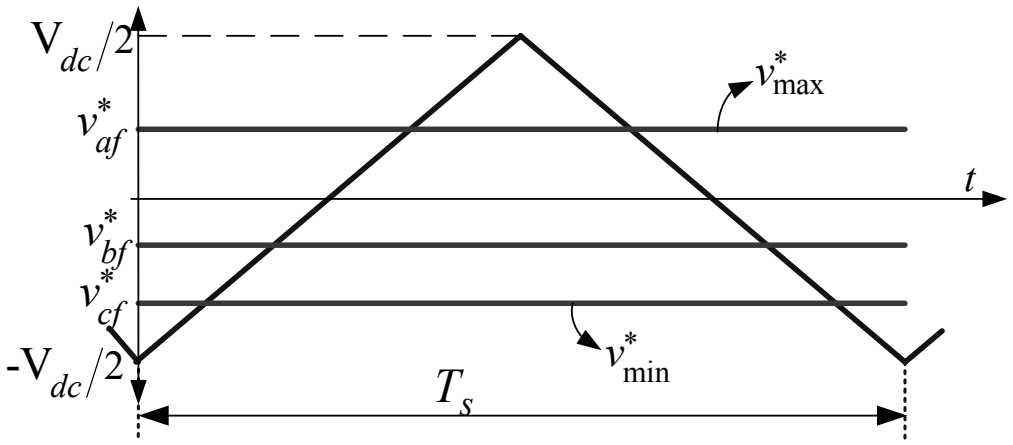


Figure 2.12 Modulation and carrier signals of the four-leg inverter with v_{fo}^{*} set to zero illustrating the two extreme modulation signals as $v^{*}_{\max}$ and $v^{*}_{\min}$.

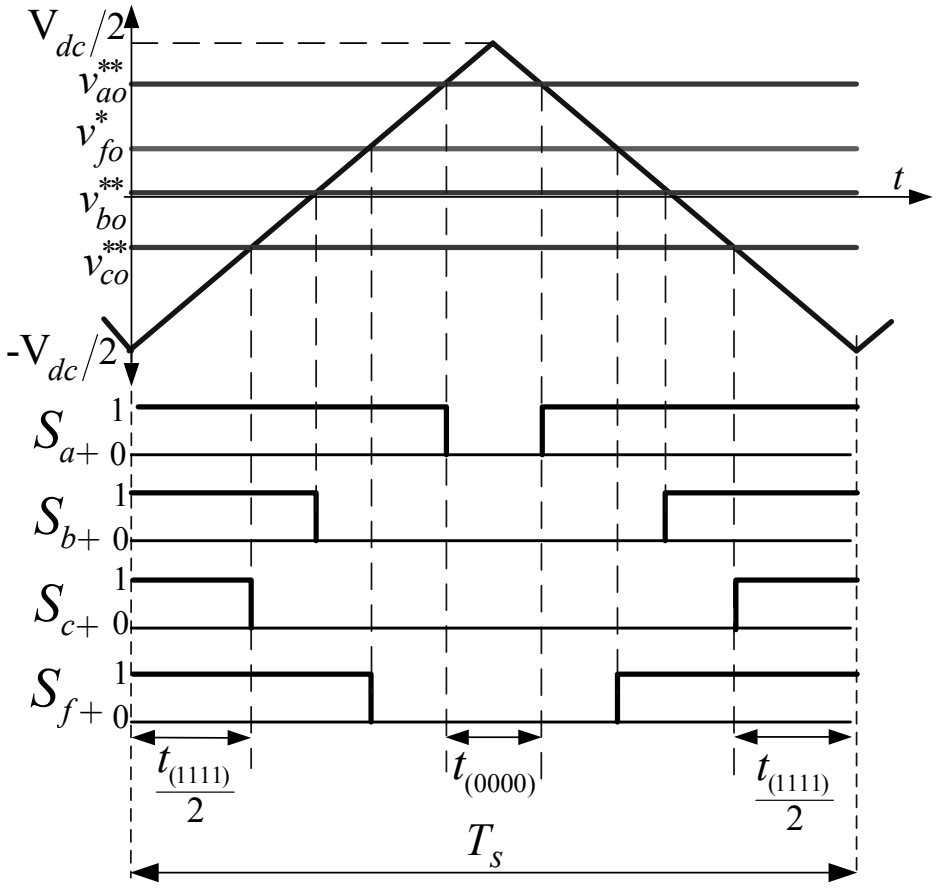


Figure 2.13 Modulation and carrier signals and switching diagram of the four-leg inverter with v_{fo}^{*} set to a positive value illustrating the influence on the width of the two zero states.

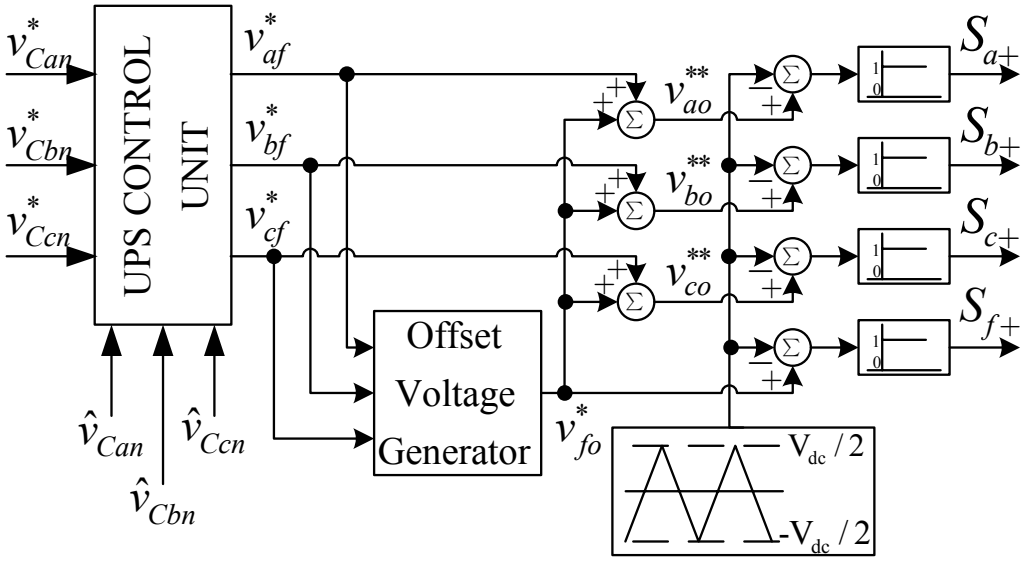


Figure 2.14 Block diagram of the scalar modulation in the four-leg inverter.

2.2.2.1. Sinusoidal PWM (v_{fo}^{*}=0)

As shown in Figure 2.15 (for M_i=0.64), in this method there is no offset voltage addition (v_{fo}^{*}=0). Thus, the v_{af}^{*}, v_{bf}^{*}, v_{cf}^{*} signals are retained as the original values. This is the simplest method as it requires no additional calculation in the offset calculation block in Figure 2.14. However, the maximum achievable peak value of the output voltage in SPWM is limited to $V_{dc}/2$ which is less than what is obtained in the space vector method 2.2.1.2. Since UPS systems involve high modulation index operation such that the DC bus voltage is benefited from at a high rate, the SPWM method which has low voltage linearity range is not preferable in such applications. Thus, no further investigations will be done on this method.

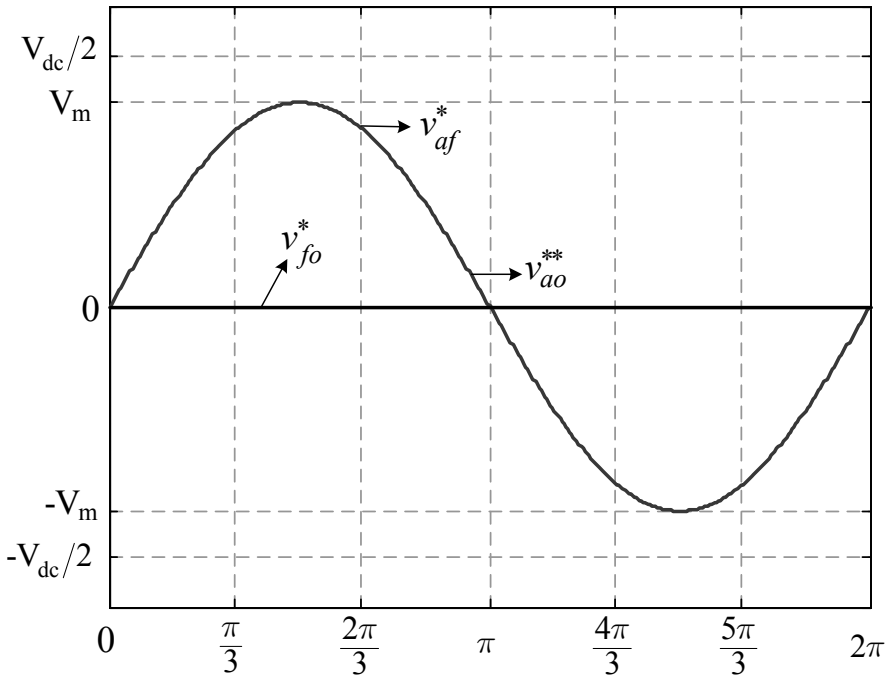


Figure 2.15 Illustrating the modulation wave of one phase of the four-leg inverter for SPWM at M_i=0.64.

2.2.2.2. Offset Signal Injection Methods

In this section, methods that involve a signal injection other than zero will be considered. A systematic approach will be pursued so that all methods could be wholly treated. The method proposed is based on the inverter zero state partitioning, which is the extension of the concept previously established for the three-leg inverter [10], [30]. Defining the two inverter zero states as $V_{(0000)}$ and $V_{(1111)}$ and their duration as $t_{(0000)}$ and $t_{(1111)}$ respectively as shown in Figure 2.13, the zero state partitioning function ξ can be defined as given in (2.19) as the ratio of the zero state $t_{(0000)}$ to the total time of the zero states. Since it defines a duty ratio, the partitioning function has a range between zero and unity. The ξ variable is proportional to v_{fo}^* as can be seen in Figure 2.13. As v_{fo}^* increases the ξ value linearly decreases. Involving the top and bottom limits of the injection signals, the relation between the ξ and v_{fo}^* can be written as in (2.20). Since the top and bottom limits of the injection signal are defined in (2.17) and (2.18), (2.20) can be written as a function of v^*_{max} and v^*_{min} in detail in equation (2.21).

$$\xi = \frac{t_{(0000)}}{t_{(0000)} + t_{(1111)}} \tag{2.19}$$

$$v_{fo}^{*} = \left(1-\xi\right)\left(v_{fo\_top}^{*}\right) + \xi\left(v_{fo\_bottom}^{*}\right) \tag{2.20}$$

$$v_{fo}^{*} = \begin{cases} \left(\frac{1}{2}-\xi\right)\mathrm{V_{dc}} - \xi \cdot v_{\min}^{*} & v_{\max}^{*} < 0 \\ \left(\frac{1}{2}-\xi\right)\mathrm{V_{dc}} + \left(\xi-1\right)\cdot v_{\max}^{*} & v_{\min}^{*} > 0 \\ \left(\frac{1}{2}-\xi\right)\mathrm{V_{dc}} + \left(\xi-1\right)\cdot v_{\max}^{*} - \xi \cdot v_{\min}^{*} & \text{elsewhere} \end{cases} \tag{2.21}$$

In order to illustrate the zero state partitioning and offset voltage relations, operation at various M_i levels will be investigated in the following. Figure 2.16 shows the balanced sinusoidal voltage references v_{af}^{*}, v_{bf}^{*}, v_{cf}^{*}, at M_i=0.785. Figure 2.17 shows the maximum and minimum (extremum) values of these signals as described in (2.15) and (2.16). Taking the maximum (minimum) signal and the DC bus side closest to it to find the largest (smallest) v_{fo}^{*} signal as defined in (2.17) (equation (2.18)), the upper (lower) boundary for v_{fo}^{*} can be obtained: The boundaries for v_{fo}^{*} are shown in Figure 2.18. To illustrate the relation between ξ and v_{fo}^{*}, in the next step the $v^{*}_{\min}$ and $v^{*}_{\max}$ values are processed for various ξ values (from 0 to 1 by an increment of 0.1) by utilizing (2.20) and the graphics are shown in Figure 2.19. As can be seen from the figure, at the extreme values of ξ, the boundary values of v_{fo}^{*} as defined in (2.17) and (2.18) are found. For ξ values in between, the v_{fo}^{*} signal is also in between the boundaries. As the modulation index increases the range for v_{fo}^{*} decreases. As shown in Figure 2.20, for M_i=0.907, the two boundary curves of v_{fo}^{*} intersect and the area between them expires, indicating that the range for v_{fo}^{*} is expiring and the modulator is entering the overmodulation range. For the cases of $v^{*}_{\min}>0$ and for $v^{*}_{\max}<0$ which correspond to unusual operating points, the offset signal injection boundaries are calculated from (2.21) and shown with ξ as parameter in Figures 2.21 and 2.22.

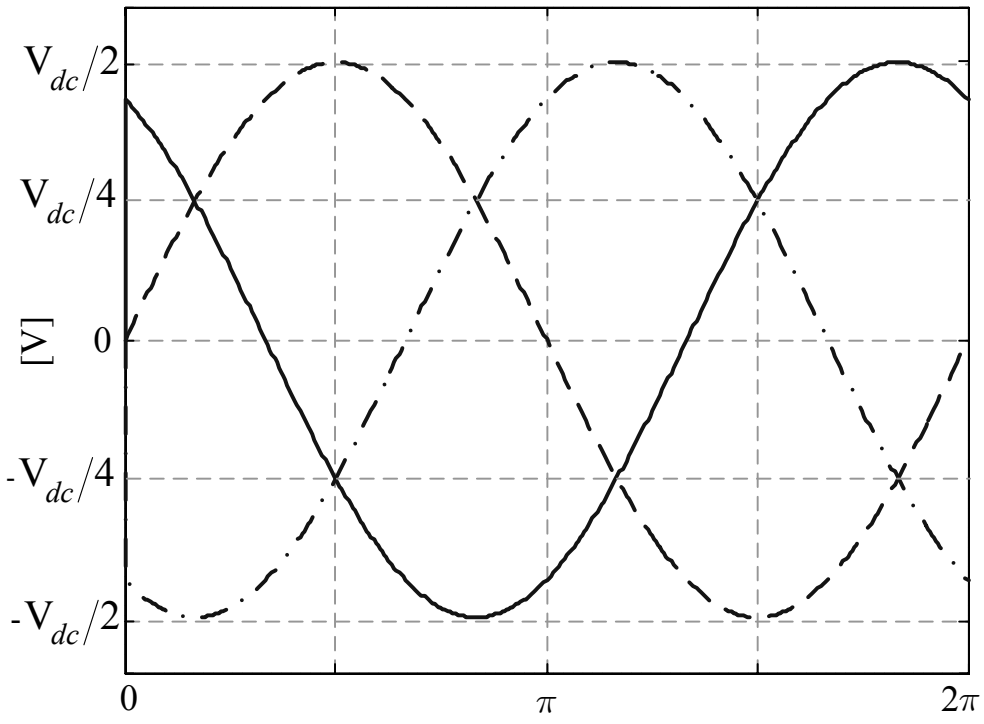


Figure 2.16 The original balanced modulation signals v_{af}^*, v_{bf}^*, v_{cf}^* for M_i=0.785.

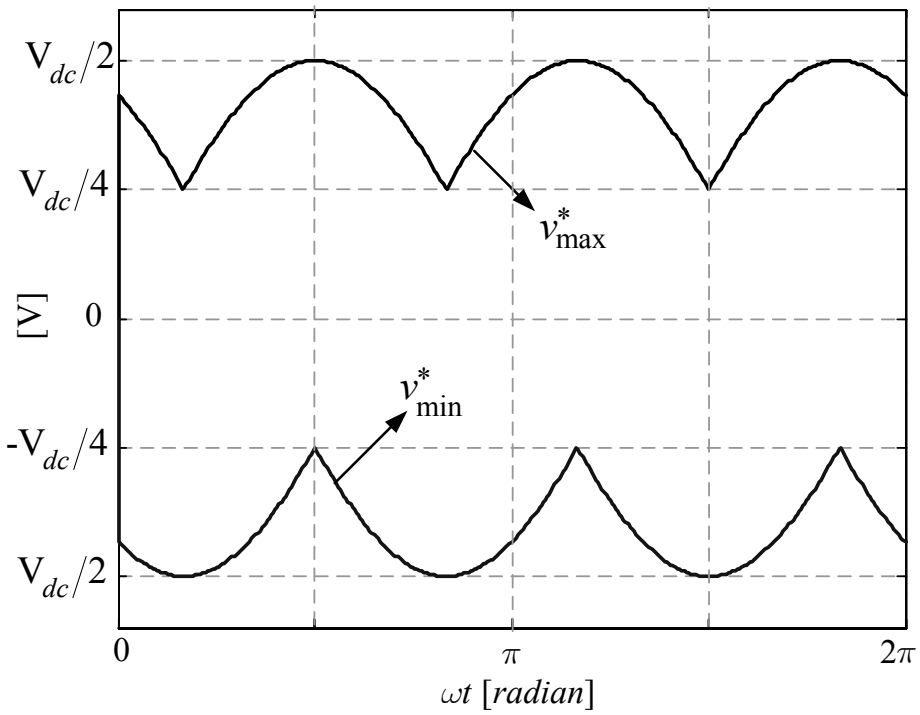


Figure 2.17 v^*_{max} and v^*_{min} signals for M_i=0.785 and balanced v_{af}^*, v_{bf}^*, v_{cf}^*.

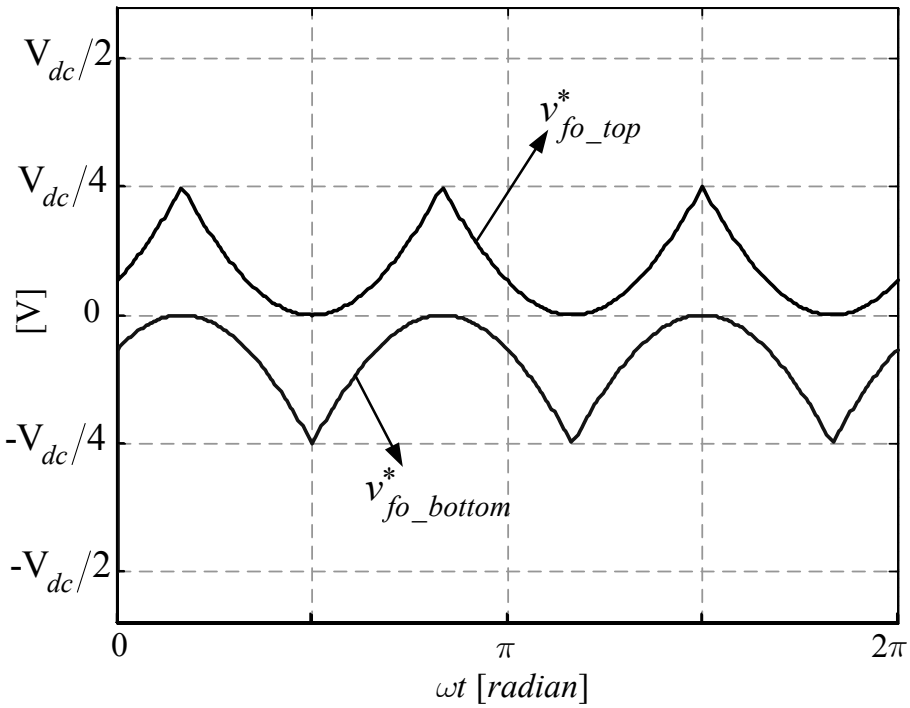


Figure 2.18 The boundaries of the injection signal for M_i=0.785.

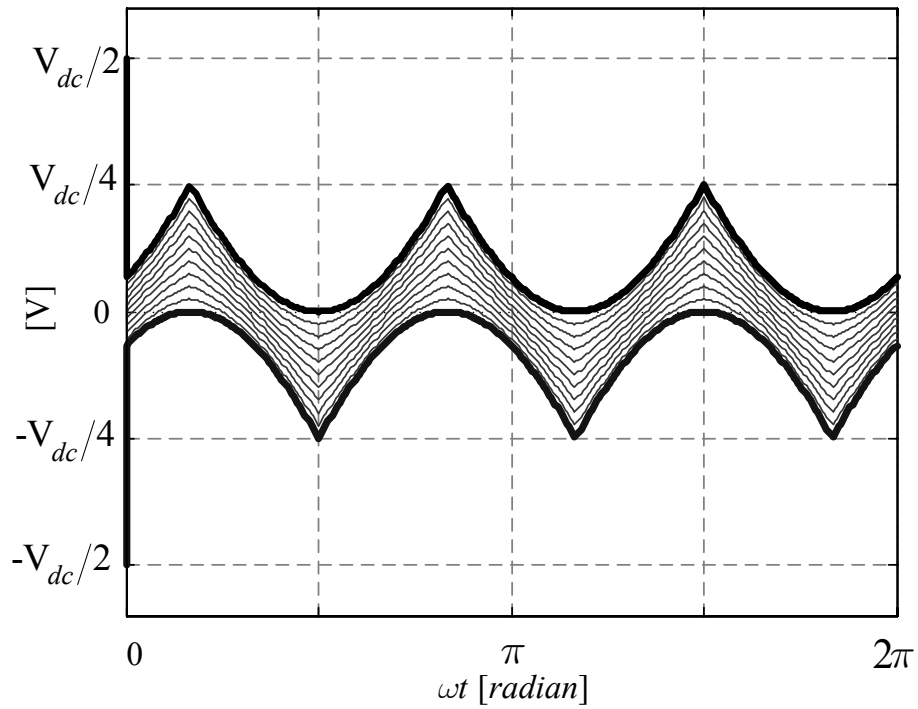


Figure 2.19 The injection signal waveforms within the $v^*_{fo\_top}$ and $v^*_{fo\_bottom}$ boundaries as a function of ξ for M_i=0.785 (ξ is incremented from 0 to 1 by 0.1).

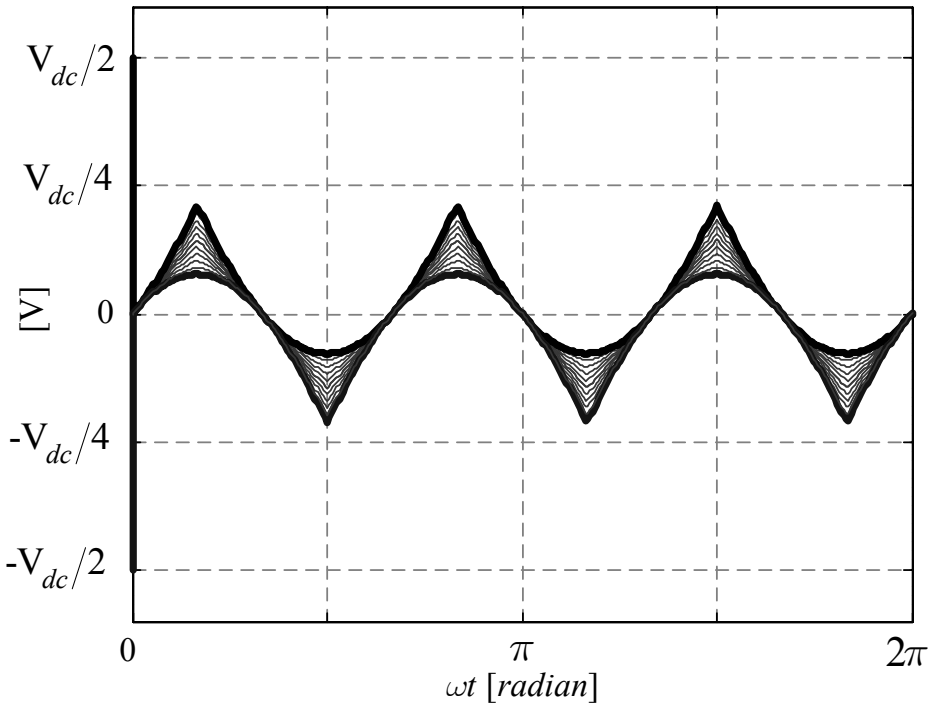


Figure 2.20 The injection signal waveforms within the $v^*_{fo\_top}$ and $v^*_{fo\_bottom}$ boundaries as a function of ξ for M_i=0.907 (ξ is incremented from 0 to 1 by 0.1).

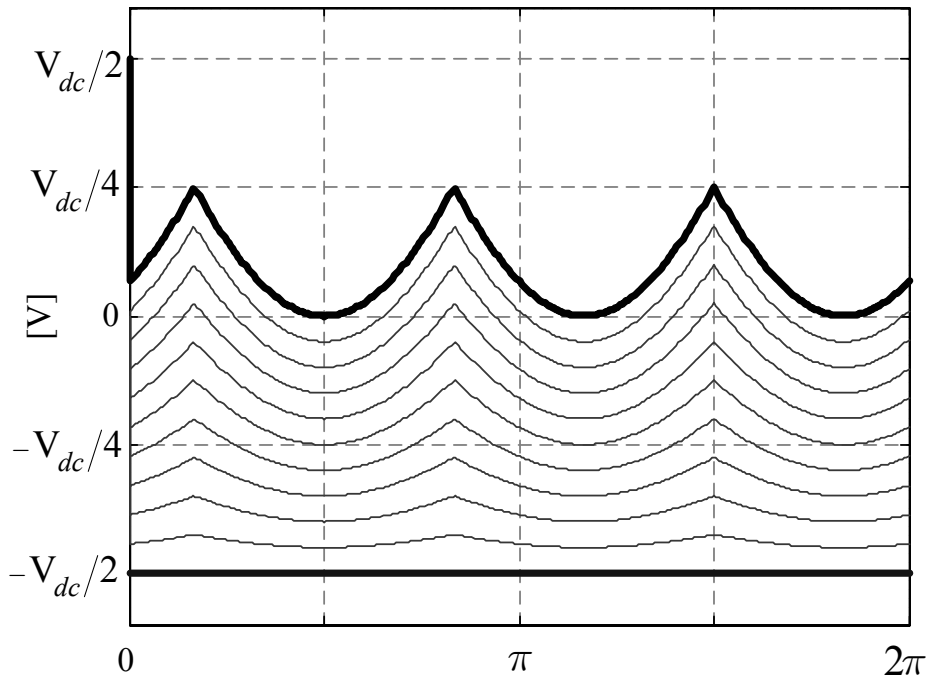


Figure 2.21 The injection signal waveforms within the $v^*_{fo\_top}$ and $v^*_{fo\_bottom}$ boundaries as a function of ξ for v^*_{min} >0 (ξ is incremented from 0 to 1 by 0.1).

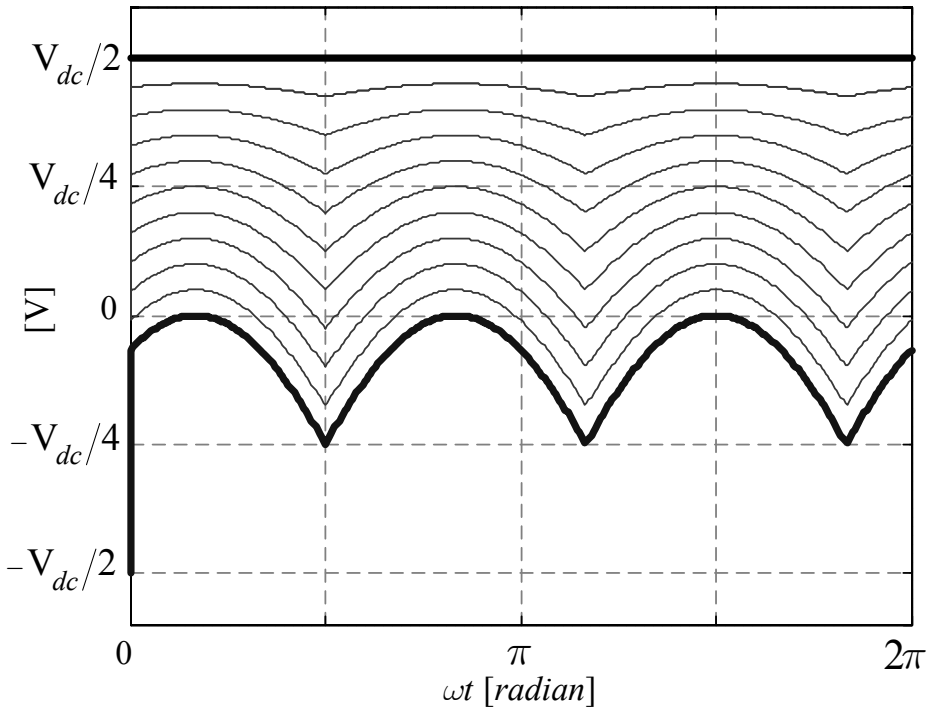


Figure 2.22 The injection signal waveforms within the $v^*_{fo\_top}$ and $v^*_{fo\_bottom}$ boundaries as a function of ξ for $v^*_{max}<0$ (ξ is incremented from 0 to 1 by 0.1).

Based on the above discussion, for each modulation index there is a specific range for v_{fo}^*. While at zero modulation index this range is extremely wide, as the modulation index increases, this range rapidly expires. Thus the availability of v_{fo}^* is dependent on the modulation index. For a given modulation index, as there exists a range for v_{fo}^*, the next step discusses how v_{fo}^* is chosen. Although there are infinite possibilities to choose from, only a few are practical. Thus, in the following the popular methods which have salient advantageous performance characteristics will be discussed. These methods will be defined in terms of the zero state partitioning function.

2.2.2.2.1. SVPWM

In 3-D SVPWM method (explained in section 2.2.1.2), the generation method of switching signals of involves a complicated procedure such as the identification of

the adjacent switching vectors, the calculation of the switching vectors with pre-defined 24 matrices. Once the voltage vectors and their duration are calculated, the next step involves defining the sequence of the vectors. Considering the minimum output voltage/current ripple criteria, the zero states are equally partitioned. And the pulse pattern is programmed by a digital PWM module. This fairly long and complex procedure has been found unnecessary as the simple scalar implementation was discovered [14]. In this thesis, a similar method to [14] is utilized and the zero state partitioning function is selected equal to 0.5 such that the 0000 state and the 1111 state have equal length that correspond to minimum switching ripple as defined in [10]. When (2.20) is evaluated for the zero state partitioning function value of 0.5, the following v_{fo}^* offset function of the SVPWM scalar implementation is obtained.

$$v_{fo}^* = \begin{cases} -\dfrac{v_{\min}^*}{2} & v_{\max}^* < 0 \\ -\dfrac{v_{\max}^*}{2} & v_{\min}^* > 0 \\ -\dfrac{v_{\max}^* + v_{\min}^*}{2} & \text{elsewhere} \end{cases} \tag{2.22}$$

Implemented in the above given simple scalar form, the SVPWM provides the benefit of low PWM ripple and a wide voltage linearity range. For the balanced sinusoidal voltage references case, the maximum voltage linearity range is the same as the three-leg inverter which is 0.907 modulation index for the full fundamental cycle. And wider linearity range which involves the whole inverter voltage hexagon (prism) during dynamic operation is available. For the balanced sinusoidal three-phase voltage references case, with two different modulation index values (M_i=0.907 and M_i=0.64), the obtained modulation waveforms are given in Figures 2.23 and 2.24. As shown in figures, the offset voltage v_{fo}^* is the well known SVPWM triangular waveform for the three-leg inverter.

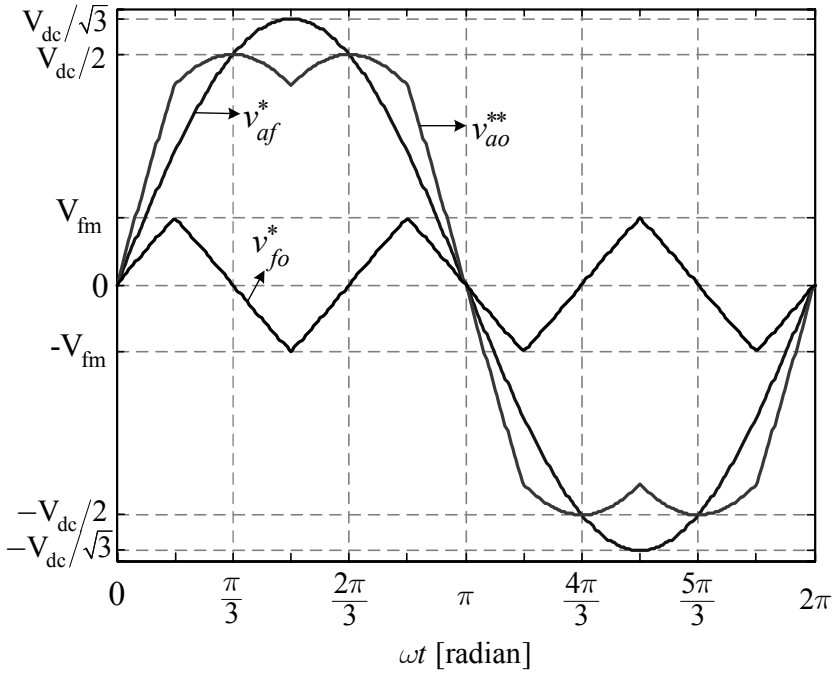


Figure 2.23 Illustrating the modulation wave of one phase of the four-leg inverter for SVPWM at M_i=0.907.

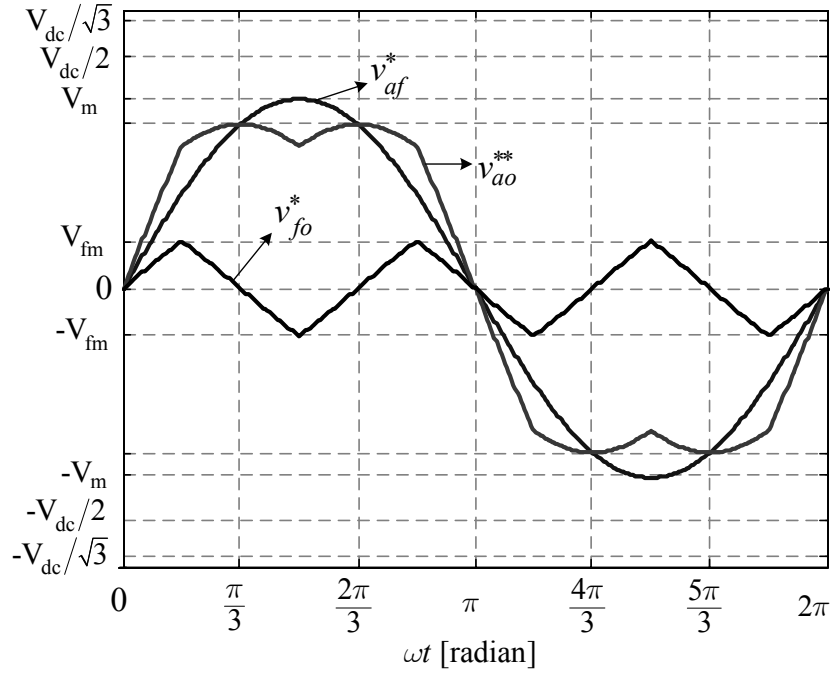


Figure 2.24 Illustrating the modulation wave of one phase of the four-leg inverter for SVPWM at M_i=0.64.

2.2.2.2.2. DPWM

The practical switches in a VSI involve finite turn-on and turn-off times resulting in switching losses during commutation. Figure 2.25 shows the simplified current and voltage waveform characteristics of a switch in one switching period. Given the switch current rise and fall times t_r and t_f over a PWM cycle T_s, the switching losses can be roughly calculated as in (2.23). In this equation, $f_i(\theta)$ represents the current that flows through the switch. If the switching in an inverter leg over a PWM cycle ceases, the switching losses in that cycle also disappear.

$$P_{sw} = \frac{1}{2\pi} \frac{V_{dc}(t_r + t_f)}{2T_s} \int_0^{2\pi} f_i(\theta) d\theta \tag{2.23}$$

The switching power loss is direct proportional to switching frequency as can be seen from equation (2.23). In low switching frequency applications, the switching loss can be tolerated. However, the switching loss affects system efficiency in high frequency applications. With an increasing demand on the power electronics switches that can be switched at high frequency like IGBT and MOSFET, high switching frequency applications become widespread. Therefore the switching power loss should be decreased to provide high system efficiency.

The discontinuous PWM (DPWM) approach is well established for three-leg inverters [31]. Its main benefit involves the reduction in switching losses by at least 33%. This is achieved by setting one of the three-phase modulation waves equal to the positive or negative DC rail voltages ($\pm 0.5V_{dc}$), thus clamping the associated inverter leg and eliminating the switching losses of the switching devices in this leg. To achieve this in a three-leg three-wire inverter, a zero sequence signal is injected to all modulation waves. The injection signal magnitude is such that it clamps the associated phase voltage to the proper DC rail side. First, of the original modulation signals the one with the largest magnitude is identified. The polarity of this signal

defines the DC rail side that the switch on this inverter leg to be clamped at. The difference between the determined DC rail voltage (either $0.5V_{dc}$ or $-0.5V_{dc}$) and the modulation signal of this phase is the zero sequence injection signal. Adding this zero sequence signal to all the modulation waves the DPWM modulation signals are generated. While the phase with the originally largest modulation signal is clamped to the DC rail with the same polarity with this signal, the other modulation signals are shifted by the zero sequence signal. Since for the clamped phase the switching process is halted, the switching losses disappear for the considered interval. In periodic steady-state with sinusoidal balanced operation (implying balanced sinusoidal modulation waveforms), the phases are clamped in a sequence every 60^o. Each switch is locked to the positive DC rail for 60^o and negative DC rail for 60^o thus, for one third of the fundamental cycle the switching process is disabled and the associated switching losses cease. In the three-phase four-leg inverter the same approach can be utilized as the three-leg inverter and instead of zero sequence signal, here the injection signal is the offset signal v_{fo}^*.

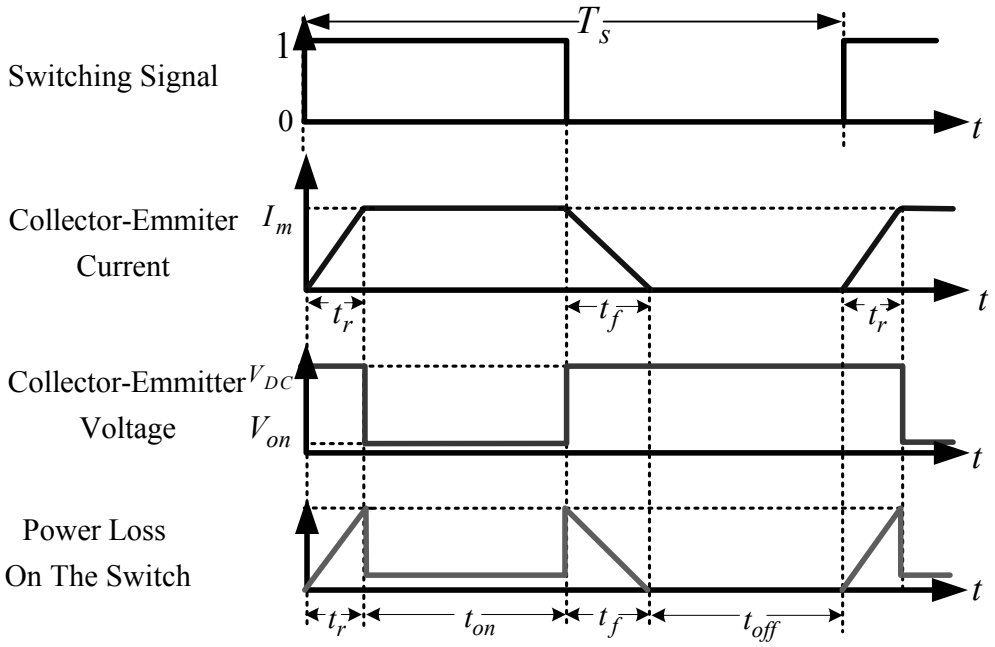


Figure 2.25 The characteristic waveforms of the switch in a switching period.

2.2.2.2.2.1. Classical DPWM (DPWM1)

For the four-leg inverter, the DPWM method can be applied in the same manner as in the three-leg inverter. In this case the original modulation waves are v_{af}^{*}, v_{bf}^{*}, v_{cf}^{*}. These signals are compared and the one with the largest magnitude is considered as the phase to be locked. The difference between the DC rail voltage with the same polarity as the signal with the largest magnitude is considered as the offset signal. Equation (2.24) describes the offset signal. Equivalently, considering the zero state partitioning function, the offset signal can be calculated as in (2.25). When the offset signal is calculated and injected to all the original modulation waves, the modulation signal becomes discontinuous. For balanced inverter reference voltages with 0.64 modulation index, the offset signal (v_{fo}^{*}) and modified reference signal (v_{ao}^{**}) are obtained as in Figure 2.26. The performance attributes of this DPWM method are similar to the three-leg inverter DPWM method characteristics [31].

$$\left|V_{xf}^{*}\right| > \left|V_{yf}^{*}\right|, \left|V_{zf}^{*}\right| \;\rightarrow\; V_{fo}^{*} = sign(V_{xf}^{*}) \cdot (V_{dc}/2) - V_{xf}^{*} \qquad \{x,y,z\} \in \{a,b,c\} \tag{2.24}$$

$$\xi = \begin{cases} 1 & \left|v_{fo\_top}^{*}\right| > \left|v_{fo\_bottom}^{*}\right| \\ 0 & \left|v_{fo\_top}^{*}\right| < \left|v_{fo\_bottom}^{*}\right| \end{cases} \tag{2.25}$$

The above discussed DPWM method offset voltage generation procedure involves the choice of the largest magnitude modulation signals. This choice provides the lowest switching losses for balanced operation with unity power factor (purely resistive) loading. However, the choice for selecting an offset voltage that clamps a switch to a DC rail is not limited to this method. A wider range exists and this can be used to the advantage of the inverter for the unbalanced loading or balanced leading/lagging power factor loading operating conditions. For this purpose, the load phase currents should also be involved in determining the zero state partitioning (or

v_{fo}^{*}). In that case, if possible it is better to choose the switch to be clamped as the switch of the phase with the largest current. Based on the angle of the phase current and modulation wave, the DPWM methods are classified as DPWM0, DPWM1, and DPWM2 or further generalized as GDPWM method [31]. Since DPWM methods can employ the offset signal injection at the largest possible range, in a similar manner to SVPWM, they can utilize the inverter voltage linearity range at the maximum rate. Although the output voltage/current ripple is noticeably higher at the low modulation index range, it has been shown that at the high modulation range their performance is comparable. It is favorable to utilize SPWM or SVPWM at low modulation index and switch over to DPWM above approximately 0.6 modulation index [9], [10], [31]. Additional advantages of DPWM are the reduction in the inverter deadtime effects, the diode reverse recovery dynamics/losses and associated noise in the circuit. For the UPS applications, it is highly favorable to employ DPWM because the operating range always involves the high modulation index range where the DPWM performance is superior to all the rest of the PWM methods.

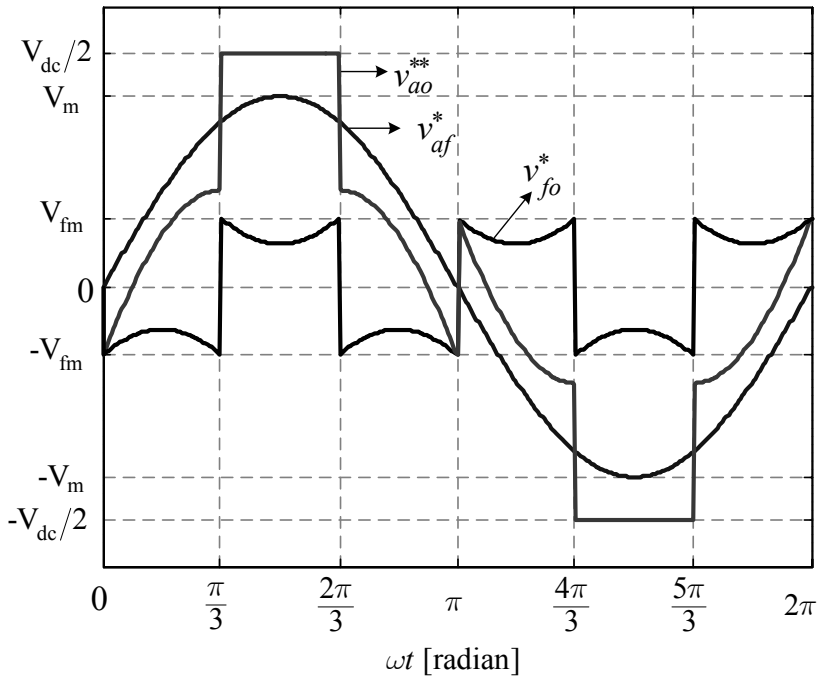


Figure 2.26 Illustrating the modulation wave of one phase of the four-leg inverter for DPWM at M_i=0.64.

2.2.2.2.2.2. Minimum Loss DPWM (MLDPWM)

The above discussed DPWM1 method provides minimum switching losses for balanced unity power factor load operating condition. As the load power factor angle deviates from zero, or as the load becomes unbalanced the DPWM1 method losses increase and become higher than the optimal losses. This is a consequence of the choice of the zero state partitioning which is developed based on the modulation signals only but not a function of the load current. With the choice of ξ being wider than what is selected in DPWM1, it is apparent that the switching losses can be decreased by choosing a more proper ξ than that of DPWM1 for such loading conditions. In this section a comprehensive method that optimally utilizes ξ for minimum switching losses is developed.

Since the v^*_{max} and v^*_{min} signals define the two possible phases to be locked to the proper rail of the DC bus, for minimum switching losses the choice between the two depends on the magnitude of the current associated with these phases. The phase that carries the larger current should be locked to the proper DC bus rail. This condition can be summarized in terms of ξ with the following formula.

$$\xi = \begin{cases} 0 & \left|I_{v_{max}}\right| > \left|I_{v_{min}}\right| \\ 1 & \left|I_{v_{max}}\right| < \left|I_{v_{min}}\right| \end{cases} \tag{2.26}$$

In equation (2.26) I_{Vmax} represents the inverter output current which corresponds to v^*_{max} and I_{Vmin} represents the inverter output current which corresponds to v^*_{min}. This modulation approach yields minimum switching losses and therefore it is termed as the minimum loss DPWM (MLDPWM) method. Figure 2.27 shows the flowchart of the proposed MLDPWM method. In the following the MLDPWM method will be discussed with respect to other DPWM methods and its superiority will be demonstrated.

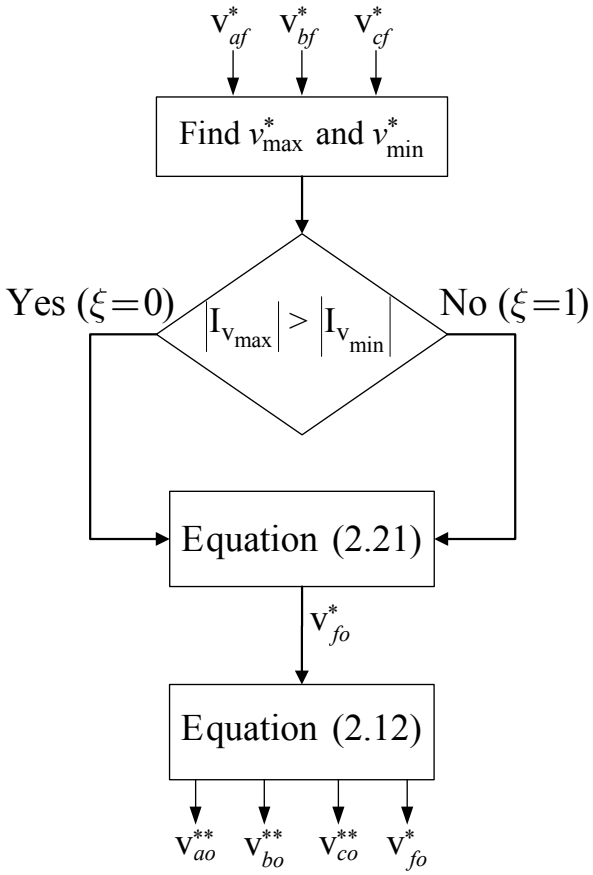


Figure 2.27 The flowchart of the MLDPWM method.

First the steady-state, balanced resistive load case will be considered. Neglecting the influence of the UPS LC filter components, the load can be considered as unity power factor load for the inverter. Also neglecting the PWM ripple, the load current can be considered sinusoidal. For the given operating condition, when the MLDPWM method is utilized, the three-phase reference voltages, inverter output currents and modulation signals for four-leg inverter are shown in Figure 2.28. It is apparent that the modulation signals of MLDPWM and DPWM1 are the same and the losses are minimal as expected. Since the power factor is unity and load current has a same shape with the reference voltage for each phase, the reference voltage with the maximum magnitude and the load current with the maximum magnitude coincide and this phase is locked to the proper DC rail. Hence, minimum switching losses are obtained. In MLDPWM switching ceases only in the a-b-c phase legs and

the fourth leg has continuous PWM characteristic. However, due to nearly zero current, the switching losses in this leg are negligible.

In UPS applications the single-phase load operating condition is quite frequent. In this case the loss characteristics of MLDPWM and DPWM1 are not exactly the same. Figure 2.29 shows the modulation waveforms for the DPWM1 method for the single-phase resistive load operating condition. As the modulation characteristics remain the same, in the single-phase operating condition the phase that conducts the loaded current (in Figure 2.29 phase "a") is locked to the positive DC rail for 60^o and negative DC rail for 60^o totaling 120^o lock-out. The fourth leg which now conducts the same phase current is operating under continuous modulation and its losses become significant as the current in the neutral wire becomes equal to the load current. As shown in Figure 2.30, in the MLDPWM case, the PWM algorithm of (2.26) results in longer DC bus clamping intervals for the modulation signal than DPWM1. As can be seen from the figure the loaded phase is locked to each side of the DC rail by 120^o yielding a total of 240^o lock-out and the switching losses decrease appreciably. In the regions of 0^o-30^o, 150^o-210^o and 330^o-360^o in Figure 2.30, v_{af}^* is not one of the extremum reference voltages. Although I_a has higher amplitude than the other load currents (which are zero), if phase "a" is clamped to one side of the DC bus in these intervals, the voltage linearity will not be maintained. Therefore in these intervals, phase "a" is not clamped to the DC rail.

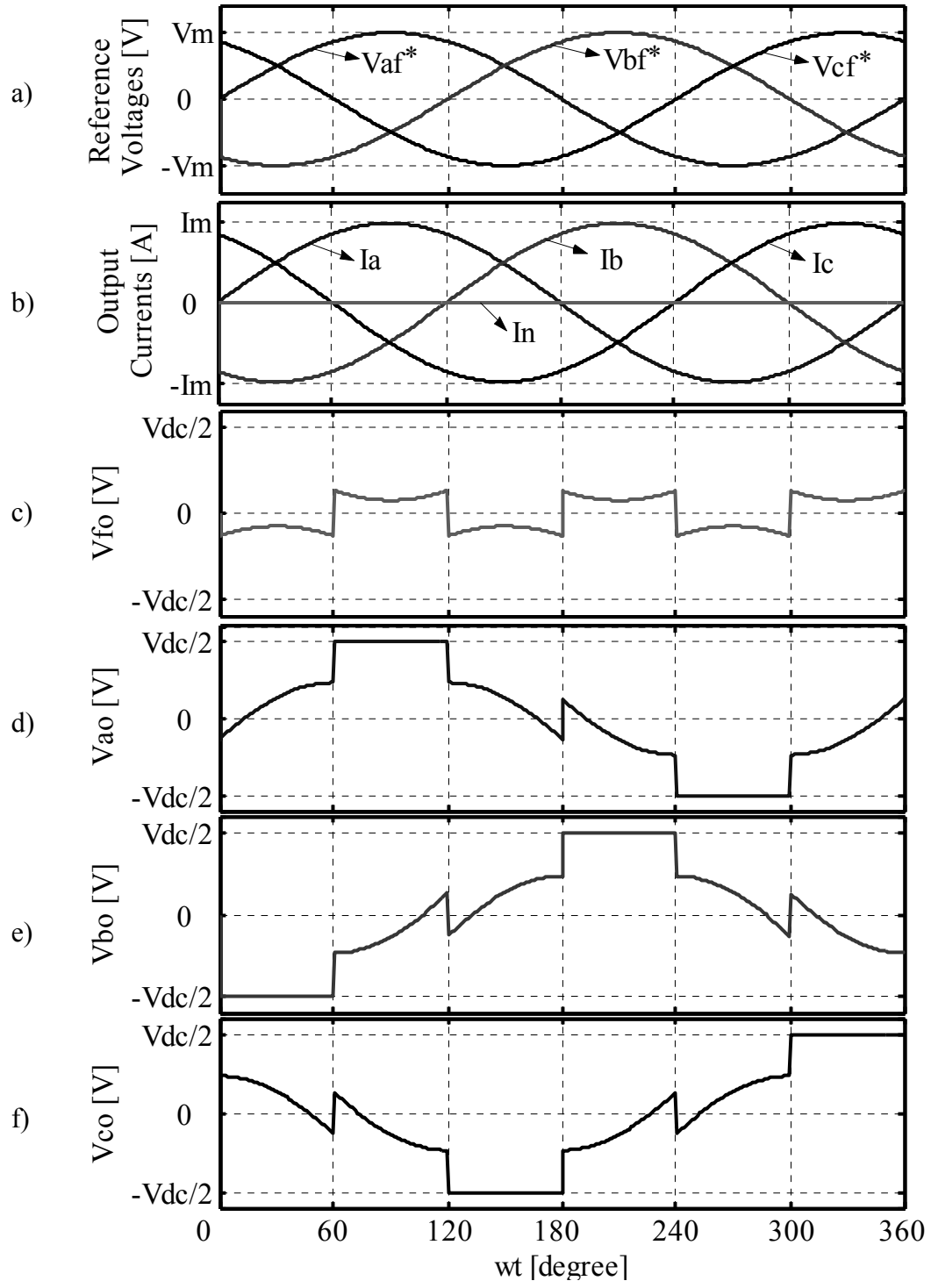


Figure 2.28 The MLDPWM waveforms of the four-leg inverter under balanced unity power factor load operating condition. (a) three-phase reference voltages, (b) inverter output currents, (c) v_{fo}^{*}, (d) v_{ao}^{**}, (e) v_{bo}^{**}, (f) v_{co}^{**}.

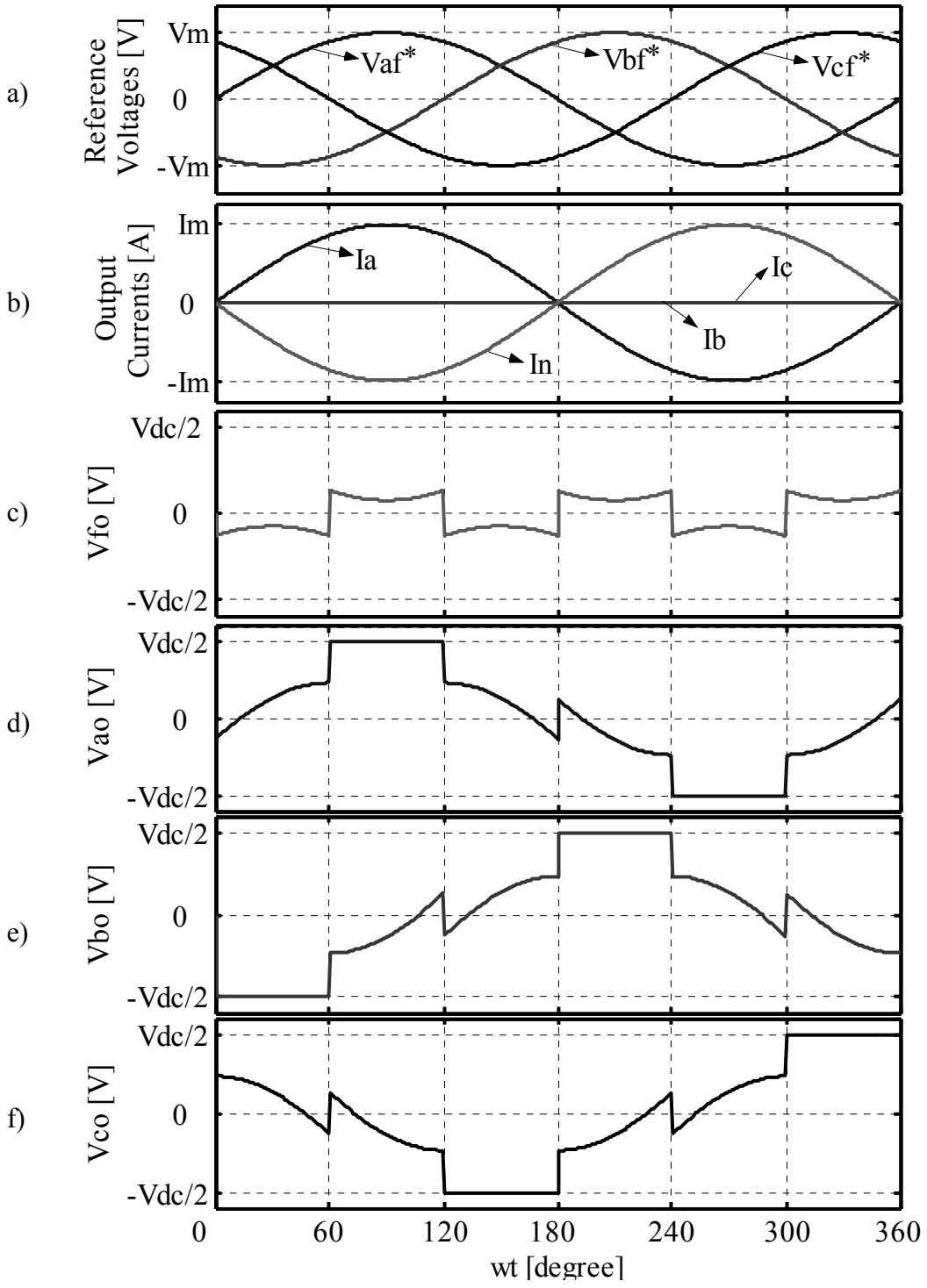


Figure 2.29 The waveforms of the four-leg inverter based three-phase UPS with DPWM1 method under line-neutral unbalanced resistive load condition, (a) three-phase reference voltages, (b) inverter output currents, (c) v_{fo}^{*}, (d) v_{ao}^{**}, (e) v_{bo}^{**}, (f) v_{co}^{**}.

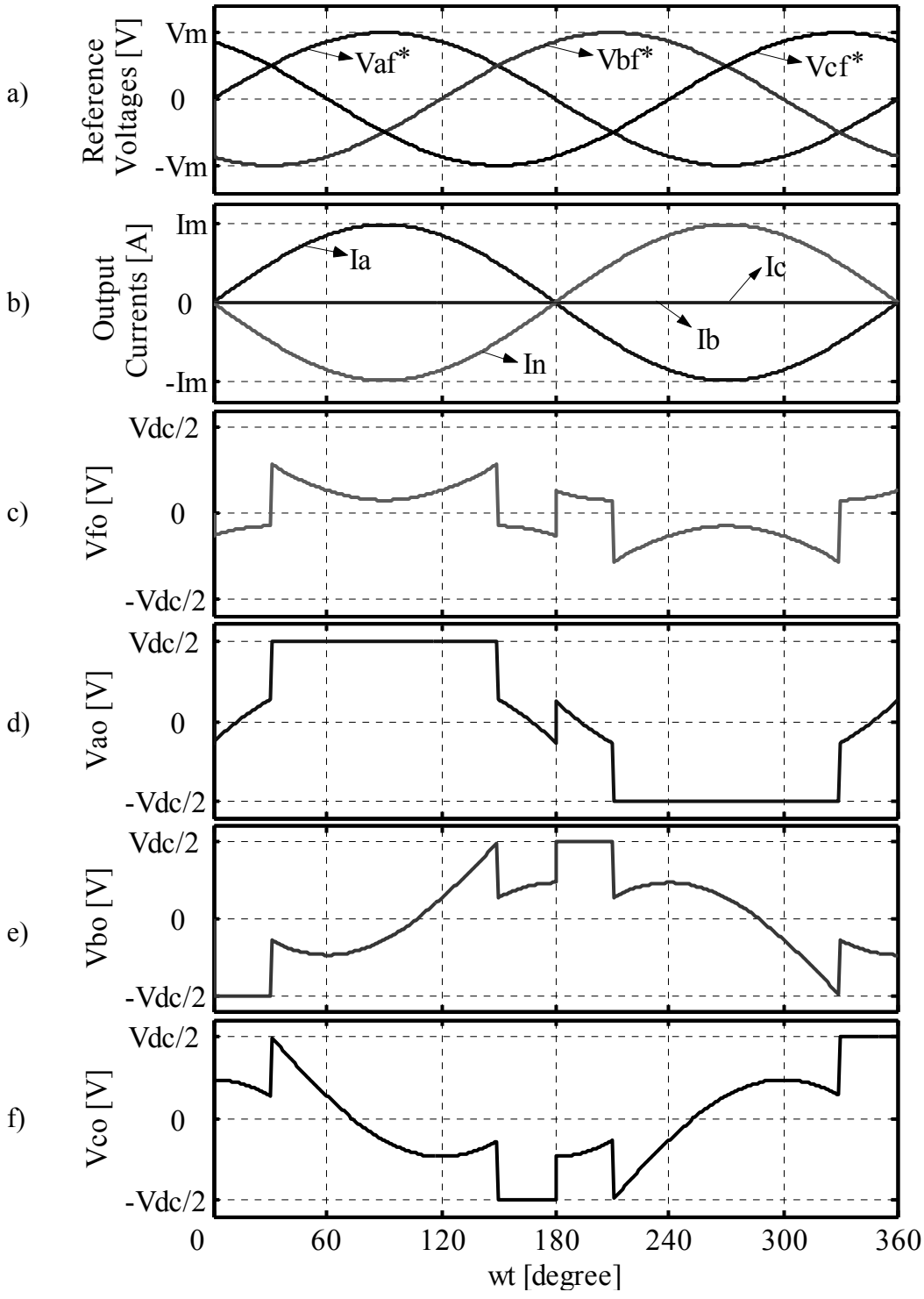


Figure 2.30 The waveforms of the four-leg inverter based three-phase UPS with MLDPWM method under single-phase resistive load operating condition, (a) three-phase reference voltages, (b) inverter output currents, (c) v_{fo}^{*}, (d) v_{ao}^{**}, (e) v_{bo}^{**}, (f) v_{co}^{**}.

Utilizing the formula in (2.23) to calculate the switching losses and considering the switching losses of CPWM methods for balanced load as the base value, the percentage of switching losses for various PWM methods can be calculated. The results are shown in Table 2.3. According to the table, for balanced resistive load the switching losses of MLDPWM and DPWM1 are the same and 50% of CPWM method losses. For the single-phase unbalanced load case MLDPWM switching losses are nearly half the CPWM losses and about 24% less than the losses of the DPWM1 method.

Notice that the unbalanced load operating condition significantly stresses the fourth leg as large current flows through this leg. As the worst case single-phase full-load operating condition stresses the fourth leg significantly. Since in this case the loaded phase leg is operating under DPWM condition, its switching losses are less than those of the fourth leg which operates under CPWM condition. Thus in this operating condition the loss partitioning of the fourth leg and the phase leg is 33/38 for the fourth leg and 5/38 for the phase leg. Therefore, during the design, the fourth leg should thermally be considered as a more dissipative element than the regular phase legs when MLDPWM is the main PWM algorithm in the UPS design. The fourth leg could be considered a normal phase designed for CPWM operating condition.

Table 2.3 Percentage of switching losses for balanced and single phase unbalanced resistive load for various PWM methods

Switching losses (%)	CPWM	DPWM	
	SVPWM	DPWM1	MLDPWM
Balanced load	100	50	50
Line-neutral unbalanced load	66	50	38

For balanced load with a power factor other than unity, the MLDPWM method performance is maintained at 50% of CPWM methods, provided that the power factor angle is within $\pm 30^{o}$ range. Outside this range the losses increase, but still remain less than the alternative method. The performance of MLDPWM method is similar to that of GDPWM method developed for the three-leg inverter [31].

The PWM voltage and current ripple performance of the MLDPWM method is inferior compared to the CPWM methods such as SVPWM. Since for the same carrier frequency the switching count decreases by a significant amount, the on durations of the inverter states increase and therefore the voltage ripple and as a result the current ripple becomes larger compared to CPWM methods. Since this attribute is also modulation index dependent and at the higher half of the linear modulation range the DPWM methods provide satisfactory performance, this is not considered as a performance issue for UPS systems which always operate at high modulation index under normal operating conditions. Therefore the PWM current ripple is not considered as an important issue in the UPS application of MLDPWM.

As a summary it can be stated that the MLDPWM method provides switching loss reduction and specifically improves the thermal performance greatly for the balanced and unbalanced load operating conditions, varying power factor load conditions of a UPS. Therefore, it should be favored in the UPS applications for the purpose of energy efficiency enhancement at practically no cost.

With the modulation methods for the four-leg inverter established and the simplicity and performance of the scalar PWM methods discussed in detail, and specifically with the superior attributes of MLDPWM method proven, the following chapter places focus on the controller structures to be utilized in a UPS that employs the four-leg inverter and the scalar PWM methods, specifically the MLDPWM method.

CHAPTER 3

OUTPUT VOLTAGE CONTROL OF THE THREE-PHASE FOUR-LEG UPS BY MEANS OF RESONANT FILTER BANKS

3.1. Introduction

This chapter focuses on the output voltage control of the four-leg inverter based UPS system. The resonant filter bank based voltage loop controller is complemented with voltage feedforward controller and capacitor current feedback based active damping loop. With this controller structure the UPS system exhibits superior steady-state and dynamic performance under all practical operating conditions such as full load, nonlinear load, unbalanced load, etc.

The study in this chapter begins with the theoretical study of the resonant filter controller. In this study the controller characteristics are investigated in detail. Controller bandwidth, damping, implementation issues etc. are investigated in depth. Following the resonant filter controller study, the capacitor current feedback based active damping loop is discussed. Via analytical modeling of the UPS system, the stability analysis of the UPS system, in which the resonant filter controller and the capacitor current feedback take place, is performed by means of the Routh-Hurwitz stability criterion. Then a design example is discussed. The given design will be later utilized in the simulations and practical implementation in the following chapters.

3.2. Resonant Filter Bank Control Method

A resonant filter controller consists of a transfer function which has very large gain and zero phase delay at a frequency of interest which is defined as the resonant frequency. Elsewhere the gain becomes negligibly small and the phase relation becomes insignificant. In control applications where the reference signal is a DC signal and perfect tracking of the reference signal without steady-state error is required, a proportional and integral (PI) type controller is utilized. In the PI controller the integral term provides infinite gain for the DC signal forcing the steady-state error to zero. The resonant filter controller applies the same principle to AC signals. With the controller gain made very large at the resonant frequency which is selected to be the frequency of the references signal, the resonant filter controller acts as an integrator at the resonant frequency and yields infinite gain resulting in zero steady-state error at this frequency. Various types of resonant filter type controllers have been reported in the literature recently [25], [26], [27], [28], [29] and applications to motor control, active power conditioners, UPSs, and other power electronic systems have been reported. Various names such as "generalized integrator" [27] and "resonant controller" [28], [29] have been utilized for this class of controllers. Since the word resonant gives intuitive meaning to the concept, this name is preferred in this thesis. Since in the UPS application a set of resonant controllers are utilized in parallel, also the control method is termed as "resonant filter bank control method."

3.2.1. Ideal Resonant Filter

In the UPS application, the resonant filter controller is constructed in the stationary (original) frame (without coordinate transformations) and has a superior performance similar to the linear PI regulator in synchronous frame [28]. The resonant filter controller has a transfer function as given in (3.1), where the K_{im} constant is the integral gain of the controller.

$$G_c(s) = \frac{2K_{im} \cdot s}{s^2 + (m\omega_e)^2} \tag{3.1}$$

The resonant filter controller has infinite gain and zero phase at the resonant frequency ($m\omega_e$), and zero gain elsewhere as shown in Figure 3.1. The phase relation is such that below the resonant frequency the resonant filter provides 90^o leading compensation while above the resonant frequency the filter provides 90^o lagging compensation. The resonant frequency is selected to be the frequency of the AC signal to be controlled. The gain is optimized by considering the system dynamic and steady-state performance requirements. As an example, employing a resonant filter at the fundamental frequency of a single phase UPS (at 50 Hz), the UPS output voltage error can be fed to the resonant filter controller and the controller precisely controls the fundamental component at the desired phase and magnitude (zero steady-state phase and magnitude error). However, the controller can not compensate the harmonic components, since the controller provides zero compensation for the harmonic components of the output voltage by applying zero gain. Likewise, dominant harmonics at the output voltage can be manipulated by a resonant filter for each dominant harmonic frequency. Thus, depending on the existing harmonic components the resonant frequency multiplier *m* is selected. For example, for a single phase UPS, the dominant harmonics are the odd harmonics. In this case, *m=2k-1* where *k=1,2,3,...* is an integer and for *k=1* the fundamental component, and for *k>1* harmonics are considered. Including as many as necessary resonant filters and connecting them in parallel a filter bank is formed. For example in the four-leg inverter based UPS, for each phase a filter bank is formed as shown in Figure 3.2. Thus three filter banks are utilized. All resonant filters of one phase are fed with the voltage error of that phase. When the output of each controller is summed, the reference inverter voltage, which is applied to the PWM module, is obtained.

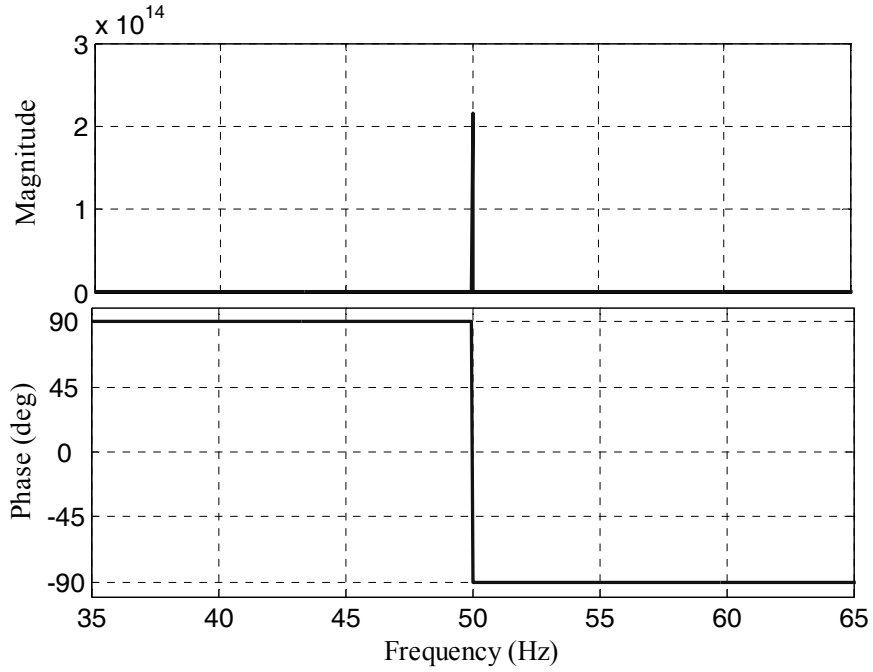


Figure 3.1 Bode plot waveforms of the ideal resonant filter controller for m=1, K_{i1}=10, ω_e=2π50 rad/sec.

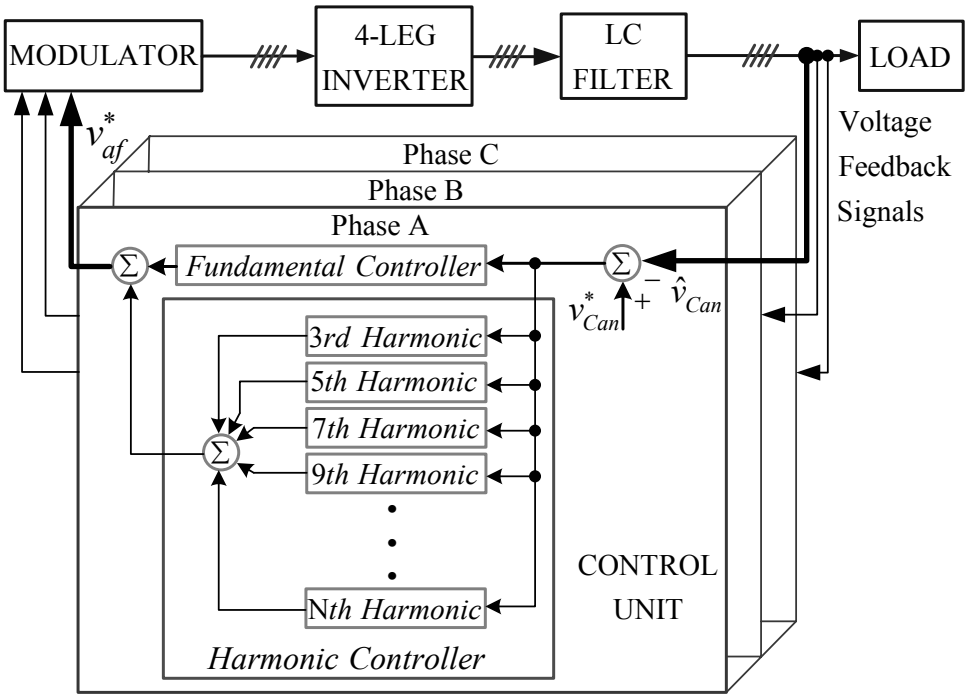


Figure 3.2 The resonant filter bank based output voltage control block diagram of the three-phase four-leg UPS.

The implementation technique of the resonant filter controller can be varied depending on the type of the inverter, which is utilized in the three-phase UPS applications. In the three-phase four-leg inverter, due to the fourth leg, each phase can be controlled independently (as if there were three independent inverters). Thus, there is no need for transformation from stationary frame a-b-c coordinates to stationary frame ds-qs-0 coordinates, and from stationary frame ds-qs-0 coordinates to synchronous frame de-qe-0 coordinates transformations. For each phase, one identical resonant filter bank is utilized and the output voltage error of each phase is converted to the inverter phase voltage reference (v_{af}^{*}, v_{bf}^{*}, v_{cf}^{*}) through the associated filter bank. Thus, the fundamental component is controlled without involved positive/negative/zero sequence decomposition and complex controllers which is the conventional approach [22]. Harmonics are also manipulated in the same manner in the simple resonant filter bank structure. The resonant filter controller provides an easy design and implementation task with respect to the synchronous frame based controller or other complex control algorithms.

3.2.2. Phase Delay Compensation of The Resonant Filter

The practical application (implementation) of the resonant filters involves more detailed structure than the ideal structure given in (3.1). If the system delay, which is the total delay originating from the individual delays of the UPS system stages, is ignored, the controller performance decreases especially at high frequencies. Practically, the measurement, signal processor, and inverter units introduce delays that can have significant influence on the controller performance, especially at the high frequency range. The measurement delay ($\tau_{measure}$) occurs at the stage of the measurement and signal conditioning of the voltage and current feedback signals. The sampling delay (τ_{samp}) is due to transferring the measured signals to the DSP. The computation delay (τ_{comp}) is due to processing the sampled signals and the algorithm. The PWM delay (τ_{PWM}) is due to the discrete nature of the inverter. These delays are illustrated with respect to a PWM cycle in Figure 3.3. As the figure shows, the sampling delay τ_{samp} includes the A/D conversion time, the computation time, and

the idling time. The sum of all these delays is the total delay τ_T and it is expressed in the following.

$$\tau_T = \tau_{measure} + \tau_{samp} + \tau_{PWM} \tag{3.2}$$

The phase shift due to these delays, ϕ_m, varies with the frequency, and can be obtained as a function of the total system delay and the resonant frequency ($m\omega_e$) of the controller, as given in (3.3). The phase shift is directly proportional to the frequency. Therefore, the phase shift becomes effective at the high frequencies while it can be ignored at the low frequencies. The ideal transfer function of the resonant filter controller, given in (3.1) should be modified such that the effect of delay is compensated (the control signals should be phase advanced by ϕ_m). Since (3.1) is the Laplace transform of cos ($m\omega_e t$), the phase shift should be considered as a process of adding a phase advance angle to the resonant term, implying the cosine function angle should be advanced. Thus the delay compensated time domain equivalent of the resonant filter is cos ($m\omega_e t+\phi_m$) and the Laplace transform of the phase advanced cosine term shown in (3.4) gives the modified resonant filter as in (3.5). In this manner, the transfer function of the phase shifted resonant filter controller is obtained.

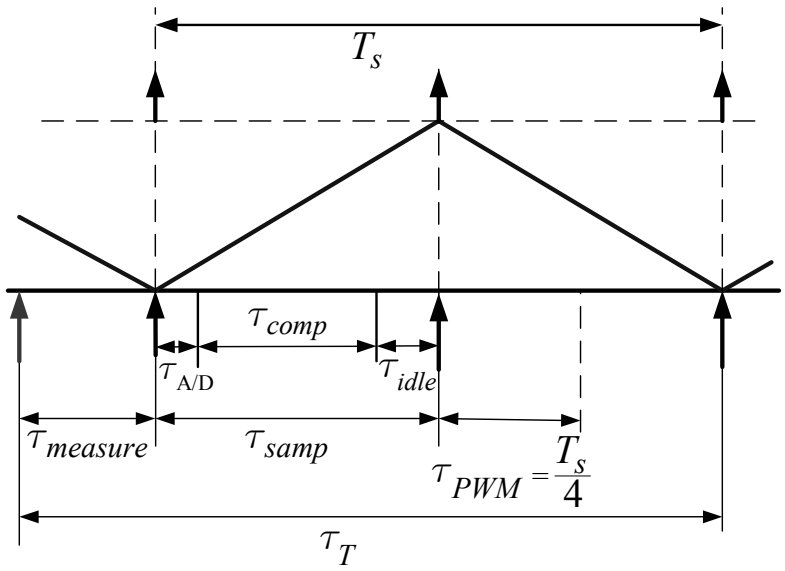


Figure 3.3 Illustration of the controller delay elements over a PWM cycle.

$$\phi_m = \tau_T \cdot m\omega_e \tag{3.3}$$

$$\mathcal{L}\left[2K_i \cos(m\omega_e t + \phi_m)\right] = 2K_{im}\left(\frac{s\cdot\cos(\phi_m) - m\omega_e \cdot \sin(\phi_m)}{s^2 + (m\omega_e)^2}\right) \tag{3.4}$$

$$G_c(s) = 2K_{im}\left(\frac{s\cdot\cos(\phi_m) - m\omega_e \cdot \sin(\phi_m)}{s^2 + (m\omega_e)^2}\right) \tag{3.5}$$

3.2.3. Damping and Selectivity of The Resonant Filter

Applying the resonant filter in the form given in (3.5) involves difficulties both from performance and implementation point of view. Since the above form is a loss-less resonant filter, the gain of the filter at the resonant frequency is very high and the sidebands are very small. This implies that the controller is highly selective and can only track a reference exactly at the designed value of $m\omega_e$. However, in certain application the frequency of the reference signal is variable. For example, in the on-line UPS application, the output voltage frequency should track the utility grid

frequency for the purpose of transient free by-pass of the load to the grid via the by-pass static switches (back-to-back thyristors). This may be necessary for the purpose of operation at high efficiency (in the so called eco-mode), providing maintenance, or operating from the utility line following a UPS system failure. For that purpose, the UPS output voltage frequency must track the line frequency which varies within a small range (typically ±0.5Hz for the 50Hz utility grid in Turkey). Therefore, applying the resonant filter bank control method to the on-line UPS involves a wider band operation than what the lossless resonant filter provides. Thus, the bandwidth of the resonant filter controller should be widened for improved tracking over a specified frequency range.

In case the controller is implemented with a fixed point signal processor, another issue comes to stage. Since in a fixed point signal processor a number can be represented with a finite word length, the coefficients of the discrete time implemented filter become an issue as loss of significance occurs in implementing the resonant controller. While the word length limitation is not an issue in floating point signal processors, this is a major issue in fixed point processors. The discrete time implemented lossless resonant filter coefficients become extreme values, some of which approach zero while others approach unity. Implementing the controller in fixed point processor results in loss of significance as some small numbers are lost. The end result is poor controller performance where the phase and magnitude of the resonant filter become significantly different from the theoretical values. This results poor output voltage tracking in performance.

For the two reasons discussed in the above two paragraphs, the resonant filter is usually not implemented in (3.1) or (3.5) forms, but the selectivity of the filter is decreased by flattening and widening the gain characteristic of the filter via modifying the original structure. Utilizing the basic lossless resonant filter equation of (3.1), the damped resonant filter can be expressed as given (3.6) where ζ_m is the damping and $m\omega_e$ is the resonant frequency of the damped resonant filter.

$$G_c(s) = \frac{2K_{im} \cdot \zeta_m m\omega_e \cdot s}{s^2 + 2\zeta_m m\omega_e \cdot s + (m\omega_e)^2} \tag{3.6}$$

By utilizing the second order transfer function characteristic via (3.6), the flattening of the gain characteristic can also be considered as increasing the damping or reducing the quality factor of the resonant filter. For the purpose of describing the degree of flattening or damping, the selectivity function S given in (3.7) is defined [32]. In this equation the resonant frequency is $m\omega_e$ and the corner frequency where the gain drops to 70.7% is $m\omega_e \pm 0.5\Delta\omega$ as shown in Figure 3.4 which is drawn by utilizing (3.7). The gain curve of the resonant filter is practically symmetric with respect to the resonant frequency $m\omega_e$ and the gain at $m\omega_e - 0.5\Delta\omega$ and $m\omega_e + 0.5\Delta\omega$ is practically the same as the substitution of both frequencies normally yield numerically negligible terms which cause the difference between the two.

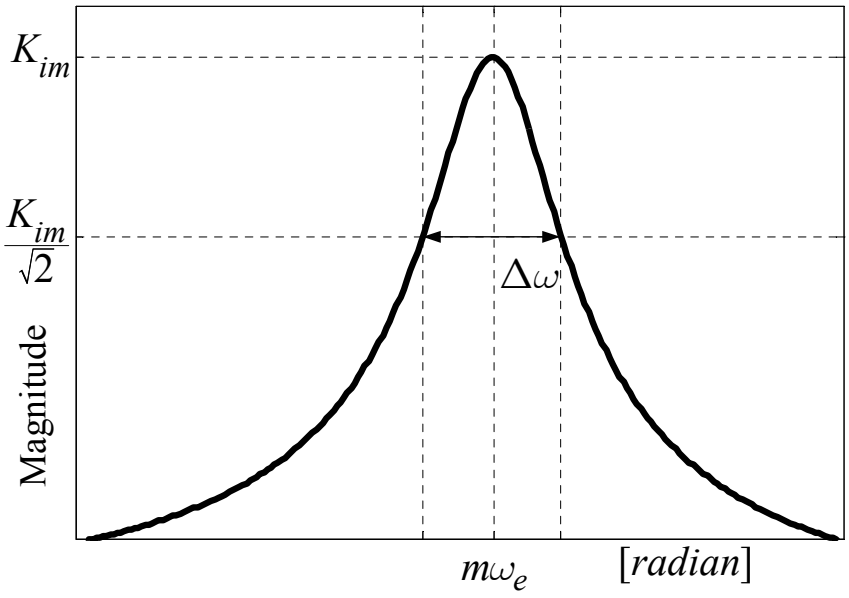


Figure 3.4 The gain characteristic of a damped resonant filter.

$$S = \frac{resonant\ frequency}{bandwidth} = \frac{m\omega_e}{\Delta\omega} \tag{3.7}$$

The resonant filter damping ζ_m is related to the resonant filter corner frequency in the following.

$$\Delta\omega = 2\zeta_m m\omega_e \tag{3.8}$$

The selectivity can be expressed in terms of the filter damping by substituting (3.8) in (3.7) in the following.

$$S = \frac{1}{2\zeta_m} \tag{3.9}$$

With the dampened characteristic, the resonant filter provides less than ideal characteristics. Comparing the ideal resonant filter of Figure 3.1 with a resonant filter with the damping value of $3.18\text{x}10^{-3}$ ($\zeta_1\omega_e$=1 rad/s) of which the gain characteristic is shown in Figure 3.5, it can be seen that both the gain and selectivity decrease significantly. However, the filter becomes more effective over a wider operating frequency range. In order to compensate for the gain loss at the resonant frequency, the K_{im} gain should be increased to a sufficient value.

In the UPS output voltage control system for each phase a fundamental frequency resonant filter controller and a specific number of harmonic frequency resonant filters are utilized. With the input being the output voltage error to all of them, the output of each filter provides compensation for its own frequency error. Thus, the superposition of all the outputs is the total feedback based reference voltage for each phase. From here it becomes clear that multiple resonant filters are connected in parallel. As a result a resonant filter bank is formed. This resultant filter is often termed as the "multi-resonant" filter. The filter bank components may have equal or different damping (or selectivity) characteristics. Figure 3.6 shows the multi-resonant filter gain and phase characteristics for the case that the selectivity or

damping remains the same for all the frequencies. This implies that for increasing frequencies the frequency sideband also increases. On the contrary for the case where the sidebands remain the same, the selectivity increases with frequency as shown in Figure 3.7. For the latter case the higher frequency filter components become highly selective and in practice if the measured harmonics are not exactly at the selected resonant frequency, the filter performance becomes unsatisfactory. In both graphics the filter gains are selected the same for all frequencies for the sake of illustration. However, in practical implementation gains should be treated differently and each frequency requires a different gain value.

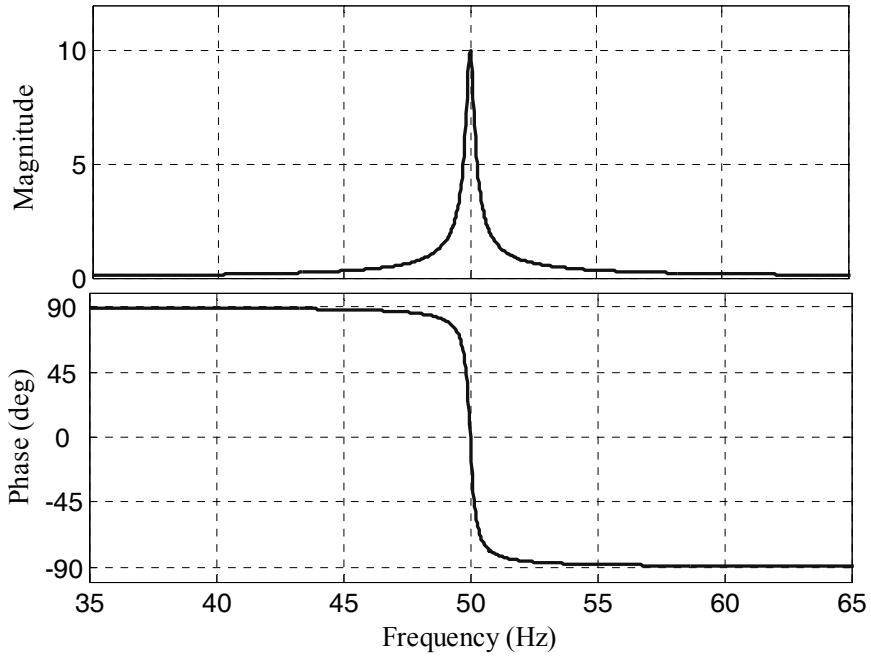


Figure 3.5 The gain and phase characteristics of the damped resonant filter for m=1, K_{i1}=10, ω_e=2π50 rad/s, ζ_1 =3.18x10^{-3}.

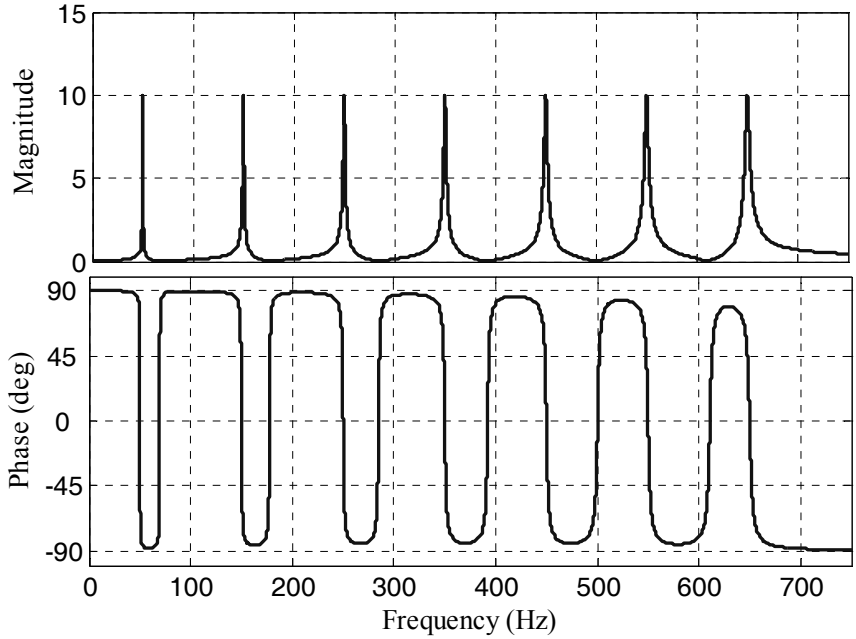


Figure 3.6 The gain and phase characteristics of the damped resonant filter bank for m={1, 3, 5, 7, 9, 11, 13}, K_{im}=10, ω_e=2π50 rad/s, ζ_m =3.18x10^{-3}, S=100π.

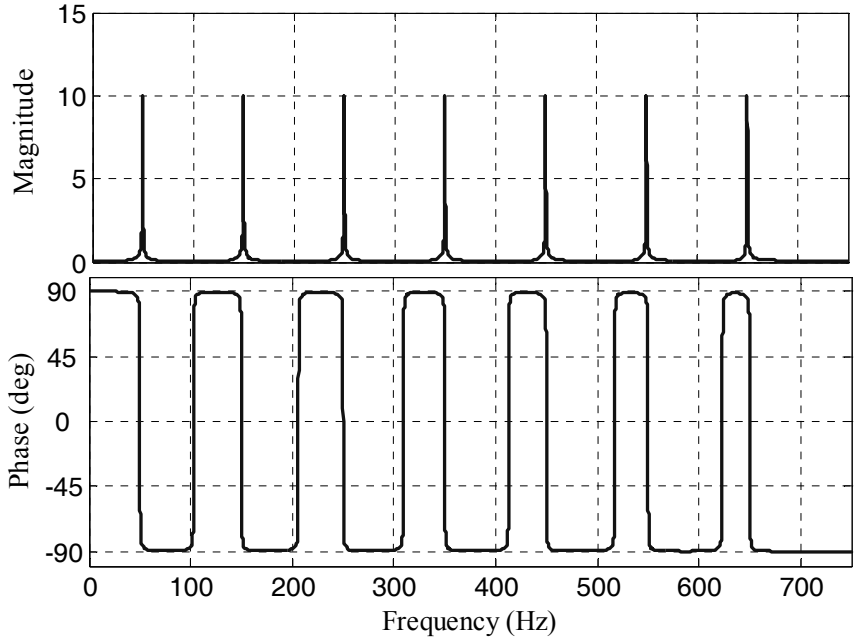


Figure 3.7 The gain and phase characteristics of the damped resonant filter bank for m={1, 3, 5, 7, 9, 11, 13}, K_{im}=10, ω_e=2π50 rad/sec, $\zeta_m = m\cdot 3.18\text{x}10^{-3}$, S=$m$·100π.

3.2.4. Phase Delay Compensated and Damped Resonant Filter Banks

By considering the phase shift compensation modification given in equation (3.5) and added damping via the damped second order structure given in equation (3.6) together, the final transfer function of the resonant controller can be obtained. For this purpose complex variables theory will be utilized. The Laplace transform of a function consisting of the multiplication of any time variable function *f(t)* and $\cos(\omega_e t)$ can be found from (3.10). Likewise, the Laplace transform of $f(t)\cdot\sin(\omega_e t)$ can be found from (3.11). Accounting for the phase delay of ϕ_m, equation (3.10) can be modified as (3.12). Selecting *f(t)* as given in (3.13), taking its Laplace transform as in (3.14), and substituting in (3.12), a transfer function $G_c(s)$ as given in (3.15) is obtained. In practical applications ζ_m is small and typically $\zeta_m \ll 1$. With this assumption, the transfer function of (3.15) can be simplified as in (3.16).

$$\mathcal{L}\left[f(t)\cdot\cos(\omega t)\right]=\frac{1}{2}\left[F(s+j\omega)+F(s-j\omega)\right] \tag{3.10}$$

$$\mathcal{L}\left[f(t)\cdot\sin(\omega t)\right]=\frac{j}{2}\left[F(s+j\omega)-F(s-j\omega)\right] \tag{3.11}$$

$$\mathcal{L}\left[f(t)\cdot\cos(m\omega_e t+\phi_m)\right]=\mathcal{L}\left[f(t)\cdot\cos(m\omega_e t)\cos(\phi_m)\right]-\mathcal{L}\left[f(t)\cdot\sin(m\omega_e t)\sin(\phi_m)\right]$$

$$\begin{aligned}&=\frac{\cos(\phi_m)}{2}\left[F(s+jm\omega_e)+F(s-jm\omega_e)\right]-\\&\ldots\frac{j\sin(\phi_m)}{2}\left[F(s+jm\omega_e)-F(s-jm\omega_e)\right]\end{aligned} \tag{3.12}$$

$$f(t)=2K_{im}\cdot\zeta_m m\omega_e e^{-j\zeta_m m\omega_e t} \tag{3.13}$$

$$F(s)=\frac{2K_{im}\cdot\zeta_m m\omega_e}{s+\zeta_m m\omega_e} \tag{3.14}$$

$$G_c(s)=\frac{\cos(\phi_m)}{2}\left[\frac{2K_{im}\cdot\zeta_m m\omega_e}{s+jm\omega_e+\zeta_m m\omega_e}+\frac{2K_{im}\cdot\zeta_m m\omega_e}{s-jm\omega_e+\zeta_m m\omega_e}\right]-$$
$$\cdots\frac{j\sin(\phi_m)}{2}\left[\frac{2K_{im}\cdot\zeta_m m\omega_e}{s+jm\omega_e+\zeta_m m\omega_e}-\frac{2K_{im}\cdot\zeta_m m\omega_e}{s-jm\omega_e+\zeta_m m\omega_e}\right] \tag{3.15}$$

$$=\frac{2K_{im}\cdot\zeta_m m\omega_e}{\left(s+\zeta_m m\omega_e\right)^2+\left(m\omega_e\right)^2}\left[\left(s+\zeta_m m\omega_e\right)\cos(\phi_m)-m\omega_e\sin(\phi_m)\right]$$

$$G_c(s)=\frac{2K_{im}\cdot\zeta_m m\omega_e\left(s\cos(\phi_m)-m\omega_e\sin(\phi_m)\right)}{s^2+2\zeta_m m\omega_e s+\left(m\omega_e\right)^2} \tag{3.16}$$

The transfer function in (3.16) corresponds to a resonant filter with damped and phase advanced resonant filter which is the practically necessary form of a resonant filter. With the phase compensation angle of the filter ϕ_m being equal to the phase delay of the system and with the damping value being equal to what is required in a practical application, the resonant filter can be shaped appropriately with these two parameters. Equation (3.16) is a basic practical resonant filter structure and its five parameters K_{im}, m, ω_e, ζ_m, and ϕ_m are the variables to be utilized in shaping the filter characteristics in the output voltage controller design procedure of the UPS. Figures 3.8 and 3.9 show the multi-resonant filter gain and phase characteristics for the phase advanced and damped resonant filter. In Figure 3.8, in the resonant filter the selectivity (or damping) remains the same and the sidebands increase with the resonant frequency for all the frequencies. In the case of varying selectivity shown in Figure 3.9, the sidebands remain the same and the selectivity increases with the frequency. In both figures, the phase delay is kept constant as $\phi_m=2T_s\cdot m\omega_e$. The final form of the resonant filter structure given in (3.16) will be utilized in this thesis for the purpose of controlling the output voltages of the four-leg UPS system. The implementation of the controller will be realized with a modern digital signal processor. Thus, the filter structure must be converted to the discrete time form which involves the z-domain rather than s-domain. In the following the discrete time equivalent of the resonant filter and its real time discrete time implementation form will be discussed.

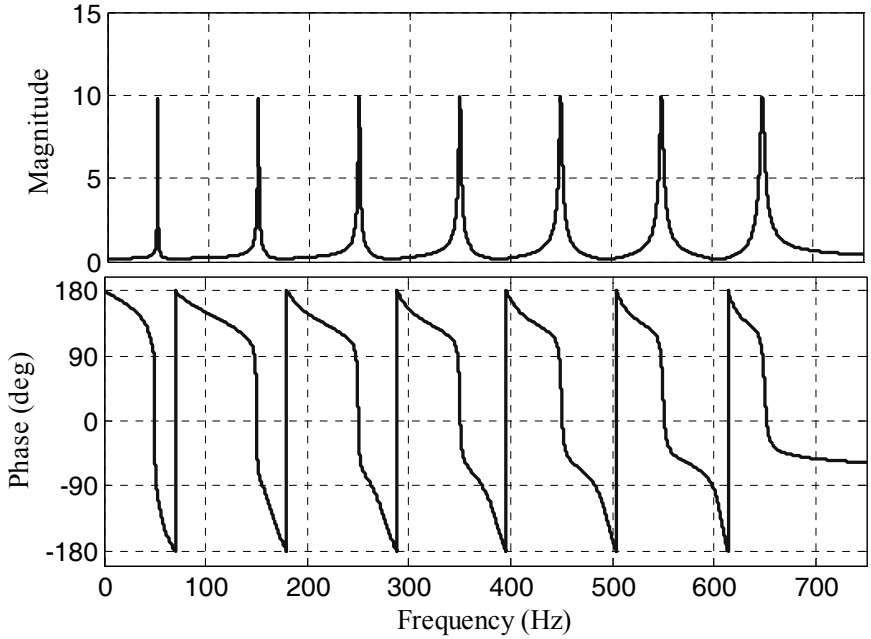


Figure 3.8 The gain and phase characteristics of the phase compensated and damped resonant filter bank for m={1, 3, 5, 7, 9, 11, 13}, K_{im}=10, ω_e=2π50 rad/sec, $\zeta_m = 3.18\text{x}10^{-3}$, S=100π, ϕ_m=2$T_s \cdot m\omega_e$.

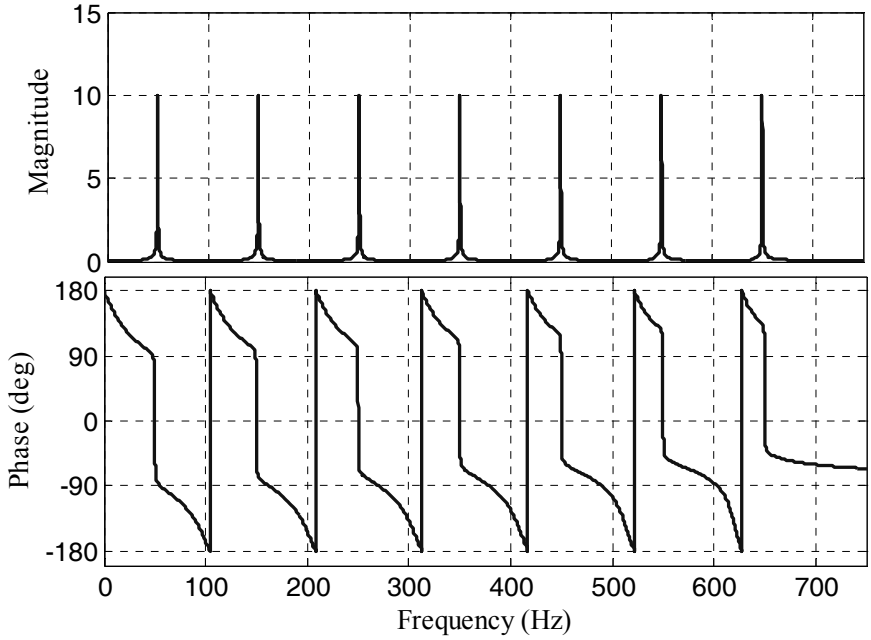


Figure 3.9 The gain and phase characteristics of the phase compensated and damped resonant filter bank for m={1, 3, 5, 7, 9, 11, 13}, K_{im}=10, ω_e=2π50 rad/sec, $\zeta_m = m \cdot 3.18\text{x}10^{-3}$, S=$m \cdot$100π, ϕ_m=2$T_s \cdot m\omega_e$.

3.2.5. Discrete Time Implementation of Resonant Filter Banks

The resonant filter controller in the above discussion was investigated in the s-domain which is the conventional design domain for the continuous time (analog) systems. Due to established literature, background, and experience in this approach, it is easy to understand and apply to analog systems. Therefore, it is common to design the resonant filter in the s-domain. However, in order to adapt the controller to a microcontroller, the controller structure should be expressed in the z-domain where the discrete time model easily leads to discrete time equations to be utilized in the real time implementation of the controller. There are several methods to provide transformation between s-domain and z-domain. In this work, the Tustin transformation method, which is given in (3.17), is applied. In the transformation, the effect of warping is compensated for via the pre-warping coefficient A_m which is defined in (3.18). The pre-warping coefficient improves the accuracy of the s-domain to z-domain transformation so that s-domain designed controller can be transformed to z-domain easily and then the discrete time equations are obtained for real time control. By utilizing the Tustin transformation, equation (3.16) is transformed to equation (3.19) where *X(z)* (the output voltage error) is the input of the resonant filter and *Y(z)* (the feedback compensation signal) is the output of the resonant filter. The coefficients, of equation (3.19) are given in equations (3.20), (3.21), (3.22), (3.23), (3.24).

$$s = \frac{z-1}{z+1} \times A_m \tag{3.17}$$

$$A_m = \frac{m\omega_e}{tan\left(m\omega_e \cdot T_s \diagup 2\right)} \tag{3.18}$$

$$G_c(z) = \frac{Y(z)}{X(z)} = \frac{a_{0m} + a_{1m} \cdot z^{-1} + a_{2m} \cdot z^{-2}}{1 + b_{1m} \cdot z^{-1} + b_{2m} \cdot z^{-2}} \tag{3.19}$$

$$a_{0m} = K_{im} \frac{2\zeta_m m\omega_e \left(A_m \cdot \cos(\phi_m) - m\omega_e \cdot \sin(\phi_m) \right)}{A_m^2 + (m\omega_e)^2 + 2\zeta_m m\omega_e A_m} \tag{3.20}$$

$$a_{1m} = K_{im} \frac{-4\zeta_m m\omega_e m\omega_e \cdot \sin(\phi_m)}{A_m^2 + (m\omega_e)^2 + 2\zeta_m m\omega_e A_m} \tag{3.21}$$

$$a_{2m} = K_{im} \frac{-2\zeta_m m\omega_e \left(A_m \cdot \cos(\phi_m) + m\omega_e \cdot \sin(\phi_m) \right)}{A_m^2 + (m\omega_e)^2 + 2\zeta_m m\omega_e A_m} \tag{3.22}$$

$$b_{1m} = \frac{-2\left(A_m^2 - (m\omega_e)^2 \right)}{A_m^2 + (m\omega_e)^2 + 2\zeta_m m\omega_e A_m} \tag{3.23}$$

$$b_{2m} = \frac{A_m^2 + (m\omega_e)^2 - 2\zeta_m m\omega_e A_m}{A_m^2 + (m\omega_e)^2 + 2\zeta_m m\omega_e A_m} \tag{3.24}$$

When the above z-domain transfer function of the resonant filter given in (3.19) is transformed to discrete time equations, the discrete response of the filter as shown in (3.25) is obtained. In (3.25), x[k] represents the output voltage error at the kT_s interval, and $y_m[k+1]$ represents the m^{th} resonant controller output to be applied to the PWM unit at the $(k+1)T_s$ interval. The discrete time control block diagram of the resonant filter defined in (3.25) is shown in Figure 3.10.

$$y_m[k+1] = a_{0m}x[k] + a_{1m}x[k-1] + a_{2m}x[k-2] - b_{1m}y_m[k] - b_{2m}y_m[k-1] \tag{3.25}$$

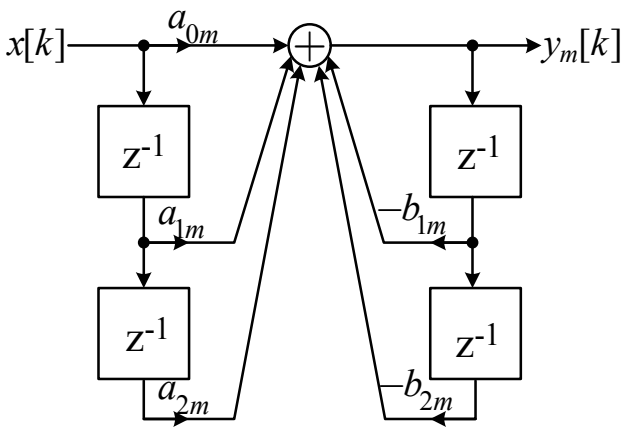


Figure 3.10 The z-domain signal flow chart of the resonant filter controller.

3.3. P+Resonant Controller

The resonant filter controller structure discussed in the previous section forms the heart of the output voltage control system for the four-leg inverter based UPS. However, the resonant filter bank based controller of the four-leg inverter based UPS shown in Figure 3.2 must be accompanied by additional controller blocks for superior overall performance. One of the control components that is beneficial to this system is the proportional gain controller. For the purpose of improving the UPS voltage control loop bandwidth and dynamic performance a proportional feedback control loop can be added to the system. In this case since the proportional controller is in parallel with the resonant controller, the total feedback control structure becomes as shown in Figure 3.11. The voltage error, which is the difference between the reference voltage and the measured voltage, is multiplied with a proportional gain (K_p) and added to the inverter reference voltage as shown in Figure 3.11. The proportional gain mainly improves the UPS performance during loading transients where the voltage error is large. Additionally it enhances the output voltage THD_v as it compensates for the frequency components higher than the largest frequency component of the resonant filter bank. It also helps further reduce the steady-state error due to the imperfection of the resonant filter bank for the voltage harmonics which are within the resonant filter bank bandwidth.

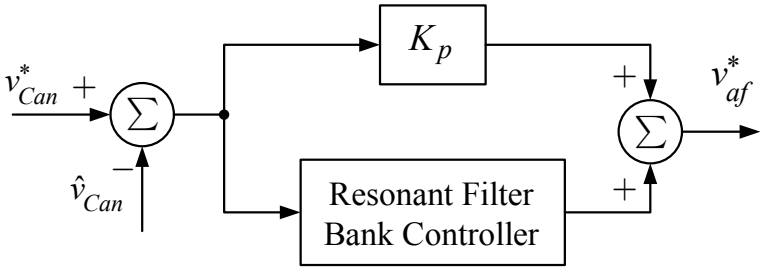


Figure 3.11 The per-phase control block diagram of the P+Resonant controller.

Since the proportional control element is in parallel with the resonant filter bank, the gain and phase characteristics of the resonant filter provided in the previous section are modified when the proportional control element is added. Figure 3.12 shows the gain and phase characteristics of the ideal resonant filter when a proportional controller is added. Comparing Figure 3.1 (the ideal resonant filter without proportional gain) and Figure 3.12, it becomes obvious that while the gain characteristics are the same for both structures, the phase characteristics are different. The phase angle in the resonant frequency range remains the same, but below and above the resonant frequency the phase angle decreases from the 90^o and -90^o values to significantly smaller values (approaching zero) as the frequency deviates from the resonant frequency. Figure 3.13 shows the gain and phase characteristics of the dampened resonant filter with proportional gain. Similar to the ideal resonant filter case, in the dampened resonant filter case also, the proportional gain improves the phase characteristic of the controller. In this case, also the proportional gain improves the finite resonant controller gain (K_{im}+K_p).

Considering the damped and phase advanced resonant filter banks of Figure 3.8 and Figure 3.9, the inclusion of the proportional controller, the modified controller gain and phase characteristics become as shown in Figure 3.14 and 3.15. While the gain characteristics improve slightly at the higher frequencies, the phase characteristics of the new structure change significantly. The phase characteristics of the former figures vary between -180^o and 180^o while those of the latter vary between -90^o and 90^o. Also as in the former case the phase characteristics move upwards with frequency as can be seen more clearly with the case with K_p than without.

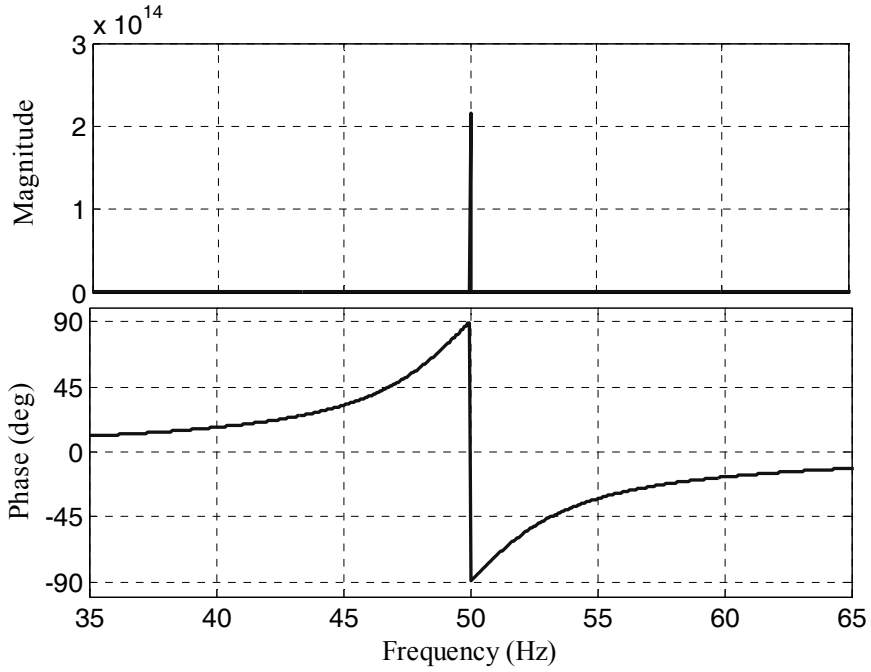


Figure 3.12 The gain and phase characteristics of the ideal P+resonant filter controller for K_p=0.5, m=1, K_{i1}=10, ω_e=2π50 rad/sec.

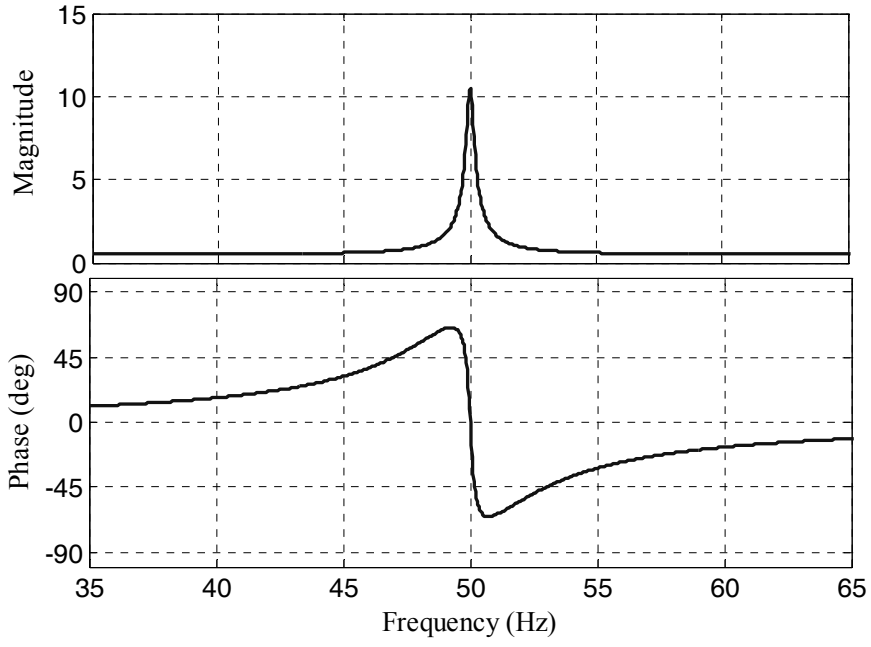


Figure 3.13 The gain and phase characteristics of the damped P+Resonant filter controller for K_p=0.5, m=1, K_{i1}=10, ω_e=2π50 rad/s, $\zeta_I = 3.18\text{x}10^{-3}$, S=100π.

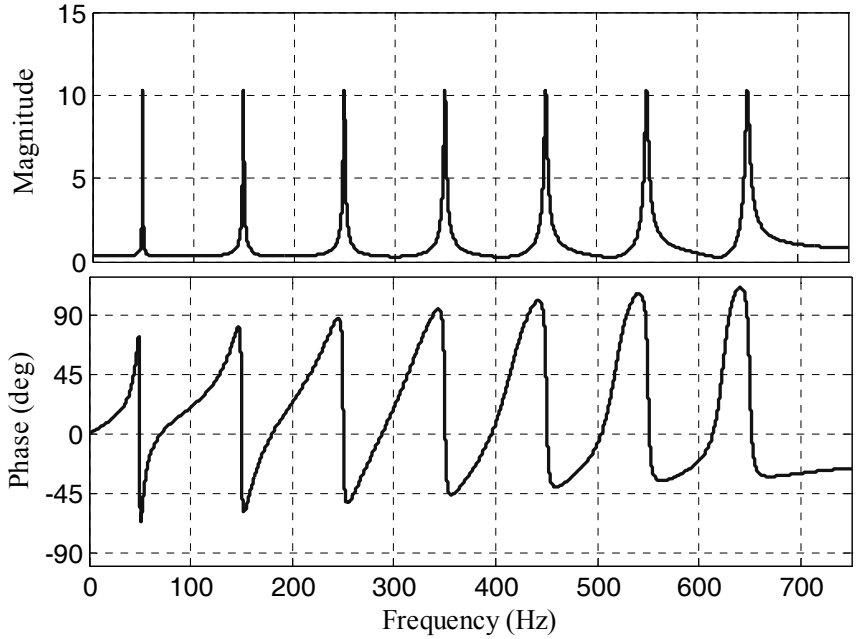


Figure 3.14 The gain and phase characteristics of the phase compensated and damped P+resonant filter bank for m={1, 3, 5, 7, 9, 11, 13}, K_p=0.5, K_{im}=10, ω_e=2π50 rad/s, ζ_m =3.18x10^{-3}, S= 100π, ϕ_m=2T$_s$·$m\omega_e$.

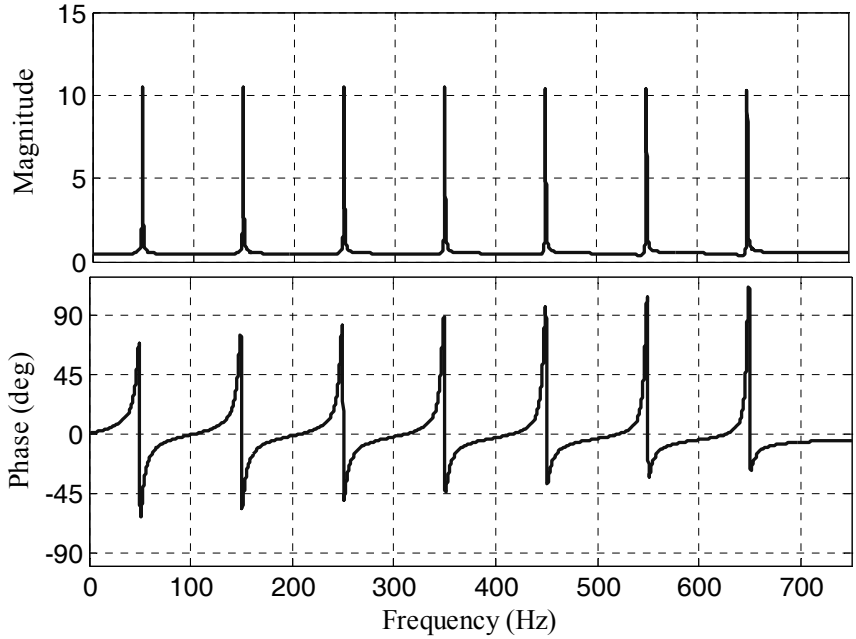


Figure 3.15 The gain and phase characteristics of the phase compensated and damped P+resonant filter bank for m={1, 3, 5, 7, 9, 11, 13}, K_p=0.5, K_{im}=10, ω_e=2π50 rad/s, ζ_m = m·3.18x10^{-3}, S=m·100π, ϕ_m=2T$_s$·$m\omega_e$.

3.4. The Effect of The Capacitor Current Feedback on The Controller Performance

The resonant filter bank controller provides superior steady-state performance. However its dynamic response is limited and proportional gain alone can not improve the dynamic response of the controller. In order to obtain high dynamic performance, the filter capacitor current feedback loop (with a K_{ad} gain) which provides active damping and improves the load disturbance rejection characteristic [14] is added to the resonant filter controller.

Transformerless UPS systems have high energy efficiency implying that the LC output filter has low damping (especially at no-load and light-load) and loading transients and harmonic loads may cause disturbances that can not be damped well by the losses in the internal elements of the UPS. As a result waveform distortion and oscillations may occur. To improve the performance of the UPS, a capacitor current feedback based active damping loop is utilized. Figure 3.16 shows the block diagram of the UPS system with the capacitor current feedback. In the figure, the active damping loop compensates the output voltage oscillations and load current disturbances via the inverter and stabilizes the output voltage. Since the load current transients are immediately reflected on the capacitor (but not on the filter inductor), the capacitor feedback signal is a proper signal to compensate the load current disturbances. The output voltage oscillations can also be compensated by the active damping loop as the capacitor current is proportional to the derivative of the capacitor voltage [14]. In the three-phase four-leg inverter based UPS, utilizing the capacitor current feedback based active damping loop along with the resonant filter bank, the superior steady-state performance of the resonant filter is complemented with the superior dynamic performance of the active damping loop, yielding an overall superior UPS system control performance. The capacitor current feedback additionally helps decrease the high frequency harmonic content of the output voltage as this controller compensation characteristics improve with frequency.

The influence of the capacitor current feedback loop on the UPS system control performance can be analytically investigated and its positive influence can be proven. In order to investigate the effect, the reference voltage to output voltage and load current to output voltage transfer functions will be derived with and without the active damping loop. This model is shown in Figure 3.17 and the transfer function is expressed in (3.26). Considering the equivalent model (Figure 3.17.b) of the UPS system and providing an active damping loop via multiplying the capacitor current with the active damping gain of K_{ad} and subtracting this signal from the reference voltage as shown in Figure 3.17.a, the actively damped system model can be obtained. Including the capacitor current feedback in the control loop, the voltage command to output transfer function of the UPS becomes as in (3.27).

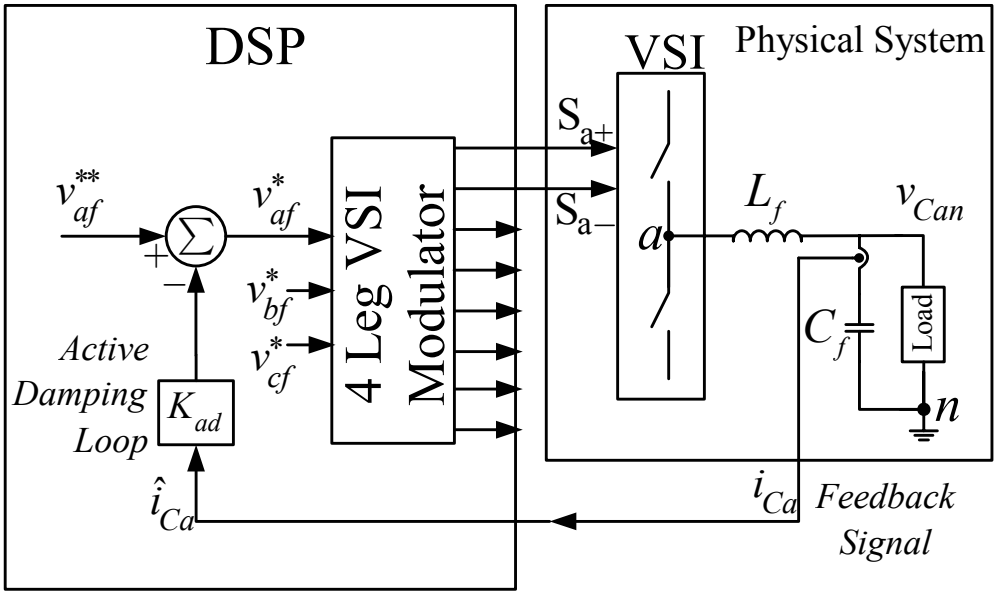
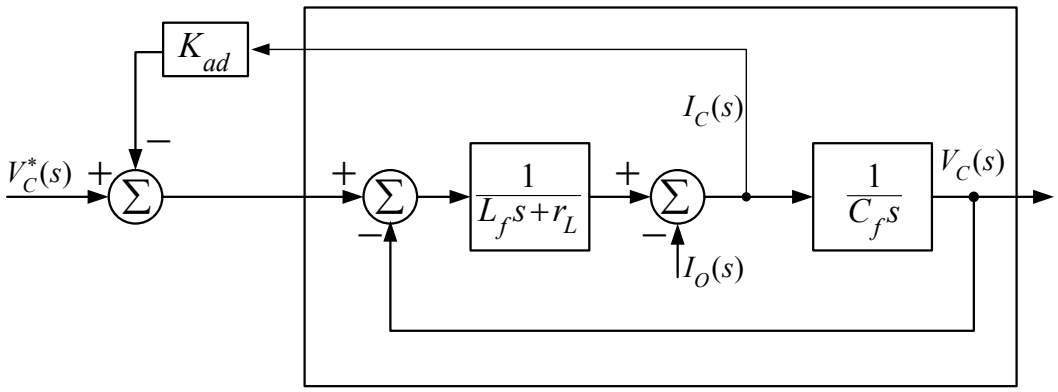
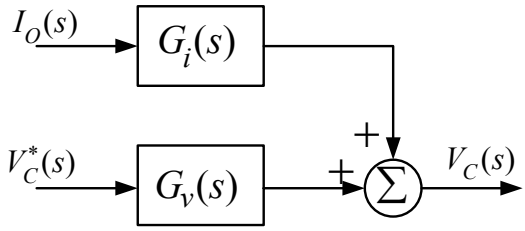


Figure 3.16 The four-leg inverter based three-phase UPS system block diagram with the capacitor current feedback for active damping.



(a)



(b)

Figure 3.17 Per-phase UPS system model with the capacitor current feedback based active damping loop, (a) the basic block diagram, (b) equivalent block diagram.

$$V_C(s) = G_v(s)V_C^*(s) + G_i(s)I_O(s) \tag{3.26}$$

$$G_v(s) = \frac{\frac{1}{L_f C_f}}{s^2 + \frac{K_{ad} + r_L}{L_f}s + \frac{1}{L_f C_f}} \tag{3.27}$$

$$G_i(s) = -\frac{\frac{1}{C_f}s + \frac{r_L}{L_f C_f}}{s^2 + \frac{K_{ad} + r_L}{L_f}s + \frac{1}{L_f C_f}} \tag{3.28}$$

Equation (3.27) shows that the input to output transfer function of the UPS system involves the active damping loop as if the active damping gain K_{ad} is an effective resistor to damp the oscillations. Considering that this equation is a second order transfer function of a system with a damping coefficient of ζ and a natural frequency of ω_o, the damping term of (3.29) can be identified by comparison with (3.29) and the damping can be found as in (3.30). In this derivation the filter inductance equivalent series resistor r_L is accounted for and it is important for the purpose of illustrating the magnitude of improvement the active damping loop provides. With the filter parameters being constant and r_L being small, the K_{ad} gain appears to play a significant role in determining the characteristic equation and the stability behavior of the system.

$$H(s) = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \tag{3.29}$$

$$\zeta = \sqrt{\frac{C_f}{L_f}} \frac{K_{ad} + r_L}{2} \tag{3.30}$$

Since the equivalent series resistance of the filter inductor is usually small, it can not provide significant damping and selecting the K_{ad} significantly larger the system damping can be enhanced. At the same time, this implies that in such a case the effect of the filter inductance ESR can be neglected. Thus, the effectiveness of the active damping loop can be measured by the value of the active damping gain K_{ad} in comparison with the filter inductor ESR. The larger the active damping gain, the higher the damping and the more stable the system.

For the purpose of illustration the effect of the capacitor current feedback based active damping on the command to output voltage transfer function $G_v(s)$ defined in (3.27) is plotted for the actively damped and without active damping cases in Figure 3.18. As the figure illustrates, without active damping, around the resonant frequency of 750Hz the gain reaches 50dB which indicates very poor damping. With the

inclusion of the active damping loop, the resonant peak is significantly suppressed and the resonant frequency is shifted to about 1 kHz and the phase margin is enhanced greatly.

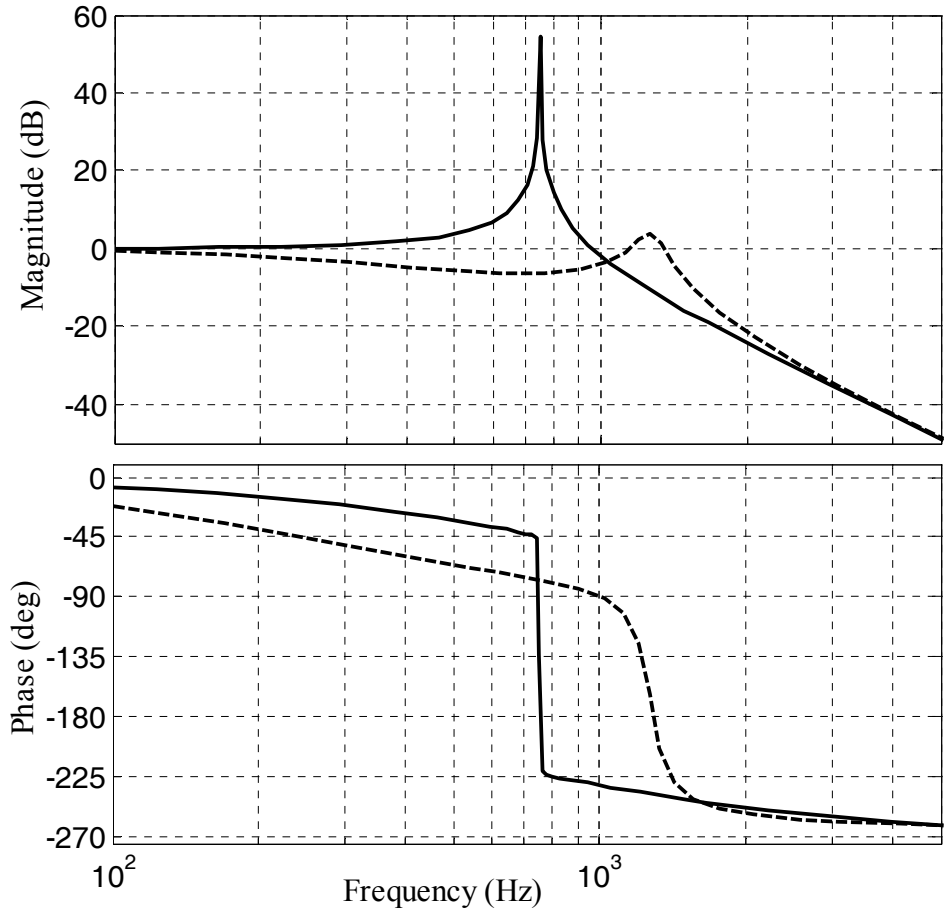


Figure 3.18 The gain and phase characteristics of the $G_v(s)$ with (dashed: K_{ad}=15) and without (solid) active damping for L=1.5mH, C=30μF, r_L=10mΩ.

3.5. The Full Control Structure of The Four-Leg Inverter Based UPS System

The three-phase four-leg inverter based UPS to be implemented in this thesis is controlled by the resonant filter bank controller based system with the proportional controller and capacitor current feedback based active damping loop. The control

system block diagram is shown in Figure 3.19 in detail. In the diagram the control structure is primarily shown for one of the phases and the other phases also have identical controller structure. As the figure illustrates, the capacitor current feedback loop is included and the sampling rate should be as high as possible (typically at the same rate as the PWM frequency). As can be seen from the figure, voltage feedforward is also added for improved command tracking performance.

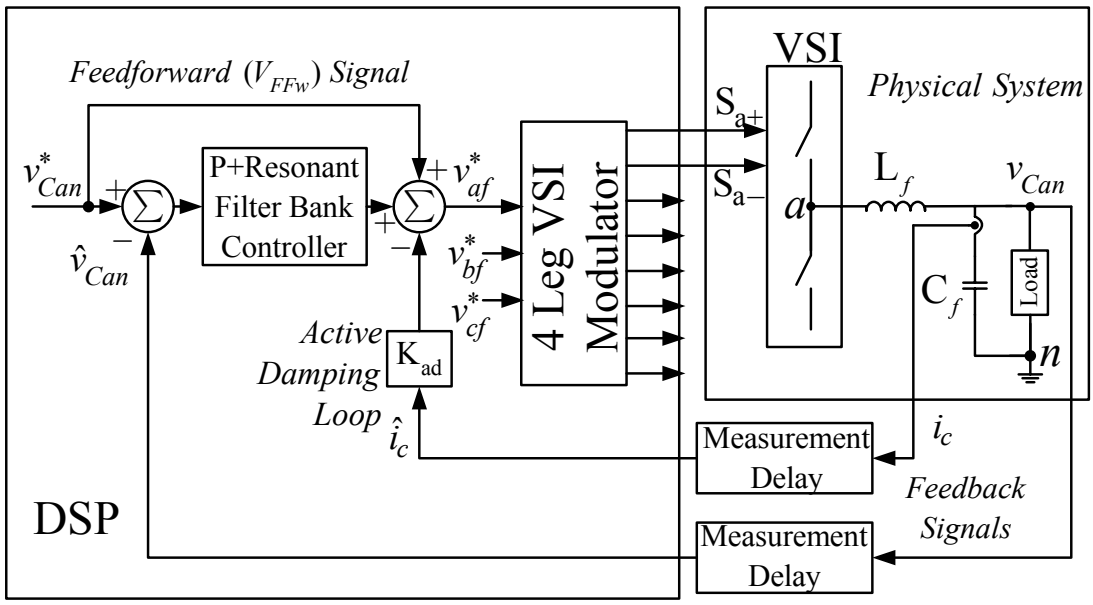


Figure 3.19 The control system block diagram of the four-leg inverter based three-phase UPS system.

3.6. Stability Analysis of The Overall Control Structure

In this section the design of the UPS control system given in Figure 3.19 will be discussed and the stability will be investigated. Replacing the physical elements of the UPS system with equivalent control blocks, the system of Figure 3.19 can be represented with a continuous time system block diagram shown in Figure 3.20. In the diagram, each component of the UPS system is modeled with an appropriate continuous time transfer function block which will be detailed in the following

discussion. Employing this model, the system stability can be investigated via tools such as Routh-Hurwitz stability criterion and controller gain limits for stability can be established. Based on the control bandwidth requirements the controller parameters can then be optimized.

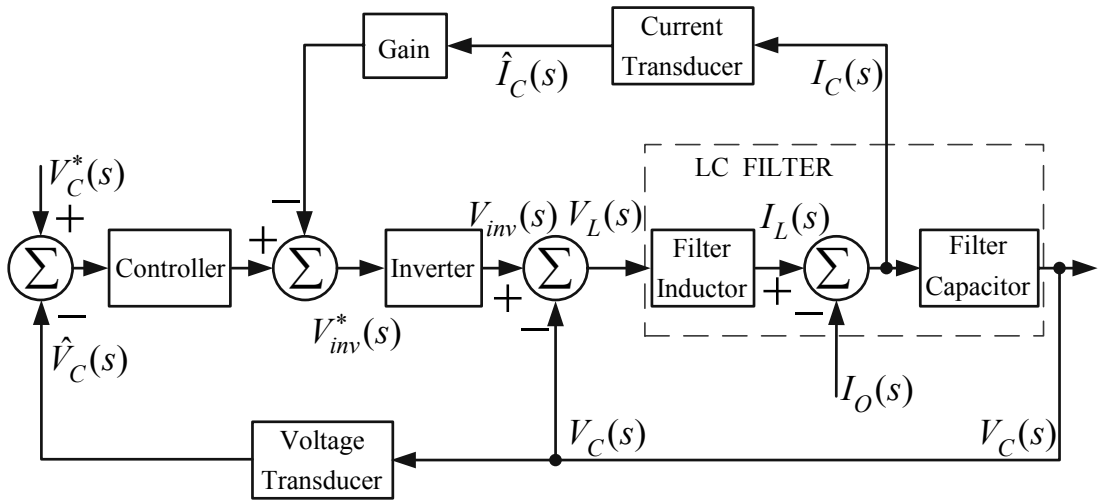


Figure 3.20 General per-phase control block diagram of the closed loop output voltage controlled UPS system.

The mathematical models of the blocks in the control diagram of Figure 3.20 involve details of the specifics of these elements. Figure 3.21 shows the block diagram which includes these elements with their simplified s-domain mathematical models. The UPS system control block diagram involves the measurement delay, sampling delay, and PWM delay blocks. As will be discussed in the fifth chapter in detail, in this thesis the controller will be implemented on a digital platform. For that purpose a Digital Signal Processor (DSP) will be employed and the control algorithm will be implemented via software.

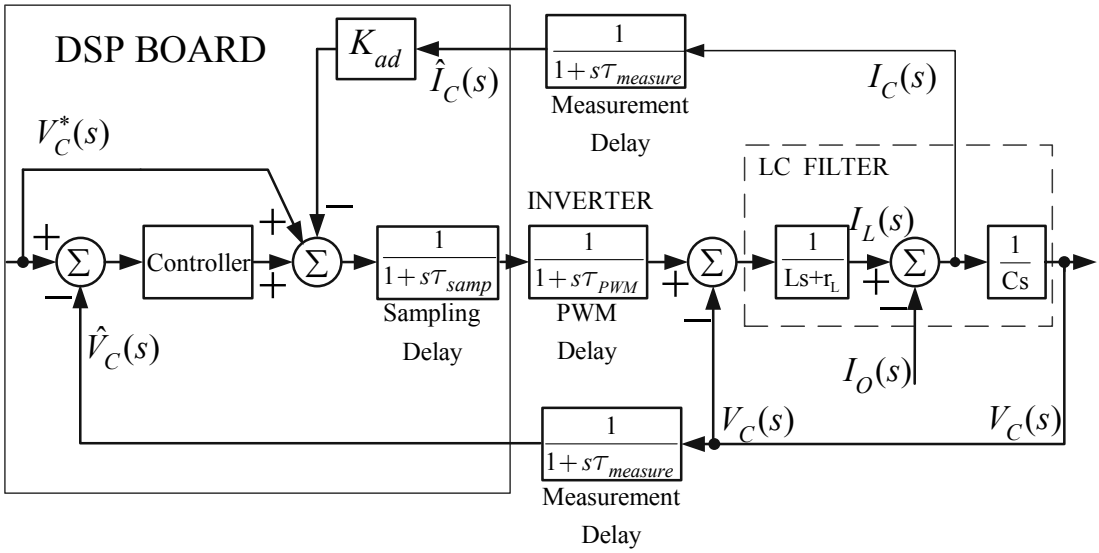


Figure 3.21 Detailed per-phase control block diagram of the closed loop output voltage controlled UPS system.

In the implemented system the output voltages, which are the main control variables of the four-leg inverter based UPS system, are measured by isolated voltage transducers with considerable delay and applied to the digital control unit as the feedback signals of the closed loop system. This results in a measurement delay ($\tau_{measure}$) of 40 μs. Thus, the measurement delay in Figure 3.21 can be modeled with a first order delay transfer function with unity gain and 40 μs time constant for output voltage measurement.

Current transformers are utilized in the experiments to measure the capacitor currents. The current transformers have a bandwidth of several kilohertz. As the bandwidth could not be measured, an approximate bandwidth of 20 kHz (50 μs time delay) will be assumed for the current transformer measurement delays. Similar to the modeling of the voltage measurement delay, current measurement delay can be modeled with a first order delay transfer function where the time constant is 50 μs.

The measured feedback signals are input to the analog-to-digital (A/D) converter of the DSP and the feedback signals are regularly sampled at the PWM frequency.

Since the A/D converter settles in a finite time length, there is a delay ($\tau_{A/D}$) associated with the A/D converter, which is typically a few microseconds or less. The sampled feedback signals are utilized in the control algorithm to generate the voltage reference signals (V_C^*), which are applied to the PWM blocks at the end of the sampling period (T_s). Since in a discrete time controller the control functions involve computations, a computation delay (τ_{comp}) corresponding to the number of processor instruction cycles from the beginning to the end of the code is generated. The PWM pulse generator accepts command signals at most twice per PWM frequency (twice update). As a result, there is an idle time between the instant where the reference voltage is ready and when the PWM signal can be updated. The A/D conversion time, the computation delay time and the idle time can all be lumped in one delay element and termed as the sampling delay (τ_{samp}) which equals to at least half a PWM cycle. If the PWM signal is updated twice per cycle the sampling delay is half PWM cycle. If the PWM signal is updated once per PWM cycle, the sampling delay is one PWM cycle.

The PWM block generates the required gate logic signals to drive the switching devices in the four-leg inverter. The inverter per-PWM cycle average model is a voltage amplifier with unity gain and first order delay element with a PWM delay (τ_{PWM}). If the PWM signal is updated every half PWM cycle, the PWM delay is a quarter PWM cycle. If the PWM signal is updated once per PWM cycle, the PWM delay is half of a PWM cycle. For example, as shown in Figure 3.3, for the double update case, the PWM delay is $T_s/4$.

For the sake of simplicity, the delays, which are discussed above and illustrated in Figure 3.21, can be considered as total system delay and can be modeled with an equivalent single delay block as shown in Figure 3.22. The system in Figure 3.22 can be represented with lumped control block diagrams as shown in Figure 3.23. In the diagram, $G_c(s)$ is the transfer function of the controller, $G_v(s)$ is the transfer function of the inverter reference voltage to output voltage, and $G_i(s)$ is the transfer function of the load current disturbance to output voltage.

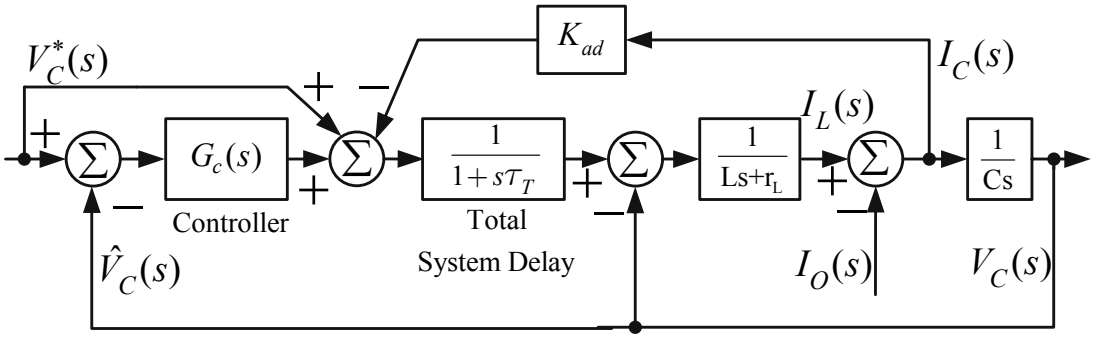


Figure 3.22 The reduced order per-phase continuous time model based block diagram of the closed loop output voltage controlled UPS system.

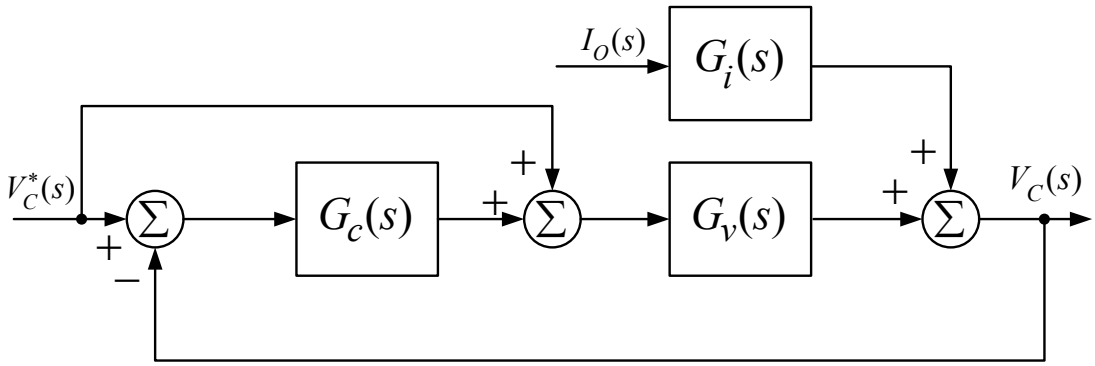


Figure 3.23 Equivalent per-phase block diagram of the closed loop output voltage controlled UPS system.

The transfer functions of Figure 3.23 are given in the following equations. As a controller P+Resonant type controller is considered. For simplification, single resonant frequency controller rather than a resonant filter bank takes place in for the stability analysis. The transfer function of this controller is given in (3.31). Based on the given transfer functions, $G_v(s)$ and $G_i(s)$ can be calculated as given in (3.32) and (3.33).

$$G_c(s) = K_p + \frac{2K_{im}s}{s^2 + (m\omega_e)^2} \tag{3.31}$$

$$G_v(s) = \frac{1}{\tau_T L_f C_f s^3 + C_f(L_f + \tau_T r_L)s^2 + \left[C_f(K_{ad} + r_L) + \tau_T\right]s + 1} \tag{3.32}$$

$$G_i(s) = \frac{-(L_f s + r_L)(1 + s\tau_T)}{\tau_T L_f C_f s^3 + C_f(L_f + \tau_T r_L)s^2 + \left[C_f(K_{ad} + r_L) + \tau_T\right]s + 1} \tag{3.33}$$

In order to investigate the stability of the given linear system, the Routh-Hurwitz stability criterion will be employed [33]. For this purpose the output voltage will be expressed in (3.34) in terms of numerator and denominator terms C(s), D(s), and R(s) as given in (3.35), (3.36), and (3.37). R(s) is the characteristic equation of the control system.

$$V_C(s) = \frac{C(s)}{R(s)} V_C^*(s) + \frac{D(s)}{R(s)} I_O(s) \tag{3.34}$$

$$C(s) = K_p s^2 + 2K_{im} s + K_p(m\omega_e)^2 \tag{3.35}$$

$$D(s) = -\left(L_f s + r_L\right)\left(1 + s\tau_T\right)\left(s^2 + (m\omega_e)^2\right) \tag{3.36}$$

$$R(s) = a_0 s^5 + a_1 s^4 + a_2 s^3 + a_3 s^2 + a_4 s + a_5 \tag{3.37}$$

In the above denominator term (*R(s)*), the coefficients are given in terms of the circuit parameters and controller parameters in equations (3.38), (3.39), (3.40), (3.41), (3.42), and (3.43).

$$a_0 = L_f C_f \tau_T \tag{3.38}$$

$$a_1 = C_f(\tau_T r_L + L_f) \tag{3.39}$$

$$a_2 = C_f(r_L + \tau_T L_f (m\omega_e)^2 + K_{ad}) + \tau_T \tag{3.40}$$

$$a_3 = C_f(m\omega_e)^2 \left(\tau_T r_L + L_f\right) + K_p + 1 \tag{3.41}$$

$$a_4 = C_f(m\omega_e)^2 \left(r_L + K_{ad}\right) + K_{im} + \tau_T (m\omega_e)^2 \tag{3.42}$$

$$a_5 = (m\omega_e)^2 \left(K_p + 1\right) \tag{3.43}$$

The Routh-Hurwitz stability criterion states that the necessary (but not sufficient) condition for stability is that all the coefficients of the characteristic equation R(s) must be positive. Since for system stability negative feedback is employed, all the controller coefficients K_{ad}, K_{im}, and K_p must be positive by definition. With this assumption, reviewing the above coefficient equations, it can be clearly seen that all the coefficients are positive for positive controller gains. Thus, the necessary condition for stability is satisfied. The sufficient condition involves ordering the coefficients according to the Routh-Hurwitz criterion ordering table shown in Table 3.1, and then obtaining the additional coefficients b_1, b_2, c_1, c_2, d_1, e_1 defined in (3.44), (3.45), (3.46), (3.47), (3.48), and (3.49).

Table 3.1 Routh-Hurwitz stability criterion table

s^5	a_0	a_2	a_4
s^4	a_1	a_3	a_5
s^3	b_1	b_2	0
s^2	c_1	c_2	
s	d_1	0	
1	e_1		

$$b_1 = \frac{a_1 a_2 - a_0 a_3}{a_1} = C_f(K_{ad} + r_L) + \frac{\tau_T^2 r_L - \tau_T K_p L_f}{\tau_T r_L + L_f} \tag{3.44}$$

$$b_2 = \frac{a_1 a_4 - a_0 a_5}{a_1} = K_{im} + (K_{ad} + r_L) C_f (m\omega_e)^2 - \frac{K_p (m\omega_e)^2 L_f \tau_T}{\tau_T r_L + L_f} \tag{3.45}$$

$$c_1 = \frac{b_1 a_3 - b_2 a_1}{b_1} = K_p + 1 - \frac{C_f(\tau_T r_L + L_f)(C_f (m\omega_e)^2 r_L + K_{im})}{C_f K_{ad} - \tau_T K_p} \tag{3.46}$$

$$c_2 = \frac{b_1 a_5 - b_3 a_1}{b_1} = (m\omega_e)^2 \left(K_p + 1\right) \tag{3.47}$$

$$d_1 = \frac{c_1 b_2 - b_1 c_2}{c_1} \tag{3.48}$$

$$e_1 = \frac{d_1 c_2 - c_1 d_2}{d_1} = (m\omega_e)^2 \left(K_p + 1\right) \tag{3.49}$$

Assuming that $L_f \gg \tau_T r_L$ and $K_{ad} \gg r_L$ the above coefficients can be approximated in the following equations.

$$b_1 \cong C_f K_{ad} - \tau_T K_p \tag{3.50}$$

$$b_2 \cong K_{im} + (m\omega_e)^2 \left(C_f K_{ad} - \tau_T K_p \right) \tag{3.51}$$

$$c_1 \cong K_p + 1 - \frac{C_f L_f K_{im}}{C_f K_{ad} - \tau_T K_p} \tag{3.52}$$

$$d_1 \cong K_{im} \left[1 - \frac{L_f C_f (m\omega_e)^2 \left(C_f K_{ad} - \tau_T K_p \right)}{\left(K_p + 1 \right)\left(C_f K_{ad} - \tau_T K_p \right) - L_f C_f K_{im}} \right] \tag{3.53}$$

The sufficient condition for the stability requires that the elements of the first column of the array should not change sign and also not be zero. This constraint can be met if the conditions of (3.54), (3.55), (3.56), and (3.57) are met simultaneously. Thus, the controller design should adhere to these conditions and the parameters must satisfy these equations.

$$for \quad b_1 > 0 \quad \Rightarrow \quad K_{ad} > \frac{\tau_T K_p}{C_f} \tag{3.54}$$

$$for \quad c_1 > 0 \quad \Rightarrow \quad K_{im} < \frac{\left(K_p + 1 \right)\left(C_f K_{ad} - \tau_T K_p \right)}{L_f C_f} \tag{3.55}$$

$$for \quad d_1 > 0 \quad \Rightarrow \quad \begin{cases} K_{im} > 0 \\ K_{im} < \left(C_f K_{ad} - \tau_T K_p \right)\left(\dfrac{K_p + 1}{L_f C_f} - \left(m\omega_e \right)^2 \right) \end{cases} \tag{3.56}$$

$$for \quad e_1 > 0 \quad \Rightarrow \quad K_p > -1 \tag{3.57}$$

3.7. A Controller Design Example

In the following, an example design will be numerically investigated. In this example, output voltage control of a four-leg inverter based UPS system is considered. The per-phase model is utilized. Thus, a single phase control system will be discussed. The output voltage of the UPS system is controlled by a P+Resonant controller. Resonant filter bank contains fundamental component of the output voltage controller (for m=1) and compensators for the first six dominant harmonics (for m=3, 5, 7, 9, 11, 13). The capacitor current feedback is employed for active damping and also suppressing the harmonics above the 13^{th} harmonic and below the resonant frequency, and the voltage feedforward is utilized for improved command tracking in the given example. The filter parameters of the UPS system to be utilized in the upcoming simulation and experimental work chapters are considered. The coefficients of the controller structure are chosen to satisfy the Routh-Hurwitz stability criteria. The inverter is assumed to be operating at 10 kHz switching frequency. The UPS LC filter and controller parameters of the considered system are given in Table 3.2.

In order to study and illustrate the control performance characteristics of the UPS system, the simplified linear UPS system model is simulated by utilizing MATLAB-Simulink. Although the real system is implemented with discrete time controller and the inverter is also a discrete element, for the sake of simplicity the system control behavior will be modeled in continuous time. In MATLAB-Simulink, the control system blocks will therefore be modeled with s-domain equivalents. The MATLAB-Simulink block diagram of the per-phase control of the UPS system is shown in Figure 3.24. In order to model the measurement, computation, PWM etc. delays, the total system delay is chosen as 200μs which corresponds to two PWM periods for the discrete-time implementation with 10 kHz switching frequency. For given filter parameters the cut-off frequency of the LC filter is 750 Hz. In the model, capacitor current feedback based active damping is added to the inverter reference voltage.

Table 3.2 The filter and controller parameters utilized in the UPS model.

Filter parameters		
Inductor	L_f	1.5 mH
Internal resistance	r_L	10 mΩ
Capacitor	C_f	30 μF
Controller parameters		
Capacitor current feedback gain	K_{ad}	15
Proportional gain	K_p	1
Fundamental component controller gain	K_{i1}	100
3rd harmonic component controller gain	K_{i3}	50
5th harmonic component controller gain	K_{i5}	100
7th harmonic component controller gain	K_{i7}	100
9th harmonic component controller gain	K_{i9}	10
11th harmonic component controller gain	K_{i11}	15
13th harmonic component controller gain	K_{i13}	10

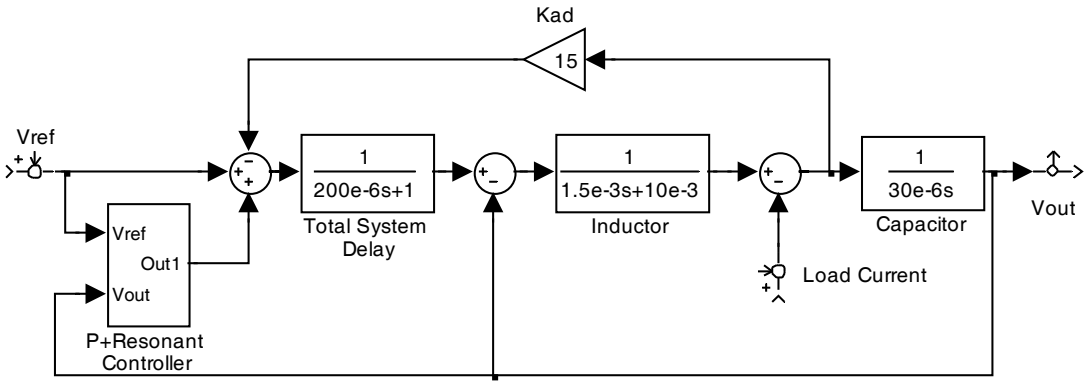


Figure 3.24 The simplified per-phase control model of the UPS system in MATLAB-Simulink.

In the study the filter delay compensation and damping values will be kept as variable and the input voltage to output voltage transfer function (showing command tracking) and load current to output voltage transfer function (showing load disturbance rejection) characteristics will be investigated. For this purpose, three cases given in Table 3.3 are considered. In Case 1 in the table, the phase compensation increases with the frequency linearly and the damping decreases with frequency linearly. In Case 2 in the table, the phase compensation for the 9^{th} , 11^{th}, and 13^{th} harmonic is advanced 50% more compared to Case 1 and the damping remains the same as Case 1. In Case 3, only the 11^{th} and 13^{th} harmonic damping differ compared to Case 2. In this final case the damping for these harmonics is not decreased compared to Case 2 and it is kept at a constant damping value equal to that of the fundamental frequency damping.

Table 3.3 The damping term and the phase shifting term of components of the resonant filter bank for various cases

		Fundamental and 3^{rd}, 5^{th}, 7^{th} harmonic components (m = 1,3,5,7)	9^{th} harmonic component (m = 9)	11^{th} harmonic component (m = 11)	13^{th} harmonic component (m = 13)
Case 1	ϕ_m	$2T_s \cdot m\omega_e$	$2T_s \cdot m\omega_e$	$2T_s \cdot m\omega_e$	$2T_s \cdot m\omega_e$
	ζ_m	$1/(100\pi \cdot m)$	$1/(100\pi \cdot m)$	$1/(100\pi \cdot m)$	$1/(100\pi \cdot m)$
Case 2	ϕ_m	$2T_s \cdot m\omega_e$	$3T_s \cdot m\omega_e$	$3T_s \cdot m\omega_e$	$3T_s \cdot m\omega_e$
	ζ_m	$1/(100\pi \cdot m)$	$1/(100\pi \cdot m)$	$1/(100\pi \cdot m)$	$1/(100\pi \cdot m)$
Case 3	ϕ_m	$2T_s \cdot m\omega_e$	$3T_s \cdot m\omega_e$	$3T_s \cdot m\omega_e$	$3T_s \cdot m\omega_e$
	ζ_m	$1/(100\pi \cdot m)$	$1/(100\pi \cdot m)$	$1/(100\pi)$	$1/(100\pi)$

In the studies, “Linear Analysis Tool” of the MATLAB is utilized to obtain the gain and phase characteristics of both input-to-output and disturbance-to-output transfer functions of the UPS system model for the cases given in Table 3.3.

The command to output transfer function, which indicates the command following performance of the UPS should be with high gain until the resonant frequency of the LC filter. Since the command signal at the fundamental frequency is the reference voltage and at all harmonic frequencies the command is zero, with a sufficiently high gain and bandwidth, the UPS output voltage will follow the command. Since the no-load operating point provides the lowest damping operating point, this operating point can be considered as the most challenging. Figure 3.25 shows the command to output phase and magnitude characteristics for the three cases in Table 3.3. Considering all the cases in Table 3.3, the gain is high at all the filter design frequencies. However, for Case 1 the selectivity is high, in particular at higher frequencies. This results in poor performance in varying fundamental frequency applications and also fixed fundamental frequency operation but with a fixed point signal processor implementation as discussed in the earlier sections of this chapter. Since Case 2 only improves the phase angle compensation but not the damping, the selectivity is still high at higher frequencies resulting in a narrow frequency band for the controller higher frequency components. In Case 3, the damping is improved as the selectivity is decreased especially at the higher frequencies where damping is needed the most. In Figure 3.26, the higher frequency range of the controller gain and phase characteristics are shown in detail to support this argument. Thus, the phase and damping coefficients of Case 3 provide superior overall performance over the given controller bandwidth which is about 650-700Hz.

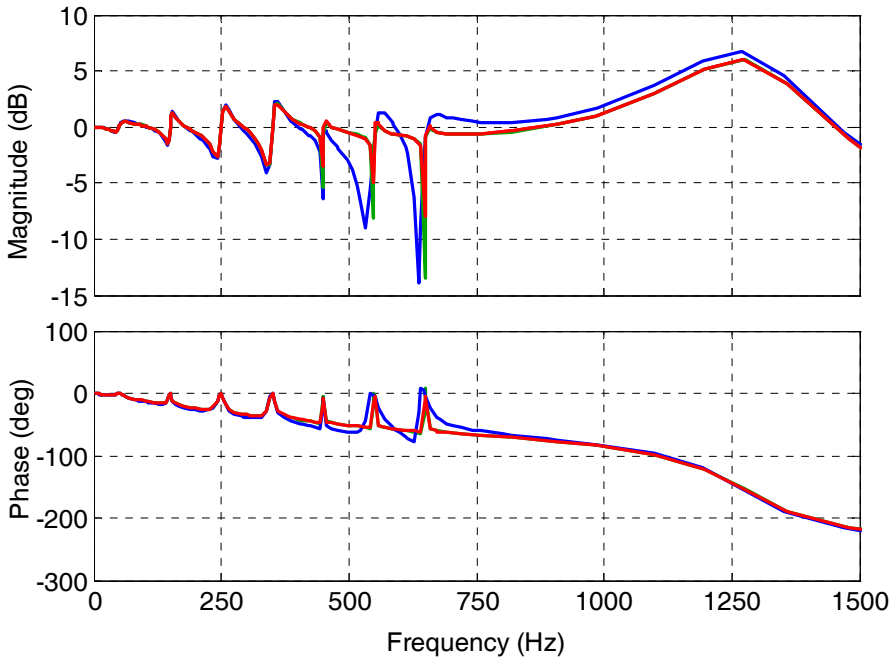


Figure 3.25 The gain and phase characteristics of the input-to-output transfer function (command tracking) of the closed loop output voltage controlled UPS system for several cases, (red: Case 1, green: Case 2, blue: Case 3).

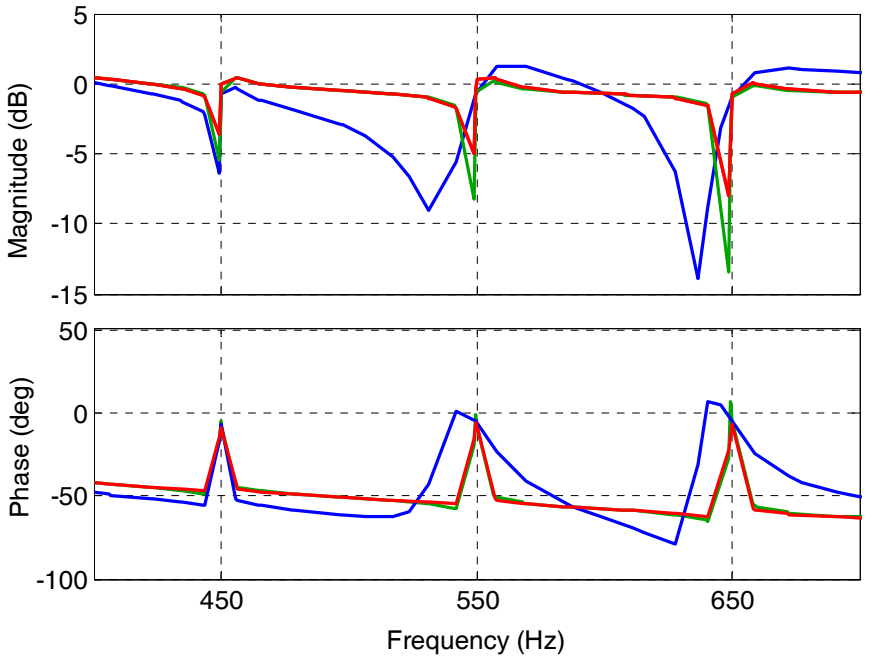


Figure 3.26 The detailed illustration of Figure 3.25,
(red: Case 1, green: Case 2, blue: Case 3).

The disturbance to output transfer function ($V_o(s)/I_o(s)=Z(s)$) is the UPS output impedance which ideally should be zero for all frequencies. Especially for the nonlinear load cases where the load current harmonics can be large in magnitude, the output voltages can be distorted when the impedance is high. Therefore, in the designed controller the impedance should be as low as possible within the bandwidth of the controller. Figure 3.27 shows the output impedance magnitude and phase characteristics for the three cases. The UPS provides high harmonic rejection for all the characteristic harmonics within the control bandwidth for all the cases. However, detailed view of the waveforms in Figure 3.28 shows that the selectivity of Case 3 parameters is less implying this case provides better performance for varying frequency and also fixed point implementation applications. From the diagrams it can also be seen that the active damping loop shifts the maximum impedance point to higher frequencies than the resonant frequency and avoids the resonance problem. Since the capacitor filter at the output filters out all the high frequency harmonics of the load above the resonant frequency, the output performance becomes superior overall.

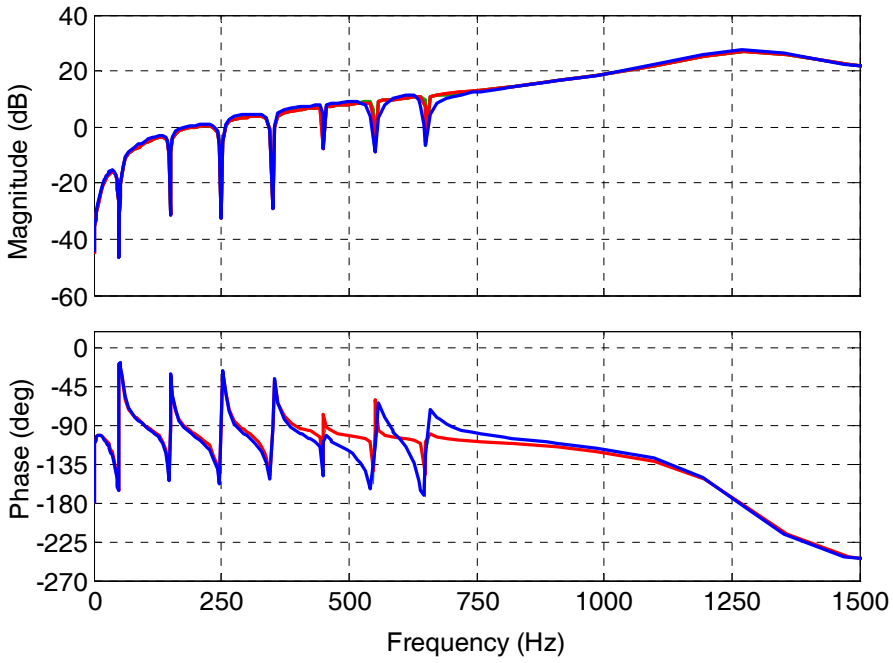


Figure 3.27 The gain and phase characteristics of the disturbance-to-output transfer function (output impedance) of the closed loop output voltage controlled UPS system for several cases, (red: Case 1, green: Case 2, blue: Case 3).

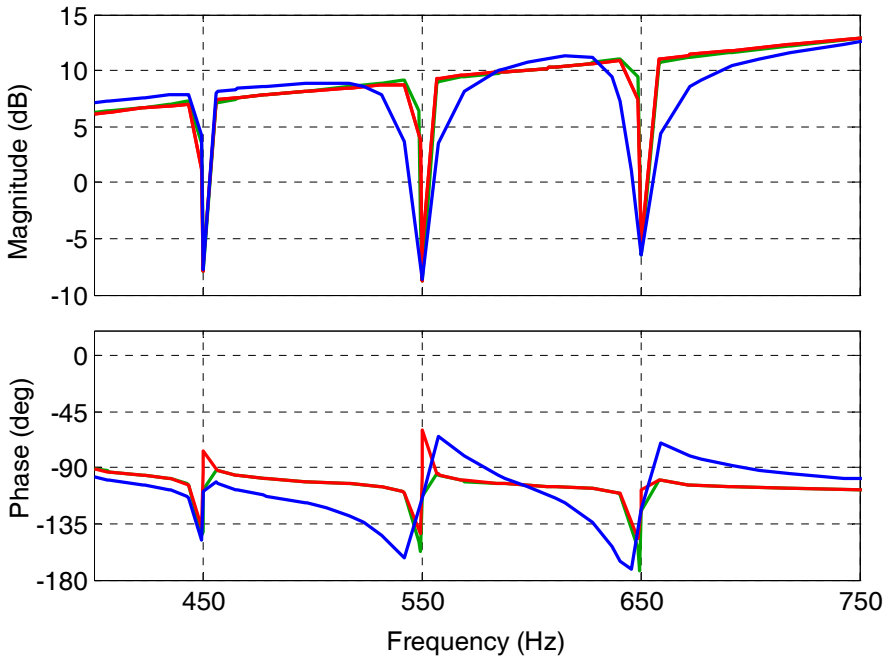


Figure 3.28 The detailed illustration of Figure 3.27,
(red: Case 1, green: Case 2, blue: Case 3).

With the filter design methodology established in this section, the coefficients can be easily obtained via MATLAB or an alternative software tool. With all the filter coefficients a_{0m}, a_{1m}, a_{2m}, b_{1m}, b_{2m} being constant and off-line calculated, the implementation on a DSP is an easy task. Inclusion of the voltage feedforward, capacitor current feedback based active damping, and a proportional gain to the structure the filter dynamic performance is further enhanced.

3.8. Anti-Windup Limiter Design For Resonant Filter Controllers

Under normal operating conditions the system exhibits performance defined by the control parameters and can be predicted as shown in the previous section. However, under strong transients if the reference voltage becomes larger than what the DC bus voltage of the inverter can provide, the output voltage of the inverter saturates (overmodulation occurs). As a result the system becomes nonlinear. Since the resonant filter controllers effectively involve integral and proportional control terms, during inverter saturation windup may occur and overshoot and sluggish response may be created. For that purpose, anti-windup limiters must be employed in the resonant filter controllers and once overmodulation occurs the anti-windup limiters must be activated to limit the integrators [34], [35].

There can be various ways to limit the integrators of the controller during overmodulation. One simple method involves freezing the variables when an overmodulation occurs. According to this approach, the overmodulation is detected from the commanded modulation signals and the modulator outputs (calculated switch duty cycles). If an overmodulation condition is detected, the variables of the resonant filter banks (y[k]) are maintained at their previous values. If the overmodulation state is exited from, then the variables are allowed to change. In Figure 3.29 the basic principle of the anti-windup limiter is illustrated.

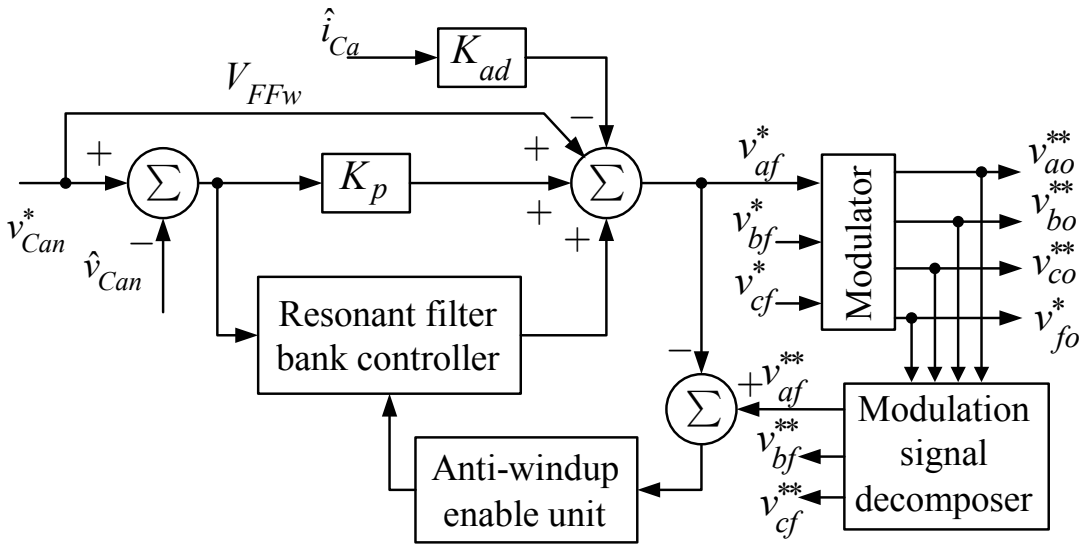


Figure 3.29 P+Resonant controller with anti-windup limiter.

This chapter investigated the resonant filter bank controller for UPS output voltage control. It has been shown that the resonant filter bank approach provides high overall performance. With the help of the active damping loop the stability of the controller could be improved. Finally anti-windup methods are discussed. The next section involves performance evaluation of the control and modulation methods suitable for the four-leg inverter based UPS by means of detailed computer simulations.

CHAPTER 4

PERFORMANCE ANALYSIS OF THE FOUR-LEG INVERTER BASED THREE-PHASE UPS SYSTEM BY MEANS OF COMPUTER SIMULATIONS

4.1. Introduction

In order to verify the theoretical studies of Chapter 2 and Chapter 3, a three-phase, four-leg inverter based UPS system is investigated by means of computer simulation in this chapter. For the purpose of investigation, a three-phase four-leg inverter based 5kVA UPS with 120 Vrms per phase and 50 Hz output rating is considered.

In this chapter, first the UPS system simulation power stage model is established and then the control and PWM algorithms are implemented. The resonant filter bank based controller parameters are tuned by trial and error. Given the practically optimized parameters, the UPS performance under steady-state and dynamic operating conditions for various load types is investigated by detailed computer simulations. The chapter will conclude with a study of modulator performance characteristics and comparison of MLDPWM and other modulators will be provided.

4.2. Modeling of The Four-Leg Inverter Based Three-Phase UPS System

The computer simulations are carried out by utilizing the Ansoft-Simplorer computer simulation package program [40]. Ansoft-Simplorer is graphic window based power electronic circuit simulator in which the power electronics system is formed by

picking and placing the required components on its graphic window. This graphic window is also called the circuit schematic diagram of the program. The simulation results, which are the waveforms of the voltages or currents generally, are displayed on the graphic window. In the day-postprocessor window, the waveforms obtained from the simulation results are evaluated by utilizing the analysis tools such as harmonic calculator, THD calculator, etc. In the simulations the diodes and IGBTs of the power converter topology are modeled by system level models of these elements. The simulation model circuit diagram of the power stage of the four-leg inverter based three-phase UPS system is given in Figure 4.1 with its building blocks defined on the same figure. These blocks are the three-phase AC utility grid, three-phase full-bridge uncontrolled rectifier, DC bus capacitors, three-phase four-leg inverter, LC filter, and load, from input to output respectively.

The utility grid is modeled as a three-phase Y-connected AC voltage source with 220Vrms/phase (380Vrms line-to-line) and 50Hz ratings. It has equivalent series impedance that consists of a resistor with 20mΩ/phase and an inductance of 100μH/phase. The DC bus is obtained from a three-phase full-bridge diode rectifier. Thus, it draws non-sinusoidal currents from the AC grid. An additional three-phase AC line reactor with 3mH/phase inductance value is inserted in series with the AC line such that the line current quality is improved. The rectified DC voltage is smoothed by the two series connected DC bus capacitors with each capacitor having a value of 2200μF and yielding a total equivalent DC bus capacitance of 1100μF. Thus, the DC bus voltage of the four-leg inverter is obtained as approximately 540V. The additional parameters used in the system are listed in Table 4.1.

The computer simulations of the system shown in Figure 4.1 are conducted for various operating conditions for the purpose of performance investigation. The simulations are carried out by utilizing sufficiently small integration step size in order to minimize the computational errors and obtain high accuracy. The parameters of the system level switching device models utilized in the simulations are given in Table 4.2. The minimum integration step size is selected as 50 ns so that the simulation results are accurate.

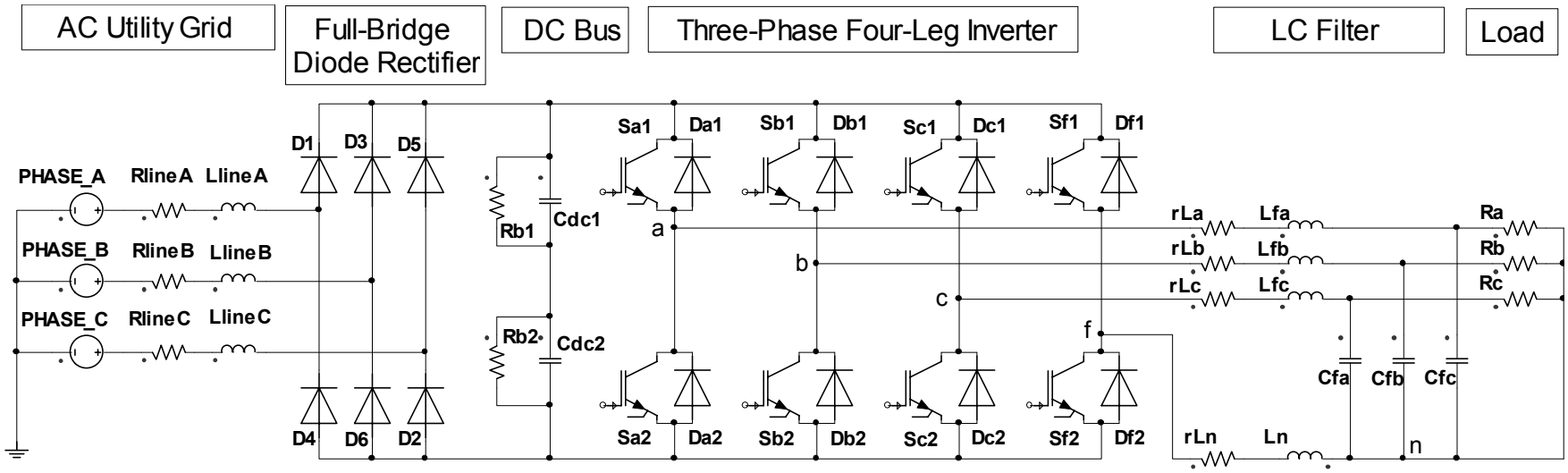


Figure 4.1 Power stage of the four-leg inverter based three-phase UPS system drawn with the Simplorer schematic program.

(Simplorer V7.0 Schematic ssh file).

Table 4.1 System parameters utilized in the simulation model

AC line	Equivalent inductance (sum of line and filter inductances per-phase)	3.1 mH
	Internal resistance (of the line, per phase)	20 mΩ
DC bus	Voltage	540 V
	Capacitor (Cdc1=Cdc2)	2200 μF
	Bleeding resistor (Rb1)	30 kΩ
Output Filter	Phase inductor	1.5 mH
	Internal resistance of inductor	400 mΩ
	Phase capacitor	30 μF
	Neutral leg inductor	500 μH
UPS Output Ratings	Power (three-phase total)	5 kVA
	Voltage (phase to neutral)	120 V_{rms}
	Frequency	50 Hz

Table 4.2 System level semiconductor device model parameters

Device	Forward voltage (V)	Bulk resistance (mΩ)	Blocking resistance (kΩ)
Diode	1.5	1	100
IGBT	2.5	1	100

In the simulations all the control functions are implemented using the equation blocks of Simplorer [40]. The equation blocks of Simplorer are executed at a preset rate which could be different than the integration step size. In this case the equation block execution rate is set as 50μs for all the simulations conducted. In the equation blocks, the physical system to be experimentally investigated in the next chapter is modeled in the simulation in detail as much as possible. In particular the measurement and computation delays are included in the simulation for they affect the control behavior of the system significantly.

Various load types are utilized in the UPS system model in the simulations to investigate the both modulator and controller performance. The load types and connection diagrams are shown in Figure 4.2 and the load parameters are listed in Table 4.3 and Table 4.4. By selecting various connection configurations between the UPS output terminals and load terminals, all the loading cases considered in Table 4.3 and Table 4.4 can be configured.

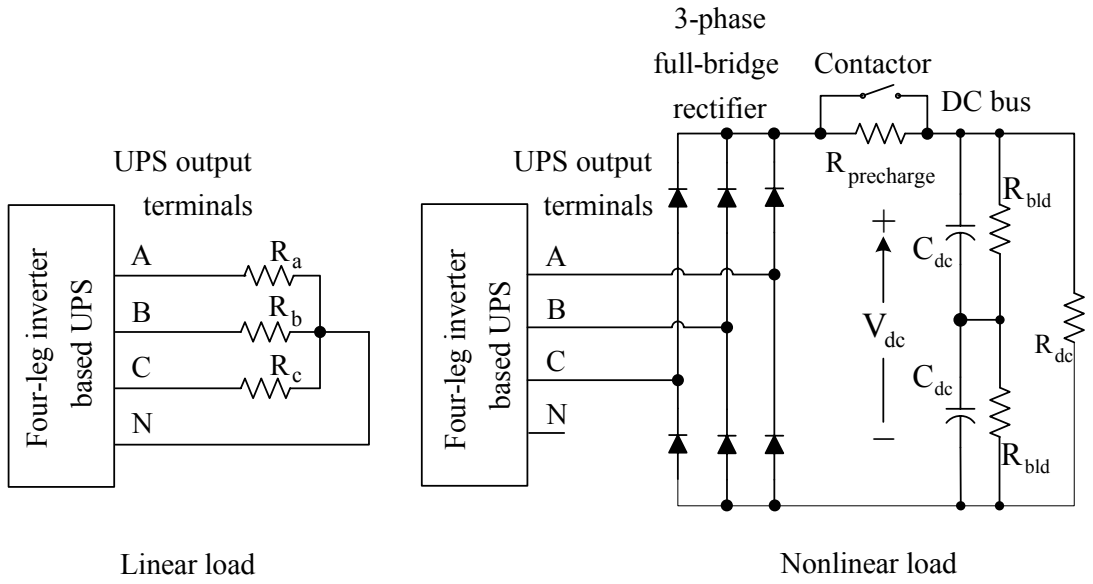


Figure 4.2 Load types utilized in the computer simulations.

Table 4.3 Linear load types utilized in the computer simulations

Balanced load	Unbalanced load	
	Line-neutral	Line-line
$Z_a = R_a = 8.5\ \Omega$	Z_a : Open-circuit	$Z_{ab} = R_{ab} = 14.5\ \Omega$
$Z_b = R_b = 8.5\ \Omega$	$Z_b = R_b = 8.5\ \Omega$	Z_{bc} : Open-circuit
$Z_c = R_c = 8.5\ \Omega$	Z_c : Open-circuit	Z_{ca} : Open-circuit

Table 4.4 The DC bus RC load parameters for nonlinear load types utilized in the computer simulations

Balanced load	Unbalanced load	
	Line-neutral	Line-line
R_{dc} = 24Ω	R_{dc} = 24Ω	R_{dc} = 42Ω
C_{dc} = 1.1 mF	C_{dc} = 1.1 mF	C_{dc} = 1.1 mF

4.3. Simulation Results

In this section, the performance of the four-leg inverter based three-phase UPS system is evaluated by means of the computer simulations. As a first step the output voltage control system is considered. The resonant filter bank based controllers are designed and their control parameters are found by the trial and error method. Since each controller is decoupled from the others, the controllers are tuned in a sequence. Via this approach also the degree of improvement each controller provides can be seen clearly. Once all the controllers are tuned, the design procedure gets completed. Following the completion of the controller design stage, the steady-state performance of the UPS system is evaluated under various loading conditions such as linear, nonlinear, balanced, and unbalanced. Then the dynamic performance of the UPS is examined under severe loading transients. The final section of this chapter involves investigation of the switching ripple and switching loss characteristics of the scalar PWM methods. Specifically the modulator developed in this thesis, the MLDPWM method will be investigated in detail and compared to other modulators in terms of overall performance.

4.3.1. Trial and Error Based Controller Parameter Tuning Procedure

For the purpose of tuning the controller the nonlinear balanced load shown in Figure 4.2 is utilized. Due to its high content of harmonics, this load provides challenging characteristics and creates large amount of harmonic distortion at the output voltage

when the control performance is poor. The load parameters are the same as in Table 4.4. The control method involved is the resonant filter bank structure, one bank per phase (Figure 3.19). In the controller voltage feedforward is utilized. In the simulation the switching frequency is set as 10 kHz and the sampling rate is set twice as the switching frequency, 20 kHz. This is to do double updating of the feedback and output signals for higher bandwidth. The modulator utilized in this procedure is the SVPWM method throughout. In the tuning procedure the UPS output voltage quality determining factors, THD_v, CF, and VR are the prime elements observed.

The tuning procedure is conducted as follows. First, open loop operation is tested. Then, the fundamental component resonant filter is added and the integral and proportional gains of the controller are tuned. Then, based on the observation of output voltage harmonic spectrum, the inclusion of the next resonant filter is decided upon; the most dominant harmonic has the highest priority. Once the resonant filter for this harmonic is built and tuned, this harmonic is suppressed and the next dominant harmonic is taken into consideration. Then the resonant filter for this harmonic is added and tuned. This procedure continues until the highest intended harmonic is suppressed to a sufficient degree. Along the procedure, the proportional gain and also the active damping gain are incremented from the initial value of zero to values that enhance the performance. The method of tuning each filter component is based on the degree of improvement. Every filter parameter is increased to a point where it is no more beneficial to further increase the parameter. The gain of each resonant filter is tuned by trial and error. However, the phase delay compensation and the damping of the filters are not based on trial and error. Rather, the phase delay compensation and damping of each resonant filter are found from Case 3 of Table 3.3 which was shown to be the best choice in terms of performance. Given the phase compensation and the damping values found from this table, the coefficients of the discrete time resonant filter controller equation (3.25) are calculated from (3.20) to (3.24) and placed in the Simplorer discrete time calculator function equation block.

The procedure is summarized in Table 4.5, where the control parameter values, sequence of parameter tuning, and the resulting performance are shown. The related

output voltage waveforms and their harmonic spectrum are shown in Figure 4.3 through Figure 4.20. From here on and throughout the thesis, in all the figures, the scaling information is given as follows. If a scale of 2.5x is shown in the graphic, this implies the number is multiplied with 2.5 and its graphic is drawn. Thus the real value can be found by dividing the number on the graphic by 2.5. During parameter tuning, in the first stage, the output voltages of UPS system are open-loop controlled. Only voltage feedforward is involved. Since the load is nonlinear and draws odd triplen harmonic currents, odd harmonics are seen on the output voltages (Figure 4.3 and Figure 4.4). Thus, the output voltages are distorted and the fifth harmonic component dominantly appears on the output voltage. At this operating point the output voltage THD is 12.12% and the voltage regulation is 4.4%. Both are unacceptable values for practical applications. Then the fundamental component resonant filter is included in the voltage loop and the integral gain is gradually increased from zero to 100 and proportional gain is chosen as 0.05. With the fundamental component controller VR is improved to 0.76% (Figure 4.5 and Figure 4.6). Since the fundamental component controller does not control the output voltage harmonics THD_v value is still poor. Adding the harmonic component controllers to the resonant filter bank (stages III, IV, and V), harmonic components of the UPS output voltage are suppressed and the output voltage quality is improved (Figure 4.7 and Figure 4.8 for stage III, Figure 4.9 and Figure 4.10 for stage IV, Figure 4.11 and Figure 4.12 for stage V). The THD_v value is observed as 5.93% at stage V. At this stage, the gains utilized are at the limit of stability and further increase in the gain results in output voltage oscillation as the system has poor damping. To enhance the system stability, in stage VI, the capacitor current feedback is added to the controller structure for active damping and the stability of the UPS system is improved. With the active damping loop enabled, harmonic components at higher frequencies are suppressed and the controller gains of the harmonic components at lower frequencies can be increased to higher values as the active damping loop increases the system stability (Figure 4.13 and Figure 4.14). In the next three stages (stages VII, VIII, IX), the gains of the harmonic component controllers are further increased without any oscillations at the UPS output voltage (Figure 4.15 and Figure 4.16 for stage VII, Figure 4.17 and Figure 4.18 for stage VIII, Figure 4.19 and Figure 4.20 for stage IX).

Since the harmonic components of the UPS output voltage are suppressed significantly, a high quality UPS output voltage is obtained with the tuned controller parameters. With the designed resonant filter controller, the THD_v is decreased from 12.12% to 1.55% and the UPS output voltages are well-regulated, the VR value is decreased from 4.4% to 0.1%. Note that the crest factor of the load increases from 1.66 to nearly 2.5 and this is due to the fact that as the output impedance of the UPS is decreased by means of the control mechanism, the UPS becomes a more ideal voltage source and the nonlinear load draws more peaky currents from the UPS. As a final remark, it should be noted that the controller gains obtained at the final stage (Stage IX) meet the Routh-Hurwitz stability criteria and these gains will be utilized for performance evaluation of the UPS system.

Table 4.5 Resonant filter controller gain tuning and steady-state performance improvement stages of the UPS output voltage (computer simulation results)

Stage	Controller	Gains	THD_v (%)	CF	VR (%)
I	Open loop	----------	12.12	1.66	4.4
II	Fundamental frequency controller added	K_{i1}=100, K_{pv}=0.05	13.2	1.65	0.76
III	5^{th} and 7^{th} harmonic controllers added	K_{i5}=15, K_{i7}=15	8.85	2.08	0.33
IV	11^{th} and 13^{th} harmonic controllers added	K_{i11}=3, K_{i13}=1	5.97	2.23	0.09
V	3^{rd} and 9^{th} harmonic controllers added	K_{i3}=5, K_{i9}=3	5.93	2.24	0.12
VI	Capacitor current feedback added, proportional gain increased	K_{ad}=15, K_{pv}=1	3.41	2.27	0.08
VII	5^{th} and 7^{th} harmonic controllers updated (K_{i5} and K_{i7} increased)	K_{i5}=75, K_{i7}=75	2.54	2.30	0.05
VIII	11^{th} and 13^{th} harmonic controllers updated (K_{i11} and K_{i13} increased)	K_{i11}=15, K_{i13}=10	1.57	2.44	0.08
IX	3^{rd} and 9^{th} harmonic controllers updated (K_{i3} and K_{i9} increased)	K_{i3}=50, K_{i9}=10	1.55	2.49	0.10

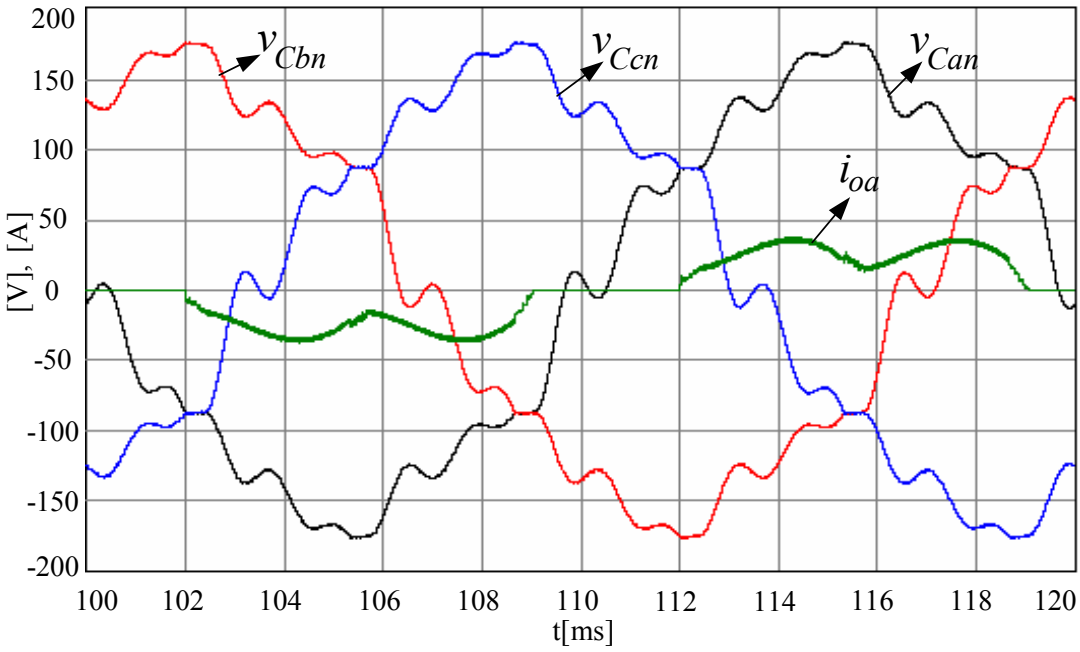


Figure 4.3 Three-phase output voltages and one phase load current (green, scale: 2.5x(the original number is multiplied by 2.5 and plotted)) during open-loop operation at balanced nonlinear full-load (Stage I of Table 4.5).

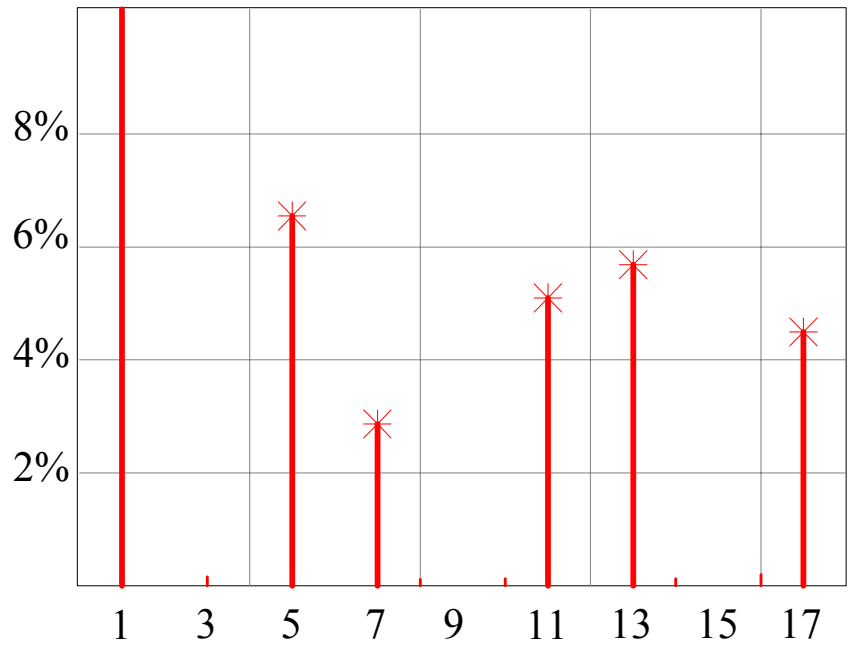


Figure 4.4 The harmonic spectrum of the output phase voltage for open-loop operation at balanced nonlinear full-load (Stage I of Table 4.5).

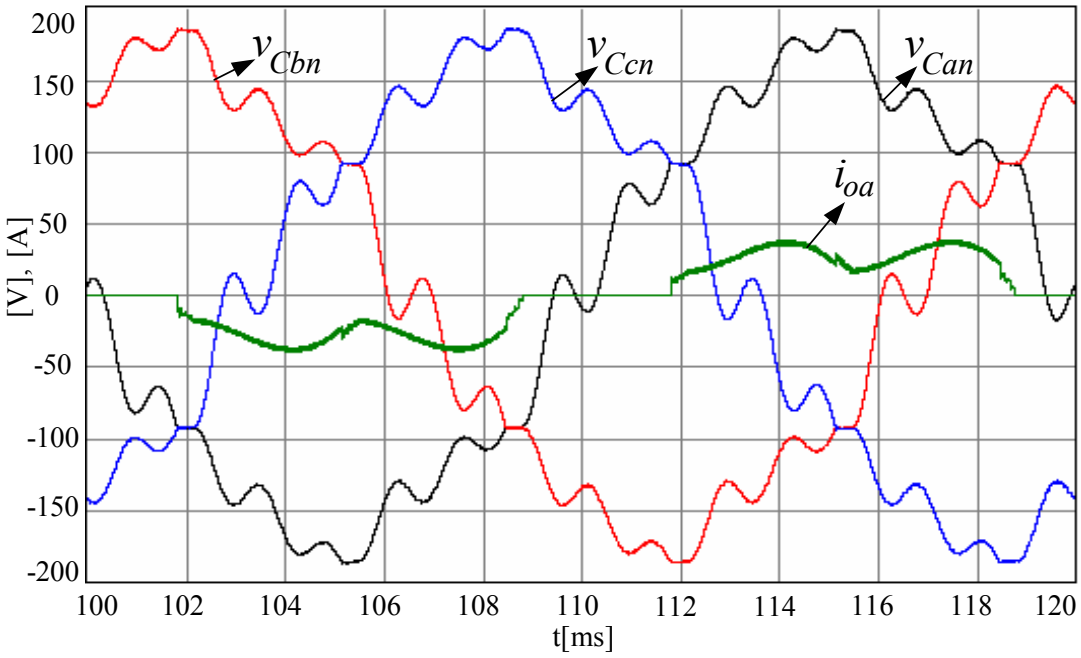


Figure 4.5 Three-phase output voltages and one phase load current (green, scale: 2.5x) closed-loop operation at balanced nonlinear full-load (Stage II of Table 4.5).

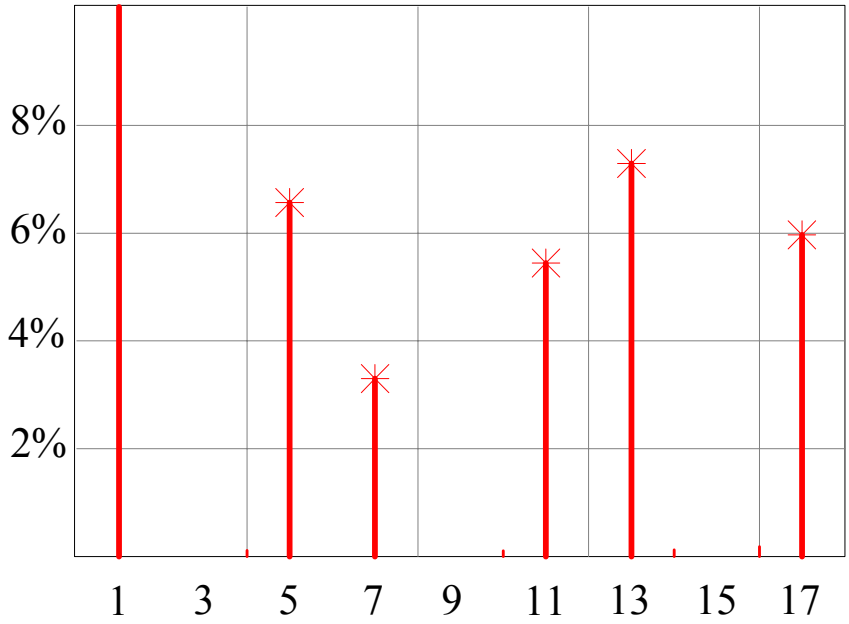


Figure 4.6 The harmonic spectrum of the three-phase output voltages during closed-loop operation at balanced nonlinear full-load (Stage II of Table 4.5).

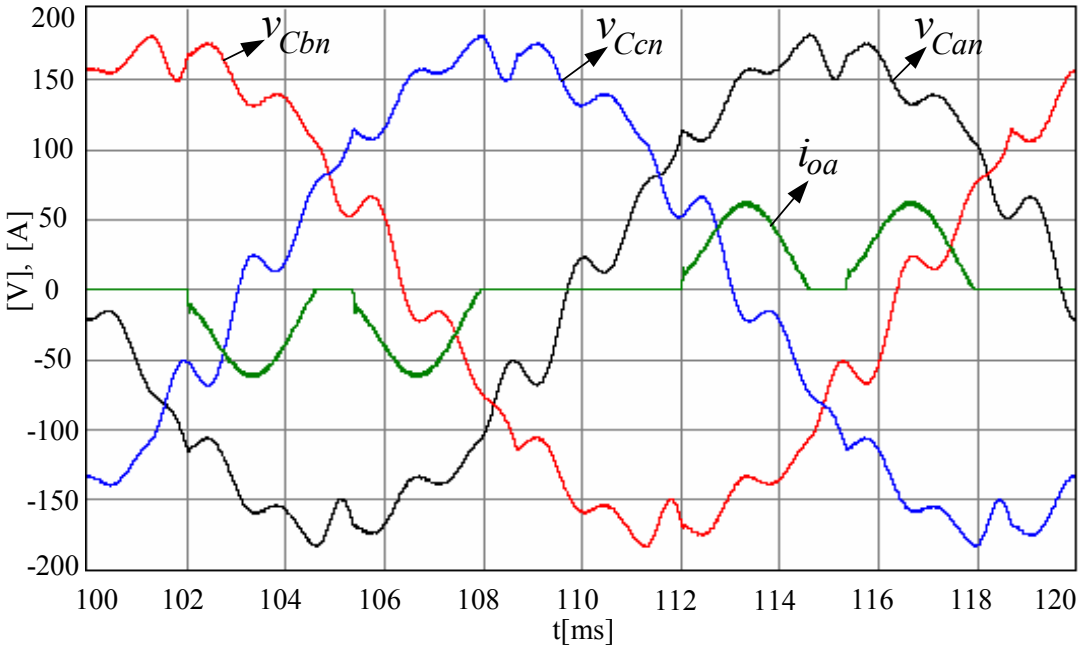


Figure 4.7 Three-phase output voltages and one phase load current (green, scale: 2.5x) closed-loop operation at balanced nonlinear full-load (Stage III of Table 4.5).

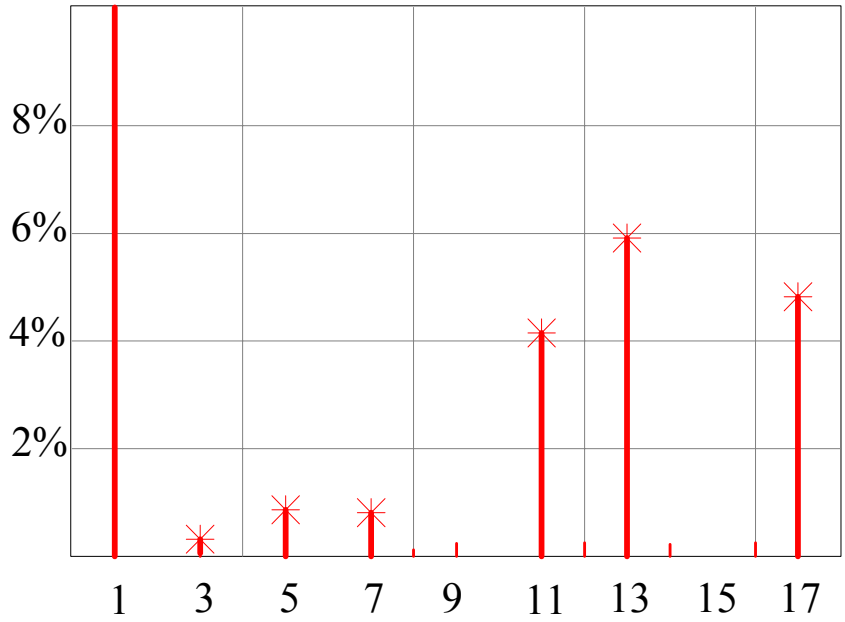


Figure 4.8 The harmonic spectrum of the three-phase output voltages during closed-loop operation at balanced nonlinear full-load (Stage III of Table 4.5).

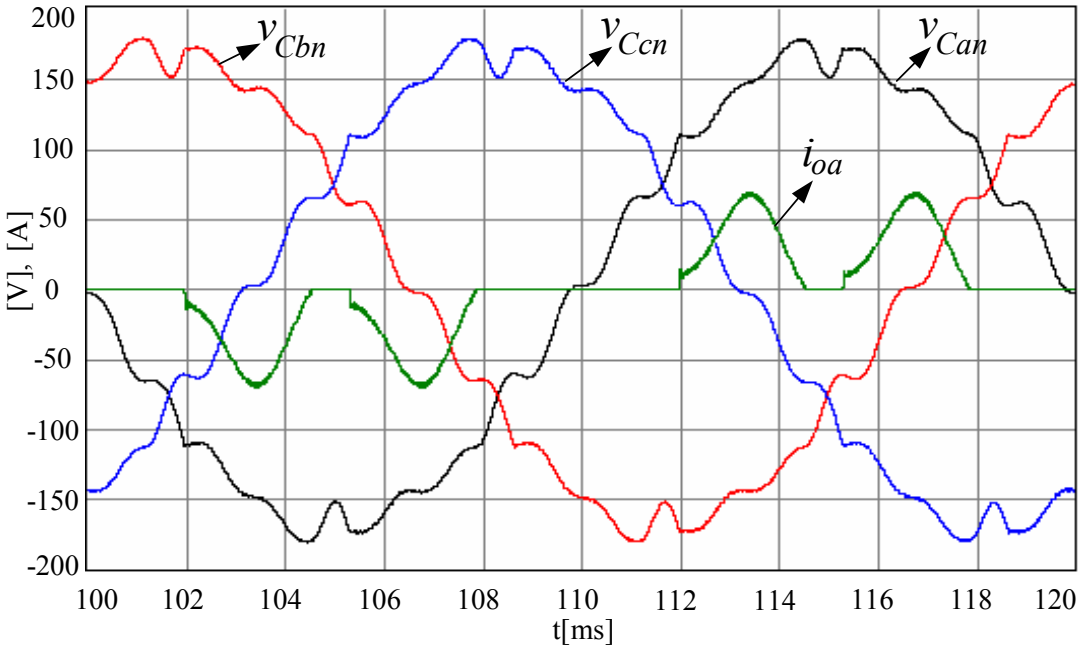


Figure 4.9 Three-phase output voltages and one phase load current (green, scale: 2.5x) closed-loop operation at balanced nonlinear full-load (Stage IV of Table 4.5).

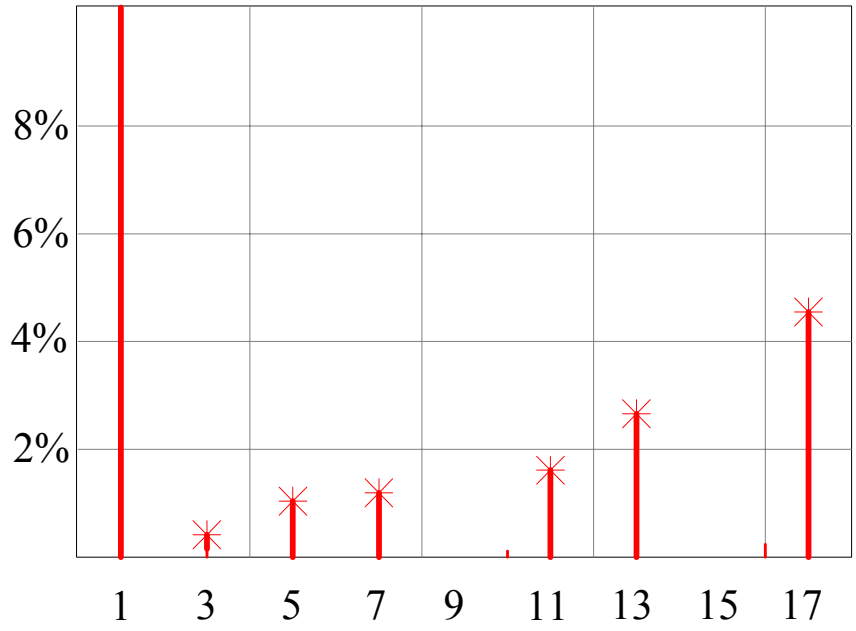


Figure 4.10 The harmonic spectrum of the three-phase output voltages during closed-loop operation at balanced nonlinear full-load (Stage IV of Table 4.5).

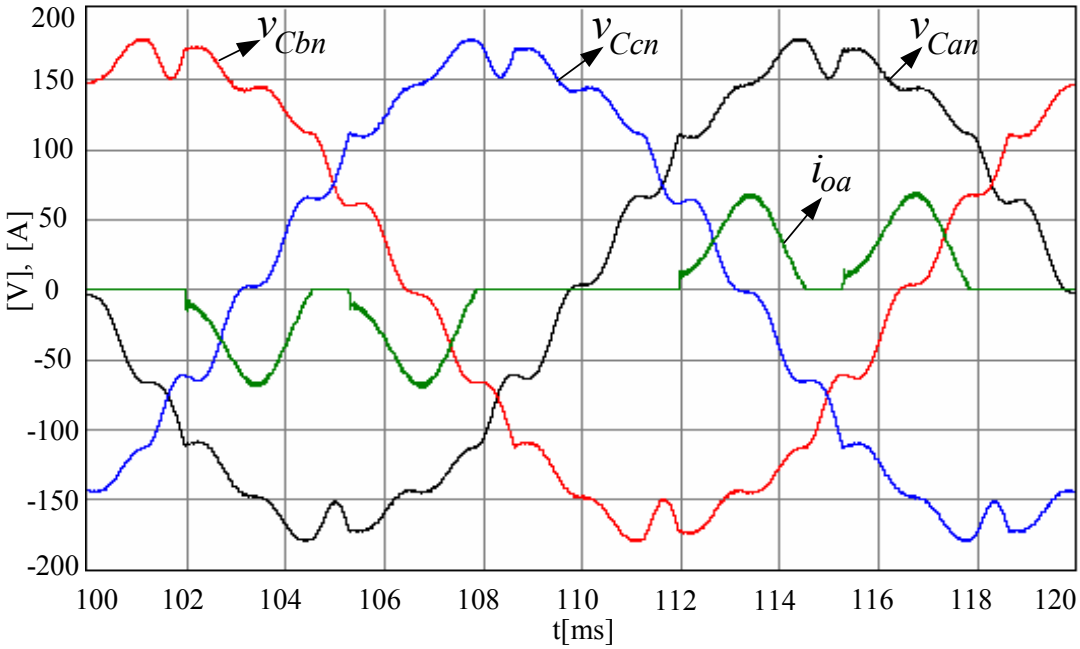


Figure 4.11 Three-phase output voltages and one phase load current (green, scale: 2.5x) closed-loop operation at balanced nonlinear full-load (Stage V of Table 4.5).

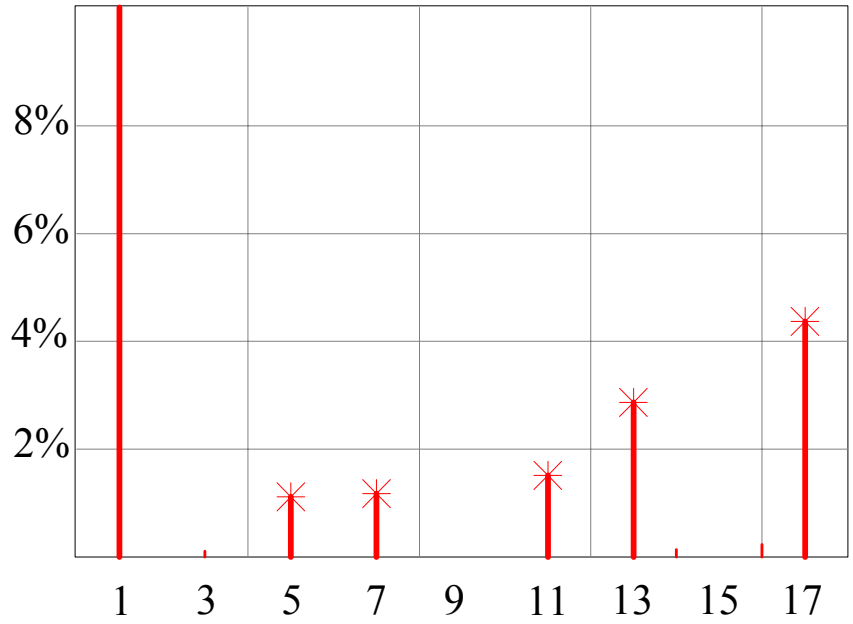


Figure 4.12 The harmonic spectrum of the three-phase output voltages during closed-loop operation at balanced nonlinear full-load (Stage V of Table 4.5).

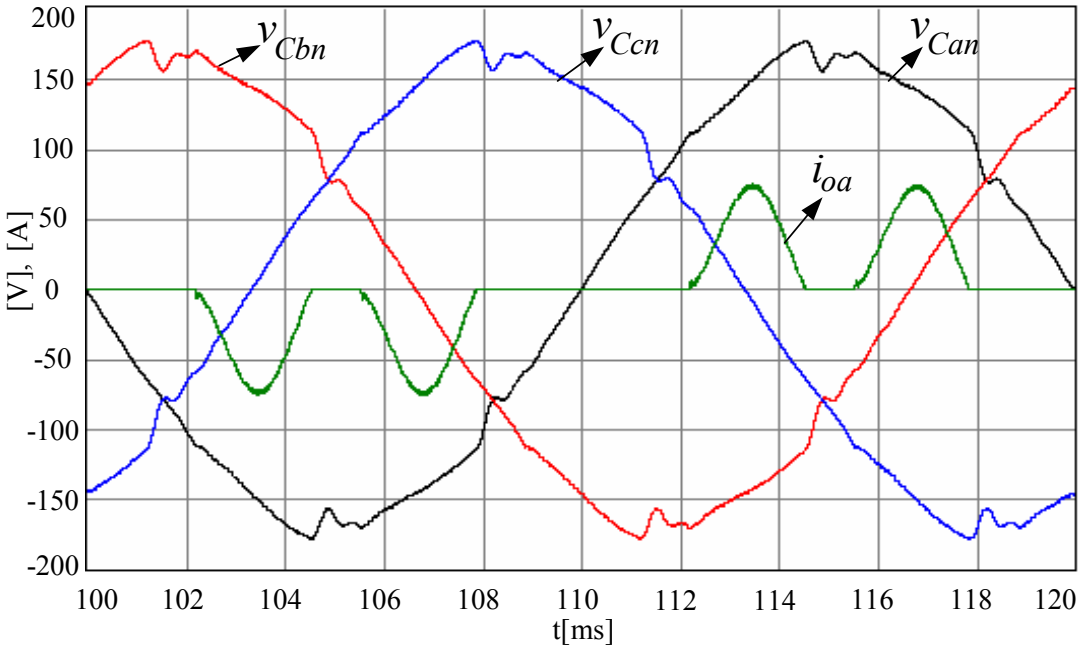


Figure 4.13 Three-phase output voltages and one phase load current (green, scale: 2.5x) closed-loop operation at balanced nonlinear full-load (Stage VI of Table 4.5).

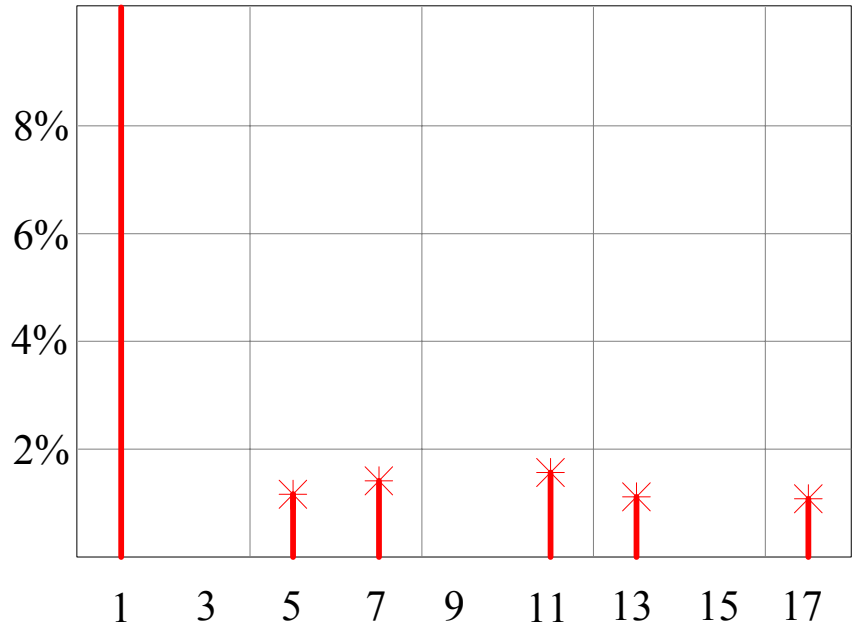


Figure 4.14 The harmonic spectrum of the three-phase output voltages during closed-loop operation at balanced nonlinear full-load (Stage VI of Table 4.5).

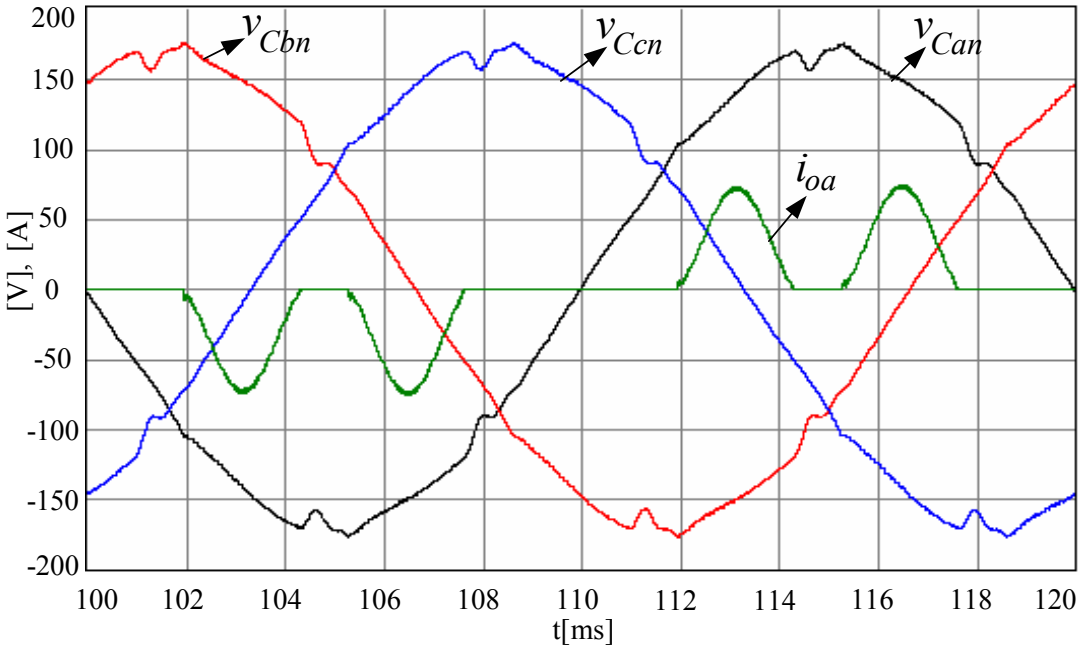


Figure 4.15 Three-phase output voltages and one phase load current (green, scale: 2.5x) closed-loop operation at balanced nonlinear full-load (Stage VII of Table 4.5).

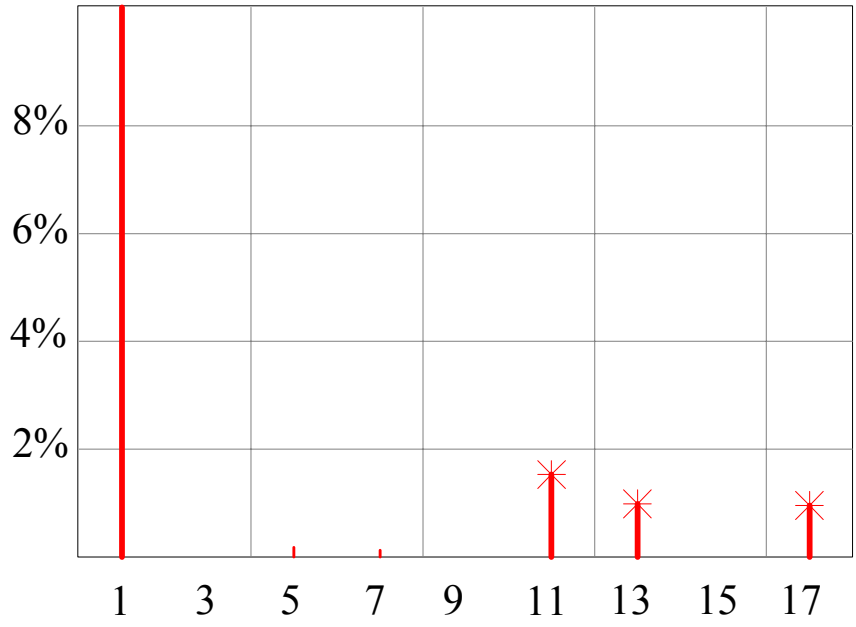


Figure 4.16 The harmonic spectrum of the three-phase output voltages during closed-loop operation at balanced nonlinear full-load (Stage VII of Table 4.5).

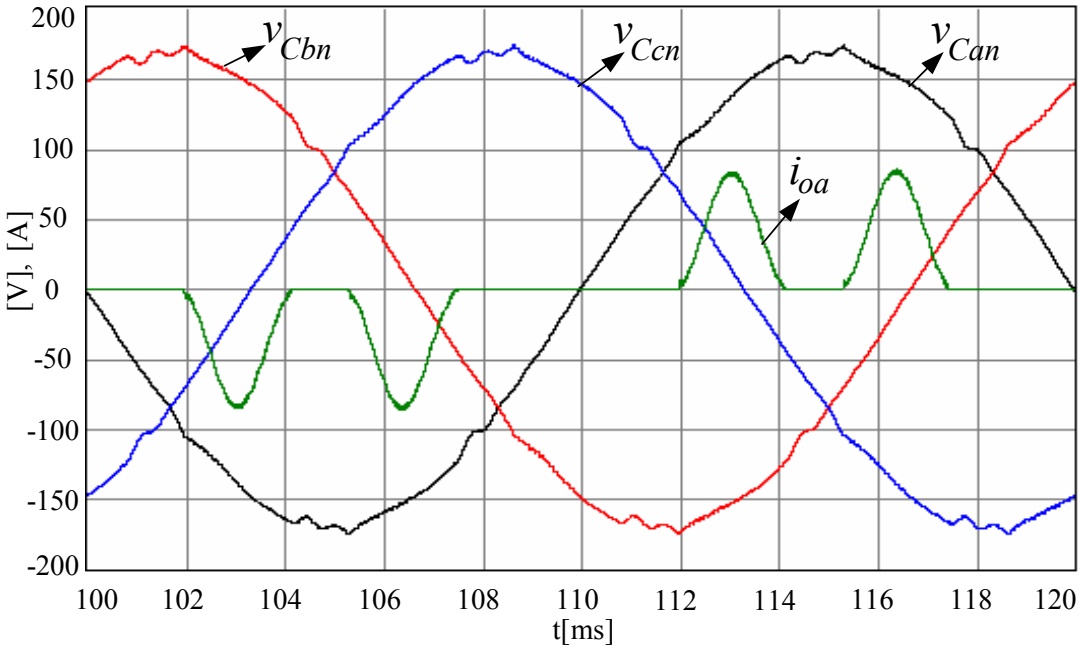


Figure 4.17 Three-phase output voltages and one phase load current (green, scale: 2.5x) closed-loop operation at balanced nonlinear full-load (Stage VIII of Table 4.5).

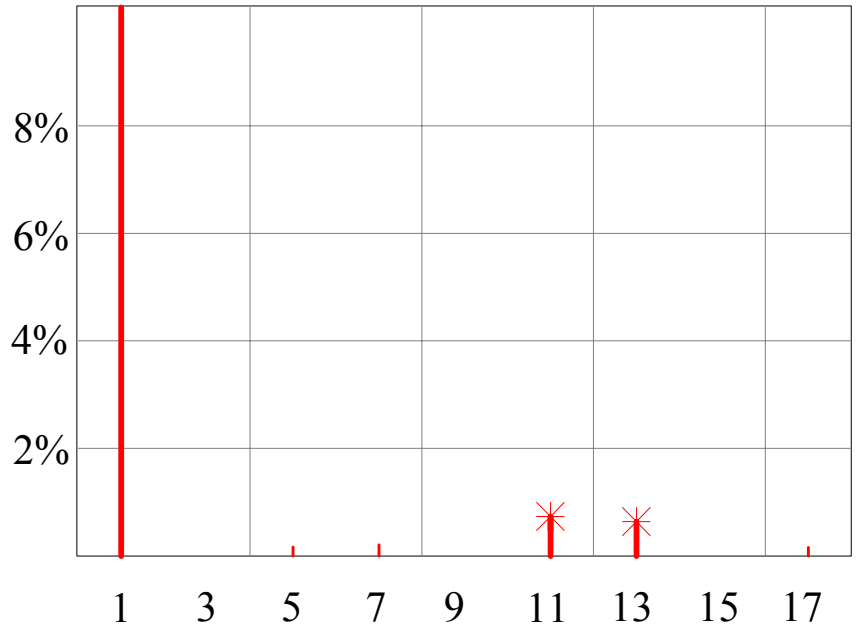


Figure 4.18 The harmonic spectrum of the three-phase output voltages during closed-loop operation at balanced nonlinear full-load (Stage VIII of Table 4.5).

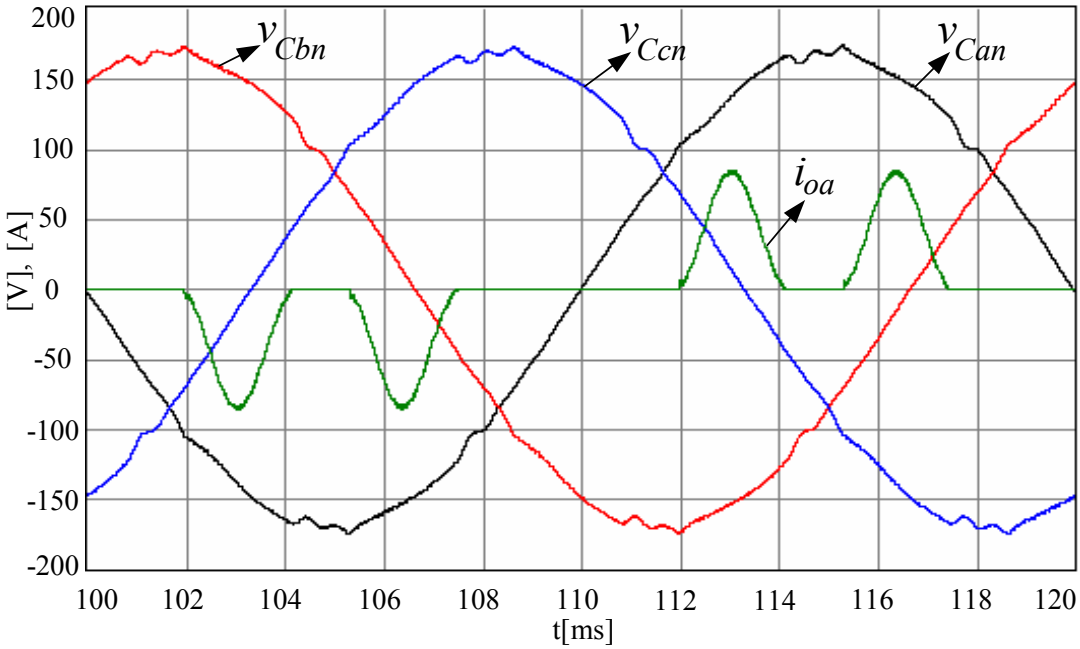


Figure 4.19 Three-phase output voltages and one phase load current (green, scale: 2.5x) closed-loop operation at balanced nonlinear full-load (Stage IX of Table 4.5).

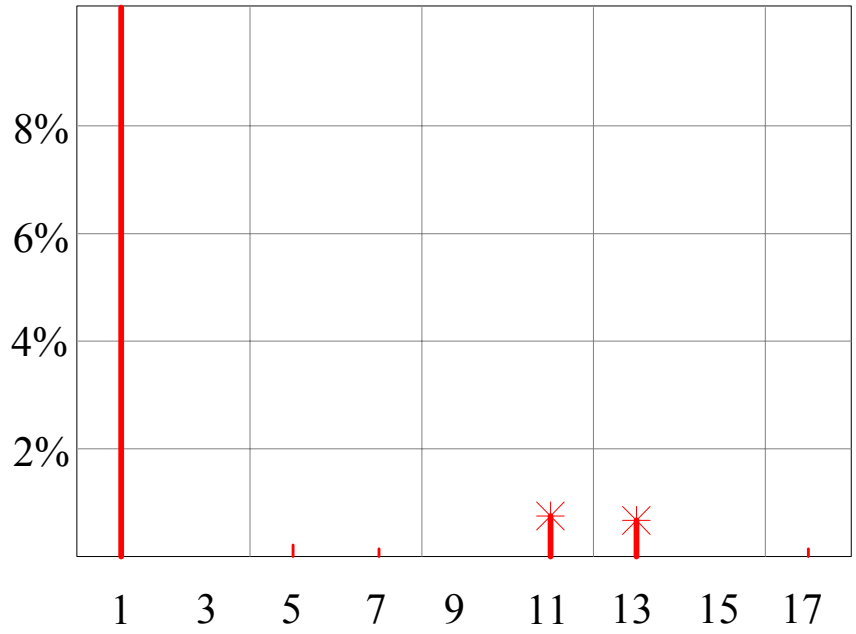


Figure 4.20 The harmonic spectrum of the three-phase output voltages during closed-loop operation at balanced nonlinear full-load (Stage IX of Table 4.5).

4.3.2. Steady-State Performance Evaluation of The Resonant Filter Controller at Various Operating Conditions

The resonant filter controller designed in the previous section will be tested under various steady-state operating conditions and its performance indices will be displayed and compared for the purpose of evaluating the feasibility of the method. No-load, linear balanced and unbalanced full-load, and nonlinear balanced and unbalanced full-load operating conditions will be considered and computer simulations for all these cases will be executed and the results will be summarized. The SVPWM method with 10 kHz carrier and 20 kHz sampling and update rate is utilized throughout these simulations. The UPS output ratings are the same as those listed in Table 4.1. Therefore, the load parameters are also the same as the above section (Table 4.3 and Table 4.4).

The controller structure to be utilized in this section is the same as the previous section and also shown in Figure 3.19. In order to illustrate the influence of each controller component on the steady-state performance, various controller combinations will be considered. The controller cases and the performance results are listed in Table 4.6. In this table the controllers are labeled as Case A, Case B, Case C, and Case D. The controller gains of case A correspond to Stage II of the previous section. Controller gains of case B correspond to Stage V of the previous section. Controller gains of case C are unique to this section and they are determined by trial and error (K_{il}=100, K_{ad}=15, K_{pv}=1). The controller gains of Case D are the same of Stage IX of the previous section which were considered as the optimal gains for the system. For this case, the computer simulation waveforms are also shown in detail in Figure 4.21 through Figure 4.48 corresponding to the loading conditions listed in the Table 4.6.

Table 4.6 The steady-state performance of the UPS under various loading conditions (A range is given when noticeable differences exist among the three-phase quantities)

		Open loop	Without capacitor current feedback		With capacitor current feedback	
			The fundamental component is controlled (A)	The fundamental and harmonic components are controlled (B)	The fundamental component is controlled (C)	The fundamental and harmonic components are controlled (D)
No-load	THD_V (%)	0.7	0.6	0.8	0.28	0.24
Linear balanced load	CF	1.42	1.42	1.42	1.43	1.43
	VR (%)	7.2	0.0~0.1	0.05	0.0	0.1
	THD_V (%)	0.6	0.6	0.35	0.3	0.2
Linear line-neutral unbalanced load	CF	1.42	1.43	1.43	1.43	1.43
	VR (%)	3.3~9.8	0.1	0.06	0.3	0.3
	THD_V (%)	1.2~1.42	1.2~1.46	0.9~1.05	0.4~0.8	0.3~0.46
Linear line-line unbalanced load	CF	1.42	1.42	1.42	1.43	1.42
	VR (%)	0.0~8.3	0.1	0.0~0.1	0.0~0.13	0.18
	THD_V (%)	0.63~0.88	0.93~1.17	0.73~0.95	0.3~0.48	0.4
Nonlinear balanced load	CF	1.66	1.65	2.24	1.84	2.6
	VR (%)	4.4	0.9	0.2	0.15	0.1
	THD_V (%)	12.03	13.2	5.93	5.9	1.55
Nonlinear line-neutral unbalanced load	CF	2.29	2.33	2.86	2.46	3.21
	VR (%)	2.3~5.44	0.2~1.1	0.0~0.4	0.1~0.3	0.05
	THD_V (%)	4.66~13.8	6.8~15.0	3.58~9.0	2.35~8.0	0.7~2.1
Nonlinear line-line unbalanced load	CF	2.3	2.34	2.94	2.52	3.26
	VR (%)	0.2~3.5	0.0~0.8	0.0~0.3	0.0~0.15	0.0~0.1
	THD_V (%)	0.6~10.8	1.1~13.0	1.23~8.7	0.3~5.86	0.3~3.21

The influence of the controller components utilized can be observed from Table 4.6 clearly. While the open-loop performance is poor overall, the closed loop performance depends on the controller type employed. In all the cases voltage regulation improves with the use of the fundamental component resonant filters. Even with unbalanced loads, the fundamental component is well regulated. While the harmonic component resonant filters improve the output voltage waveform and clean out the low frequency dominant harmonics, they can not eliminate or reduce the high frequency output voltage harmonics. The active damping loop suppresses the high frequency output voltage harmonics to the degree of its capability which is limited to the measurement, computation, and PWM delays.

The steady-state performance improvement can be best seen in the nonlinear load operating condition. In this case, under open loop operating conditions, the output voltage harmonics are significant and the current waveform is quite flat. With the harmonic compensators and active damping loop being activated, the UPS output impedance is lowered over a wide range of harmonic frequencies. Thus, a nonlinear load drawing harmonic currents does not cause an output voltage distortion. This implies that the UPS is approaching an ideal voltage source which has zero output impedance and ideal internal voltage. Thus, in Table 4.6, it can be seen that the crest factor increases significantly and the nonlinear load current becomes more and more spiky with the higher performance controller structure. When utilizing both capacitor current feedback and harmonic controller components in the controller structure, the highest performance results are obtained for all the considered load conditions.

In the following the inverter and output voltage/current waveforms are discussed for the case where all the controllers are utilized (Case D in Table 4.6) and compared with the open loop operation waveforms. Figure 4.21 shows that under no-load open loop operating condition the output voltage is sinusoidal and clean. Closed loop operation under no-load brings marginal improvement as shown in Figure 4.22. The inductor currents for all the inverter legs are small and mainly consist of the PWM ripple as shown in Figure 4.23. The SVPWM modulation signals for all the four legs

of the inverter are shown in Figure 4.24 and it can be seen that the operation is steady-state balanced. While the DC bus voltage is ±270V, the peak of the modulation signals is ±150V indicating that the DC bus voltage utilization (modulation index) is not very high.

Figure 4.25 shows the output voltages and currents for the full resistive load operating conditions for the open loop control method. Except for voltage regulation the performance seems satisfactory. Closed loop operation for the same load is illustrated in Figure 4.26 where it is seen that the voltage regulation is restored. Figure 4.27 shows the inductor currents where the ripple is not a part of the full current and the ripple current of the fourth leg is slightly larger than the three-phase legs. In Figure 4.28 the modulation signals are shown and it can be seen that the controller generates larger voltage commands so that the fundamental frequency voltage drop on the filter inductors is compensated by the inverter so that the output voltage is restored to the rated value (compared to Figure 4.24).

Figure 4.29 shows the single-phase linear balanced load operating condition voltage and current waveforms for open loop control. In this case it can be seen that the loaded phase has a larger voltage drop than the other two, implying output voltage unbalance and also poor voltage regulation. Closed loop control, as shown in Figure 4.30 helps restore the balance and voltage regulation on the output of the UPS. Figure 4.31 shows the inductor currents and from here it is clear that the fourth leg provides the path for the unbalanced zero sequence current. Also from the figure it can be seen again that the ripple on the fourth leg is larger than the active phase leg ripple current. Finally, Figure 4.32 shows the modulation waves. It is clear from the modulation waveforms that in order to provide balanced output voltages the inverter must provide unbalanced modulation signals. In the figure the active phase modulation signal is slightly extended outwards to provide voltage compensation for the voltage drop on this phase. Also the fourth leg modulation signal is no more a simple triangular shaped waveform with three times the fundamental frequency (compare with Figure 4.28) but it has some lower frequency signal on it.

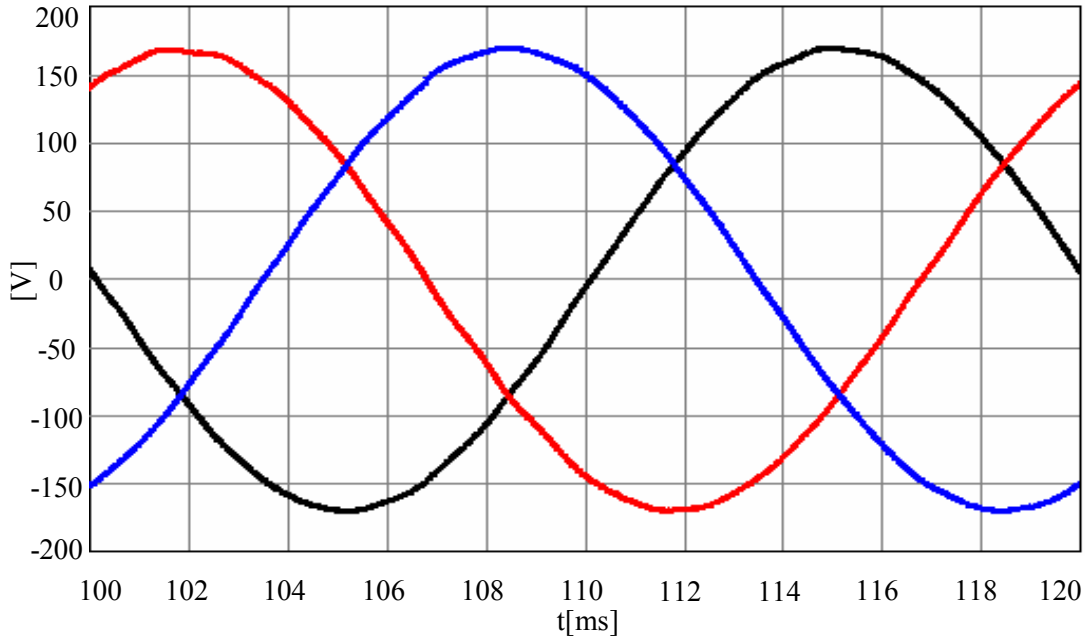


Figure 4.21 Steady-state three-phase output voltages during open-loop operation under no-load operating condition.

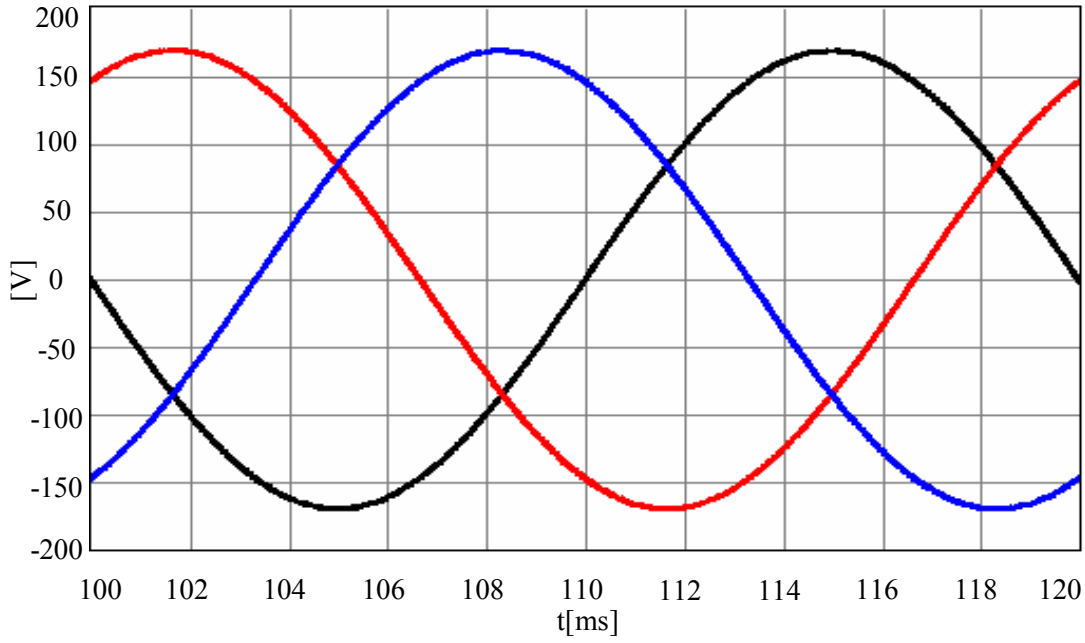


Figure 4.22 Steady-state three-phase output voltages during closed-loop operation under no-load operating condition.

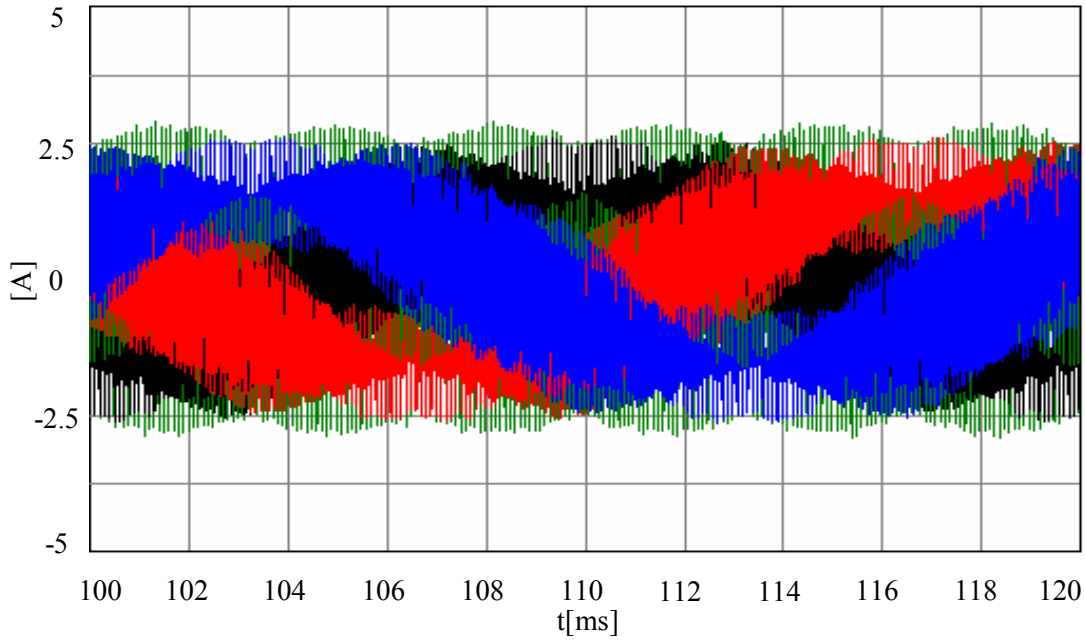


Figure 4.23 Steady-state inductor currents during closed-loop operation under no-load operating condition.

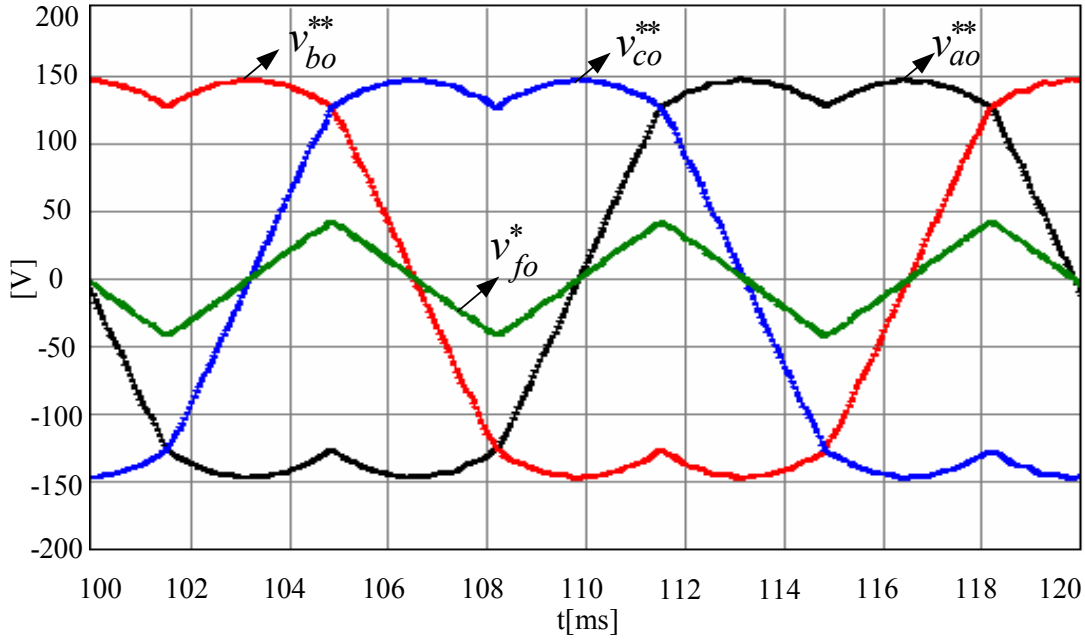


Figure 4.24 Steady-state modulation signals during closed-loop operation under no-load operating condition.

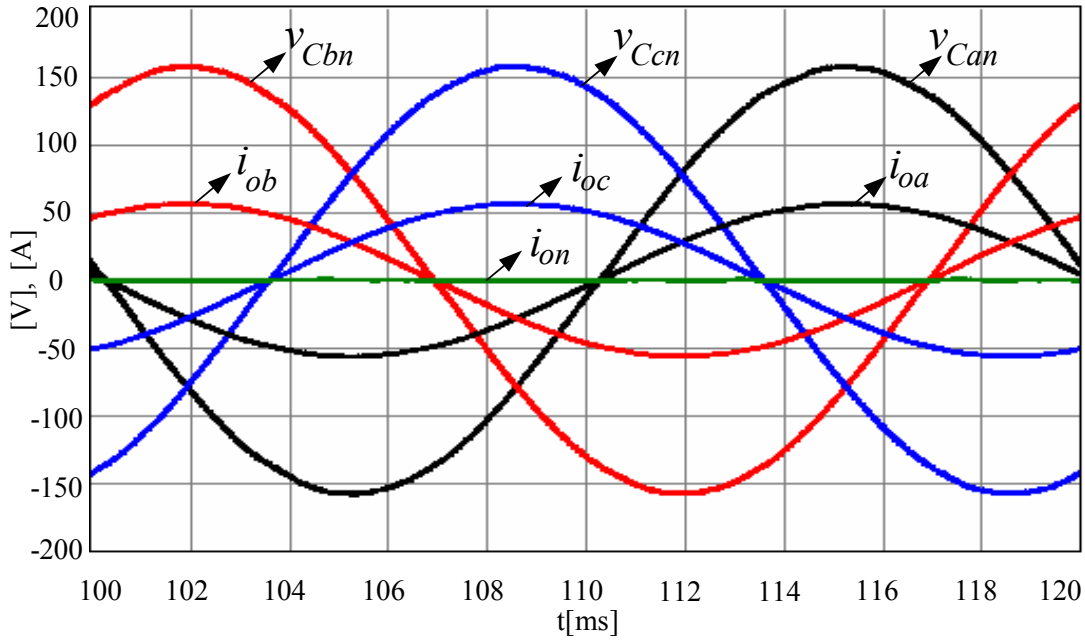


Figure 4.25 Steady-state output voltages and load currents (scale: x3) during open-loop operation under linear balanced full-load operating condition.

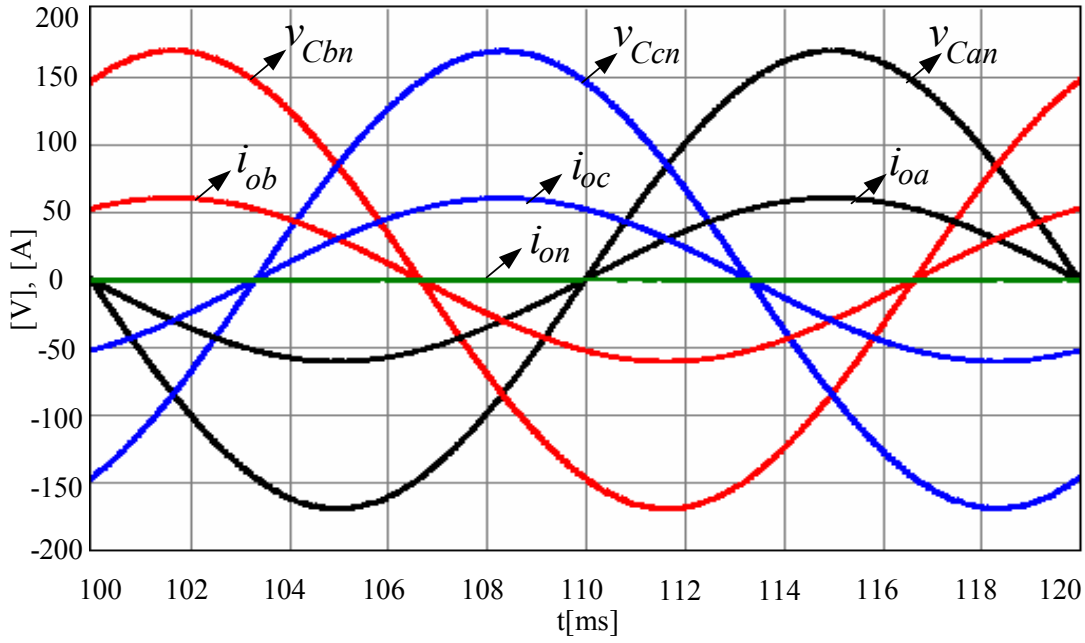


Figure 4.26 Steady-state output voltages and load currents (scale: x3) during closed-loop operation under linear balanced full-load operating condition.

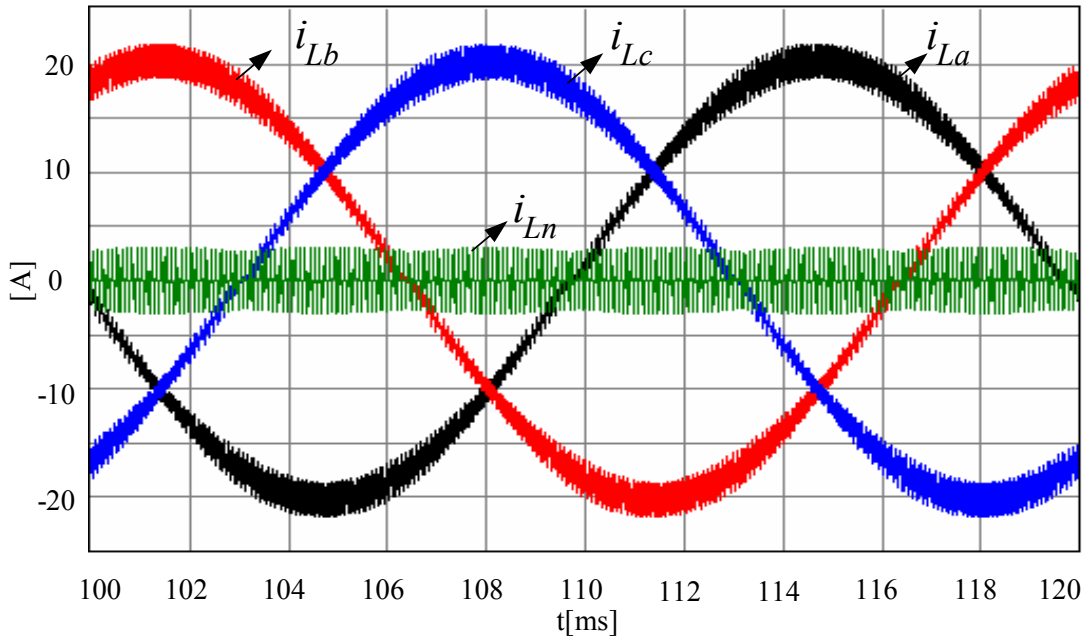


Figure 4.27 Steady-state inductor currents during closed-loop operation under linear balanced full-load operating condition.

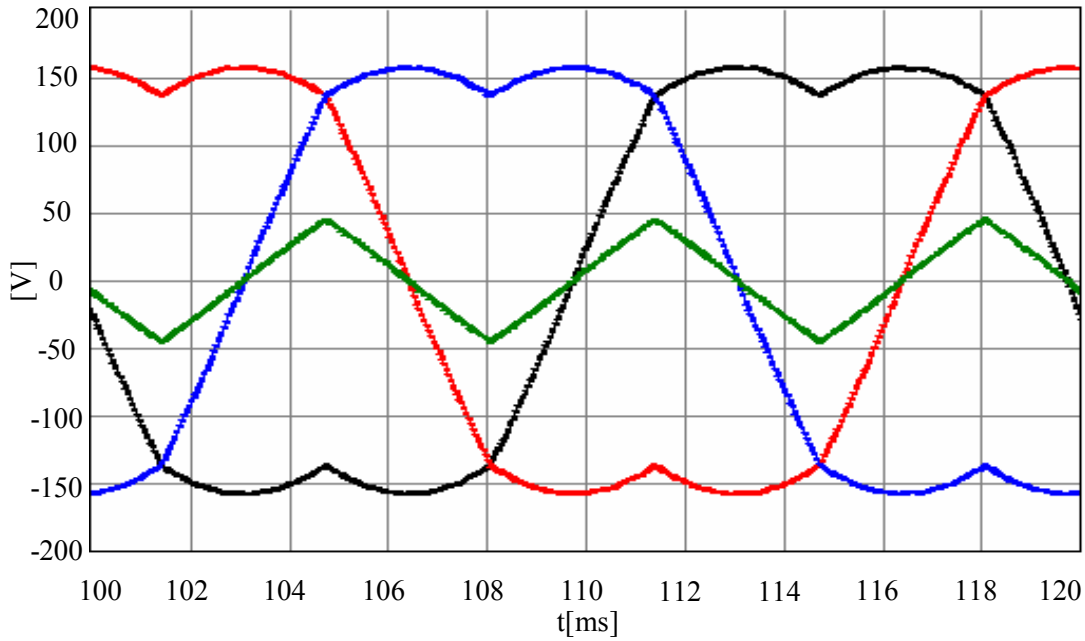


Figure 4.28 Steady-state modulation signals during closed-loop operation under linear balanced full-load operating condition.

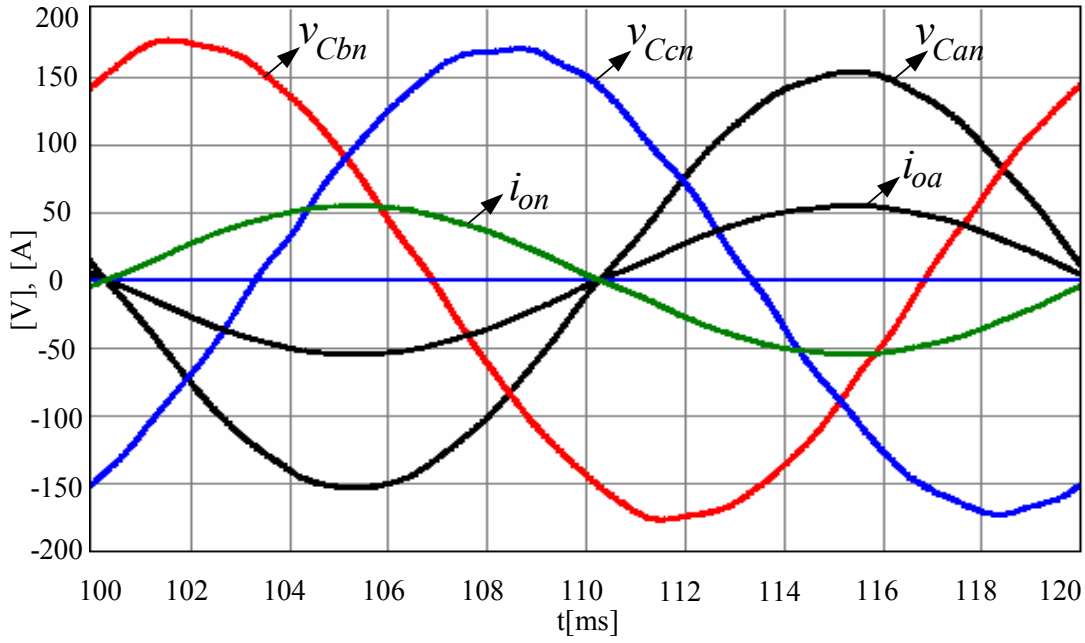


Figure 4.29 Steady-state output voltages and load currents (scale: x3) during open-loop operation under linear line-neutral unbalanced full-load operating condition.

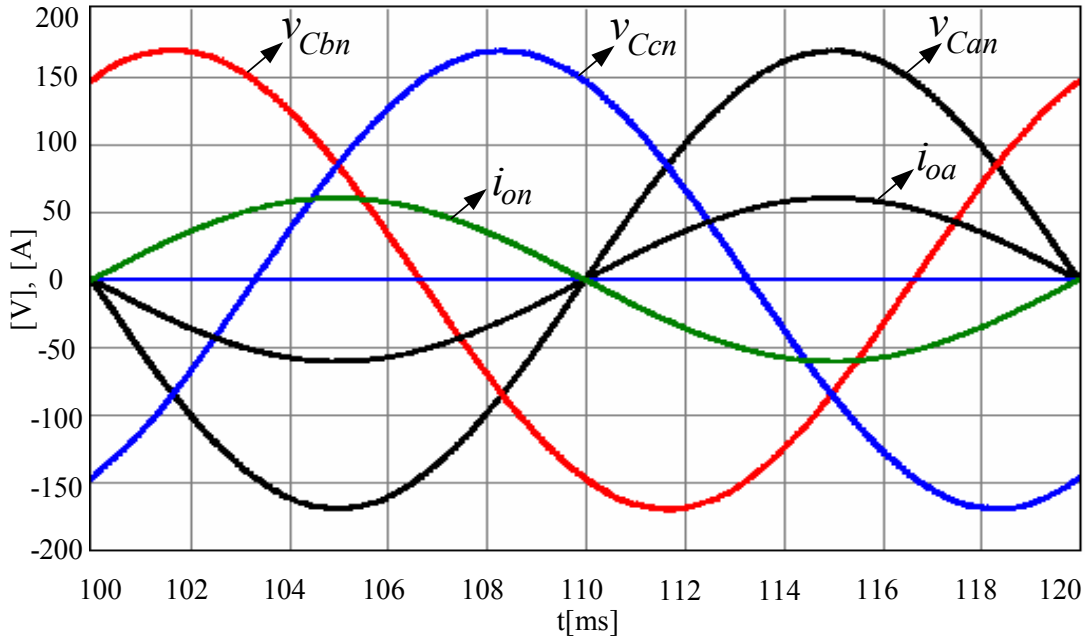


Figure 4.30 Steady-state output voltages and load currents (scale: x3) during closed-loop operation under linear line-neutral unbalanced full-load operating condition.

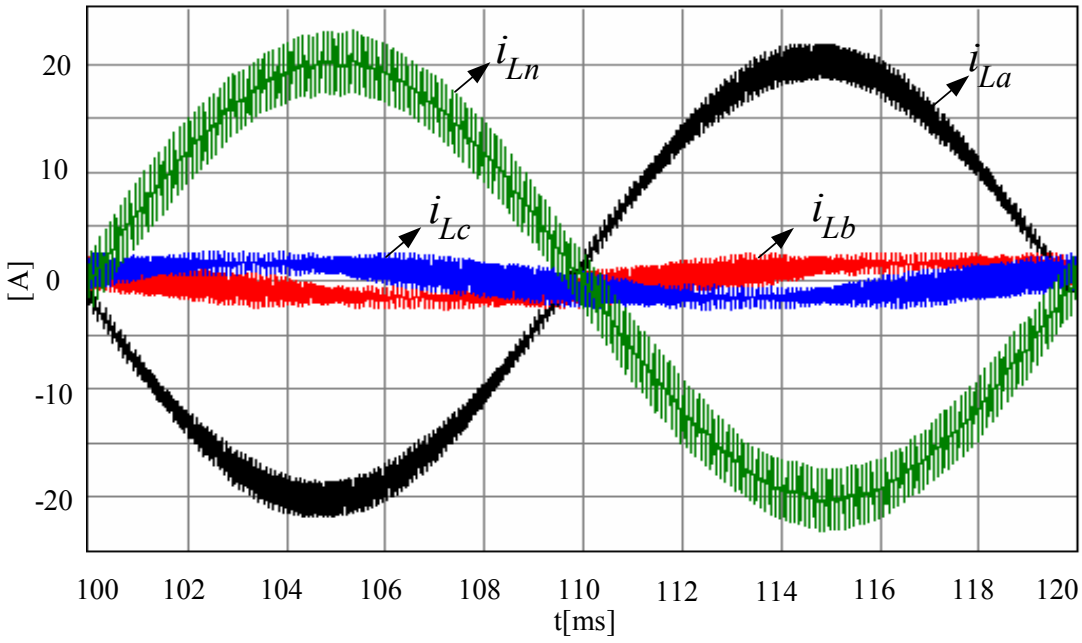


Figure 4.31 Steady-state inductor currents during closed-loop operation under linear line-neutral unbalanced full-load operating condition.

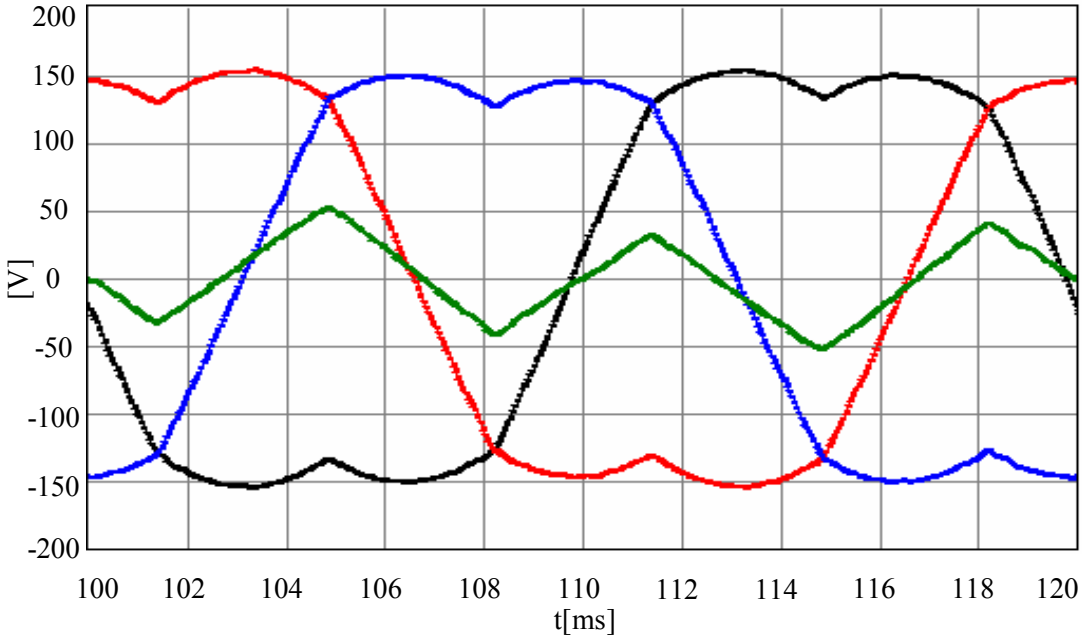


Figure 4.32 Steady-state modulation signals during closed-loop operation under linear line-neutral unbalanced full-load operating condition.

For the line to line unbalanced resistive full load case the open loop control operation waveforms are shown in Figure 4.33. As can be seen that the output voltage unbalance is significant and the regulation is poor. Shown in Figure 4.34 the closed loop operating waveforms indicate that the voltage balance and regulation are restored. As shown in Figure 4.35 the inductor currents associated with the two active output phases are of opposite sign and same magnitude. The fourth leg current is only consisting of the PWM ripple. As in the line to line unbalanced load case there is no zero sequence current component, the fourth leg has no load on it. As a result the modulation signal of the fourth leg is supposed to be the same. As Figure 4.36 confirms this fact, the modulation signals of the active phases are unbalanced and the fourth leg modulation signal is unaltered.

In Figure 4.37 the open loop controlled nonlinear balanced fully loaded operating condition output voltage and current waveforms are shown. In addition to the voltage regulation problems, here a significant output voltage harmonic distortion appears. Employing the high performance output voltage control algorithm, as shown in Figure 4.38, the output voltage harmonics are significantly improved and the voltage regulation is restored. In this case the crest factor is increased from 1.66 to 2.6 which is a prime indicator of the output voltage waveform improvement. Also note that the load currents become sharper and two rabbit ears appear instead of one per half cycle. As shown in Figure 4.39, the inductor currents take the shape of the load current and the load harmonic currents are compensated from the inverter instead of flowing through the output capacitors and causing output voltage distortion. Since the load is balanced the fourth leg current is small and negligible. As it provides the harmonic currents, the inverter must generate modulation signals accordingly. The modulation signals shown in Figure 4.40 confirm this fact. The modulation signals are highly distorted but still balanced as a consequence of the fact that the load is balanced. Also it should be noticed that the voltage utilization in this case is quite high. The modulation signals reach ±220V which is quite close to the maximum available values of ±270V. As a consequence of balanced operation and quite negligible fourth leg current, the modulation signal of the fourth leg retains its shape similar to the linear balanced load case.

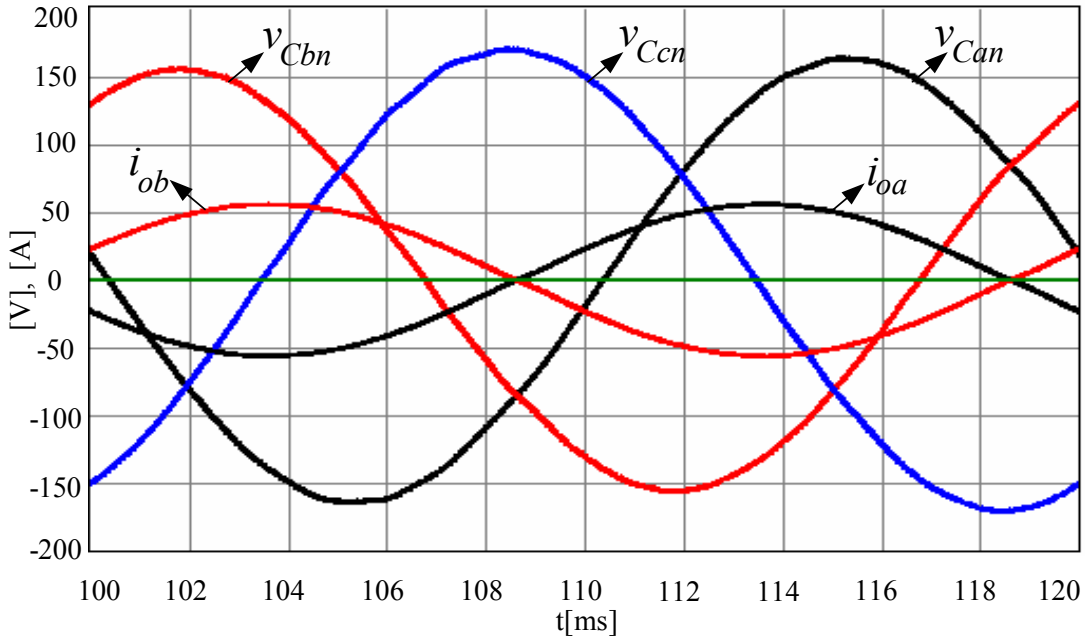


Figure 4.33 Steady-state output voltages and load currents (scale: x3) during open-loop operation under linear line-line unbalanced full-load operating condition.

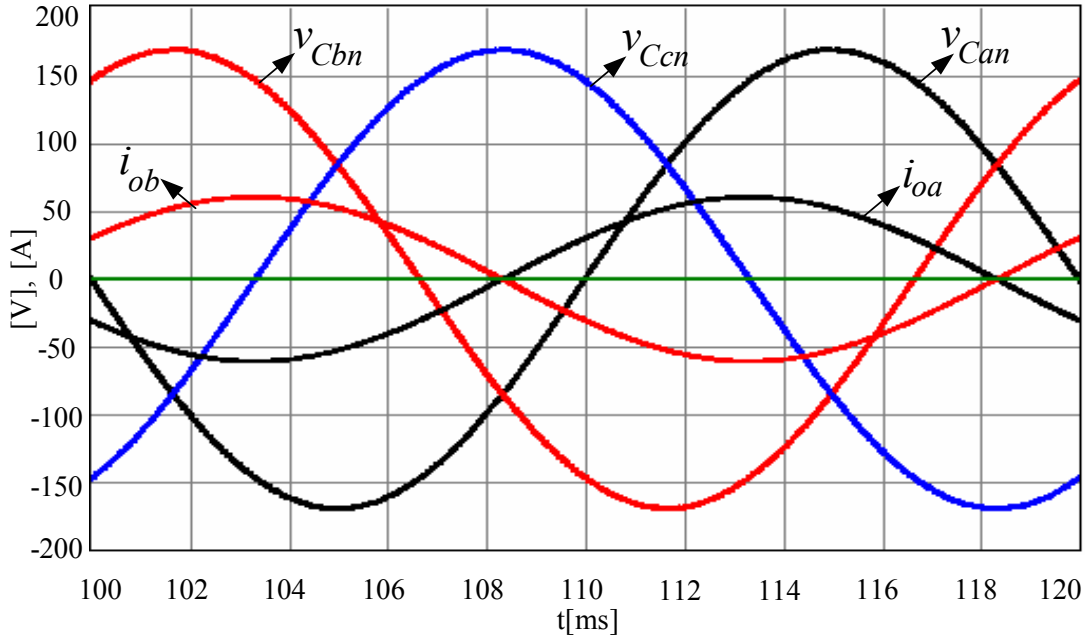


Figure 4.34 Steady-state output voltages and load currents (scale: x3) during closed-loop operation under linear line-line unbalanced full-load operating condition.

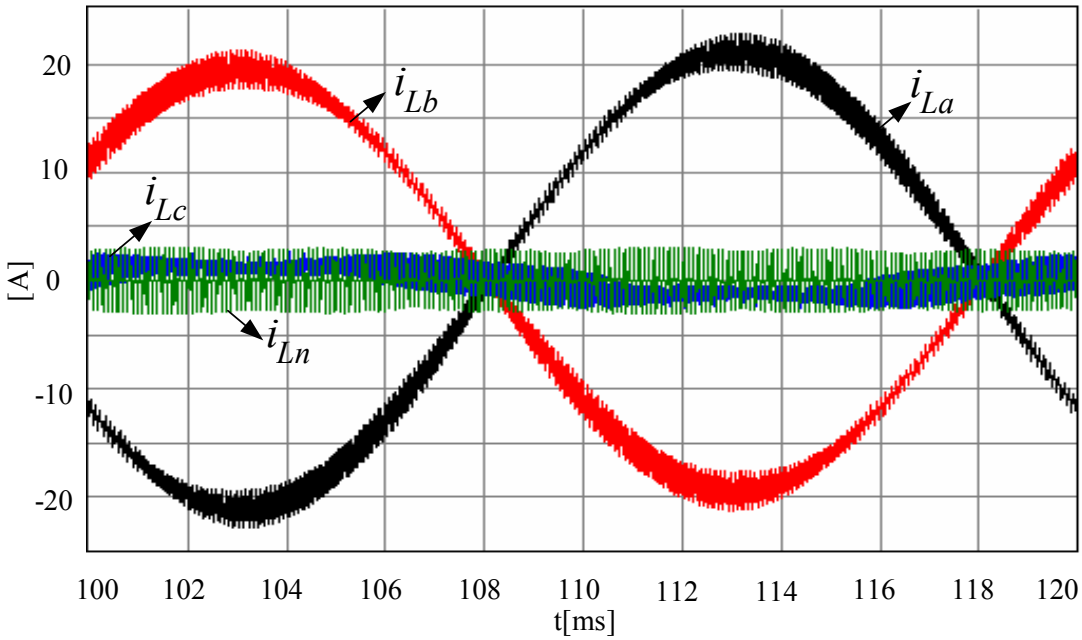


Figure 4.35 Steady-state inductor currents during closed-loop operation under linear line-line unbalanced full-load operating condition.

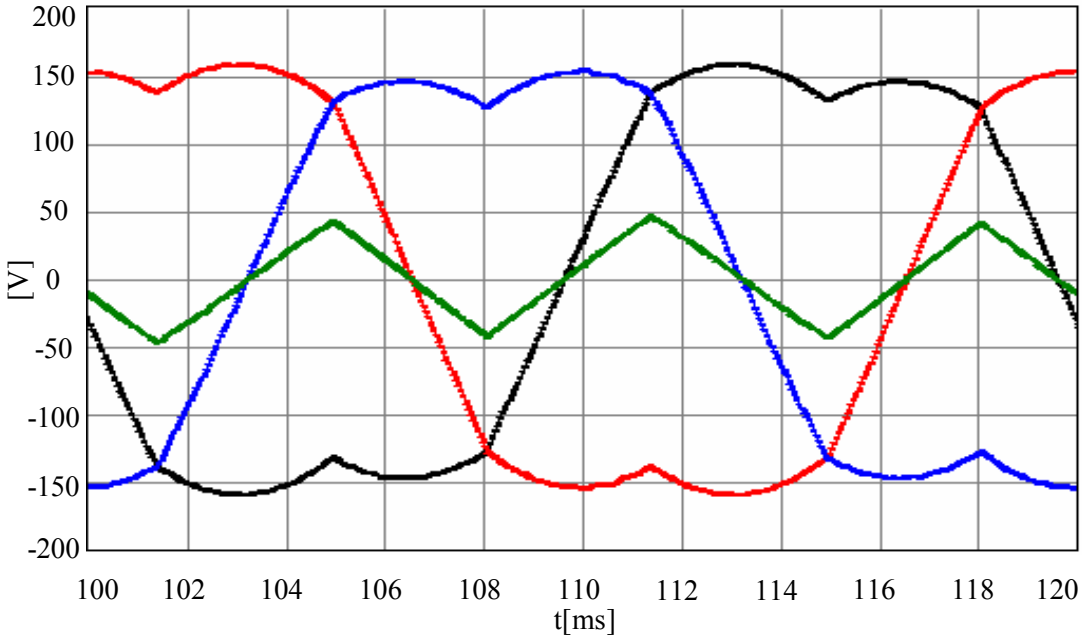


Figure 4.36 Steady-state modulation signals during closed-loop operation under linear line-line unbalanced full-load operating condition.

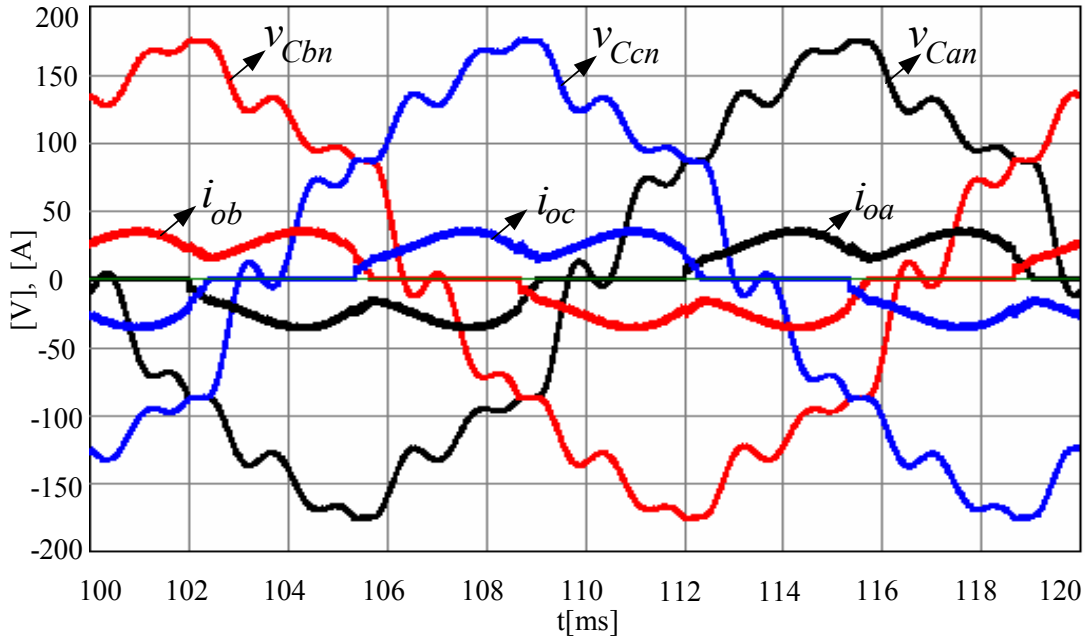


Figure 4.37 Steady-state output voltages and load currents (scale: x2.5) during open-loop operation under nonlinear balanced full-load operating condition.

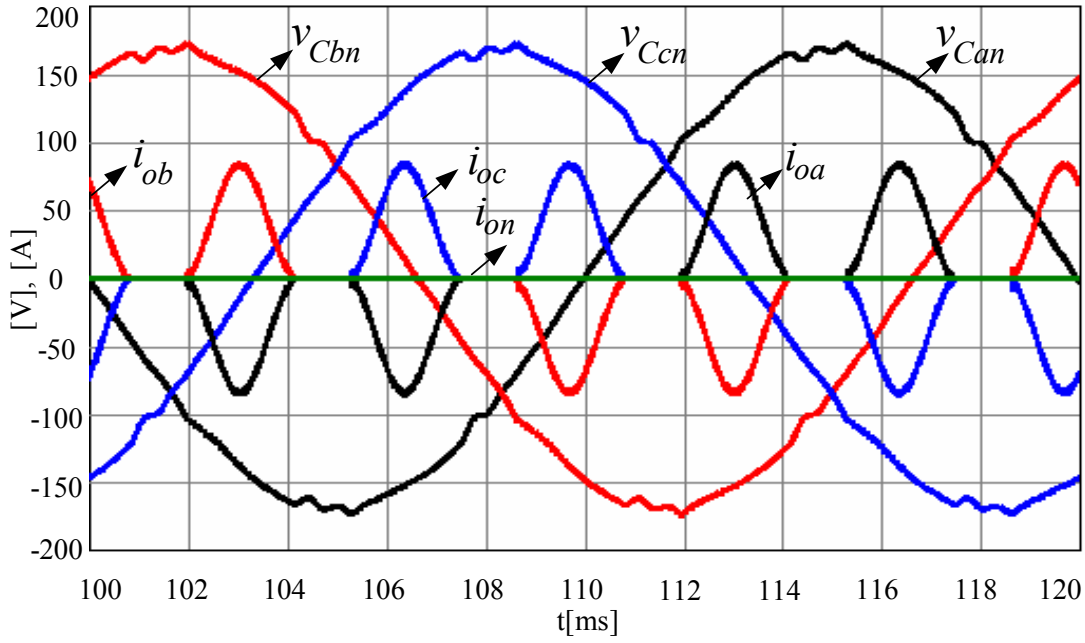


Figure 4.38 Steady-state output voltages and load currents (scale: x2.5) during closed-loop operation under nonlinear balanced full-load operating condition.

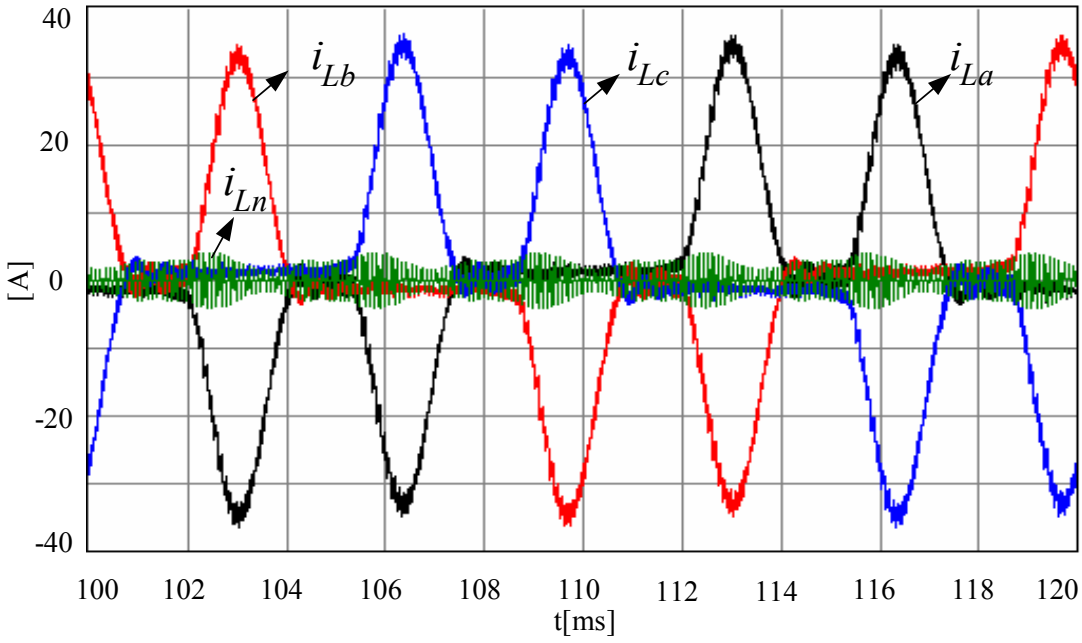


Figure 4.39 Steady-state inductor currents during closed-loop operation under nonlinear balanced full-load operating condition.

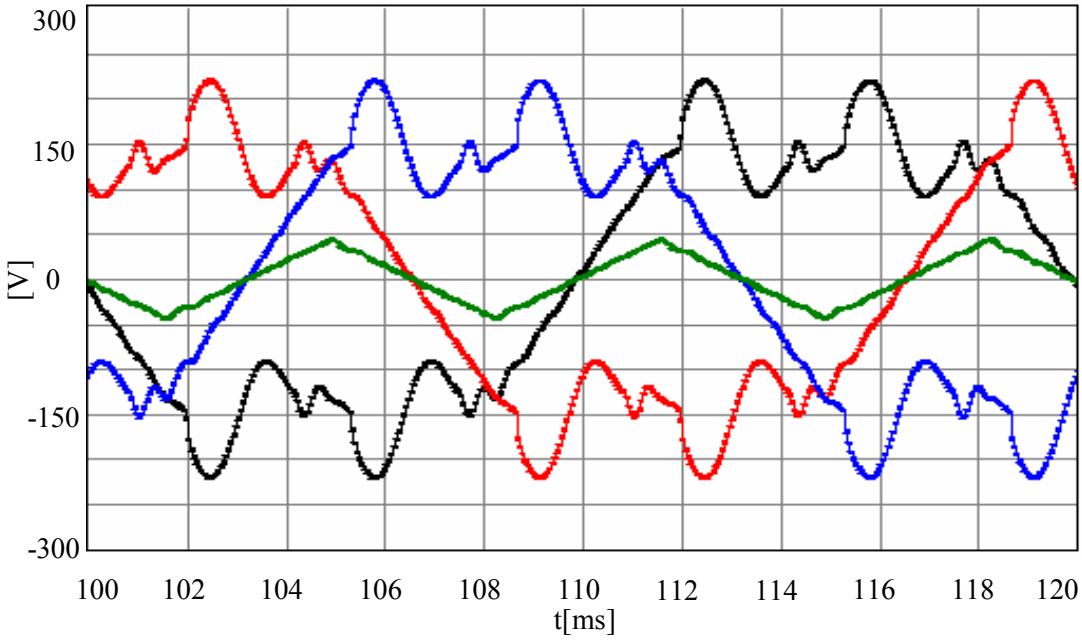


Figure 4.40 Steady-state modulation signals during closed-loop operation under nonlinear balanced full-load operating condition.

The waveforms for the single-phase nonlinear unbalanced load operation with open loop and closed loop control are shown in Figure 4.41 through Figure 4.44. As can be seen from the output voltage and current waveforms in Figure 4.41, the distortion is significant and the voltage regulation is quite poor. The closed loop control highly improves the output voltage and as a consequence the load current waveform becomes sharper as shown in Figure 4.42. As Figure 4.43 illustrates the single-phase unbalance current comes from the fourth leg. Finally, as Figure 4.44 shows, the modulation signals are highly distorted and the zero sequence signal is large and involves a lower frequency component than the three times the output voltage fundamental frequency.

For the line to line unbalanced full load case the open loop control operation waveforms are given in Figure 4.45 through Figure 4.48. As Figure 4.45 shows, the open loop operation results in poor output voltage regulation and quality. The closed loop controller restores the output voltage waveform quality and regulation as shown in Figure 4.46. The current becomes sharper and the crest factor increases. The inductor currents are similar to the load currents as shown in Figure 4.47, so that the capacitor voltage is not distorted via the load current harmonics. As shown in Figure 4.48 the modulation signals are distorted for the active phases, but the fourth leg modulation signal is the same as the linear unbalanced case as this leg carries no load current.

It can be concluded from these studies that the high performance output voltage controller involving resonant filter banks provides satisfactory performance over a wide range of loads. The output voltage regulation and waveform quality are within the high performance UPS standard values. Thus, it can be stated that the method helps the practical UPS approximate the ideal UPS which has zero internal impedance and ideal internal voltage which equals the rated voltage under all operating conditions.

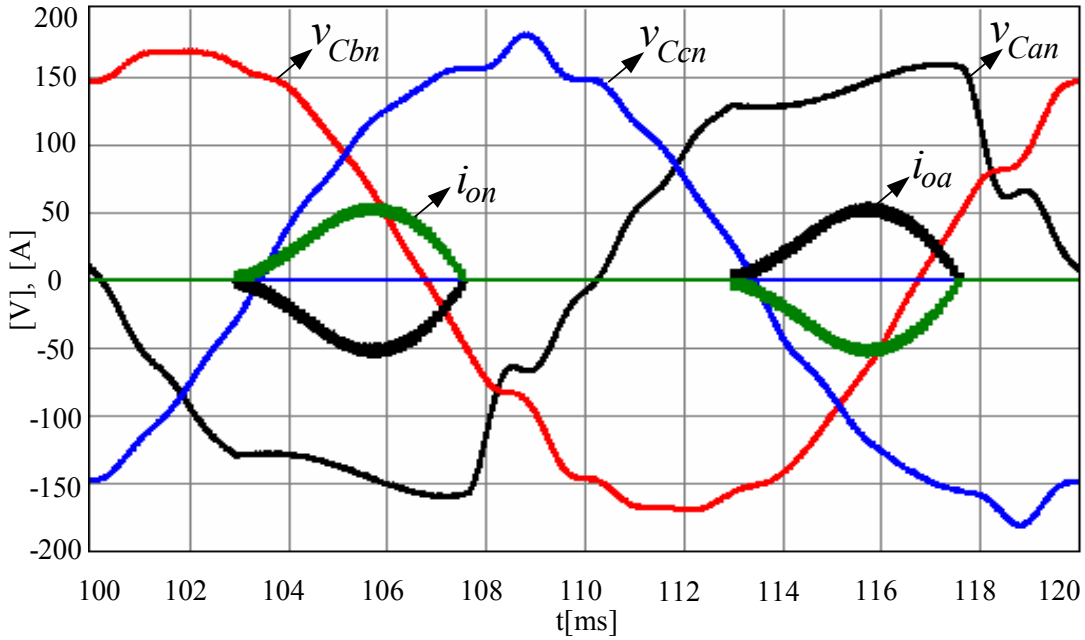


Figure 4.41 Steady-state output voltages and load currents (scale: x2.5) during open-loop operation under nonlinear line-neutral unbalanced full-load operating condition.

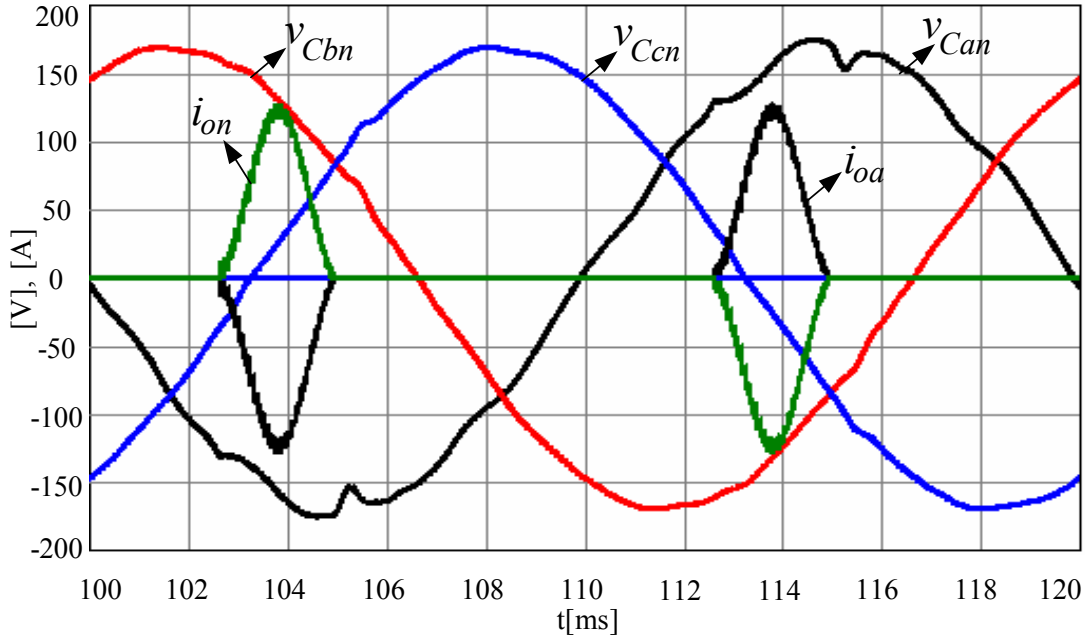


Figure 4.42 Steady-state output voltages and load currents (scale: x2.5) during closed-loop operation under nonlinear line-neutral unbalanced full-load operating condition.

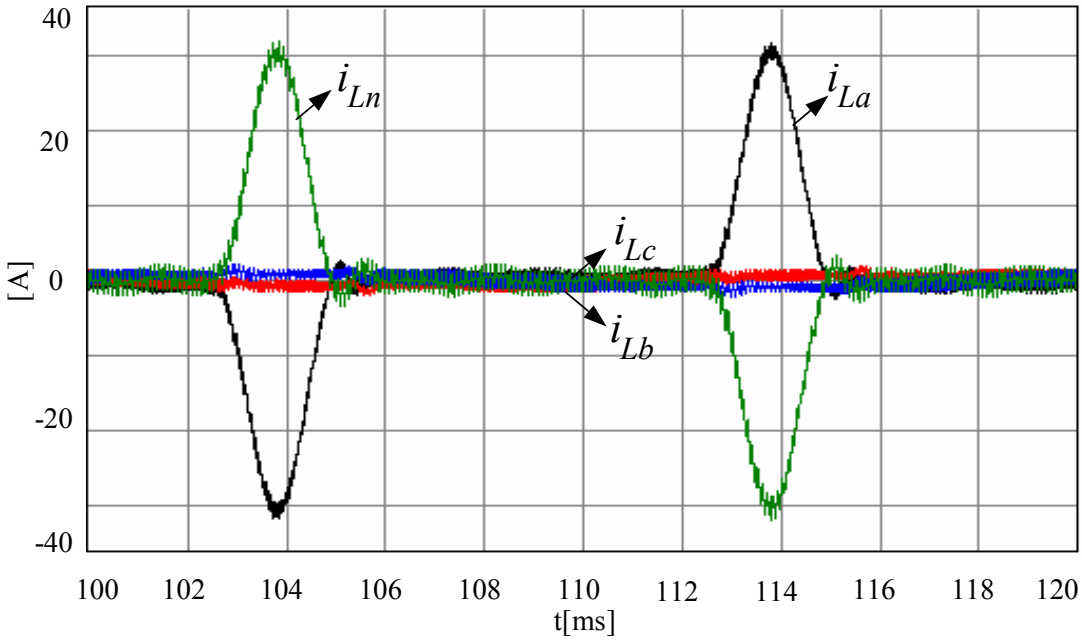


Figure 4.43 Steady-state inductor currents during closed-loop operation under nonlinear line-neutral unbalanced full-load operating condition.

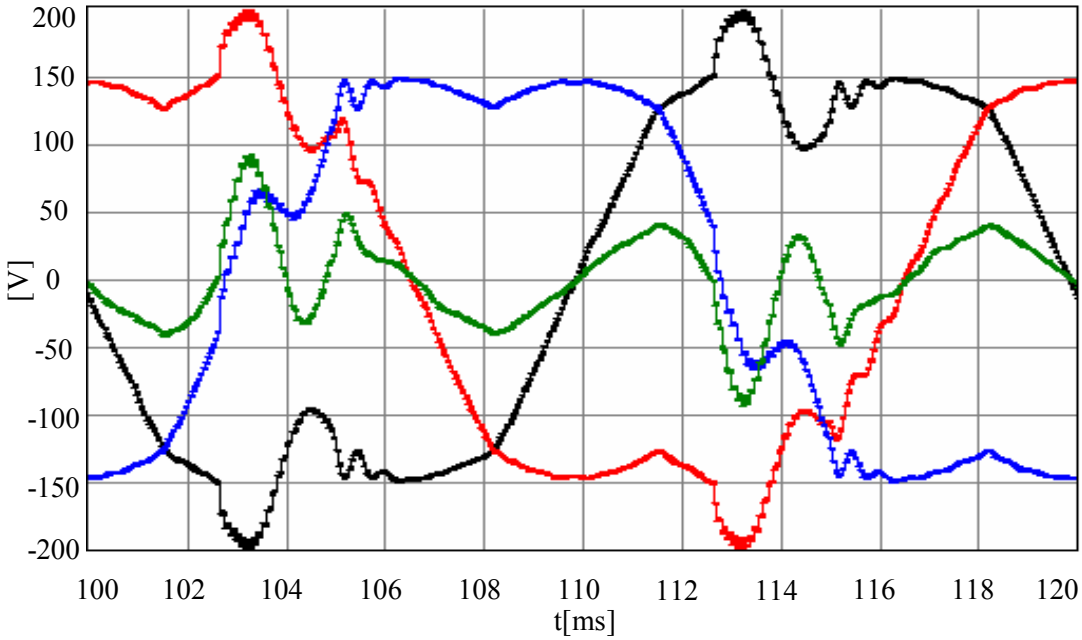


FİGure 4.44 Steady-state modulation signals during closed-loop operation under nonlinear line-neutral unbalanced full-load operating condition.

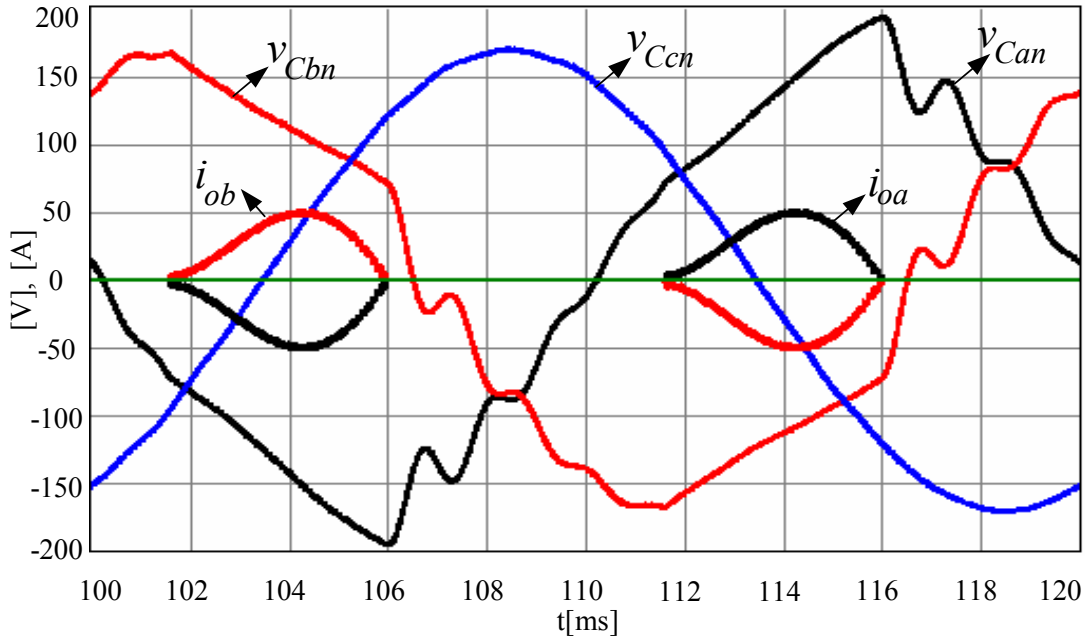


Figure 4.45 Steady-state output voltages and load currents (scale: x2.5) during open-loop operation under nonlinear line-line unbalanced full-load operating condition.

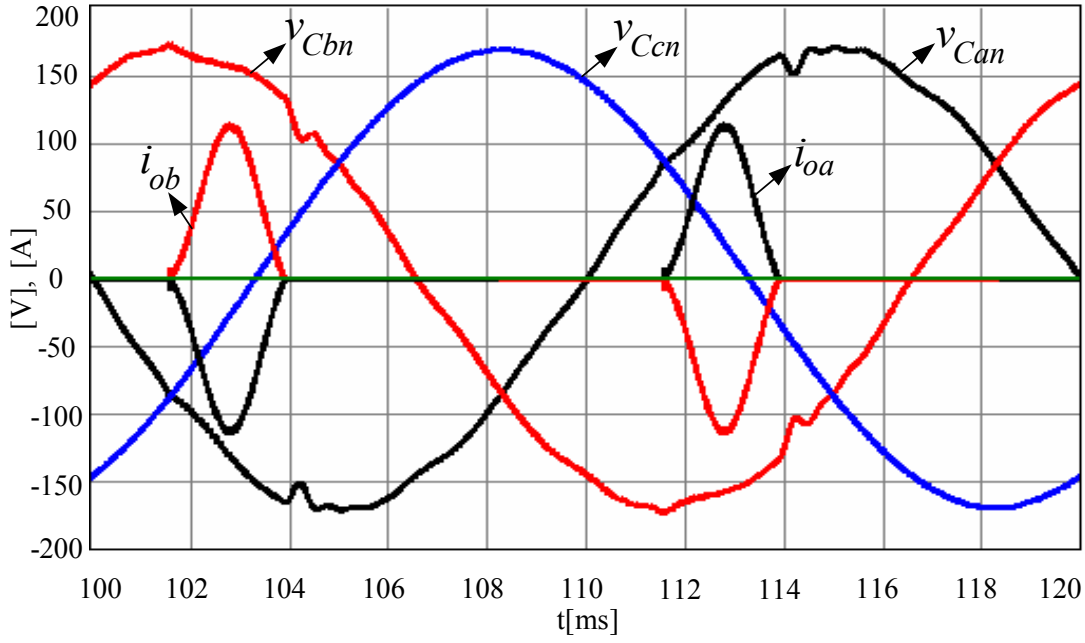


Figure 4.46 Steady-state output voltages and load currents (scale: x2.5) during closed-loop operation under nonlinear line-line unbalanced full-load operating condition.

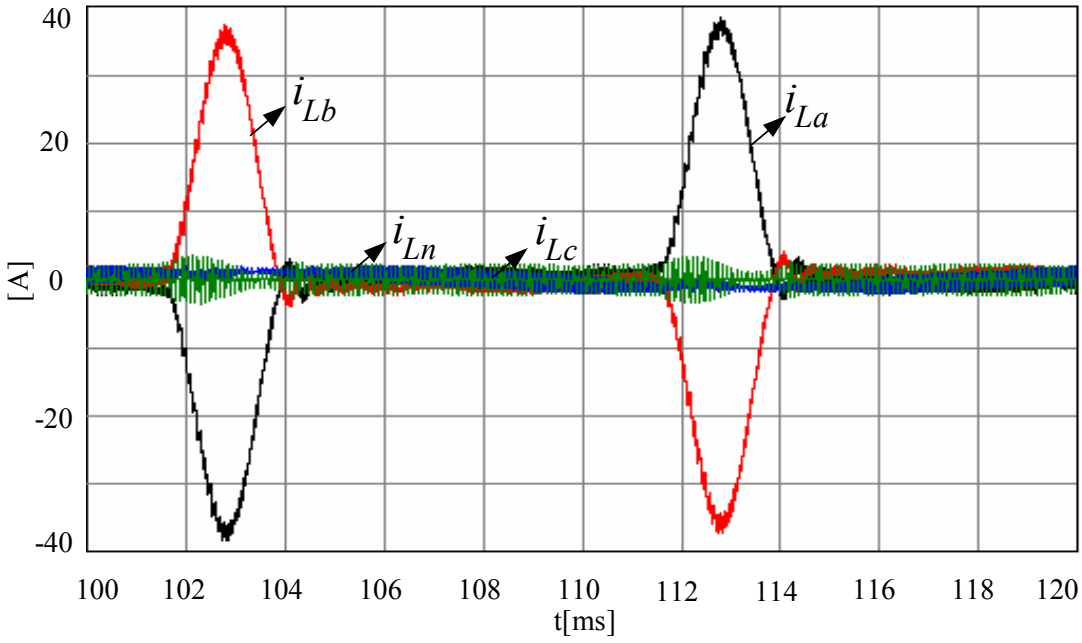


Figure 4.47 Steady-state inductor currents during closed-loop operation under nonlinear line-line unbalanced full-load operating condition.

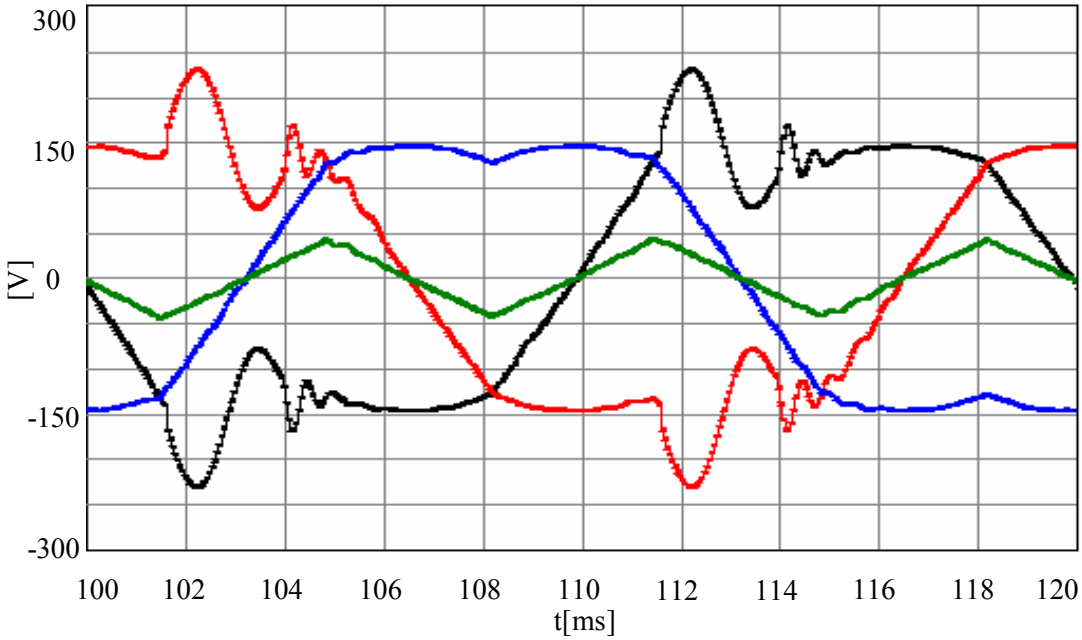


Figure 4.48 Steady-state modulation signals during open-loop operation under nonlinear line-line unbalanced full-load operating condition.

4.3.3. Dynamic Performance Investigation of The Four-Leg Inverter Based Three-Phase UPS System By Means of Computer Simulations

One important performance indicator of UPS systems is the response to impact loading. During sudden loading transients the load current is mostly drawn from the output capacitors and therefore the output voltage dips significantly and fails to follow the command. In an ideal UPS the output voltages during and after the loading instants are unaffected by loading and closely follow the reference voltage. In a practical UPS the amount of voltage dip and the duration of the sag should be relatively small. Similar to a sag condition excited by a loading transient, a surge condition may occur during load removal transients and in this case the voltage surge and duration must be negligible. In a high performance UPS, the output voltage is controlled with a high bandwidth controller such that the loading transient based disturbances are rejected by the controller. In this section, the loading transients of the developed UPS control system will be tested and the influence of each controller on the dynamic performance of the UPS will be identified by means of computer simulations.

The worst case loading dynamics occur under resistive loading and specifically when the loading transient is started at the maximum voltage level of the output voltage. Since the resistive load draws current with the same shape as the voltage, when a resistive load is connected to the UPS at the peak of the output voltage, then maximum load current is drawn and the UPS output voltage experiences a large dip instantaneously. For this reason, the dynamic performance test of the developed controller will be conducted in the following: while the UPS is operating at no-load at steady-state, a three-phase resistive rated load will be switched on. In the three-phase system one of the phases is observed and the switching instant is selected to be the instant where this phase voltage is the peak value. Then, the output voltage and the current of this phase will be observed along its capacitor and inverter current. The resulting voltage dip, the settling time, and the approximate volt-seconds lost will be reported.

In order to illustrate the effect of each control component of the resonant filter bank based controller developed in the previous chapter and shown in Figure 3.19, computer simulations will be conducted for various controller component combinations and the results will be interpreted. Table 4.7 shows the controller combinations investigated and the voltage dip, settling time, and lost volt-seconds. The control gains as shown in the table are the same as those finalized in section 4.3.1 Stage IX.

Based on the data on Table 4.7, and the waveform of Figure 4.49, it can be seen that the open loop dynamic performance is poor as the dip is 88V (nearly 50%) and the settling time is longer than a millisecond. From the table it can also be seen all controller combinations without active damping (cases 2 to 8) provide small incremental improvement in the dynamic performance. While the harmonic compensators provide a small reduction in the settling time, they increase the output voltage oscillations noticeably. The proportional gain provides marginal reduction in the oscillations. The fundamental component controller does not have any notable influence on the dynamic performance as the duration of the dynamics is too small compared to the fundamental cycle. With all the controllers included except for the active damping controller, the voltage and current waveforms are shown in Figure 4.50. It can be seen that the inverter current responds slowly to the loading transient and the capacitor current is large, resulting in a deep and long sag in the output voltage.

With the active damping loop enabled but all other controllers disabled, the dynamic test gives significantly better results compared to the first 8 cases. This is case 9 in the table and it is shown in Figure 4.51 in detail. In this case, the voltage dip decreases by about 25% and therefore the lost volt-seconds improve by the same amount. This is due to the direct effect of the active damping loop. The increase in the load current is compensated by the inverter (rather than the capacitor) via the active damping loop. However, the compensation is not instantaneous. The capacitor current is measured with a delay (approximately 40μs), the controller computes the active damping term (50μs) and the PWM pulse pattern is generated and becomes

effective with an average delay of (25μs). This total delay of approximately 115μs is the response time of the active damping loop. This implies the active damping loop is ineffective within the first 110μs. During this time the voltage dip occurs. However once the inverter responds, the inverter takes charge and increases the inductor current to match the load current such that the capacitor voltage will not further dip. With the active damping loop being enabled, if the other controllers are activated the controller that has any significant influence on the dynamic performance is the proportional gain. As cases 10 to 16 in Table 4.7 show, the proportional gain improves the settling time noticeably (from 1.1ms to 0.79ms). The waveform for this case is shown in Figure 4.52. The other controllers have marginal influence and when all are present (case 16, Figure 4.53) the total lost volt-seconds is 20mVs which is less than half of the open-loop case (46.2mVs).

The above computer simulation based investigations illustrate that the active damping loop is vital for the dynamic performance of the UPS. Not only the steady-state waveforms improve, the controller gains can be increased due to enhanced stability, but the impact loading transients can be efficiently manipulated. Thus, a high UPS performance with very small lost volt-seconds during loading transients can be achieved.

Table 4.7 Influence of controller components on the UPS dynamic performance

	Fundamental controller		Harmonic components	K_{ad}	Δt (ms)	ΔV (V)	∫vdt (V·ms)
	K_{iv}	K_{pv}					
Case 1	0	0.00	Uncontrolled	0.00	1.05	88	46.2
Case 2	0	0.00	Controlled	0.00	1.0	88	44.0
Case 3	100	0.00	Uncontrolled	0.00	1.05	88.5	46.46
Case 4	100	0.00	Controlled	0.00	1.0	88	44.0
Case 5	0	0.05	Uncontrolled	0.00	1.07	85	45.48
Case 6	0	0.05	Controlled	0.00	1.07	85	45.48
Case 7	100	0.05	Uncontrolled	0.00	1.09	83	45.235
Case 8	100	0.05	Controlled	0.00	1.08	83	43.2
Case 9	0	0.00	Uncontrolled	15.00	1.0	65	32.5
Case 10	0	0.00	Controlled	15.00	1.07	62.5	33.44
Case 11	100	0.00	Uncontrolled	15.00	1.1	67.5	37.12
Case 12	100	0.00	Controlled	15.00	1.1	70	38.5
Case 13	0	1.00	Uncontrolled	15.00	0.79	70	27.65
Case 14	0	1.00	Controlled	15.00	0.65	66.5	21.61
Case 15	100	1.00	Uncontrolled	15.00	0.65	69	22.43
Case 16	100	1.00	Controlled	15.00	0.58	69	20.0

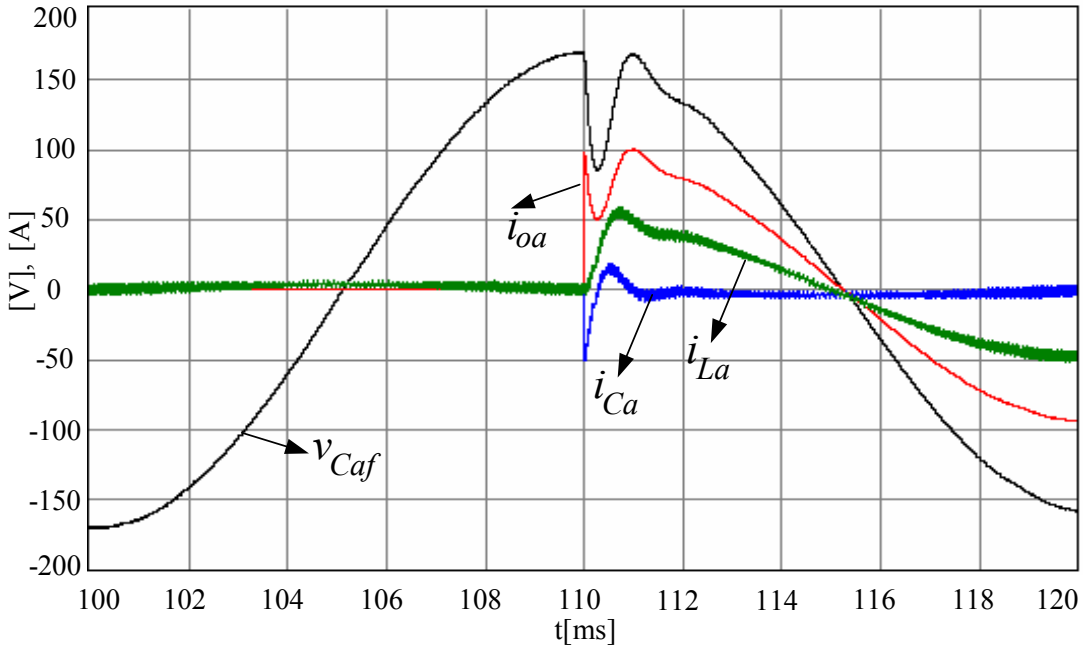


Figure 4.49 Output voltage (black), load current (red, x5), inductor current (green, x2.5), and capacitor current (blue, x2.5) waveforms of the open-loop controlled UPS during loading transient (Case 1 of Table 4.7).

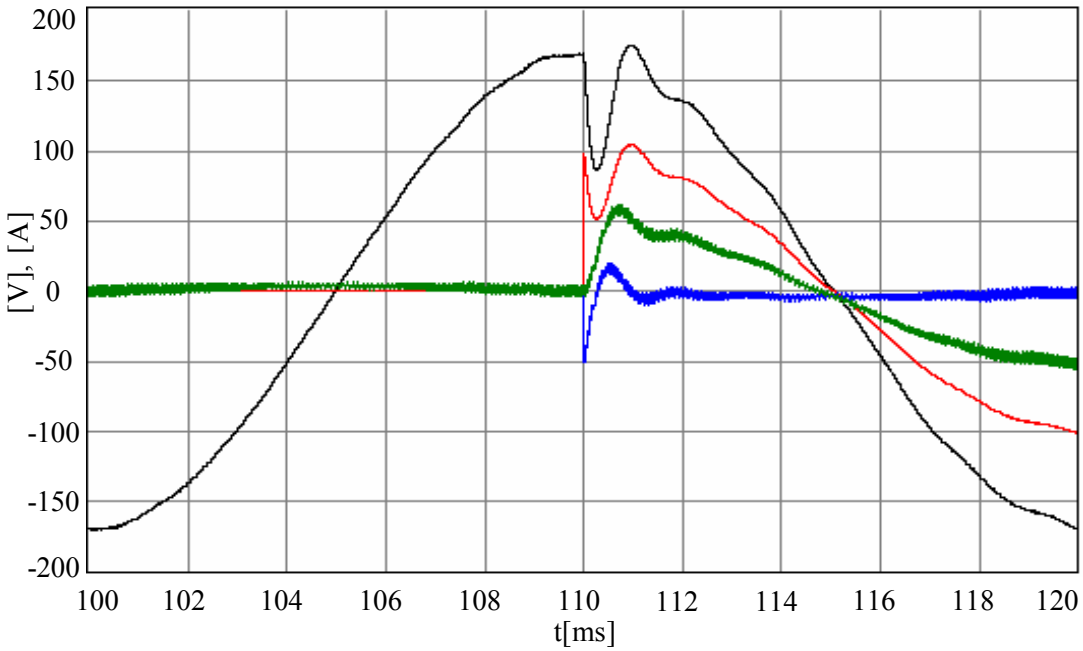


Figure 4.50 Output voltage (black), load current (red, x5), inductor current (green, x2.5), and capacitor current (blue, x2.5) waveforms of the closed-loop controlled UPS during loading transient (Case 8 of Table 4.7).

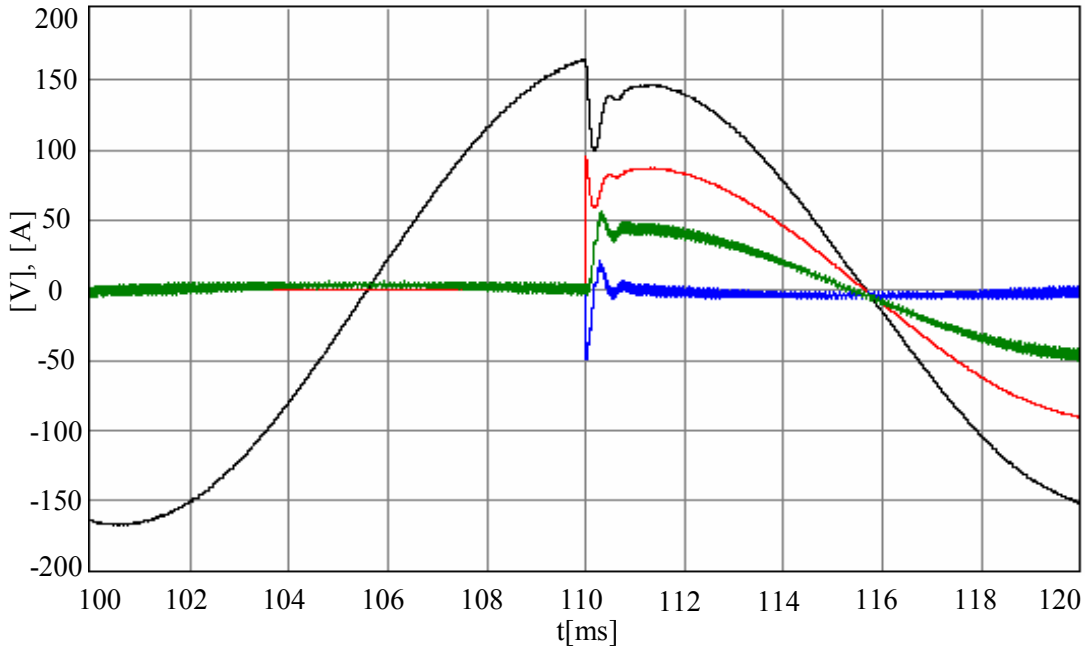


Figure 4.51 Output voltage (black), load current (red, x5), inductor current (green, x2.5), and capacitor current (blue, x2.5) waveforms of the closed-loop controlled UPS during loading transient (Case 9 of Table 4.7).

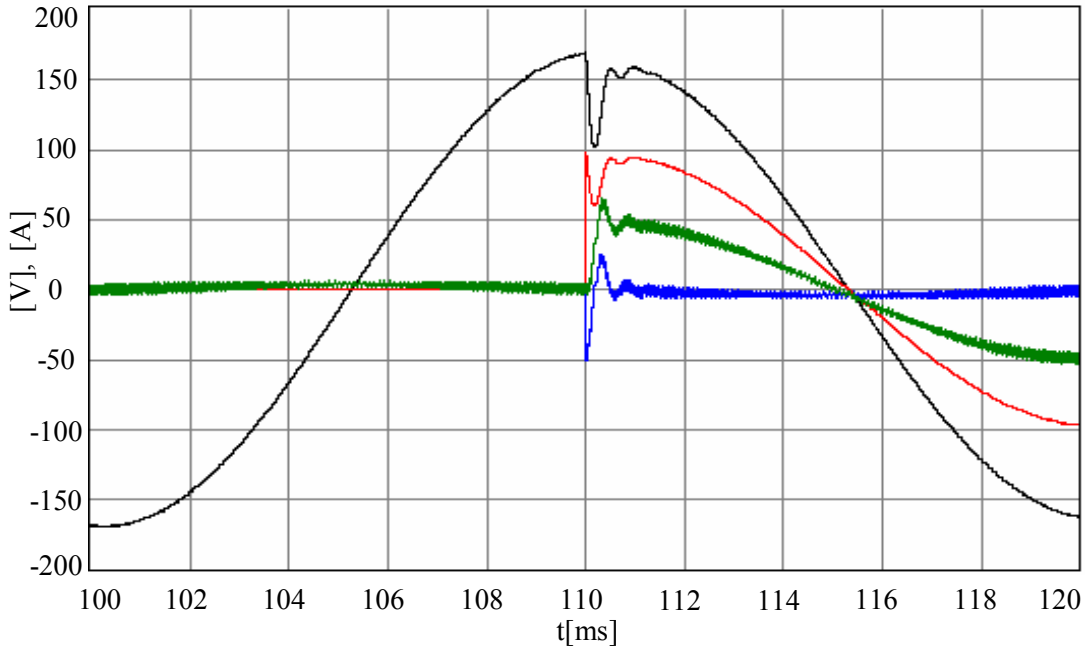


Figure 4.52 Output voltage (black), load current (red, x5), inductor current (green, x2.5), and capacitor current (blue, x2.5) waveforms of the closed-loop controlled UPS during loading transient (Case 13 of Table 4.7).

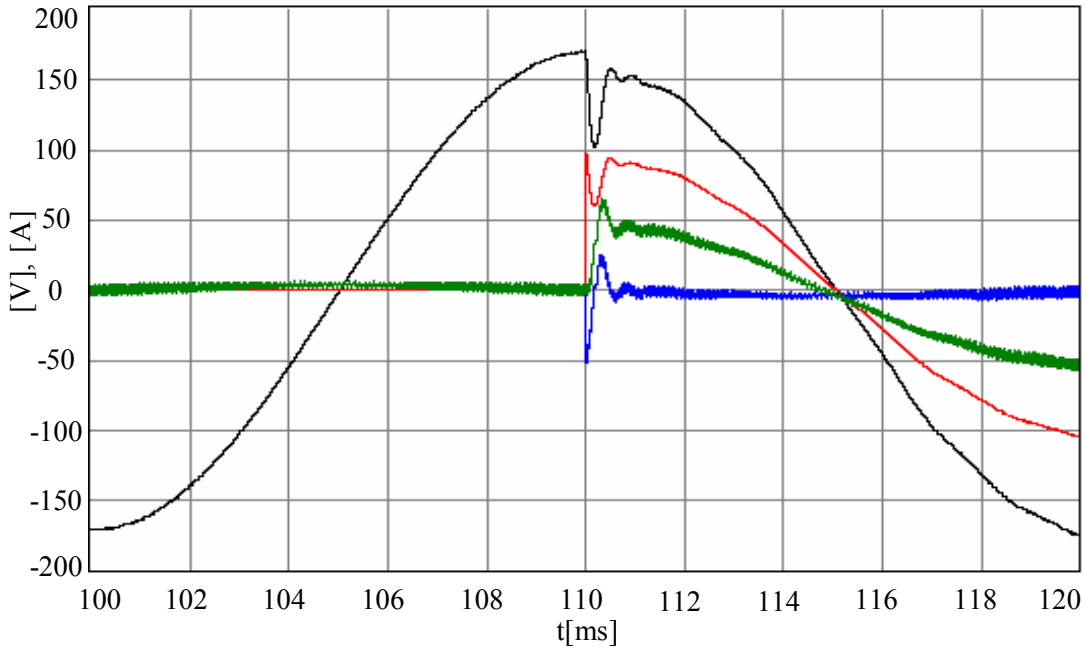


Figure 4.53 Output voltage (black), load current (red, x5), inductor current (green, x2.5), and capacitor current (blue, x2.5) waveforms of the closed-loop controlled UPS during loading transient (Case 16 of Table 4.7).

4.3.4. Investigation of Switching Ripple and Switching Loss Characteristics of Various PWM Methods

This section investigates the modulator switching ripple and loss characteristics for SVPWM, DPWM1, and MLDPWM. Based on the study results the modulator performances are evaluated and compared. The methods will be evaluated for linear balanced resistive and lagging power factor load cases, for line to neutral unbalanced linear resistive load, for nonlinear balanced and single-phase unbalanced load. For the linear resistive load case the full-load power operating condition is tested. For the linear inductive load the output kVA is kept at the rated value. For the nonlinear balanced and unbalanced loads, the power rating is half the UPS power rating.

Throughout the modulator performance studies closed loop control is involved and the high performance resonant filter controller structure shown in Figure 3.19 is

utilized. The controller coefficients are the same as those of Stage IX of Table 4.5. The carrier frequency is 20 kHz and the sampling rate is also the same as the carrier frequency (single update mode). This is done for the purpose of meeting an experimental constraint to be discussed in the next chapter.

In the study first the balanced load operating conditions are considered and modulators are compared in terms of their switching ripple and losses. Then single-phase loading, in other words, the line-to-neutral unbalanced loading case is considered. Both linear and nonlinear load cases given in section 4.2 will be considered. The aim of this study is to illustrate the loss mechanism of each modulator and show the significant differences between MLDPWM and other modulators.

Figure 4.54 through Figure 4.57 show the SVPWM performance under full resistive balanced load. As the inductor currents shown in Figure 4.56 illustrate the PWM ripple current is small for the normal phases and slightly larger for the fourth leg. All the switches are commutated periodically (Figure 4.57) resulting in an average switching frequency equal to the PWM frequency. Operating the UPS under the same conditions but only changing the modulation scheme from SVPWM to DPWM1, the ripple and switching losses change considerably. The waveforms for this operating condition are shown in Figure 4.58, Figure 4.59, and Figure 4.60. As Figure 4.58 shows the DPWM1 modulation waves indicate that commutations will be discontinuous. This affects the locked phase inductor currents (Figure 4.59). The phase that ceases commutation has larger ripple which is nearly the same as the fourth leg ripple current. Figure 4.60 shows that each phase is locked to the DC rail for a total of 120° so that the switching losses are reduced. In this case, since the load is resistive, the inverter load (consisting of the UPS load and capacitive filter) power factor is near unity and the switching losses of the phase legs decrease to the minimum possible value. For this operating condition DPWM1 and MLDPWM have the same performance as was discussed in the second chapter. Therefore, waveforms for MLDPWM will not be shown.

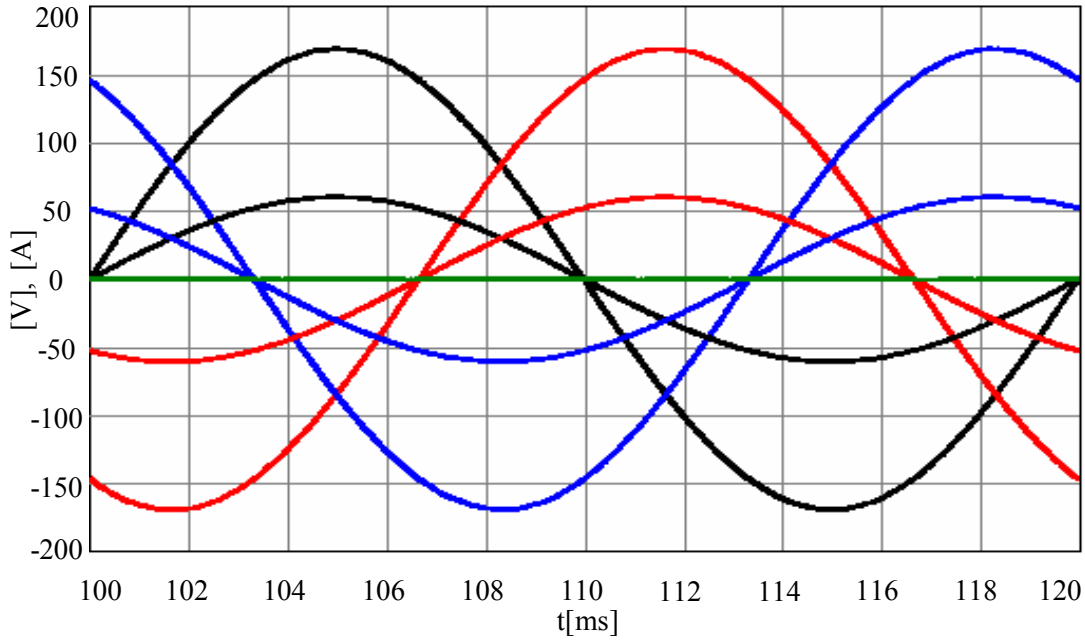


Figure 4.54 Steady-state three-phase output voltages and load currents (scale: x3) during SVPWM operation under linear balanced full-load.

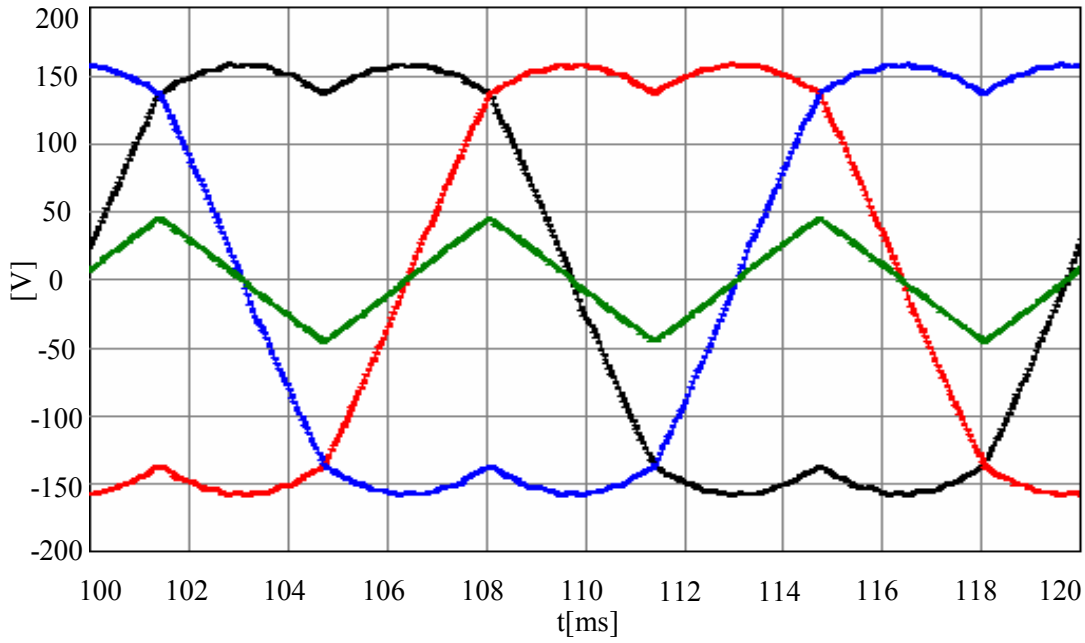


Figure 4.55 Steady-state modulation signals during SVPWM operation under linear balanced load.

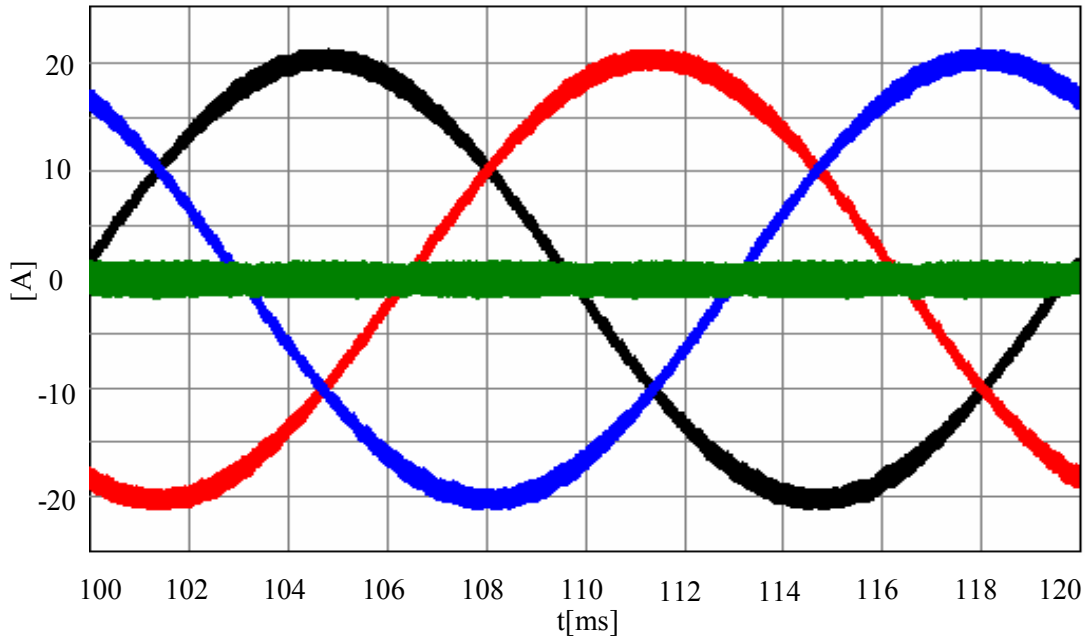


Figure 4.56 Steady-state inverter output currents during SVPWM operation under linear balanced load.

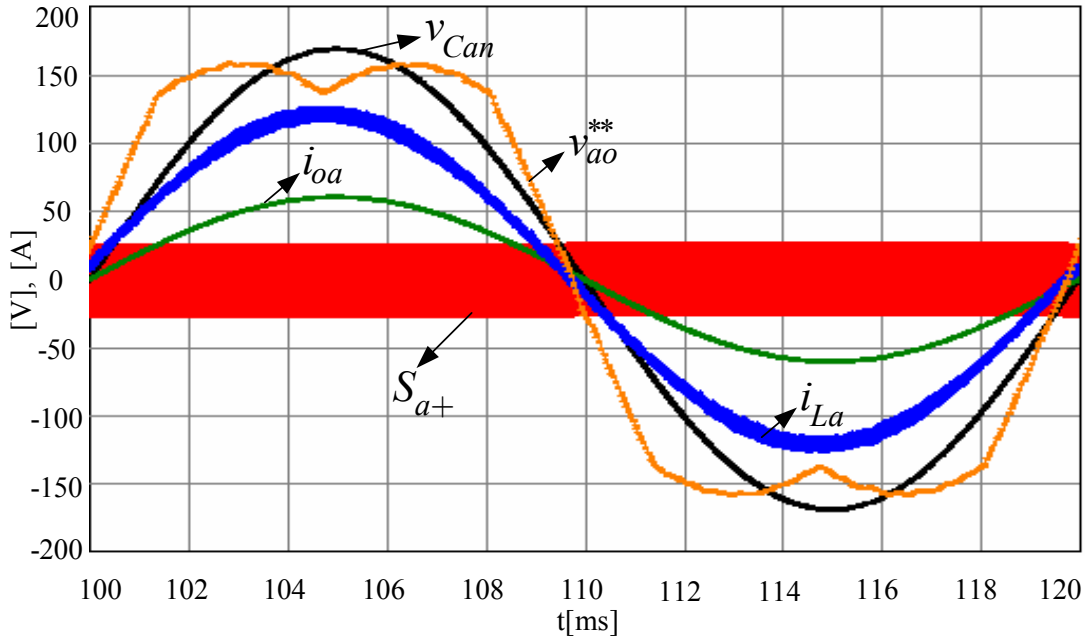


Figure 4.57 Steady-state output voltage (black), modulation signal (orange), load current (green, x3), inductor current (blue, x6), switch signal (red, x0.1) during SVPWM operation under linear balanced load.

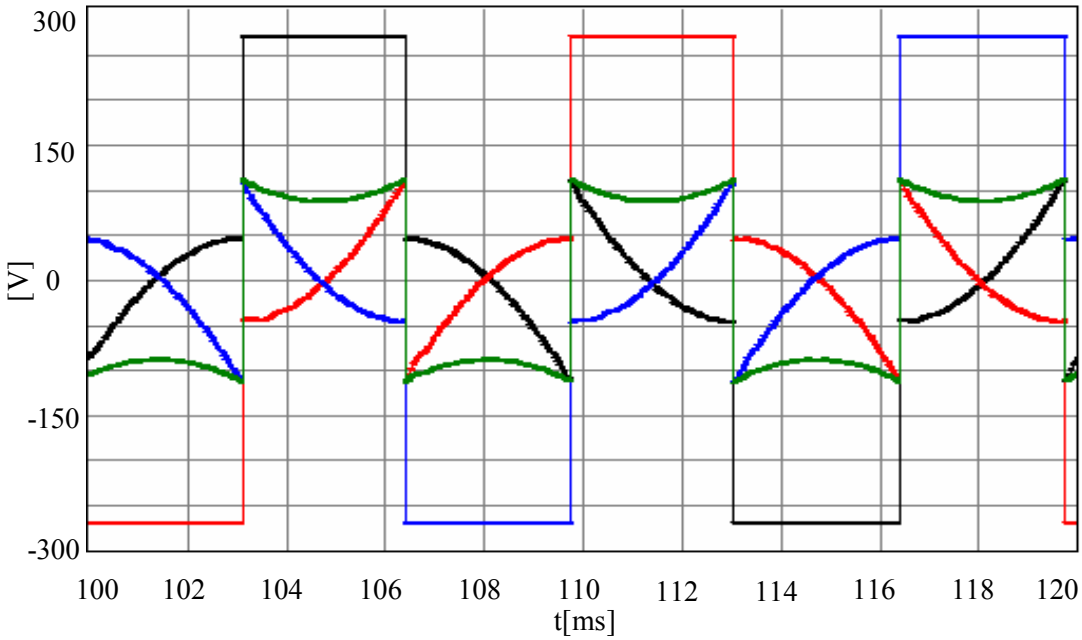


Figure 4.58 Steady-state modulation signals during DPWM1 operation under linear balanced load.

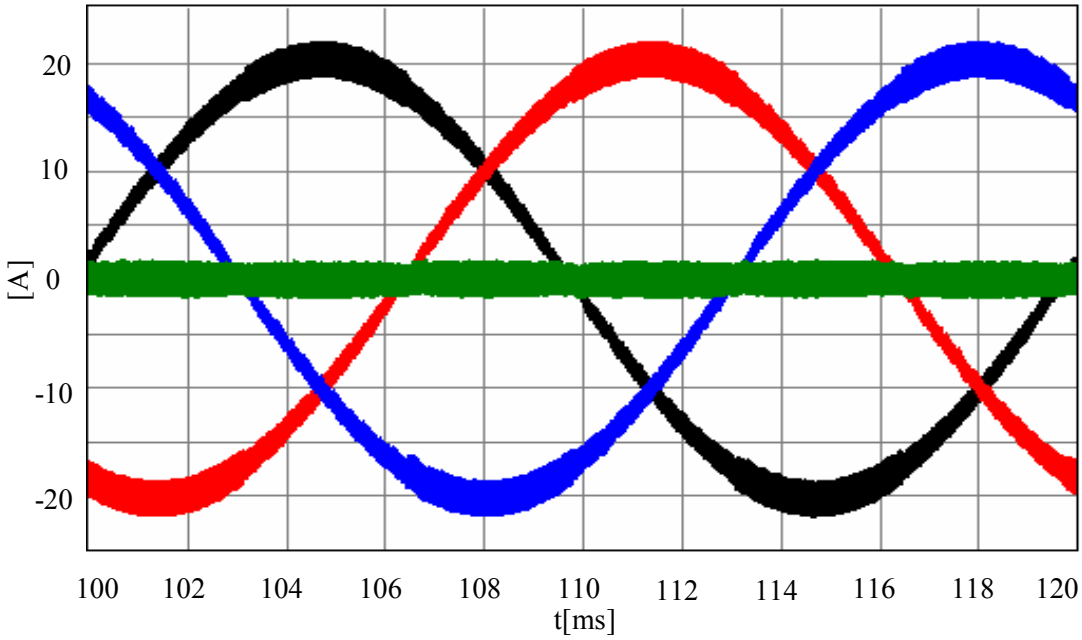


Figure 4.59 Steady-state inverter output currents during DPWM1 operation under linear balanced load.

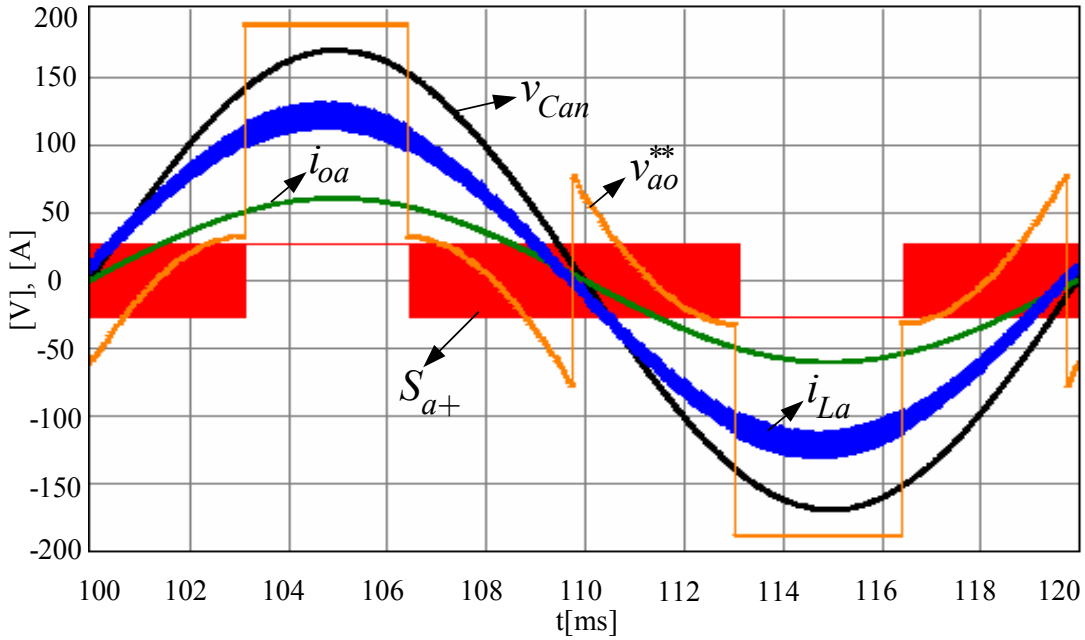


Figure 4.60 Steady-state output voltage (black), modulation signal (orange, x0.7), load current (green, x3), inductor current (blue, x6), switch signal (red, x0.1) during DPWM1 operation under linear balanced load.

Next, the 0.8 lagging power factor balanced RL load operating condition is considered. Since SVPWM performs the same regardless the power factor angle, the carrier frequency and the average switching frequency remain the same. Thus the losses are independent of the load power factor in SVPWM. The ripple is also independent of the power factor for SVPWM. Therefore, waveforms for this case are not illustrated. Performance characteristics of the DPWM1 and MLDPWM methods are evaluated at linear balanced inductive load condition and the waveforms in Figure 4.61 through Figure 4.64 show the DPWM1 performance under inductive balanced load. The load currents lag the output voltages by approximately 37^{o} (Figure 4.61). As shown in Figure 4.62, the DPWM1 modulation waves have the same shape as in the balanced resistive load condition. The inductor current is not aligned with the output voltage. And as a consequence, the $2x60^{o}$ segments in which the currents are maximum and the $2x60^{o}$ segments in which the current ripple is maximum are phase shifted by the power factor angle (Figure 4.63, Figure 4.64). Since the inverter leg with the largest current is not clamped to the DC rail for some

intervals, in this method the switching losses are not minimal, except for the unity power factor case. On the other hand, the MLDPWM selects the phase with the largest current and it decreases the switching power loss under lagging power factor load condition. Figure 4.65 shows the MLDPWM modulation waves. Comparing Figure 4.62 and Figure 4.65, the discontinuity regions are shifted to right with displacement angle for MLDPWM. Shifting the discontinuity region causes the switching ripple to appear at the larger values of the inverter output current as illustrated in Figure 4.66. Since commutation ceases at the larger values of the inverter output current (Figure 4.67), switching losses are reduced substantially. Therefore MLDPWM is a method performing in the same manner as the generalized discontinuous PWM method proposed in [31] for the three-leg inverter.

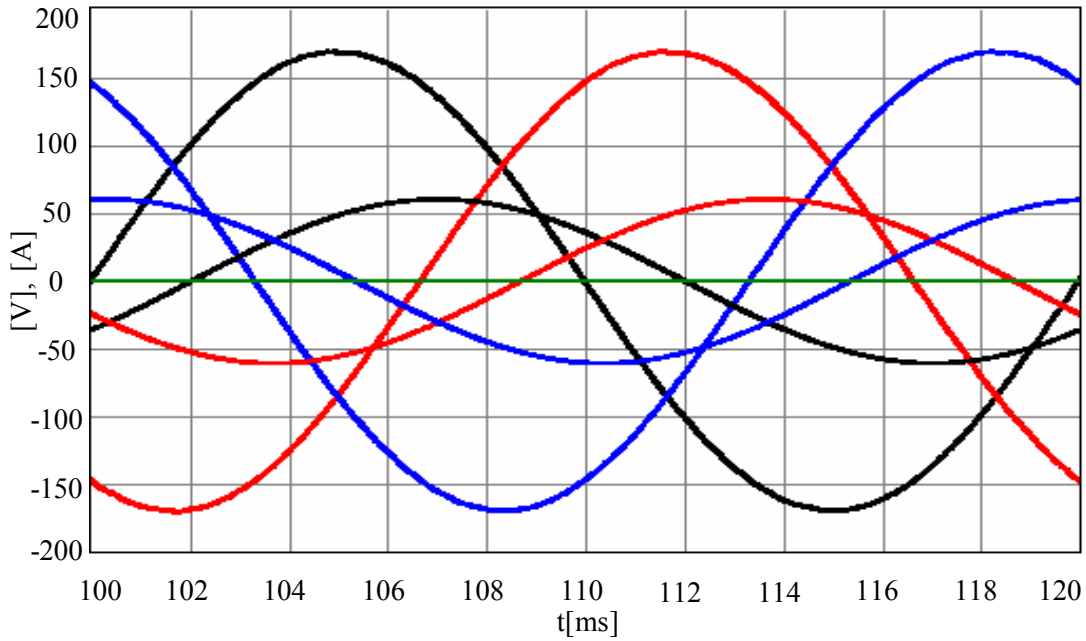


Figure 4.61 Steady-state three-phase output voltages and load currents (scale: x3) during DPWM1 operation under linear balanced inductive load (PF=0.8).

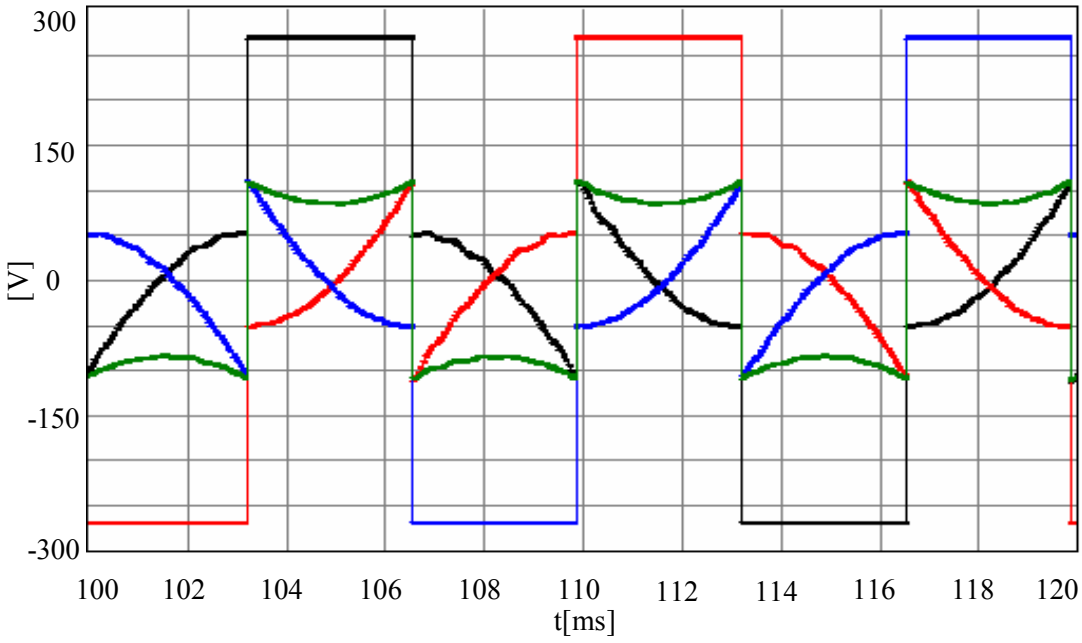


Figure 4.62 Steady-state modulation signals during DPWM1 operation under linear balanced inductive load (PF=0.8).

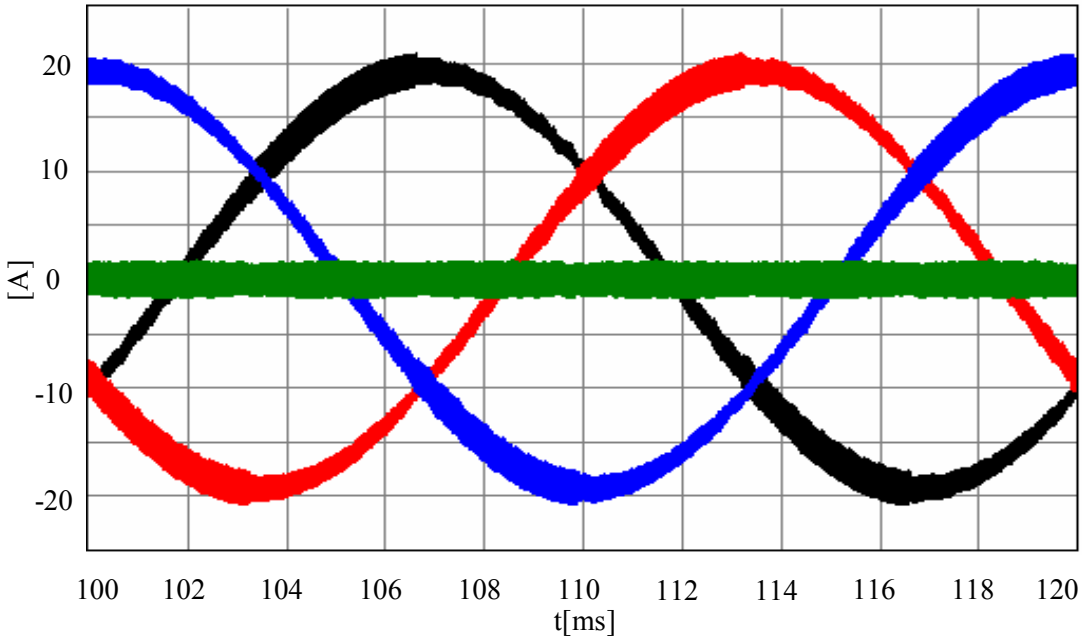


Figure 4.63 Steady-state inverter output currents during DPWM1 operation under linear balanced inductive load (PF=0.8).

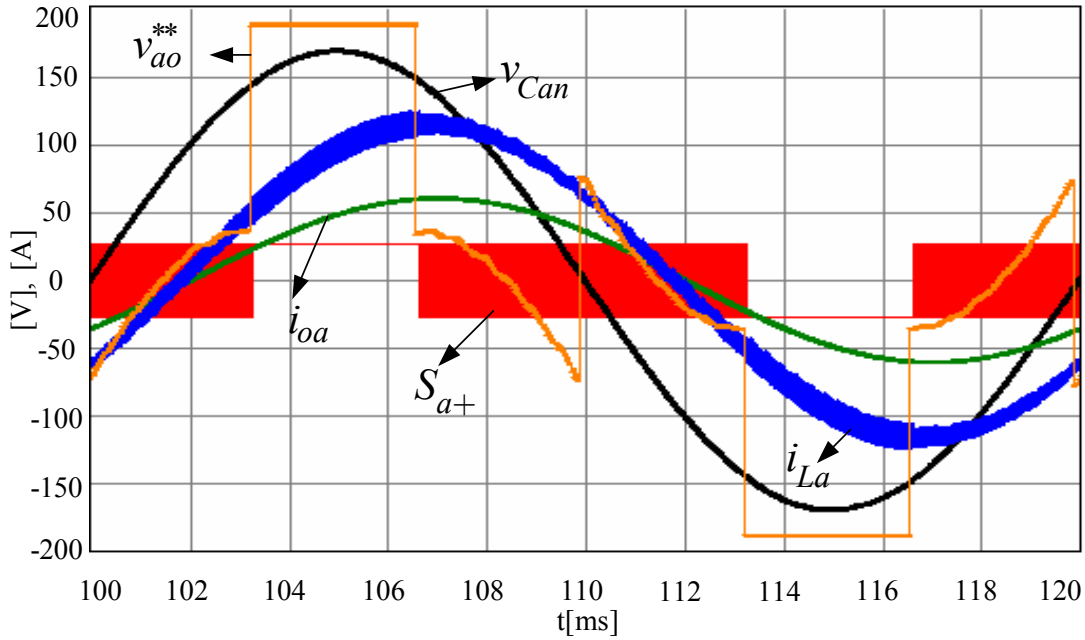


Figure 4.64 Steady-state output voltage (black), modulation signal (orange, x0.7), load current (green, x3), inductor current (blue, x6), switch signal (red, x0.1) during DPWM1 operation under linear balanced inductive load (PF=0.8).

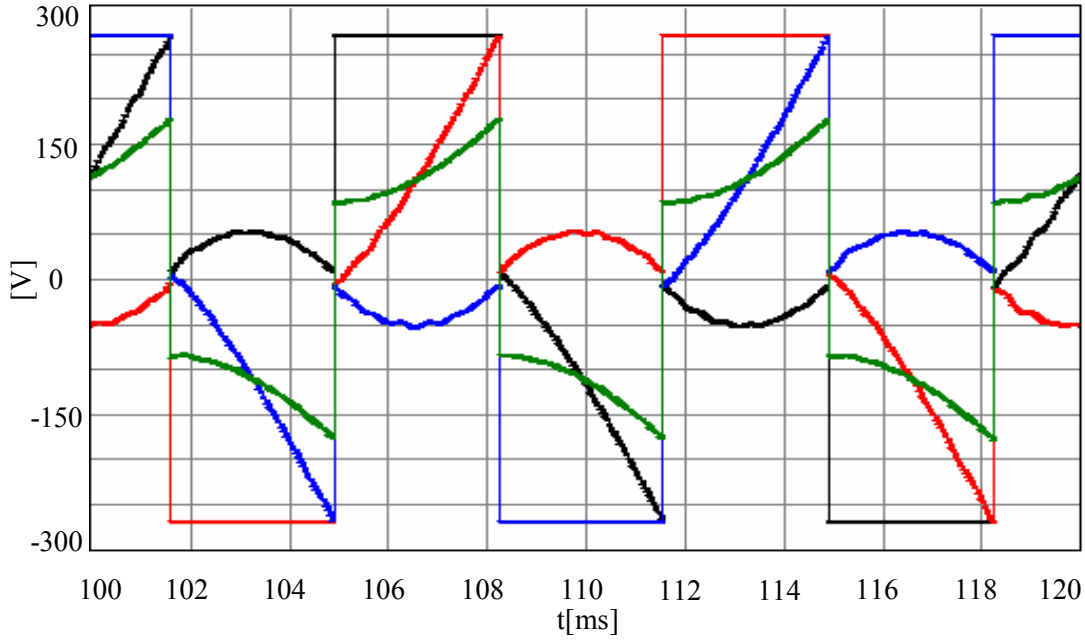


Figure 4.65 Steady-state modulation signals during MLDPWM operation under linear balanced inductive load (PF=0.8).

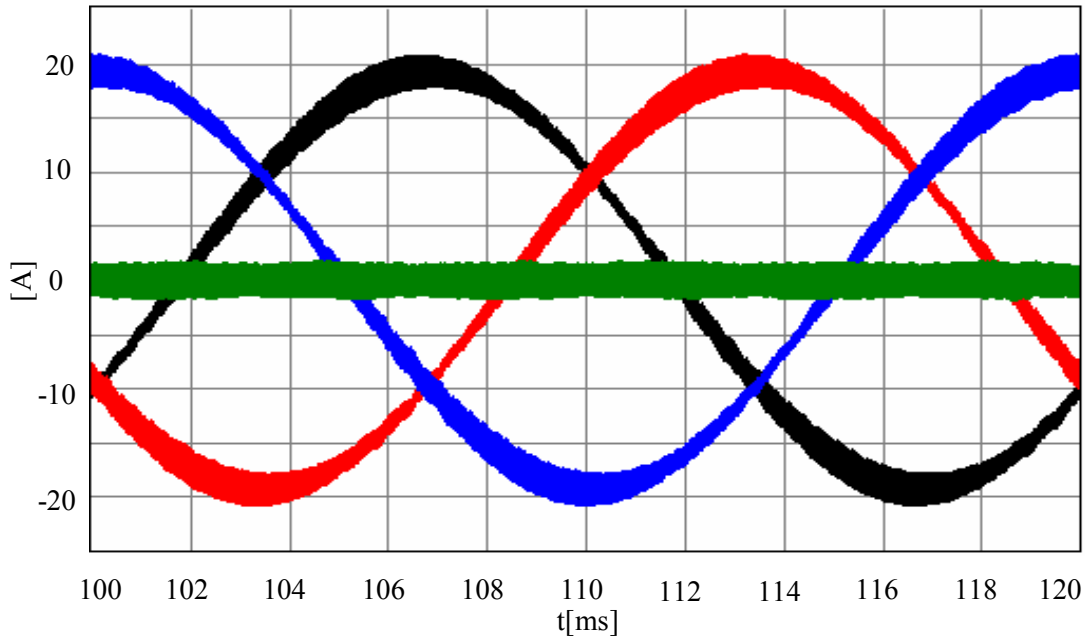


Figure 4.66 Steady-state inverter output currents during MLDPWM operation under linear balanced inductive load (PF=0.8).

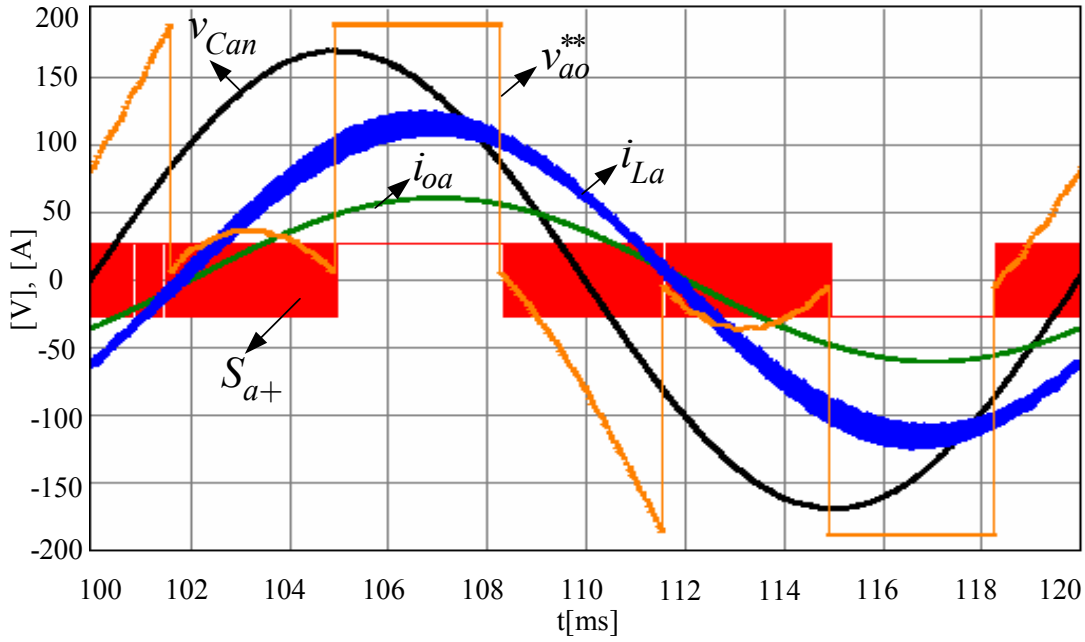


Figure 4.67 Steady-state output voltage (black), modulation signal (orange, x0.7), load current (green, x3), inductor current (blue, x6), switch signal (red, x0.1) during MLDPWM operation under linear balanced inductive load (PF=0.8).

In the next stage, the performance of the scalar modulation methods is evaluated under linear line to neutral unbalanced load condition. Figure 4.68 shows the output voltages and load currents; since this figure is observed same for all modulation methods, it is given just for SVPWM method. The characteristic waveforms, shown in Figure 4.69, are nearly the same as in balanced linear load case for SVPWM. Figure 4.70 illustrates the DPWM1 modulation waves. The symmetry of the modulation signals is lost for the purpose of obtaining balanced output voltages. The commutation of the loaded phase (phase "a") ceases in a larger region than other phases and this affects the switching ripple characteristics as given in Figure 4.71. The MLDPWM modulation signals are illustrated in Figure 4.73. As discussed in Chapter 2, the loaded phase switches are locked to the DC rail for a total of 240° and hence the switching losses are decreased further. As given in Figure 4.74, the switching ripple is shown on the loaded phase inductor current at clamped regions. Figure 4.75 clearly shows the waveforms of the loaded phase.

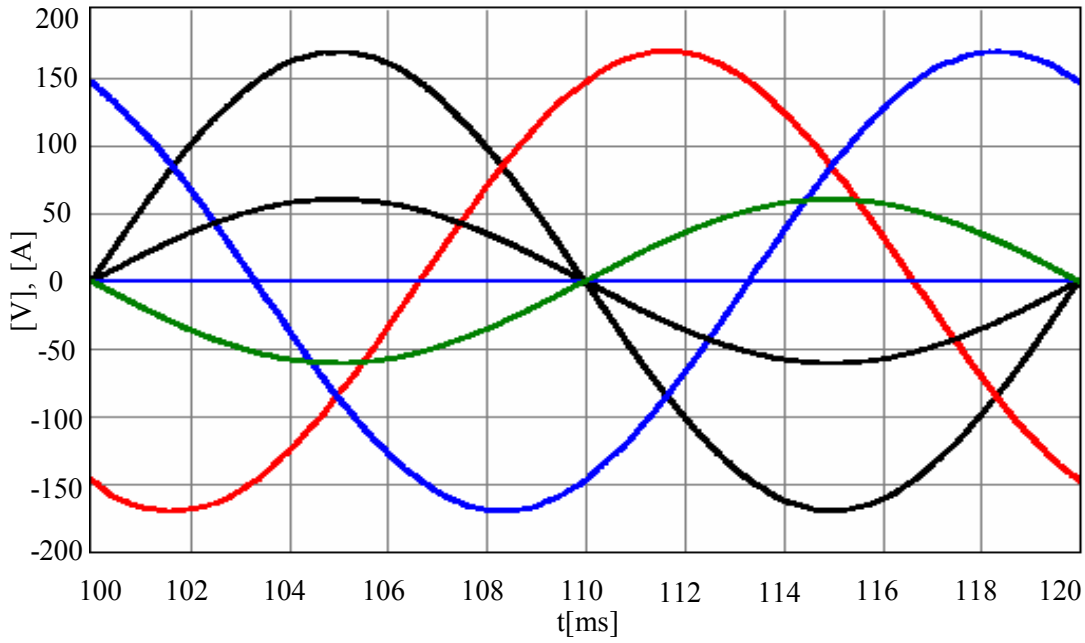


Figure 4.68 Steady-state three-phase output voltages and load currents (scale: x3) during SVPWM operation under linear line-neutral unbalanced load.

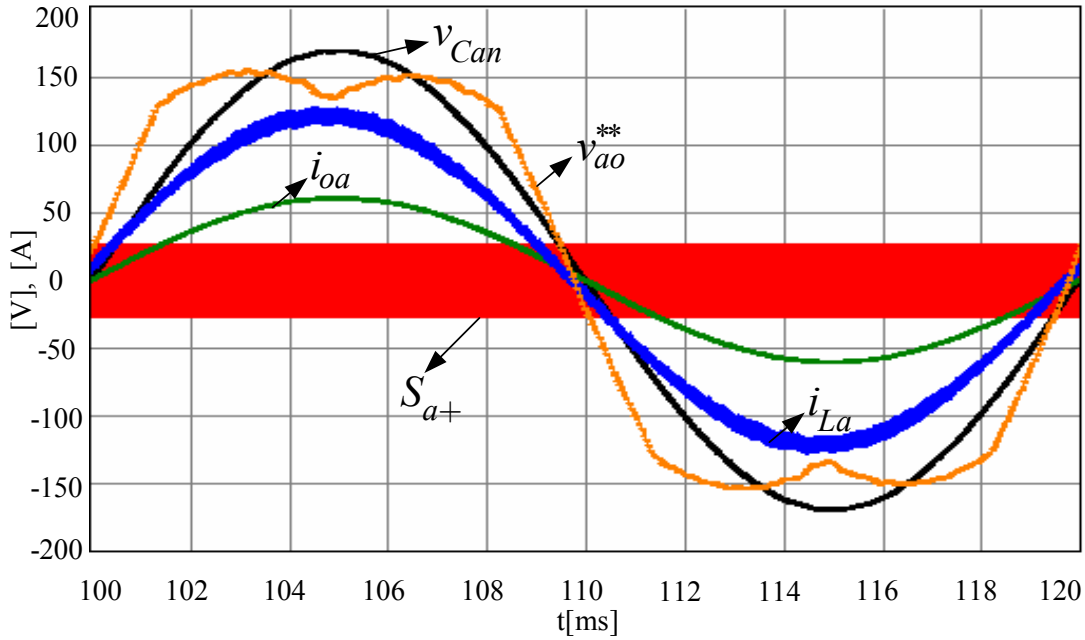


Figure 4.69 Steady-state output voltage (black), modulation signal (orange), load current (green, x3), inductor current (blue, x6), switch signal (red, x0.1) during SVPWM operation under linear line-neutral unbalanced load.

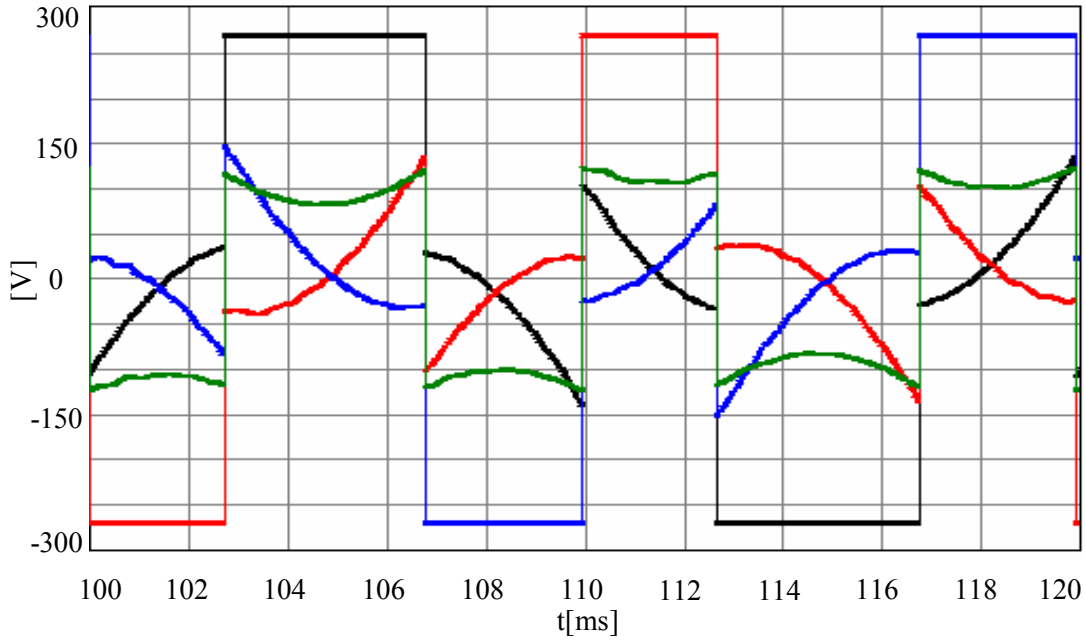


Figure 4.70 Steady-state modulation signals during DPWM1 operation under linear line-neutral unbalanced load.

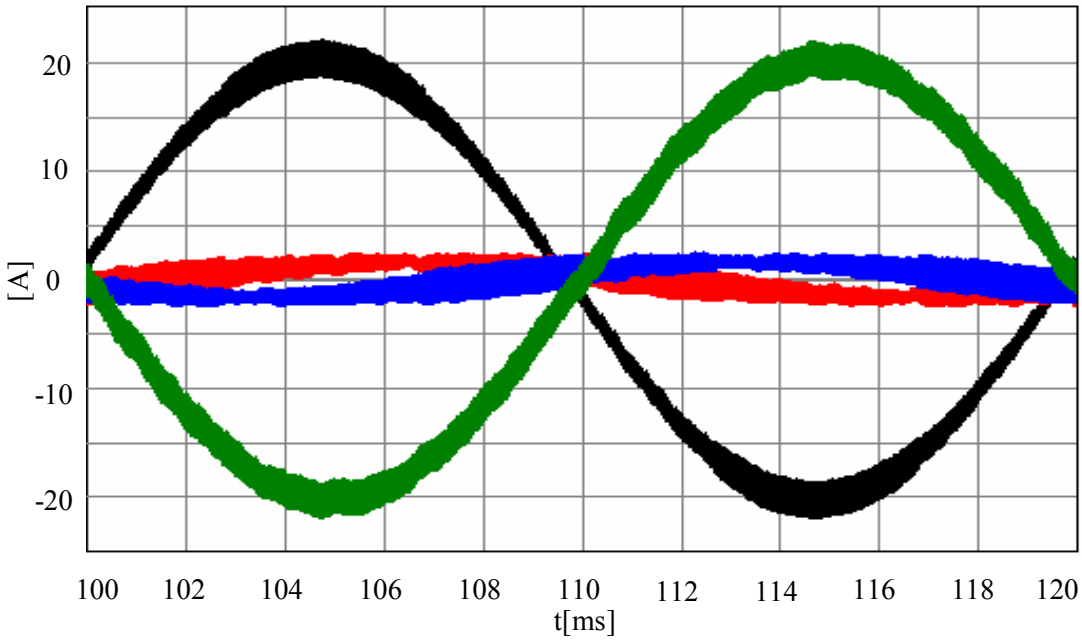


Figure 4.71 Steady-state inverter output currents during DPWM1 operation under linear line-neutral unbalanced load.

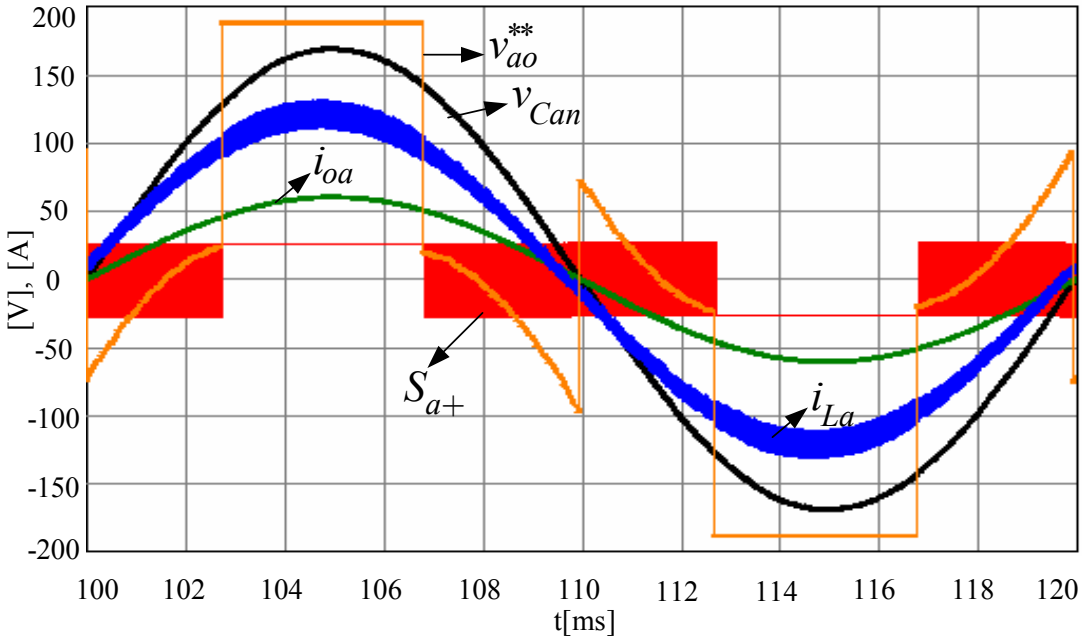


Figure 4.72 Steady-state output voltage (black), modulation signal (orange), load current (green, x3), inductor current (blue, x6), switch signal (red, x0.1) during DPWM1 operation under linear line-neutral unbalanced load.

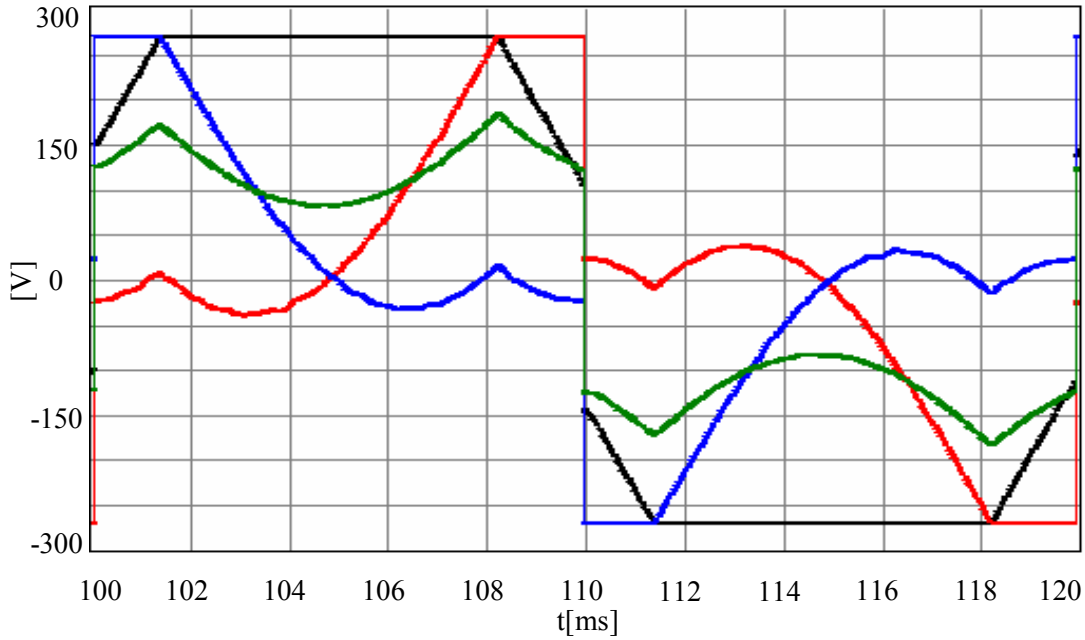


Figure 4.73 Steady-state modulation signals during MLDPWM operation under linear line-neutral unbalanced load.

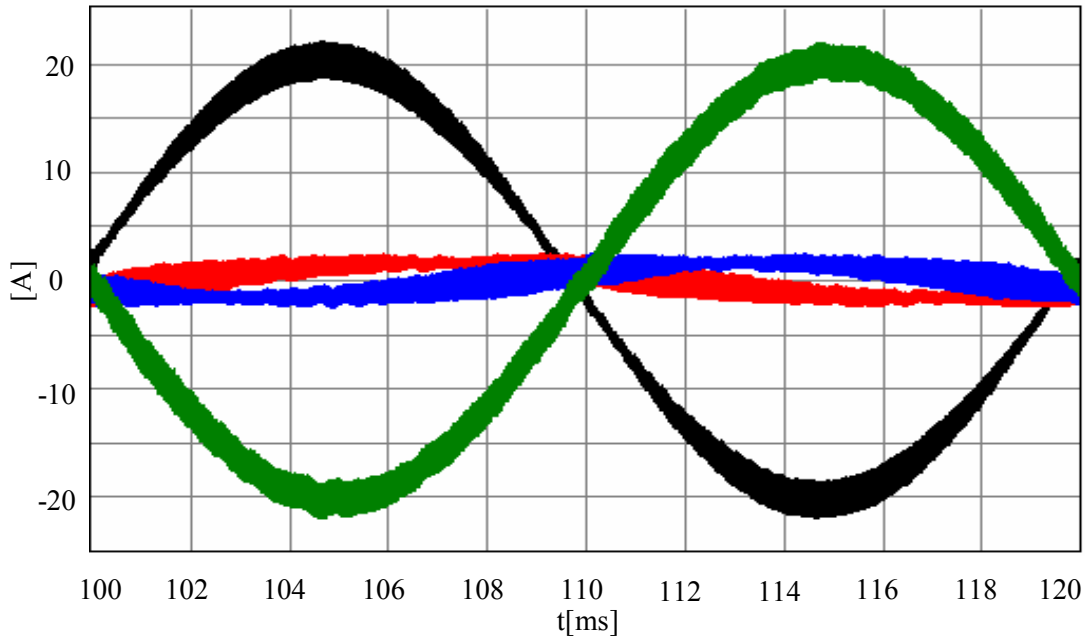


Figure 4.74 Steady-state inverter output currents during MLDPWM operation under linear line-neutral unbalanced load.

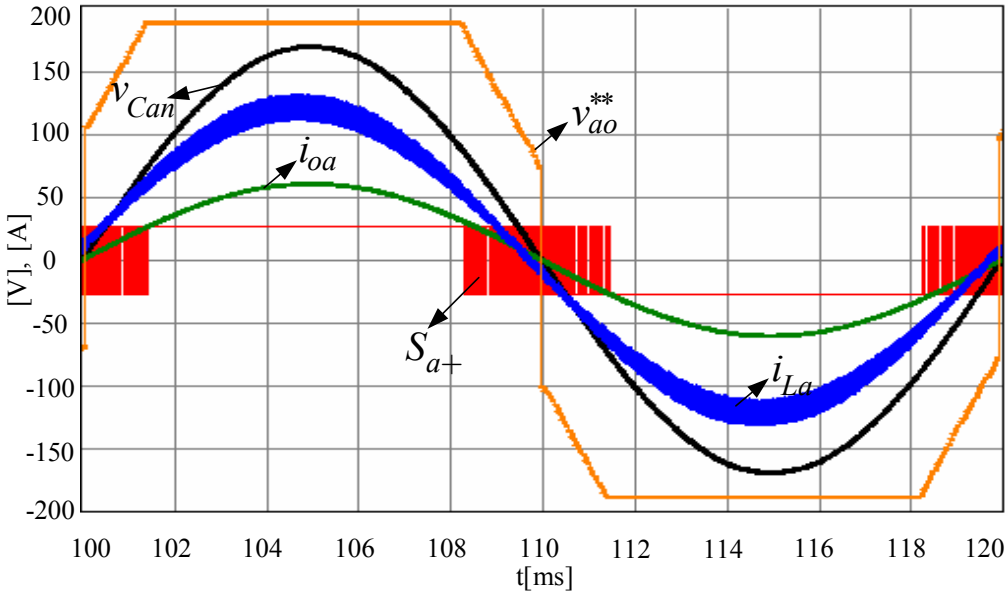


Figure 4.75 Steady-state output voltage (black), modulation signal (orange, x0.7), load current (green, x3), inductor current (blue, x6), switch signal (red, x0.1) during MLDPWM operation under linear line-neutral unbalanced load.

Figure 4.76 illustrates the output voltages and load currents under nonlinear balanced half-load operation. For all investigated modulation methods, these waveforms have approximately the same shape. Thus these results will not be repeated. In terms of modulation waves, there are differences. Shown in Figure 4.77, the SVPWM modulation waves for this case are not the same as those of the linear balanced load case (compare with Figure 4.55). The modulation signals are harmonic rich but not very peaky. The fourth leg modulation signal remains approximately same as in linear balanced load condition. Figure 4.78 shows output voltage, load current, inductor current switching signal, and modulation signal of one phase during SVPWM operation under nonlinear balanced half-load condition. DPWM1 modulation signals for this operating condition are given in Figure 4.79. Switching operations cease a total range of 120^{o} for each phase leg as in the balanced linear load condition. Figure 4.80 represents the one phase characteristic waveforms for DPWM1 operation. In Figure 4.81 and Figure 4.82 the MLDPWM modulation and voltage/current waveforms under balanced nonlinear load condition are given.

Comparing the DPWM1 and MLDPWM switching characteristics, it can be seen that MLDPWM always considers the load current magnitude and locks to the largest current as much as possible while the DPWM1 method operates with fixed lock-out characteristic yielding higher switching losses (compare Figure 4.80 to Figure 4.82).

As a final study, the nonlinear line to neutral unbalanced half-load operating condition is considered. Figure 4.83 through Figure 4.85 show the SVPWM performance for this condition. As the waveforms indicate, the modulation signals are harmonic rich and unbalanced. Figure 4.86 and Figure 4.87 show the DPWM1 waveforms and Figure 4.88 and Figure 4.89 show the MLDPWM waveforms. It can be seen that the MLDPWM method clamps to the larger phase currents for a longer time than the DPWM1 method yielding switching loss reduction.

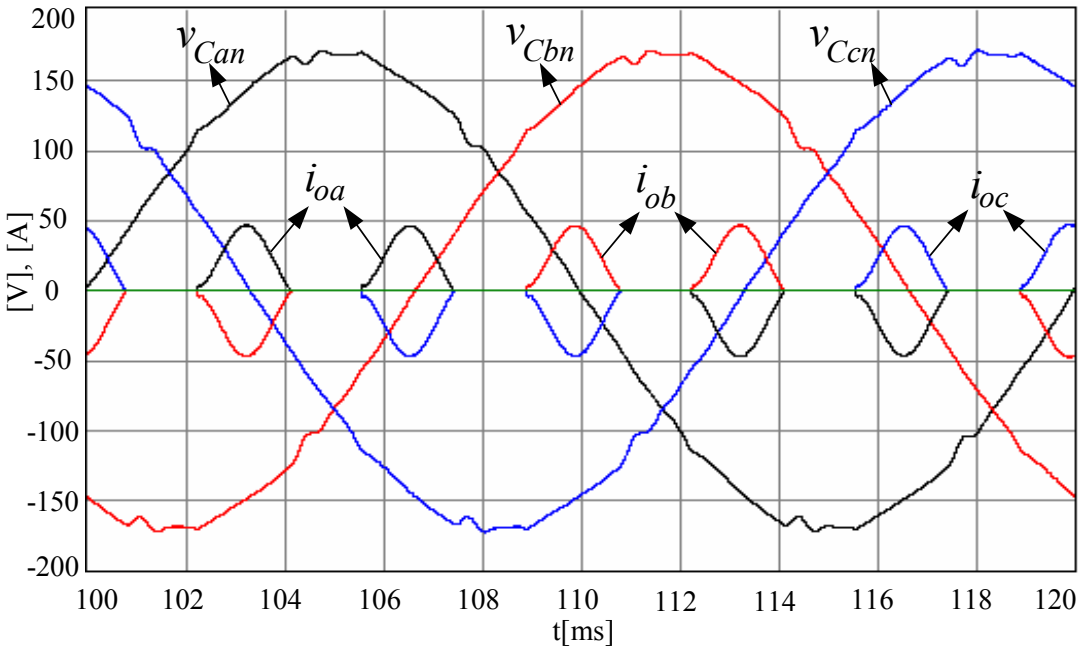


Figure 4.76 Steady-state three-phase output voltages and load currents (scale: x2.5) during SVPWM operation under nonlinear balanced half-load.

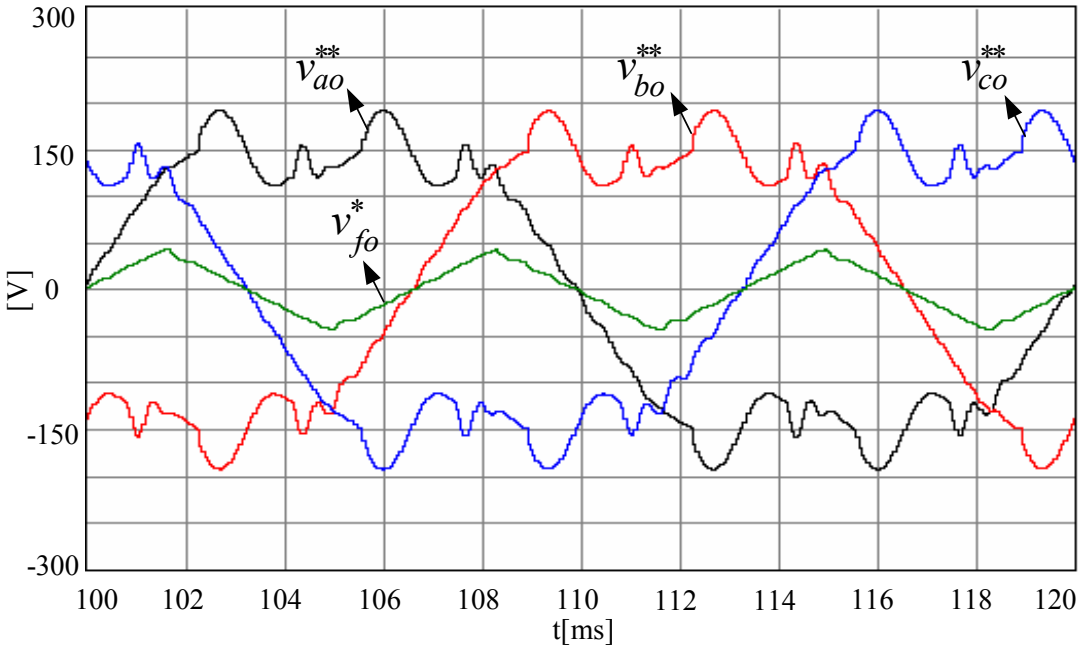


Figure 4.77 Steady-state modulation signals during SVPWM operation under nonlinear balanced half-load.

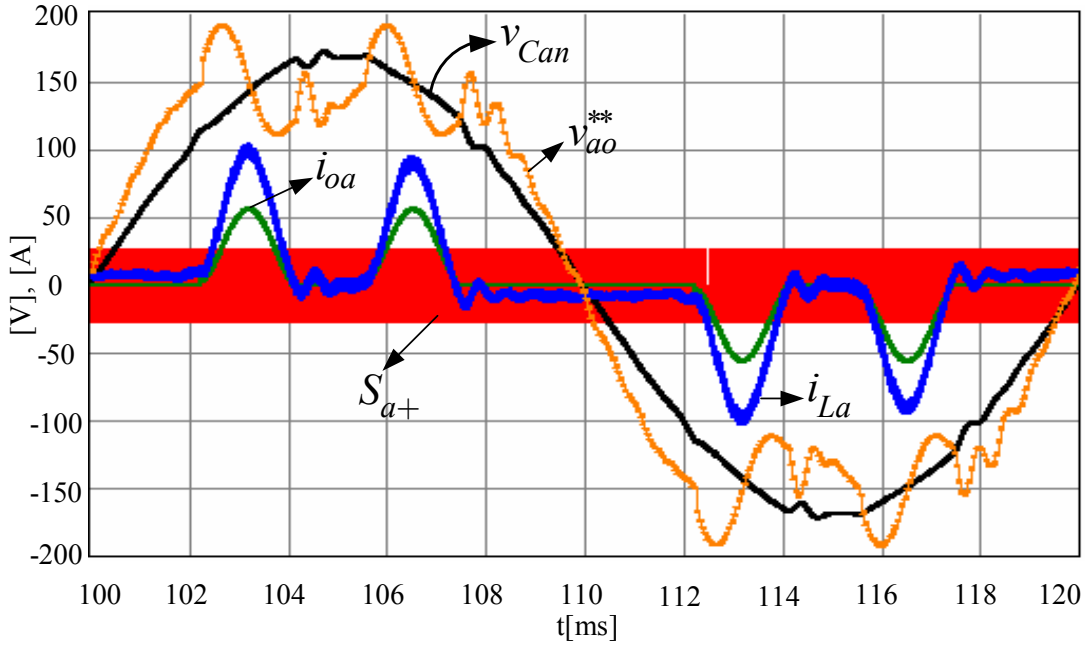


Figure 4.78 Steady-state output voltage (black), modulation signal (orange), load current (green, x3), inductor current (blue, x5), switch signal (red, x0.1) during SVPWM operation under nonlinear balanced half-load.

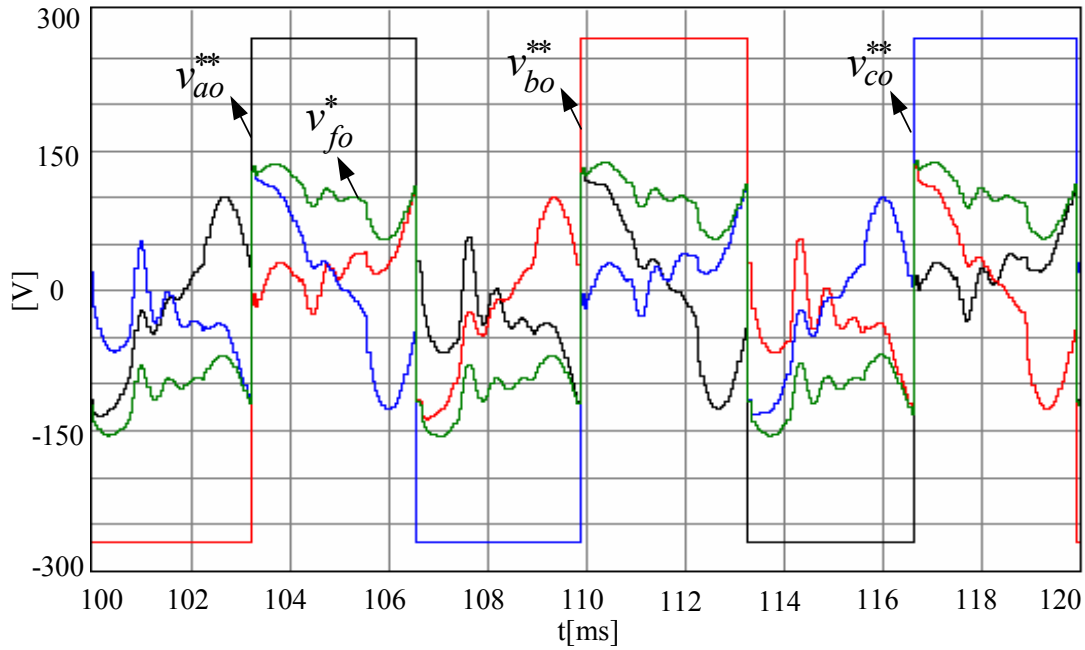


Figure 4.79 Steady-state modulation signals during DPWM1 operation under nonlinear balanced half-load.

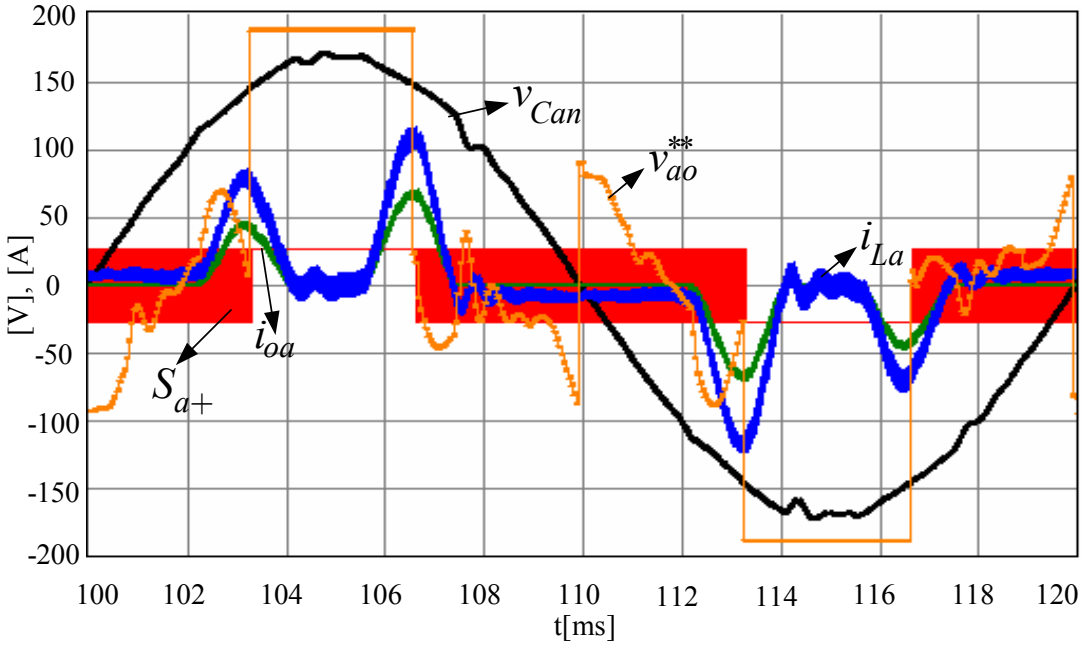


Figure 4.80 Steady-state output voltage (black), modulation signal (orange, x0.7), load current (green, x3), inductor current (blue, x5), switch signal (red, x0.1) during DPWM1 operation under nonlinear balanced half-load.

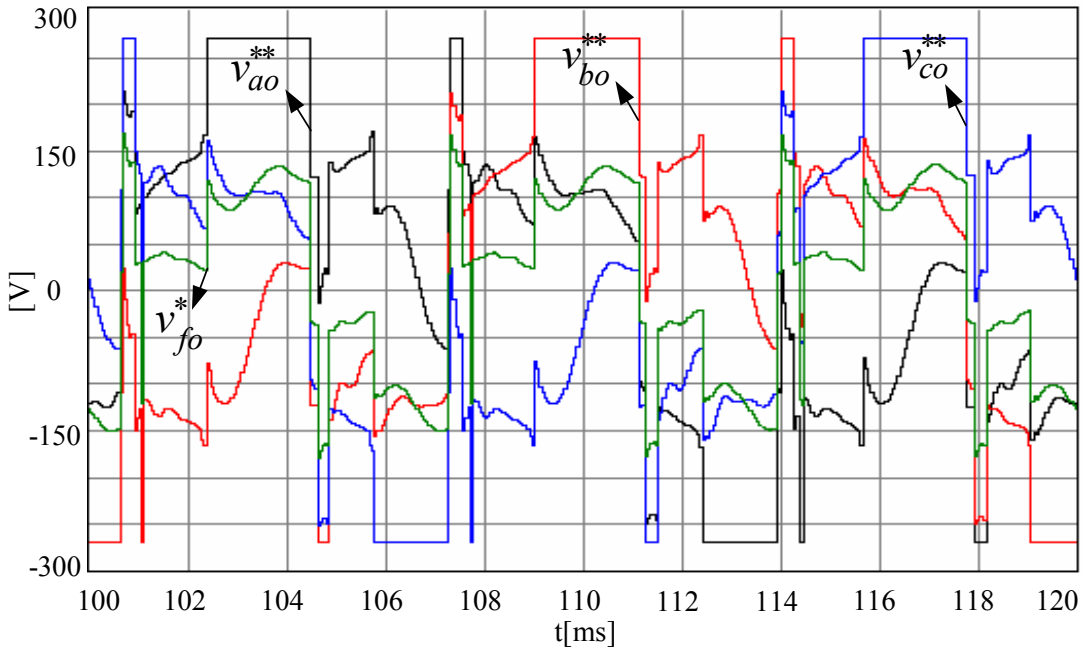
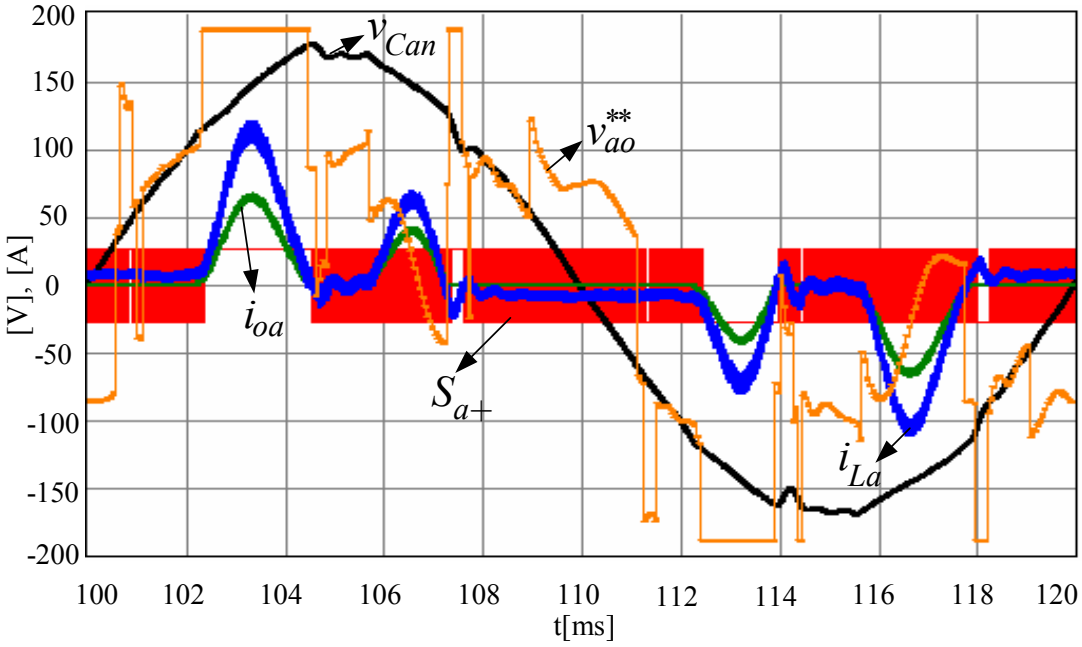


Figure 4.81 Steady-state modulation signals during MLDPWM operation under nonlinear balanced half-load.



,Figure 4.82 Steady-state output voltage (black), modulation signal (orange, x0.7), load current (green, x3), inductor current (blue, x5), switch signal (red, x0.1) during MLDPWM operation under nonlinear balanced half-load.

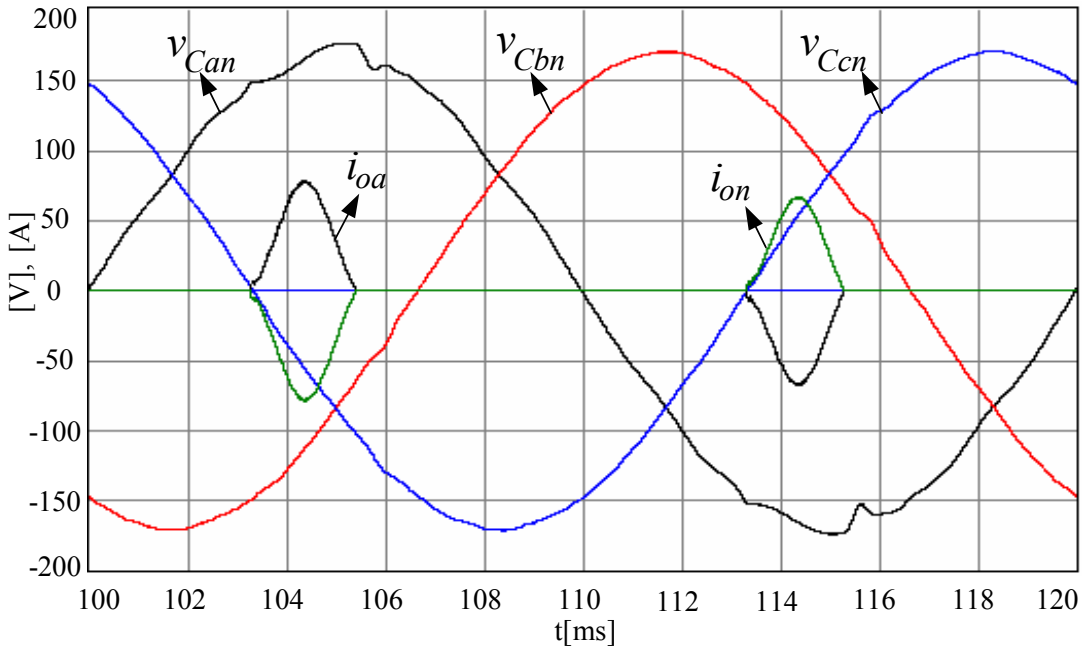


Figure 4.83 Steady-state three-phase output voltages and load currents (scale: x2.5) during SVPWM operation under nonlinear line-neutral unbalanced half-load.

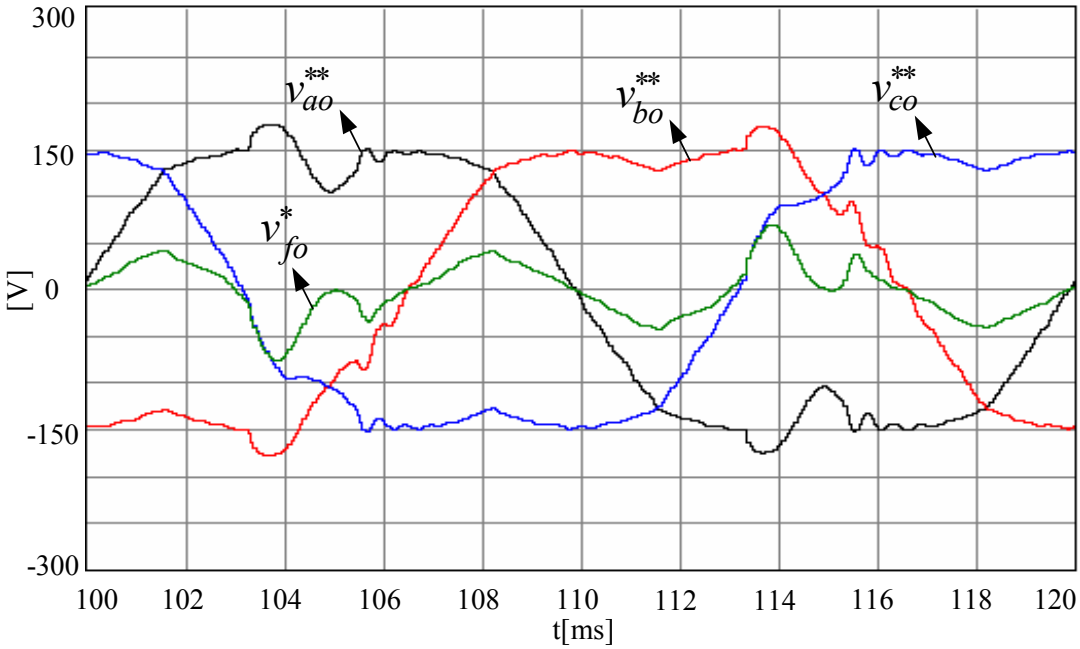


Figure 4.84 Steady-state modulation signals during SVPWM operation under nonlinear line-neutral unbalanced half-load.

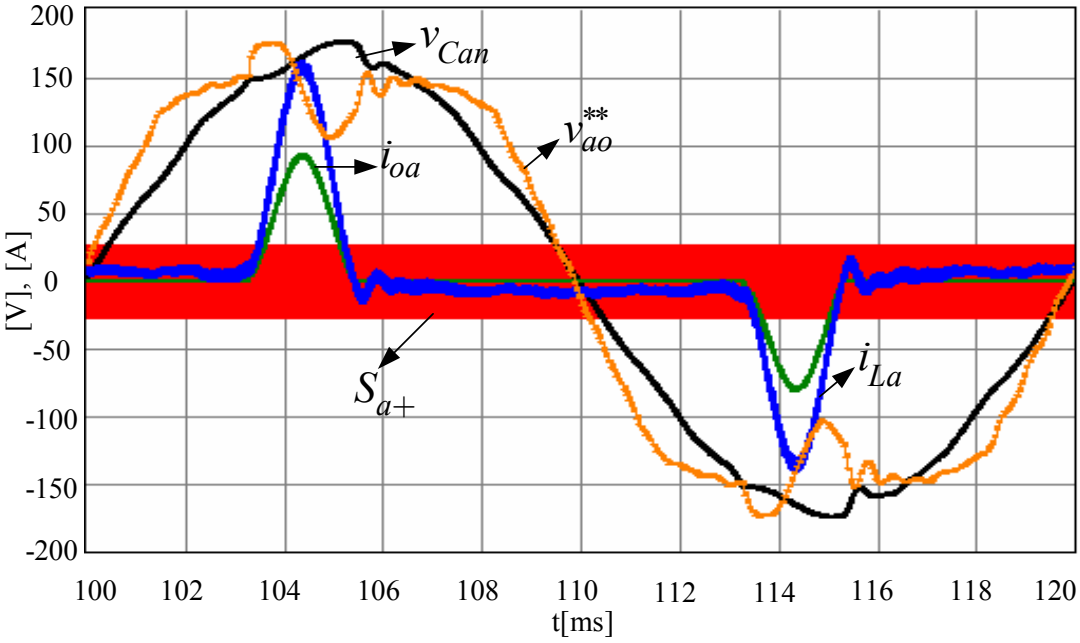


Figure 4.85 Steady-state output voltage (black), modulation signal (orange), load current (green, x3), inductor current (blue, x5), switch signal (red, x0.1) during SVPWM operation under nonlinear line-neutral unbalanced half-load.

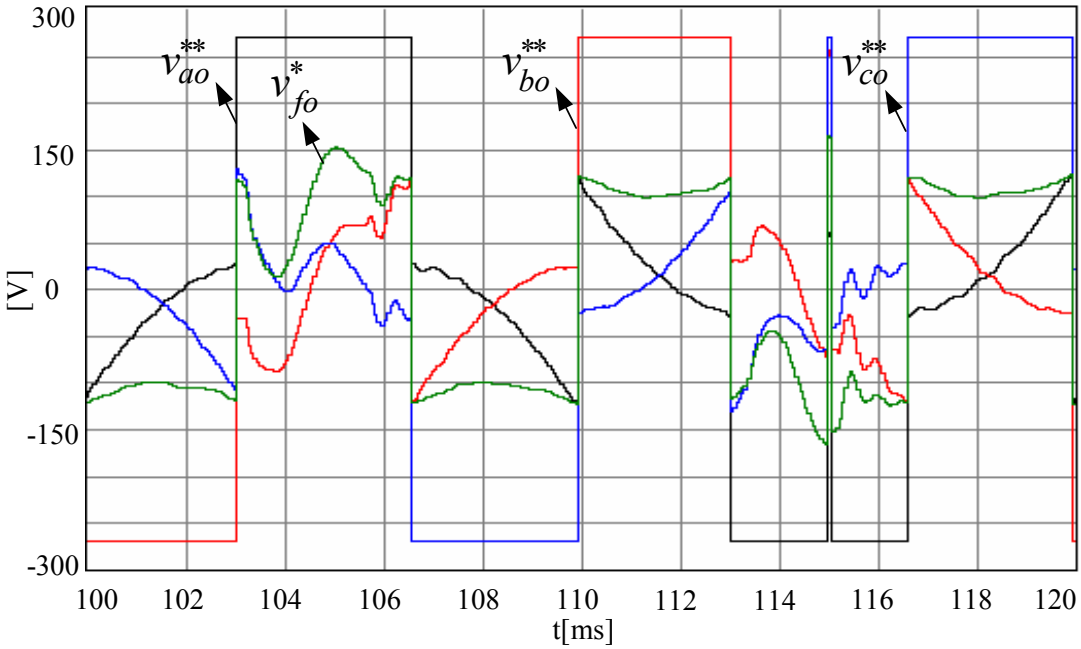


Figure 4.86 Steady-state modulation signals during DPWM1 operation under nonlinear line-neutral unbalanced half-load.

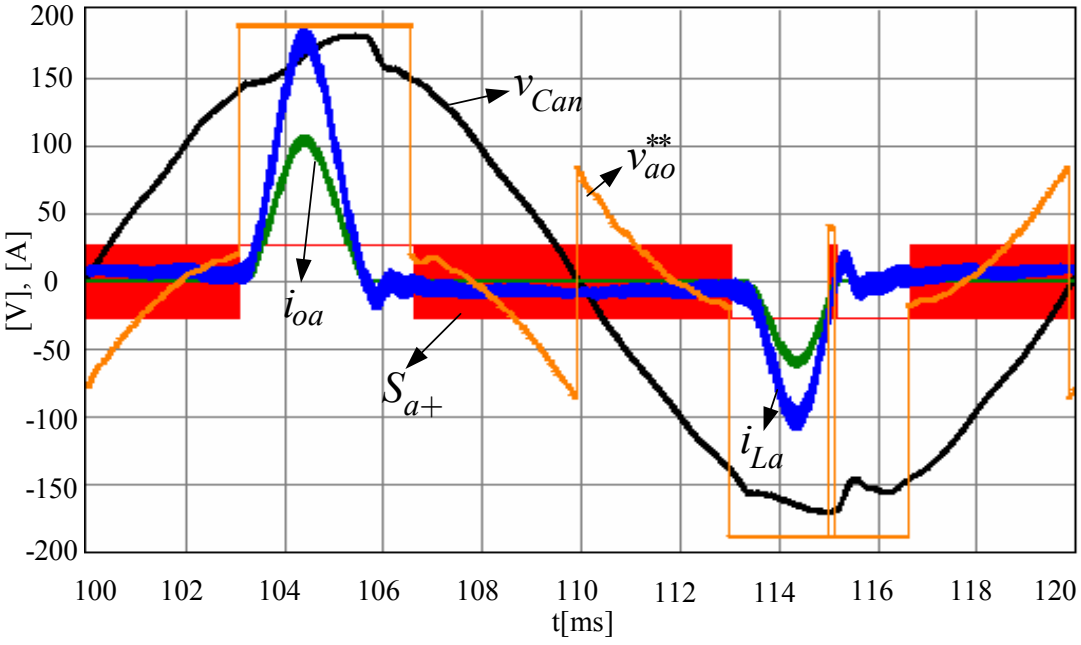


Figure 4.87 Steady-state output voltage (black), modulation signal (orange, x0.7), load current (green, x3), inductor current (blue, x5), switch signal (red, x0.1) during DPWM1 operation under nonlinear line-neutral unbalanced half-load.

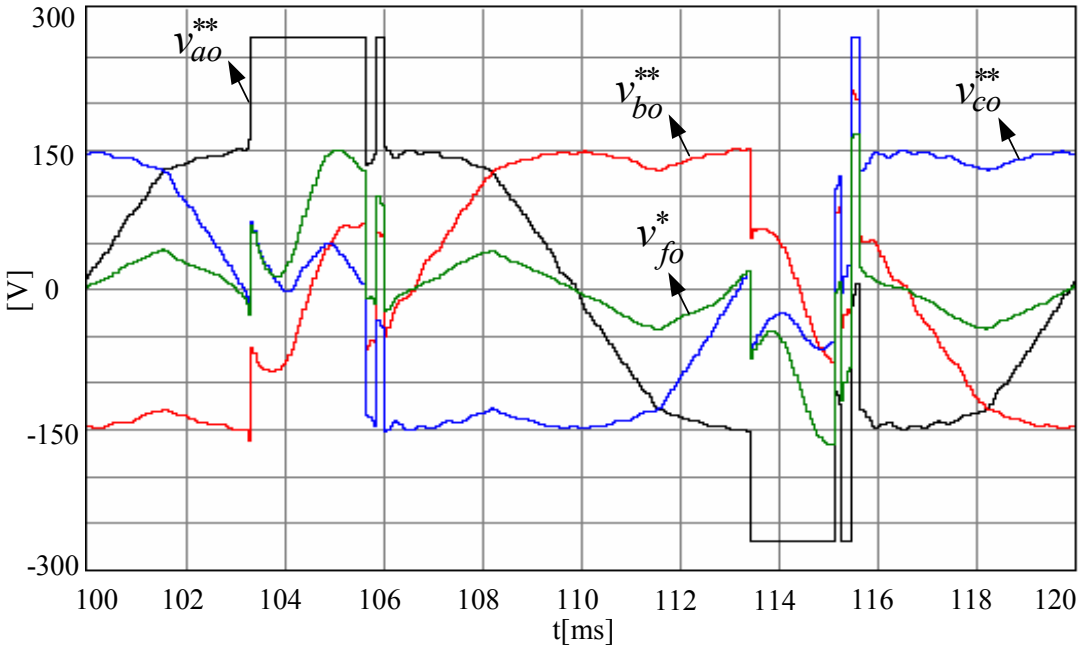


Figure 4.88 Steady-state modulation signals during MLDPWM operation under nonlinear line-neutral unbalanced half-load.

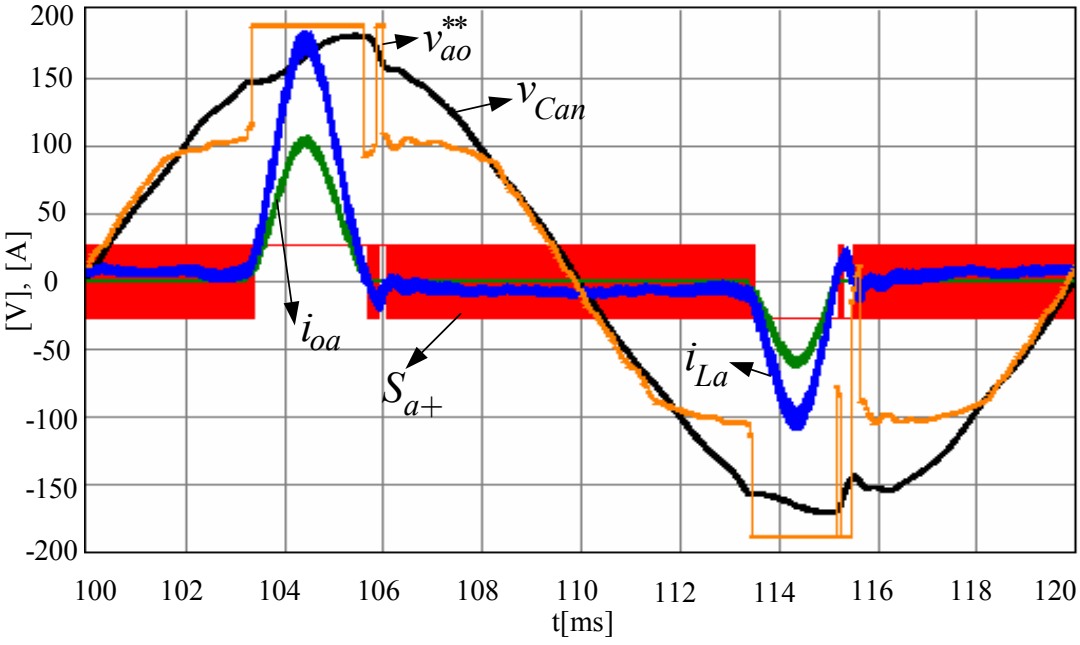


Figure 4.89 Steady-state output voltage (black), modulation signal (orange, x0.7), load current (green, x3), inductor current (blue, x5), switch signal (red, x0.1) during MLDPWM operation under nonlinear line-neutral unbalanced half-load.

With the study of modulation waveform characteristics, this chapter concludes. In this chapter it has been shown by means of detailed computer simulations that the high performance resonant filter bank controller with active damping provides a superior solution. Also in the final section the study involving modulation types has illustrated that the MLDPWM method has comparable PWM ripple to SVPWM but has lower switching losses than any other method. Thus, it should be favored in practical applications. The following section involves the practical implementation of a three-phase four-leg inverter based UPS. The practical results there will hold light towards the usefulness of the proposed methods.

CHAPTER 5

EXPERIMENTAL PERFORMANCE INVESTIGATION OF THE FOUR-LEG INVERTER BASED THREE-PHASE UPS SYSTEM

5.1. Introduction

In this chapter, the experimental performance investigation of the three-phase four-leg inverter based UPS system is conducted. The scalar modulation methods and the resonant filter controller structure are employed and the UPS system performance is experimentally investigated under steady-state and dynamic operating conditions for linear, nonlinear, balanced, and unbalanced load cases. Thus, the theoretical study results of Chapter 2, Chapter 3, and the computer simulation studies of chapter 4 are verified by the experimental work in this chapter. First the experimental system hardware and software are described, and then the steady-state performance study is followed by the dynamic performance investigation.

5.2. Hardware Implementation of The Three-Phase Four-Leg UPS System

The four-leg inverter based three-phase UPS system is designed and manufactured at METU Electrical and Electronics Engineering Department, in the Electrical Machines and Power Electronics Laboratory. An experimental setup is established to operate the UPS system. The block diagram of the experimental setup is given in Figure 5.1. The electrical power circuitry of the overall system is shown in Figure 5.2. The parameters, which are utilized in the experimental setup and experiments, are given in Table 5.1. Figure 5.3 shows the laboratory prototype four-leg UPS.

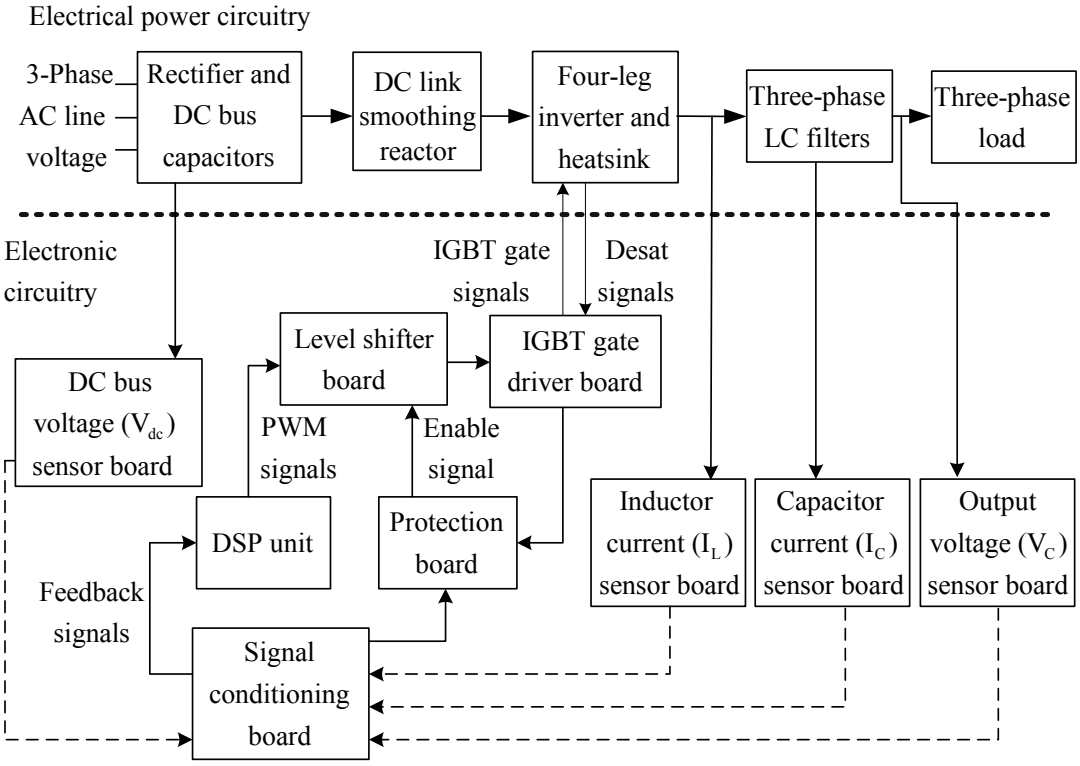


Figure 5.1 The system block diagram of the experimental setup.

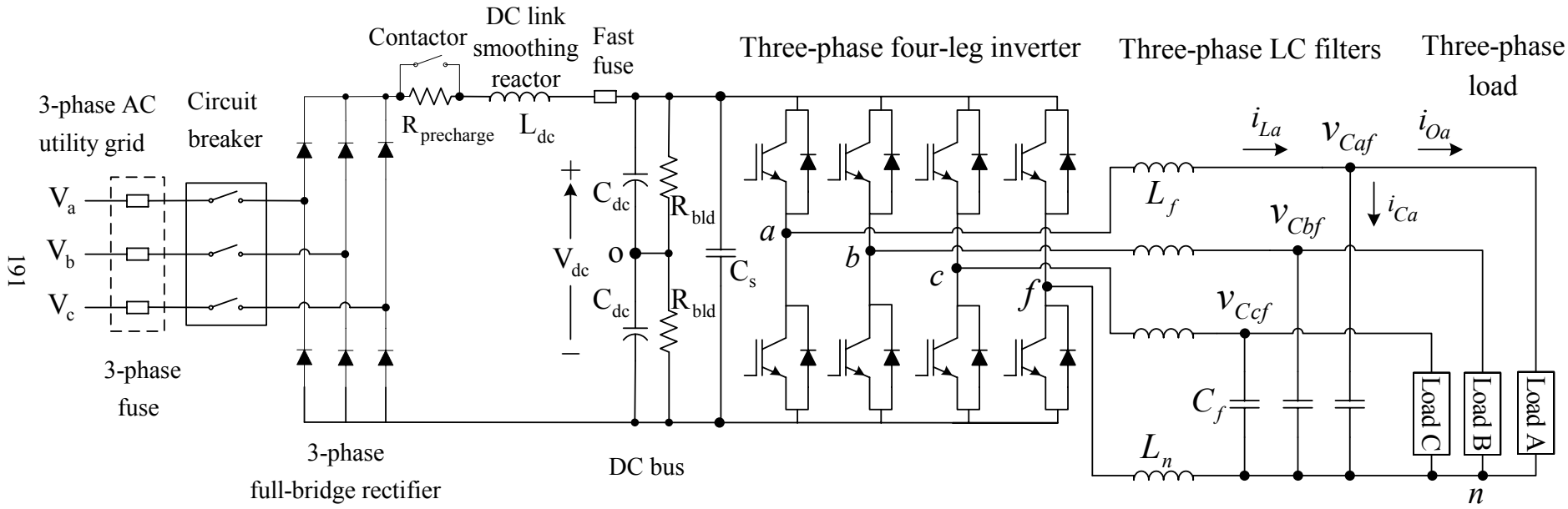


Figure 5.2 The electrical power circuitry of the overall system.

Table 5.1 Experimental system parameters

DC bus	Voltage	540 V
	Capacitor	1100 μF (2 series connected capacitors with 2200 μF, 450 V, 10.7 A-rms each)
	DC link smoothing reactor	1.46 mH
	Pre-charge resistor	47 Ω , (50W)
	Bleeding resistor	30 kΩ , (10 W)
	Snubber capacitor	220 nF , (1000V)
Output filter	Inductor	1.5 mH/phase
	Capacitor	30 μF/phase
	Neutral leg inductor	500 μH
UPS output	Rated power	5 kVA
	Rated voltage	120 V_{rms}
	Rated frequency	50 Hz

A three-phase 20 A automatic fuse and a three-phase 25 A circuit breaker are employed at the utility grid connection point for the protection purpose. The obtained AC voltage is converted to DC voltage by a 1600 V, 88 A three-phase full-bridge diode rectifier. IXYS brand, VUO82-16 NO7 model three-phase full-bridge diode rectifier is utilized. Two bulk capacitors (C_{dc}) are connected in series to form the DC bus of the four-leg inverter. The bleeding resistors (R_{bld}), which discharge the DC bus capacitors when the converter system is shut down and balance the capacitor voltages normally, are connected across the DC bus capacitors. Each utilized bleeding resistor has a resistance value of 30 kΩ and a power rating of 10 W. To prevent hazards during a short-circuit condition on the DC bus, a 20 A fast fuse is employed between the positive terminal of the diode rectifier and the DC bus capacitor bank. A DC link reactor (L_{dc}=1.46 mH with 20 A rms current rating) is inserted between the rectifier output and the DC bus of the inverter in order to further improve the input current waveform and reduce the rms current stress on the DC bus capacitors. A pre-charge resistor ($R_{precharge}$) is utilized to limit the inrush current

during the start-up of the system and the precharge resistor is short-circuited (by-passed) by means of a manual by-pass switch after the DC bus capacitor is charged to its steady-state value. The precharge resistance value is equal to 47 Ω and it has a 50 W power rating. The DC bus of the three-phase four-leg inverter is constructed by utilizing a planar bus structure to obtain low parasitic inductance on the DC bus. Two aluminum plates are mounted on the inverter IGBT modules for positive and negative DC bus rails. Between these plates an insulation material having an insulation level of 10 kV is inserted. A snubber capacitor (C_s) for each IGBT module is inserted across the DC bus terminals of the IGBT module. On each IGBT module a snubber capacitor is installed so that the switching stress on the IGBTs due to the parasitic inductances is reduced. The utilized snubber capacitors in the four-leg inverter have a 220 nF capacitance and 1000 V voltage rating.

The laboratory utility supply is 220Vrms line-to-neutral and 380Vrms line-to-line voltage. With this utility grid, the three-phase full-bridge diode rectifier is utilized to convert the AC utility voltage to DC voltage. In this case the maximum achievable value of the DC bus voltage is 540V. Since the DC voltage level is not sufficient to produce a 220 V_{rms} UPS output voltage, the rated UPS output voltage is set to 120 V_{rms} in this study.

The four-leg inverter is built by using four dual-pack IGBT modules. Semikron brand IGBT modules, SKM 50 GB 123 D are utilized. The IGBT modules are driven by the Semikron SKHI 22B gate driver modules. The basic specifications of the power semiconductors and gate drive circuit utilized in the designed inverter are summarized in Table 5.2. The gate driver board, which includes four gate driver modules, converts a PWM signal with +5/0 voltage levels to an isolated and amplified +15/-7 voltage levels, which is required for the IGBT turn-on and turn-off operations. The gate driver board outputs +15 V during the conduction interval of the IGBT and it applies -7 V to the gate terminal of the IGBT during the off interval to fully discharge the stored gate charge, guarantying the turn-off operation of the IGBT. While the gate driver module generates the gate voltage for the IGBTs, it also monitors the collector-emitter voltage for short-circuit failure condition. While the

IGBT is conducting, if the collector-emitter voltage of the IGBT is higher than the preset de-saturation limit voltage value, which is slightly larger than V_{CEsat}, the gate driver module turns off the IGBT and outputs an error signal to the protection board (the desat signal). The gate driver module applies the gate voltage to the IGBT gate terminals via a series gate resistor having a value of 22 Ω.

Table 5.2 Specifications of the power semiconductor modules and gate driver modules utilized in the experimental setup

SKM 50 GB 123 D (IGBT of the dual-pack)		
V_{CES}	Collector-emitter blocking voltage rating	1200 V
I_C	Continuous collector current rating (rms)	50 A
V_{CEsat}	Collector-emitter saturation voltage at 50 A	2.7 V
$t_{d(on)}$	Turn-on delay time	70 ns
t_r	Rise time	60 ns
$t_{d(off)}$	Turn-off delay time	400 ns
t_f	Fall time	45 ns
SKM 50 GB 123 D (Diode of the dual pack)		
V_F	Forward voltage drop at I_F=50 A	2 V
I_{RRM}	Peak reverse recovery current	23 A
Q_{rr}	Recovered charge at I_F=40 A	2.3 μC
SKHI 22B Gate Driver Module		
V_S	Supply voltage primary side	15 V
I_{SO}	Supply current primary side at no-load/max.	80 / 290 mA
V_i	Input signal voltage ON/OFF	5 / 0 V
V_{iT+}	Input threshold voltage (High)	3.7 V
V_{iT-}	Input threshold voltage (Low)	1.75 V
R_{in}	Input resistance	3.3 kΩ
$V_{G(ON)}$	Turn-on gate voltage output	+15 V
$V_{G(OFF)}$	Turn-off gate voltage output	-7 V
t_{TD}	Top-Bottom interlock dead-time min. / max.	no interlock / 4.3 μs

In the UPS system the LC filter design is critical as it determines the resonant frequency of the filter and the control bandwidth requirements. In the experimental system, 1.5 mH inductor (L_f) and 30 μF output capacitor (C_f) are utilized to form an LC filter (per-phase). To suppress the neutral current ripple, a series inductor (L_n), which has an inductance of 500μH, is utilized in the neutral line and connected to the midpoint of the fourth leg as shown in Figure 5.2. Notice that this inductance is intentionally selected to be one third of the phase inductances.

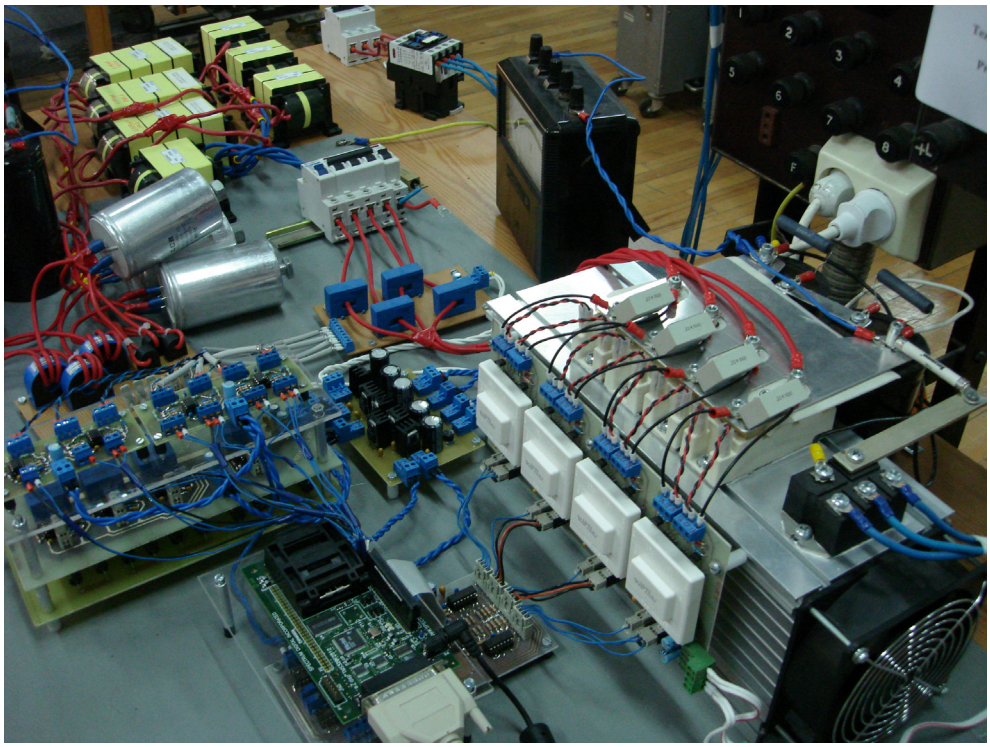


Figure 5.3 Laboratory four-leg inverter based three-phase UPS system.

In order to do the load test of the UPS system, in the experiment, mainly two load types are utilized. Resistive load is preferred for linear load. For nonlinear load a diode rectifier with DC bus capacitor and a resistive load in parallel with the DC bus capacitor are used. The parameters of both load types are the same as those defined in Table 4.3 and Table 4.4. The connection configurations of the loads are also the same as described in Chapter 4 for and shown in Figure 4.2.

The resistive load is provided through resistive load banks available at the university laboratory. Each load bank has 3kW ratings and consists of 12 parallel connected resistances which can be turned on and off via manual switches. With each resistor having a value of 192 Ω, the resistance of each load bank can be varied from 192 Ω to 192/12 Ω in 12 decrements by the manual switches. In order to match the resistance values required in Table 4.3 a set of load banks is utilized.

For the nonlinear load test, a three-phase full-bridge diode rectifier is built utilizing an identical module to that used to form the inverter DC bus (IXYS VUO82-16 NO7). Two bulk capacitors (C_{dc}), having 2200 μF capacitance, 450 V DC voltage rating and 10.7 A rms current rating each, are connected in series to form the DC bus of the nonlinear load. Also two bleeding resistors (R_{bld}) with 56 kΩ and 5 W ratings are connected across the DC bus capacitors of the nonlinear load. The same load bank as discussed for the linear load test is utilized and the load bank is connected across the rectifier output terminals to form the RC load. The load bank switches are manipulated such that the resistance values required in Table 4.4 are configured. By selecting various connection configurations between the UPS output terminals and load terminals, all the cases considered in Table 4.3 and Table 4.4 can be configured.

The three-phase output voltages of the UPS, the DC bus voltage, the output capacitor currents, and the inverter output currents are measured for control and protection purpose. The DC bus voltage of the inverter and the three-phase output voltages are measured by utilizing the Hall Effect based isolated voltage sensor, LV25-P model manufactured by LEM. The inverter output currents are measured by utilizing the same type and different model current sensors, LA 55-P/SP1 model manufactured by LEM. The capacitor currents are measured by utilizing current transformers which have 1:200 turns ratio. All the measured signals are scaled and filtered by utilizing basic operational amplifier circuits and passive noise filters in the signal conditioning board. The cut-off frequency of the passive filters, which are utilized in the signal conditioning board, is chosen as 100 kHz. The signal conditioning board provides feedback signals at the required voltage level (between 0 V and 3 V) for the Digital Signal Processor (DSP) unit. The inverter output current measurement is utilized

only for overcurrent protection of the IGBT modules. The scaled and filtered inverter output currents are supplied to the protection board. The protection board monitors the overcurrent and IGBT desaturation signals and if an error does not occur, it enables the IGBT gate signals to be applied to the IGBT gate driver board. If an error occurs in the UPS system, a disable signal forces all the PWM signals, which are transferred to the gate driver modules, to low logic voltage level and keeps them at the low level unless the error state is reset. The level shifter board is designed to increase the DSP output PWM logic signals from voltage level of 0/3.3V to the level of 0/5V, which is required by the gate driver module. All the electronic boards are designed as double layer printed circuit board in order to reduce the Electromagnetic interference (EMI), which is sourced by the power circuitry.

To implement the UPS output voltage control function and generate the required IGBT gate signals, a DSP unit is utilized in the experimental system. In the DSP unit, analog to digital (A/D) conversions, control block calculations, and PWM output signal generation are carried out. In the experimental set-up, for a DSP, the eZdsp F2812 board manufactured by Spectrum Digital Inc., is employed to accomplish the control functions. The features of the eZdsp F2812 board are given in Table 5.3. The board contains the TMS320F2812 DSP manufactured by Texas Instruments and the features of TMS320F2812 are given in Table 5.4 [41]. In the implementation, the UPS system control loops are periodically executed. The control and PWM cycles are synchronized and they are executed at the same rate. The main DSP code reads the feedback signals, executes the control loops, generates the PWM duty cycles and loads the duty cycles to the PWM units. These goals are achieved systematically and efficiently with the use of the event managers of the DSP. The TMS320F2812 DSP chip utilized in controlling the UPS system has event managers which have timers that can be used for generating the PWM signals [42]. Two event managers, EVA and EVB exist. With each one of them, by utilizing a timer, three comparators and dead-time generators, three-phase modulation signals can be converted to six PWM logic signals. For the four-leg inverter since four phases and thus eight PWM logic signals are required, both event managers must be utilized and the timers used must be synchronized so that the triangular wave is the same for all modulation waves.

The synchronization is provided via proper initial value setting of one of the event manager timers EVA and EVB. From EVA, Timer1 and from EVB Timer3 are utilized in the implementation. Timer1 counter (T1CNT) of EVA is set to continuous up/down counting mode to create symmetric PWM pulses. Counting time of the T1CNT is determined by period register of Timer1 counter (T1PR), which is uploaded according to the desired PWM switching cycle (frequency).

When the first timer (Timer1) reaches zero value (underflow) or the full value (period) an interrupt may be given. To obtain an interrupt at the zero value of Timer1, the Timer1 underflow interrupt (T1UFINT) should be enabled. To obtain an interrupt at the period value of Timer1, the Timer1 period interrupt (T1PRDINT) should be enabled. If only one of these two interrupts is enabled, the PWM logic signals are updated once in a PWM cycle and this is called as "single update mode." If both of these interrupts are enabled, the PWM logic signals are updated twice in a PWM cycle and this is called as "double update mode." Comparing the numbers loaded in the compare registers with the T1CNT and T3CNT, the PWM output logic signals to the specific phase leg are generated. For each comparison two complementary output logic signals are generated. The signals are delayed by the dead-time (t_d, which is built into the PWM module of the DSP chip) to avoid shoot-through in the inverter. Figure 5.4 aids understanding the PWM generation process, illustrates the period and underflow loading instants and including the effect of dead-time.

Loading the compare register with the duty cycle of the specific phase leg involves one instruction cycle of the DSP. In the TMS320F2812 the maximum clock cycle is 150 MHz which corresponds to 6.67 ns instruction cycle. This 6.67 ns delay causes problems in realizing various PWM methods. The problem arises when the calculated duty cycle is loaded to the counter at the period instant and its previous value is not 100% but the calculated value is 100%. This condition is encountered during implementation of discontinuous PWM methods and specifically either when loading with single update rate and at the period point or when loading with double update rate and at the period point. Since during loading at the period instant a delay

of 6.67ns exists, the opportunity for loading the correct duty cycle to the compare register is missed and a faulty signal which distorts the PWM waveforms and disturbs the output voltages/currents is generated.

With the aid of the event managers the PWM and control cycles are synchronized as discussed above and while the PWM duty cycle uploading process takes one instruction cycle, the control loop is executed within the event manager timer interrupt period. When the interrupt occurs, the DSP processes the “interrupt service routine” function to generate the PWM output signals for the IGBT switches. The flow chart of the interrupt service routine is shown in Figure 5.5. As seen from the figure, the interrupt service routine starts with the A/D conversion of the feedback signals. Then, picking up the stored A/D signals from the allocated memory locations, the signals are scaled and normalized to appropriate values. After generating the UPS output voltage reference signals, the error signals, which are the difference between the reference signals and measured feedback signals, are calculated. The output voltage errors are fed to the discrete time implemented resonant filter controller to generate the inverter reference voltages. Given the reference voltages and selecting a modulation method, the PWM signals are generated and converted to switch duty cycles and fed to the PWM counters. The PWM unit generates the inverter gate logic signals. Then the protection circuit, level shifter and gate driver circuits guide the IGBTs to the proper outputs such that the inverter output voltages are generated. In the experiments, tests are conducted for two different operating switching frequencies, 10 kHz, and 20 kHz as will be discussed in the upcoming sections. For both cases the dead-time is set to 2μs for the complementary PWM logic signals.

Table 5.3 Main features of the eZdsp F2812 board

Digital signal processor	TMS320F2812
External clock frequency	30 MHz
External memory	64K words SRAM
Expansion connectors	• Analog • Digital I/O • External interface
Interface	• IEEE 1149.1 JTAG* controller • IEEE 1149.1 JTAG emulation connector

*: Joint Test Action Group

Table 5.4 Main features of TMS320F2812 DSP

Operating frequency	150 MHz
Clock and system clock	• On-chip oscillator • Watchdog timer
Central processing unit (CPU)	32-bit high performance CPU
On-chip memory	• 128K×16 Flash memory • 18K×16 RAM** • 1K×16 OTP ROM***
Timers	Three 32-Bit CPU Timers
Motor control peripherals	Two event manager (EVA, EVB)
Analog-digital converter (ADC)	• 12-Bit ADC • 16 Channels • Fast conversion rate: 80ns/12.5 MSPS
General purpose input/output	Up to 56 pins
External interface	• Up to 1M total memory • Three individual chip selects
Serial port peripherals	• Serial peripheral interface • Two serial communications interfaces • Enhanced controller area network • Multi-channel buffered serial port

**: Random Access Memory

***: One-Time Programmable Read Only Memory

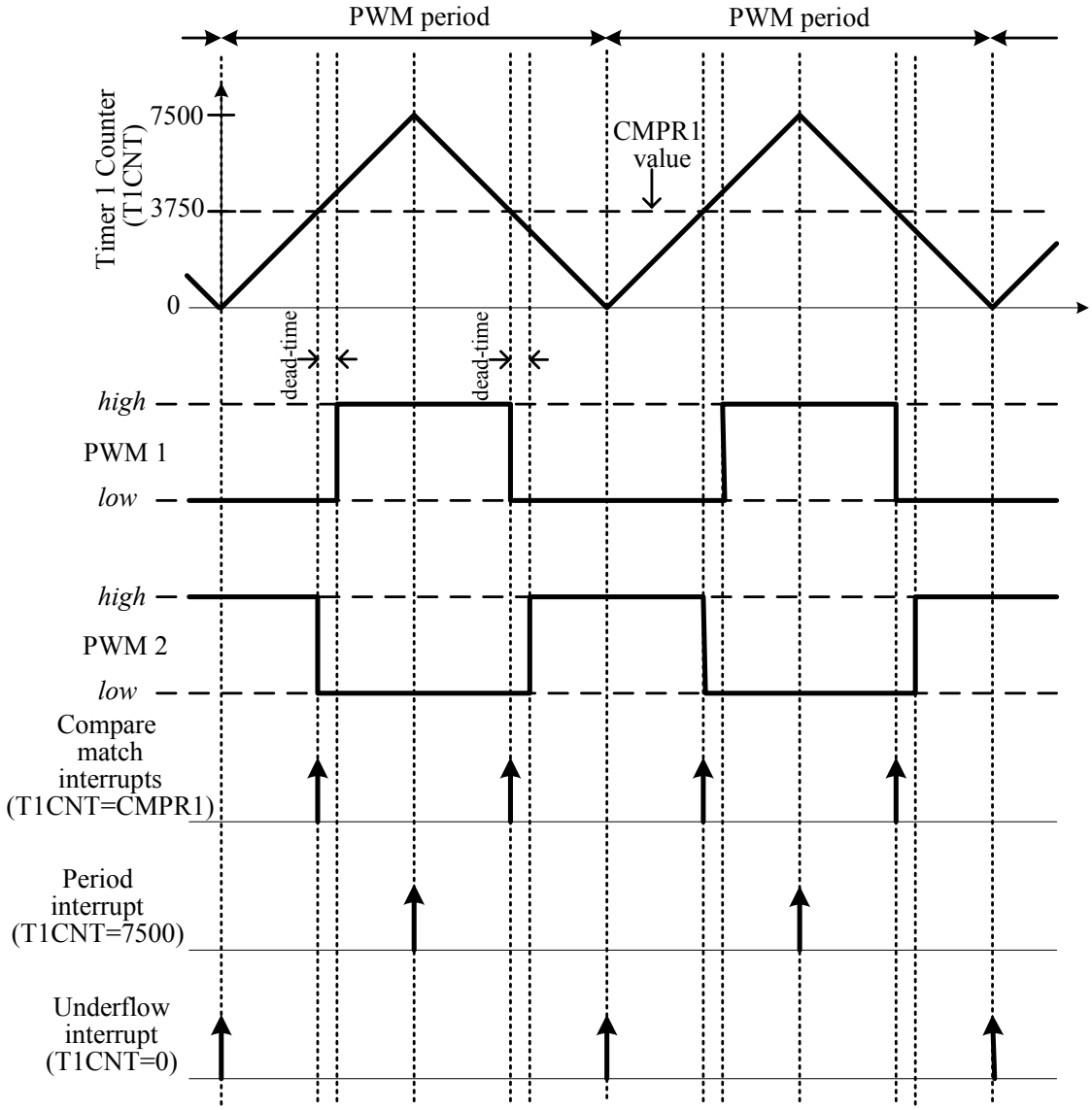


Figure 5.4 PWM pulse pattern generation method of TMS320F2812 illustrating the influence of dead-time and loading at the peak or bottom of the triangle.

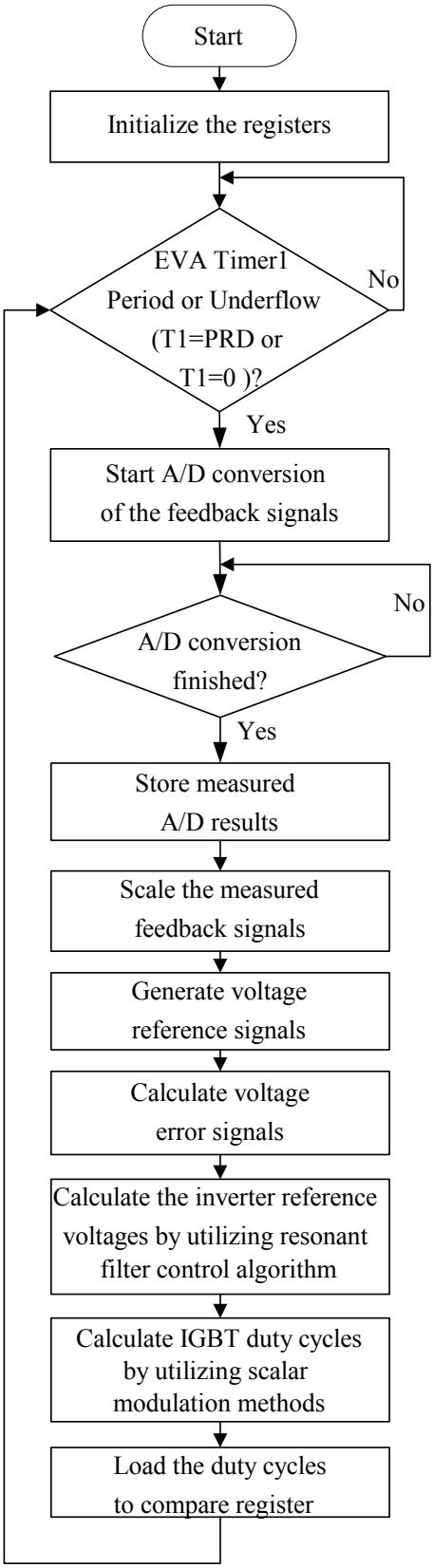


Figure 5.5 The flowchart of the main DSP program for UPS output voltage control.

5.3. Experimental Investigations

In this section, the performance of the four-leg inverter based three-phase UPS system is evaluated experimentally. As a first step, the output voltage control system is considered. The resonant filter bank based controllers are designed and the control parameters obtained in the previous chapter are utilized. The design is verified by the same study as in the associated section of the previous chapter. Following the completion of the controller design stage, the steady-state performance of the UPS system is evaluated under various loading conditions such as linear, nonlinear, balanced, and unbalanced load. Then the dynamic performance of the UPS is examined under severe loading transients. The final section of this chapter involves investigation of the switching ripple and switching loss characteristics of the scalar PWM methods. Specifically the modulator developed in this thesis, the MLDPWM method will be investigated in detail and compared to other modulators in terms of overall performance.

Due to the difficulties involved in applying discontinuous PWM methods with double updated PWM outputs via the TMS320F2812, high dynamic response can not be obtained with these modulators. Because the PWM delay of half PWM cycle reduces the control system bandwidth significantly. However, this is a chip based limitation and when available other products with no such limitations can be utilized to overcome this limitation (for example, TMS320F2809).

In this thesis, as the available device is the TMS320F2812, the device limitation will have impact on the experiments. In order to demonstrate the capabilities of the four-leg inverter and the resonant filter bank based controller, high bandwidth system will be targeted. For this purpose, to study the control behavior of the UPS system, the SVPWM method which exhibits no deficiencies in terms of modulator performance will be utilized. The experiments involving the dynamic loading and output voltage regulation will be conducted with SVPWM operating at 10 kHz carrier frequency with double PWM update and double feedback signal measurement update (both at 50us). The experiments involving the modulator performance will be conducted at

20 kHz with single PWM update and single feedback signal measurement update (both at 50us). Thus, both experiments will have the same delay, but the carrier frequency will be different resulting in different current ripple values.

Throughout the experimental studies the waveform and power quality measurements are conducted with high performance measurement tools. While the waveform measurements are conducted with a 500 MHz four channel oscilloscope LeCroy Waverunner 6050A, the harmonic spectrum, voltage/current THD, voltage/current unbalance, CF, and voltage regulation data are obtained via the Fluke 434 model three-phase power analyzer which measures harmonics up to the 50^{th} harmonic.

5.3.1. Controller Implementation

The control method involved is the resonant filter bank structure, one bank per phase (Figure 3.19). In the controller voltage feedforward is utilized. In the experiments the switching frequency is set as 10 kHz and the sampling rate is set twice as the switching frequency, 20 kHz as in the simulations. The modulator utilized in this procedure is the SVPWM method throughout.

The control system parameters which were tuned by means of computer simulations in the previous chapter are utilized in the experimental stage. In this section, the performance of the controller for these parameters are experimentally evaluated and compared to the performance obtained by simulations (see Chapter 4, section 4.3.1). In the experiments the same load and operating conditions as those described in the pervious chapter (section 4.3.1) are utilized. The experimental results are summarized in Table 5.5, where the control parameter values, the sequence of tuned parameters, and the performance indicators are shown. The related output voltage waveforms and their harmonic spectrum are shown in Figure 5.6 through Figure 5.23. The experimental results throughout the study have been found quite similar to those obtained in the simulations of the previous chapter. This is due to the design accuracy of the inverter and design accuracy of the computer simulation model.

First open-loop controlled system output voltage and load current waveforms and the output voltage harmonic spectrum are illustrated in Figure 5.6 and Figure 5.7 respectively. As can be seen the output voltage is highly distorted. At this operating point THD_v is 11.2% and the voltage regulation is 5.52%. With the fundamental component controller VR is improved to 0.21% (Figure 5.8 and Figure 5.9). Since the fundamental component controller does not control the output voltage harmonics THD_v value is still poor (12.4%). Adding the harmonic component controllers to the resonant filter bank (stages III, IV, and V), harmonic components of the UPS output voltage are suppressed and the output voltage quality is improved (Figure 5.10 and Figure 5.11 for stage III, Figure 5.12 and Figure 5.13 for stage IV, Figure 5.14 and Figure 5.15 for stage V). The THD_v value is observed as 3.5% at stage V.

When the active damping loop enabled, harmonic components at higher frequencies are suppressed and the controller gains of the harmonic components at lower frequencies can be increased to higher values as the active damping loop increases the system stability (Figure 5.18 through Figure 5.23). It can be seen from the THD data on Table 5.5, the effect of the active damping loop in the experiment is not as strong as it was seen in the simulation. This is due to the fact that the experimental system has higher damping (losses, parasitic components, dead-time, etc.) than the simulation model. In the simulation the voltage THD decreases from 5.9% at stage V to 3.4% at stage VI. In the experiments THD values of 3.5% at stage V and 2.8% at stage VI are obtained. With the damping behavior exception, the simulation performance and experimental performance match with high accuracy as can be observed via comparison of Table 4.5 and Table 5.5.

In the experimental system, with the designed resonant filter controller, the THD_v is decreased from 11.2% at open-loop to 1.8% (Figure 5.22 and Figure 5.23) and the UPS output voltages are well-regulated, the VR value is decreased from 5.57% to 0.12%. Note that the crest factor of the load increases from 1.69 to nearly 2.6 and this is due to the fact that as the output impedance of the UPS is decreased by means of the control mechanism, the UPS becomes a more ideal voltage source and the nonlinear load draws more peaky currents from the UPS.

Table 5.5 Resonant filter controller gain tuning and steady-state performance improvement stages of the UPS output voltage (experimental results)

Stage	Controller	Gains	THD_v (%)	CF	VR (%)
I	Open loop	----------	11.2	1.69	5.52
II	Fundamental frequency controller added	K_{i1}=100, K_{pv}=0.05	12.4	1.80	0.21
III	5^{th} and 7^{th} harmonic controllers added	K_{i5}=15, K_{i7}=15	6.0	2.10	0.29
IV	11^{th} and 13^{th} harmonic controllers added	K_{i11}=3, K_{i13}=1	4.3	2.14	0.37
V	3^{rd} and 9^{th} harmonic controllers added	K_{i3}=5, K_{i9}=3	3.5	2.16	0.37
VI	Capacitor current feedback added, proportional gain increased	K_{ad}=15, K_{pv}=1	2.8	2.22	0.21
VII	5^{th} and 7^{th} harmonic controllers updated (K_{i5} and K_{i7} increased)	K_{i5}=75, K_{i7}=75	2.8	2.38	0.17
VIII	11^{th} and 13^{th} harmonic controllers updated (K_{i11} and K_{i13} increased)	K_{i11}=15, K_{i13}=10	1.9	2.54	0.13
IX	3^{rd} and 9^{th} harmonic controllers updated (K_{i3} and K_{i9} increased)	K_{i3}=50, K_{i9}=10	1.8	2.60	0.17

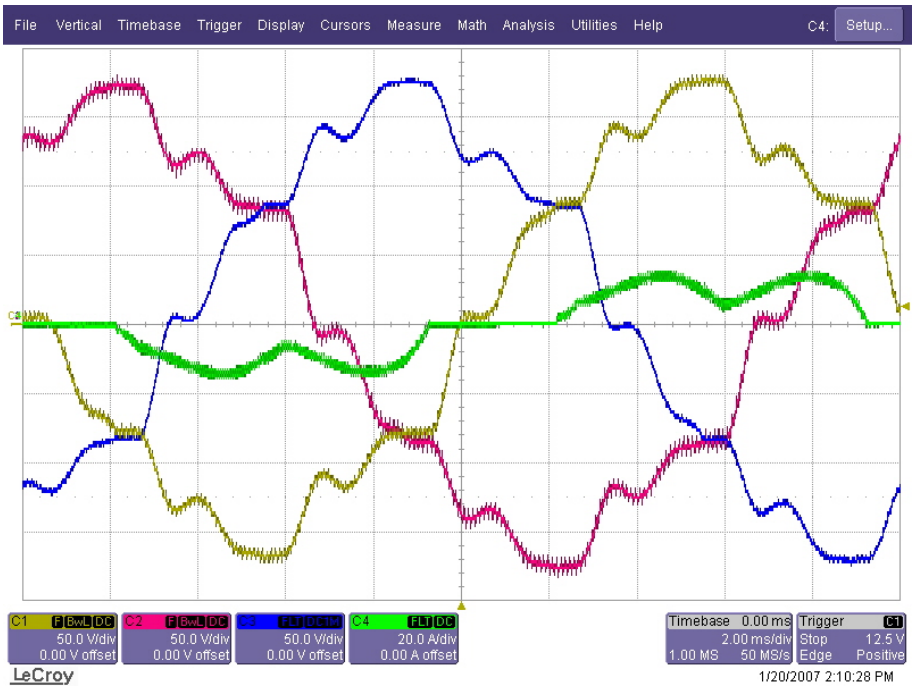


Figure 5.6 Three-phase output voltages and one phase load current during open-loop operation under balanced nonlinear full-load (Stage I of Table 5.5), (Scales: 50V/div, 20A/div, 2ms/div).

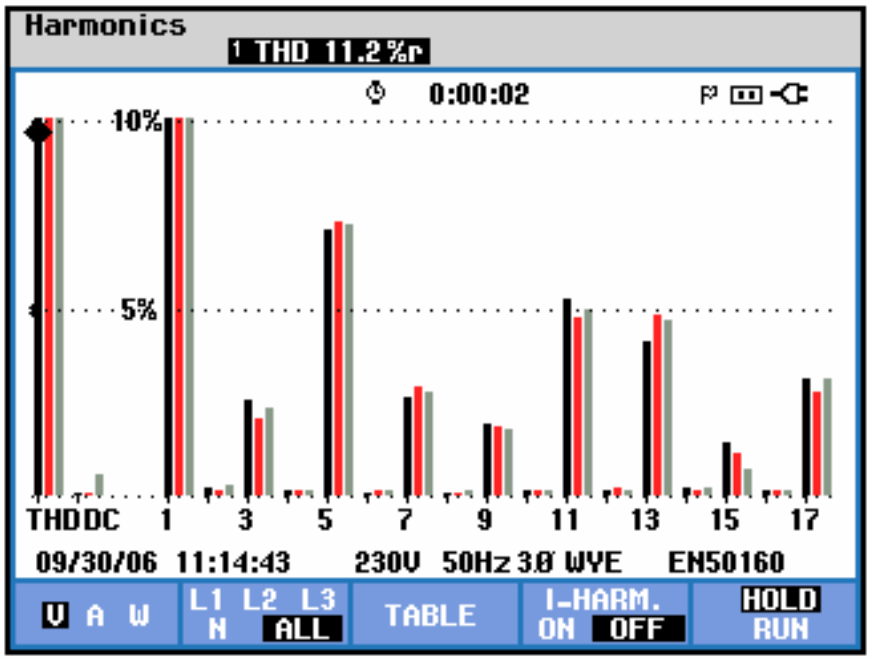


Figure 5.7 The harmonic spectrum of the three-phase output voltages during open-loop operation under balanced nonlinear full-load (Stage I of Table 5.5).

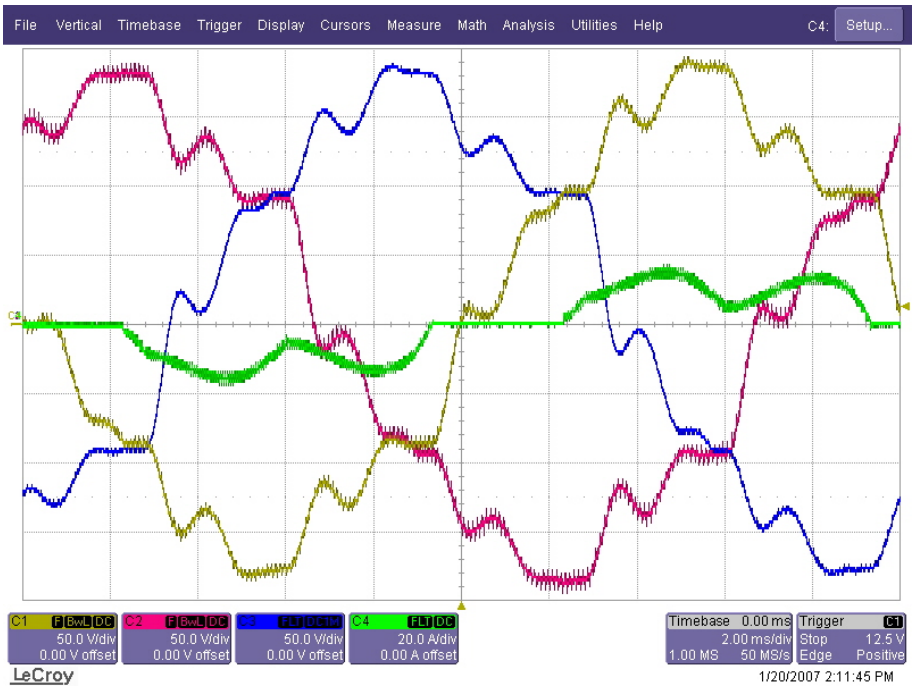


Figure 5.8 Three-phase output voltages and one phase load current during closed-loop operation under balanced nonlinear full-load (Stage II of Table 5.5), (Scales: 50V/div, 20A/div, 2ms/div).

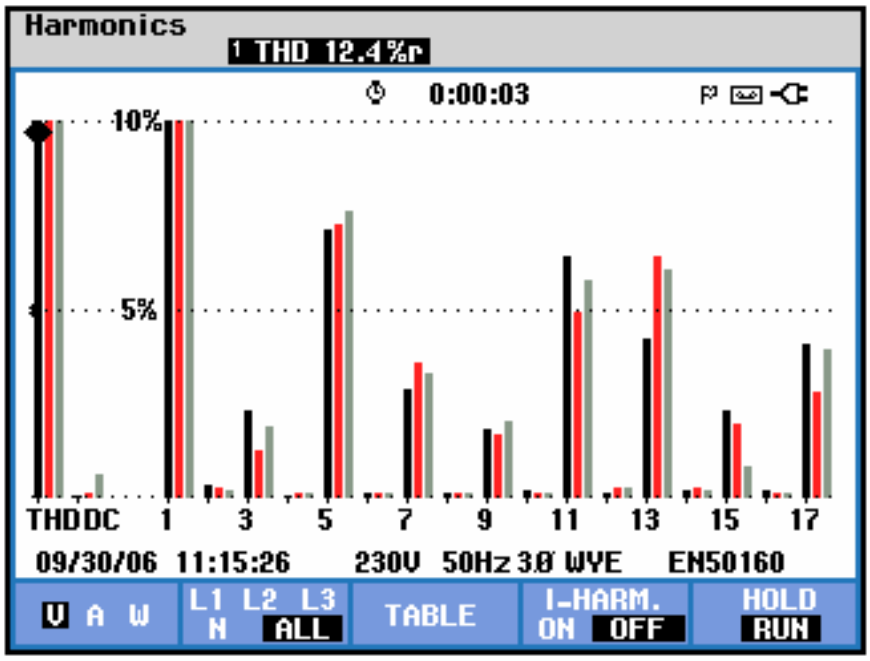


Figure 5.9 The harmonic spectrum of the three-phase output voltages during closed-loop operation under balanced nonlinear full-load (Stage II of Table 5.5).

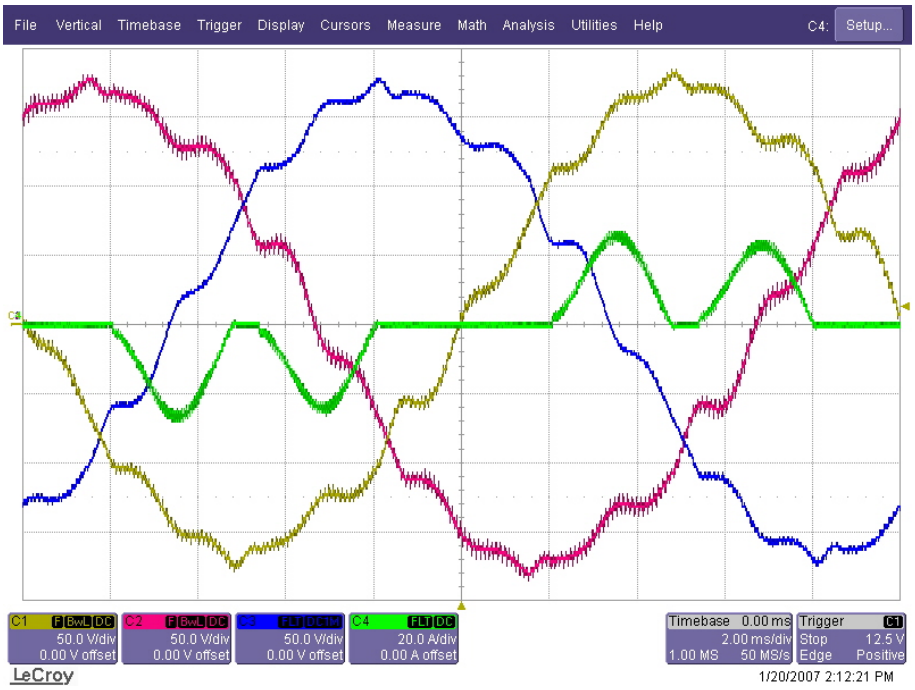


Figure 5.10 Three-phase output voltages and one phase load current during closed-loop operation under balanced nonlinear full-load (Stage III of Table 5.5), (Scales: 50V/div, 20A/div, 2ms/div).

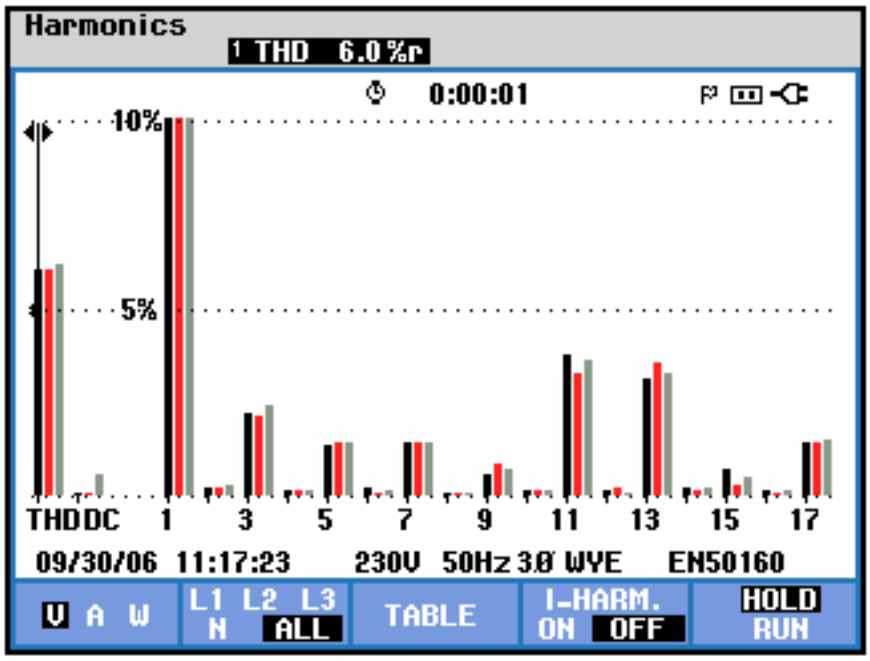


Figure 5.11 The harmonic spectrum of the three-phase output voltages during closed-loop operation under balanced nonlinear full-load (Stage III of Table 5.5).

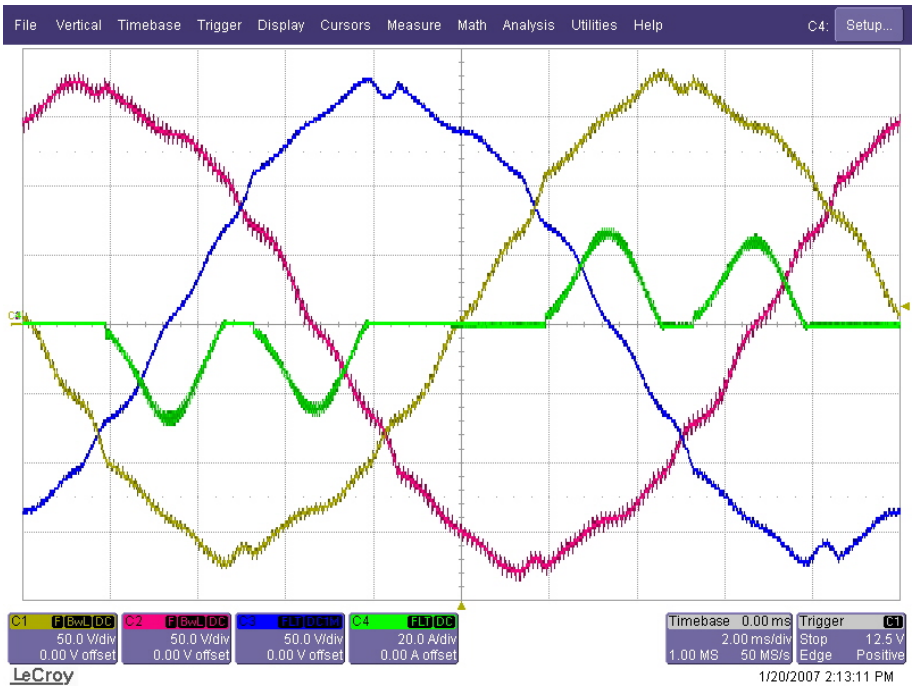


Figure 5.12 Three-phase output voltages and one phase load current during closed-loop operation under balanced nonlinear full-load (Stage IV of Table 5.5), (Scales: 50V/div, 20A/div, 2ms/div).

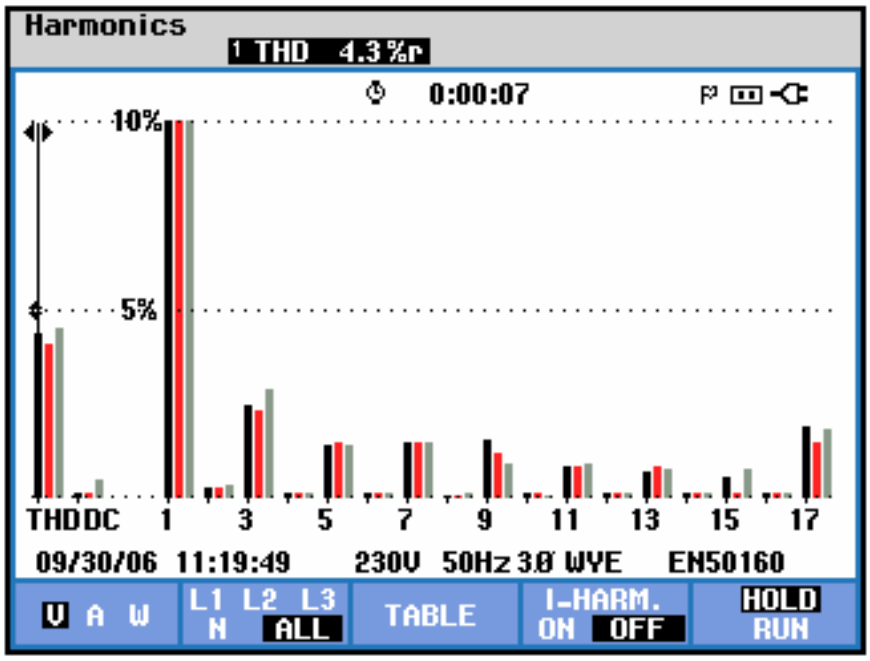


Figure 5.13 The harmonic spectrum of the three-phase output voltages during closed-loop operation under balanced nonlinear full-load (Stage IV of Table 5.5)

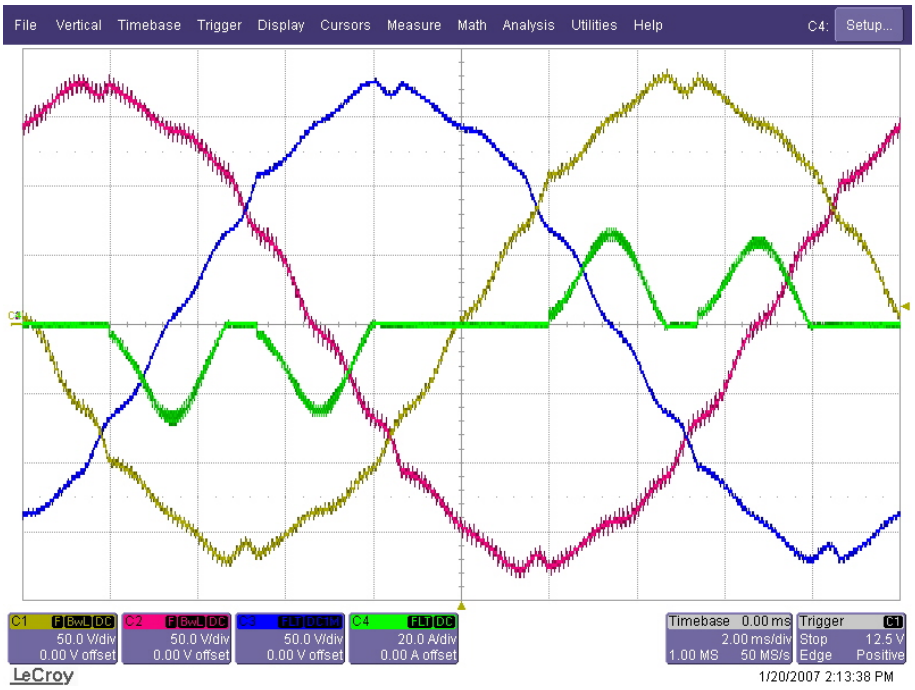


Figure 5.14 Three-phase output voltages and one phase load current during closed-loop operation under balanced nonlinear full-load (Stage V of Table 5.5), (Scales: 50V/div, 20A/div, 2ms/div).

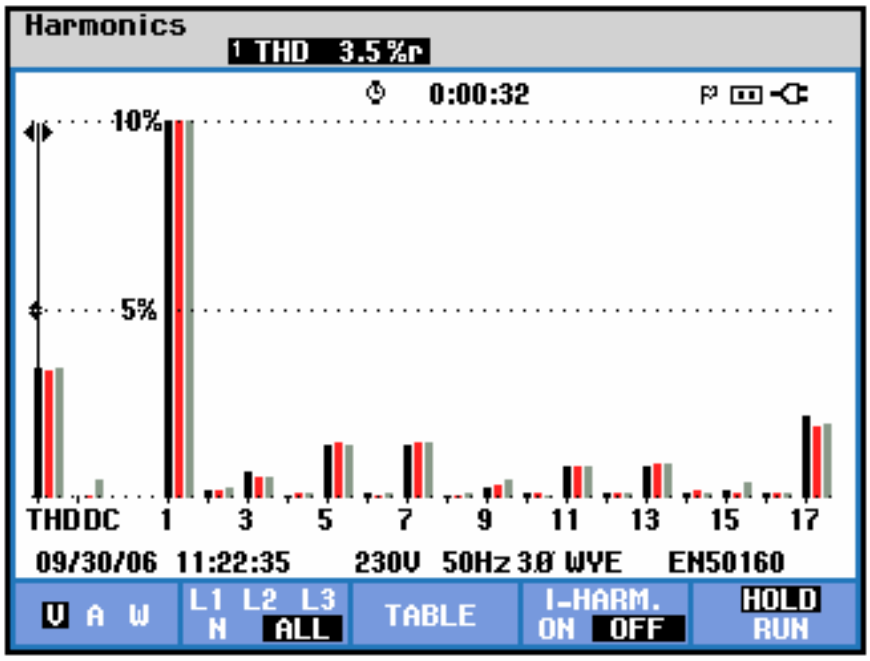


Figure 5.15 The harmonic spectrum of the three-phase output voltages during closed-loop operation under balanced nonlinear full-load (Stage V of Table 5.5)

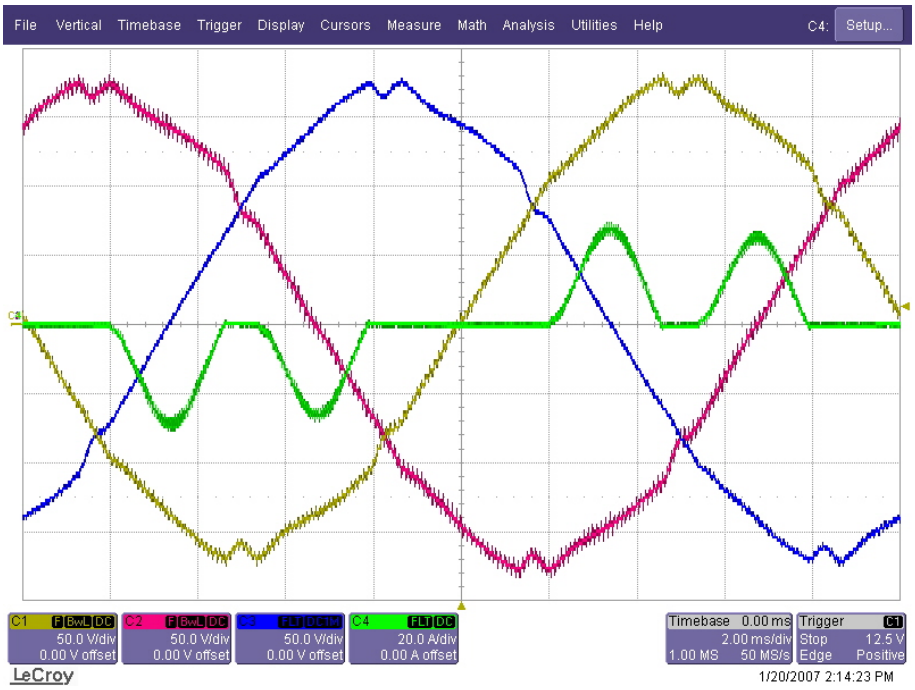


Figure 5.16 Three-phase output voltages and one phase load current during closed-loop operation under balanced nonlinear full-load (Stage VI of Table 5.5), (Scales: 50V/div, 20A/div, 2ms/div).

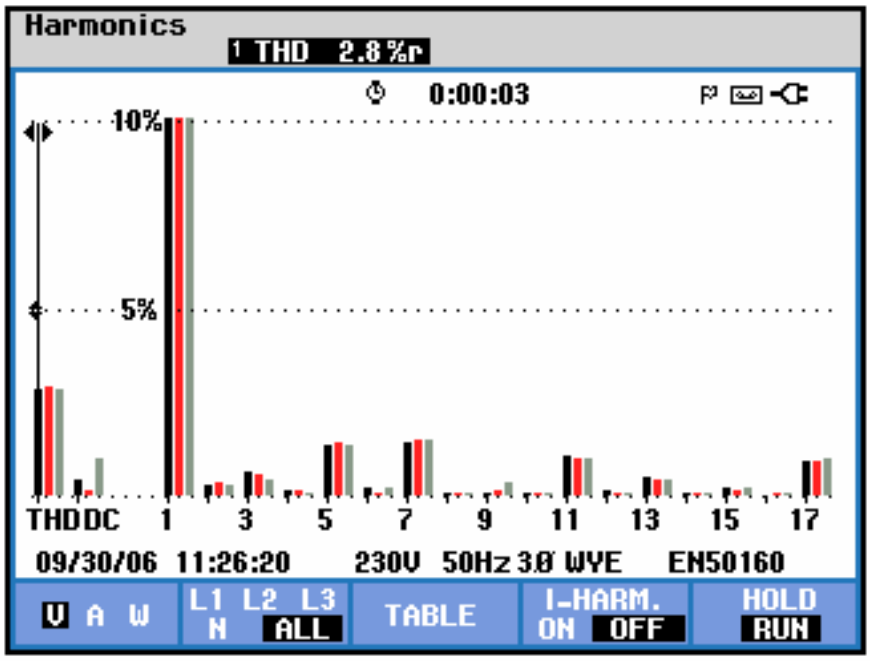


Figure 5.17 The harmonic spectrum of the three-phase output voltages during closed-loop operation under balanced nonlinear full-load (Stage VI of Table 5.5).

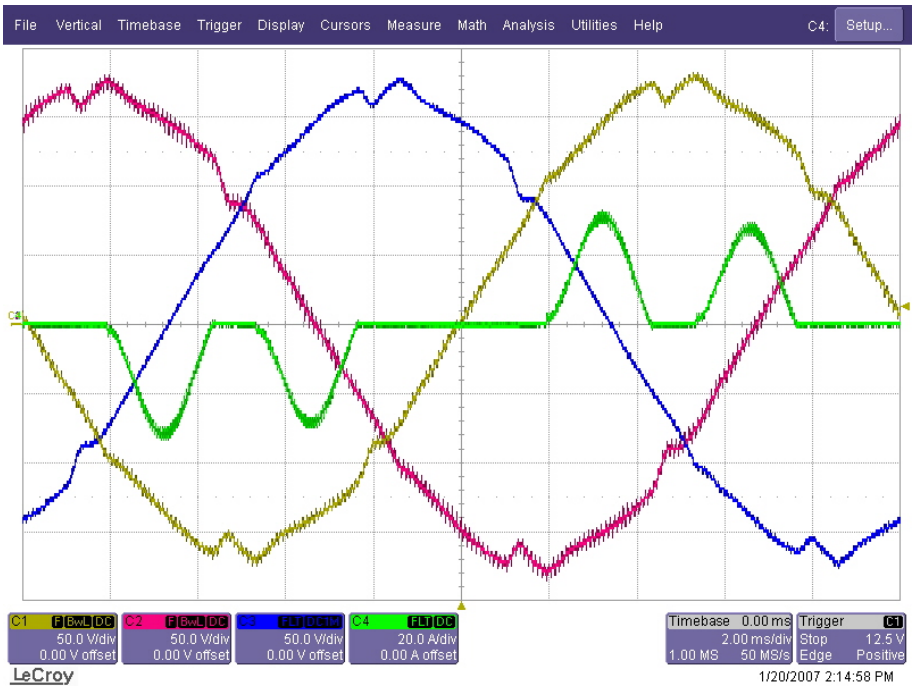


Figure 5.18 Three-phase output voltages and one phase load current during closed-loop operation under balanced nonlinear full-load (Stage VII of Table 5.5), (Scales: 50V/div, 20A/div, 2ms/div).

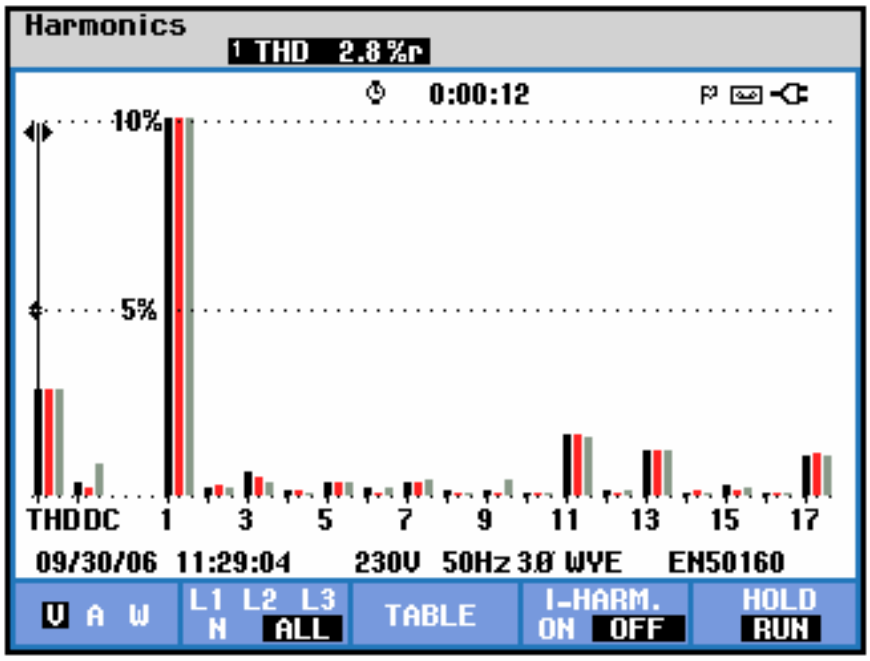


Figure 5.19 The harmonic spectrum of the three-phase output voltages during closed-loop operation under balanced nonlinear full-load (Stage VII of Table 5.5)

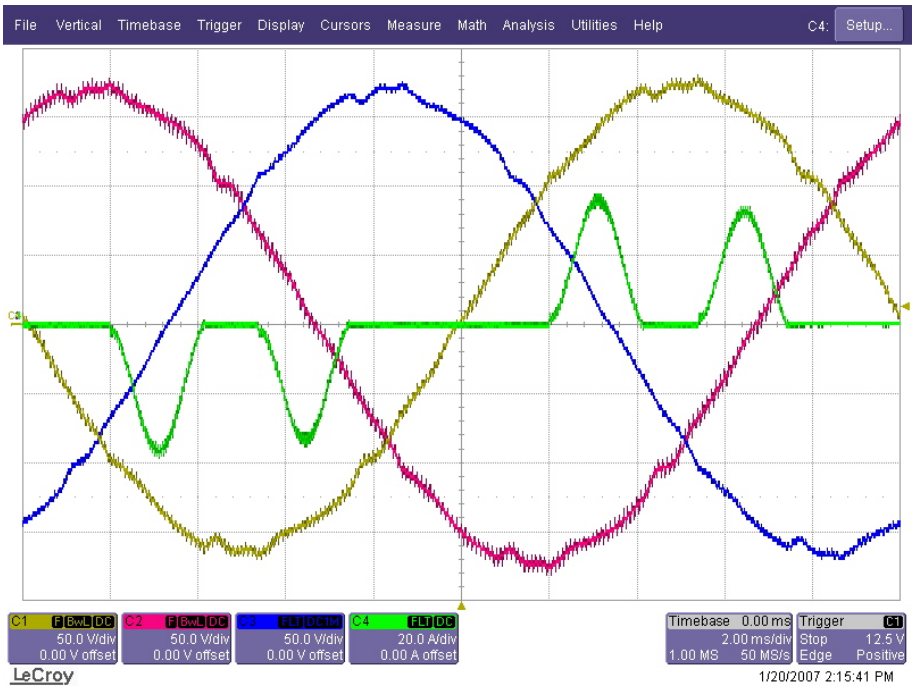


Figure 5.20 Three-phase output voltages and one phase load current during closed-loop operation under balanced nonlinear full-load (Stage VIII of Table 5.5), (Scales: 50V/div, 20A/div, 2ms/div).

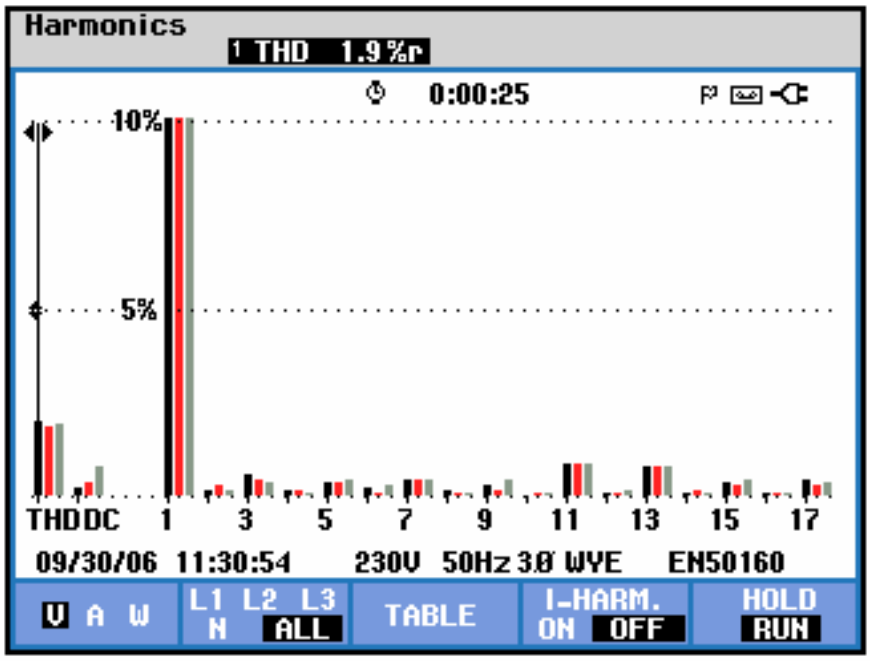


Figure 5.21 The harmonic spectrum of the three-phase output voltages during closed-loop operation under balanced nonlinear full-load (Stage VIII of Table 5.5)

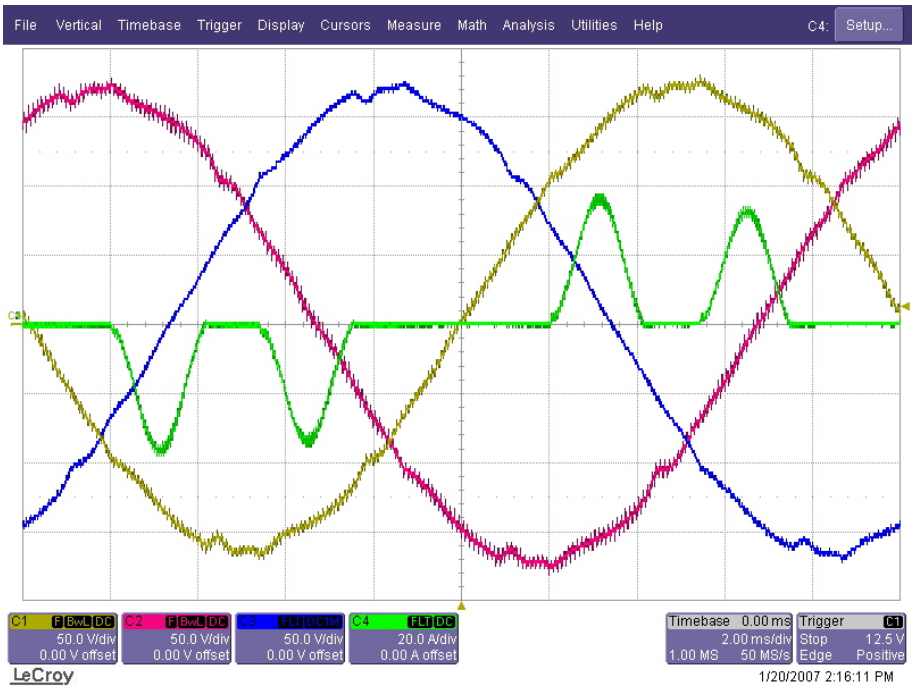


Figure 5.22 Three-phase output voltages and one phase load current during closed-loop operation under balanced nonlinear full-load (Stage IX of Table 5.5), (Scales: 50V/div, 20A/div, 2ms/div).

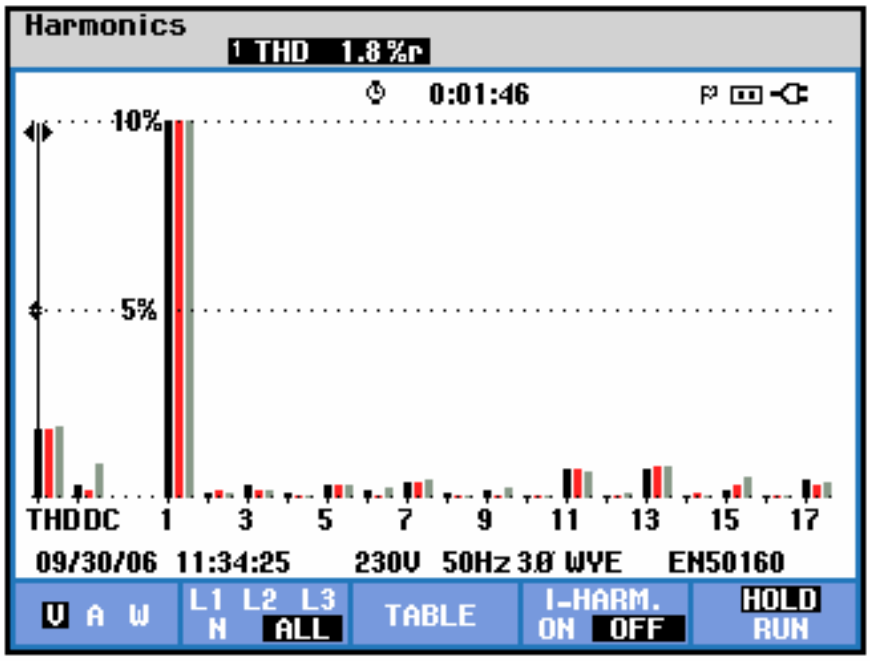


Figure 5.23 The harmonic spectrum of the three-phase output voltages during closed-loop operation under balanced nonlinear full-load (Stage IX of Table 5.5).

5.3.2. Experimental Steady-State Performance Evaluation of The Resonant Filter Controller at Various Operating Conditions

The resonant filter controller designed in the previous section is tested under various steady-state operating conditions and its performance indices are displayed and compared for the purpose of evaluating the feasibility of the method. No-load, linear balanced and unbalanced full-load, and nonlinear balanced and unbalanced full-load operating conditions are considered and experimental results are summarized. The SVPWM method with 10 kHz carrier and 20 kHz sampling and update rate is utilized throughout these experiments. The UPS output ratings are the same as those listed in Table 5.1. Therefore, the load parameters are also the same as in computer simulations (Table 4.3 and Table 4.4).

The controller structure to be utilized in this section is the same as the previous section and also shown in Figure 3.19. In order to illustrate the influence of each controller component on the steady-state performance, various controller combinations will be considered. The controller cases and the performance results are listed in Table 5.6 and Table 5.7. In these tables the controllers are labeled as Case A, Case B, Case C, and Case D. These cases are the same as those described in the computer simulation studies of section 4.3.2 of Chapter 4. In the tables in this section, in addition to the performance results of the computer simulation studies, the load current and output voltage unbalances defined in terms of the negative and zero sequence unbalances are reported. The data could be obtained by utilizing the Fluke 434 power analyzer which measures and calculates these quantities. With these quantities being available, the degree of unbalance could also be observed and important results associated with these characteristics could be emphasized. The experimental results of Table 5.6 and Table 5.7 are supported with voltage and current oscilloscope waveforms shown in Figure 5.24 to Figure 5.43. In the oscillograms only the open-loop control and Case D control cases are shown.

Table 5.6 The steady-state performance at no-load and linear load conditions
(A range is given when noticeable differences exist among three-phase quantities)

		Open loop	Without capacitor current feedback		With capacitor current feedback	
			The fundamental component is controlled (A)	The fundamental and harmonic components are controlled (B)	The fundamental component is controlled (C)	The fundamental and harmonic components are controlled (D)
No-load	THD_V (%)	1.40	1.50	1.1	0.8	0.40
	V_{neg} (%)	0.3	0.3	0.4	0.4	0.4
	V_{zero} (%)	0.3	0.5	0.4	0.4	0.4
Linear balanced load	CF	1.44	1.44	1.44	1.44	1.44
	VR (%)	7.43	0.25	0.22	0.16	0.13
	THD_V (%)	3.10	3.30	1.10	1.70	0.50
	V_{neg} (%)	0.3	0.4	0.4	0.4	0.4
	V_{zero} (%)	0.2	0.5	0.5	0.5	0.5
	I_{neg} (%)	0.6	0.6	0.7	0.7	0.7
	I_{zero} (%)	0.5	0.9	0.9	0.9	0.9
Linear line-neutral unbalanced load	CF	1.48	1.47	1.45	1.45	1.44
	VR (%)	9.0~16.83	0.08~0.33	0~0.25	0.16~0.50	0.08~0.42
	THD_V (%)	3.2~6.5	3.8~5.9	1.1~1.6	1.8~3.2	0.6~0.7
	V_{neg} (%)	3.8	0.3	0.3	0.3	0.3
	V_{zero} (%)	13.8	0.8	0.8	0.8	0.8
	I_{neg} (%)	100	100	100	100	100
	I_{zero} (%)	100	100	100	100	100
Linear line-line unbalanced load	CF	1.45	1.44	1.44	1.43	1.43
	VR (%)	2.39~7.7	0.08~0.33	0.08~0.33	0.0~0.17	0.0~0.17
	THD_V (%)	1.4~3.7	1.5~3.5	1.0~1.2	0.8~1.70	0.5~0.6
	V_{neg} (%)	6.3	0.2	0.2	0.2	0.2
	V_{zero} (%)	2.1	0.4	0.4	0.4	0.4
	I_{neg} (%)	100	100	100	100	100
	I_{zero} (%)	0.2	0.2	0.2	0.2	0.2

The no-load operation of the UPS with open-loop control results in some waveform distortion (Figure 5.24). However, the closed-loop operation yields high waveform quality (Figure 5.25).

For linear balanced full-load operating condition, the open-loop operation mode gives a noticable output voltage waveform distortion due to the inverter dead-time (Figure 5.26 and Figure 5.27). The output voltage THD is 3.1% and the voltage regulation is 7.43% for this operating condition. This distortion could not be seen in the simulations (compare to Figure 4.21) as the inverter model in the simulation did not include a dead-time generator. When the UPS feeds the same load with the closed-loop controller, the waveform distortion is substantially reduced (Figure 5.28 and Figure 5.29). With the closed loop controller the output voltage THD decreases to 0.5% and voltage regulation to 0.13%.

Both the line-to-neutral linear unbalanced load and the line-to-line linear unbalanced load cases for the open-loop operating conditions illustrate the open loop control method is insufficient as far as the output voltage waveform quality (Figure 5.30, Figure 5.31, Figure 5.34 Figure 5.35). Closed-loop control case D results in high performance for all these cases (Figure 5.32, Figure 5.33, Figure 5.36 Figure 5.37). For the line-to-neutral unbalanced load, the output voltage unbalance has 13.8% zero sequence unbalance and 3.8% negative sequence unbalance for the open-loop operating condition. For the line-to-line unbalanced load, the zero sequence unbalance is 2.1% and the negative sequence unbalance is 6% for the open-loop operating condition. For both cases, closed loop operation results in a high output voltage waveform quality with an unbalance of less than 1%. In both cases, the output voltage improvement reflects on the load current which becomes a cleaner sinusoidal wave.

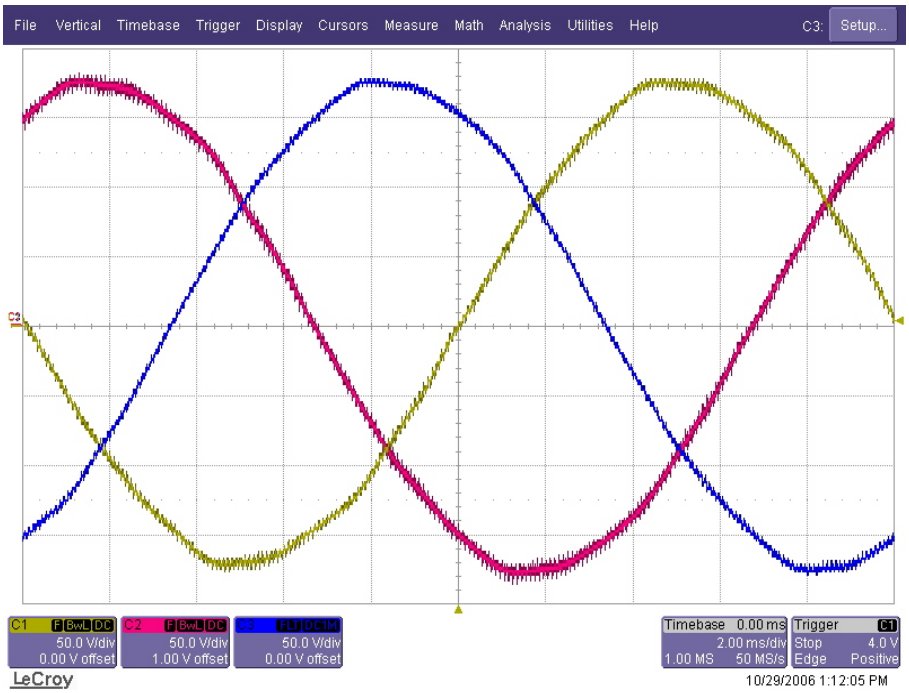


Figure 5.24 Steady-state three-phase output voltages during open-loop operation under no-load condition (Scales: 50V/div, 2ms/div).

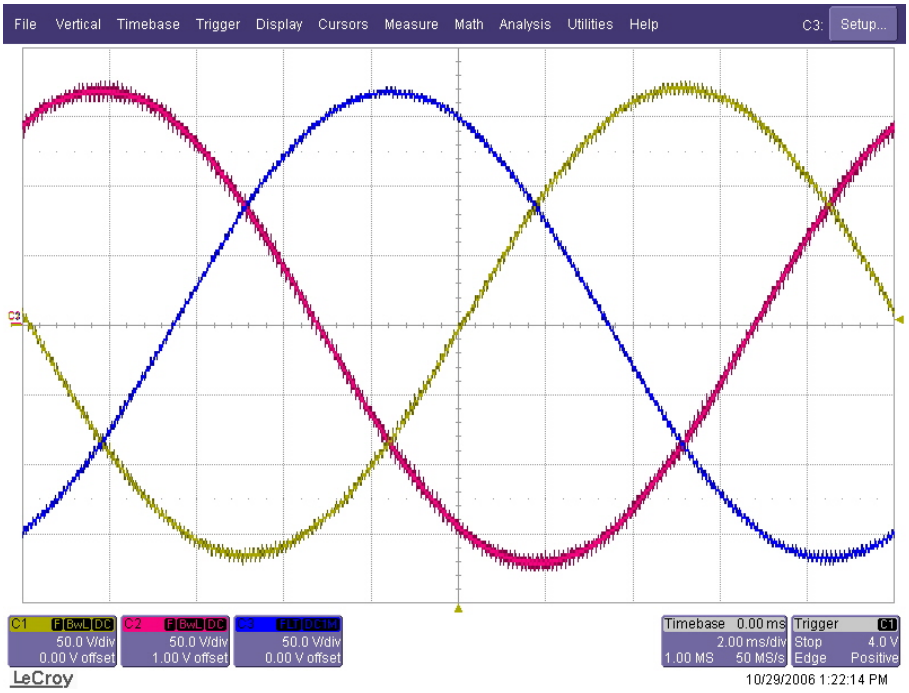


Figure 5.25 Steady-state three-phase output voltages during closed-loop operation under no-load condition (Scales: 50V/div, 2ms/div).

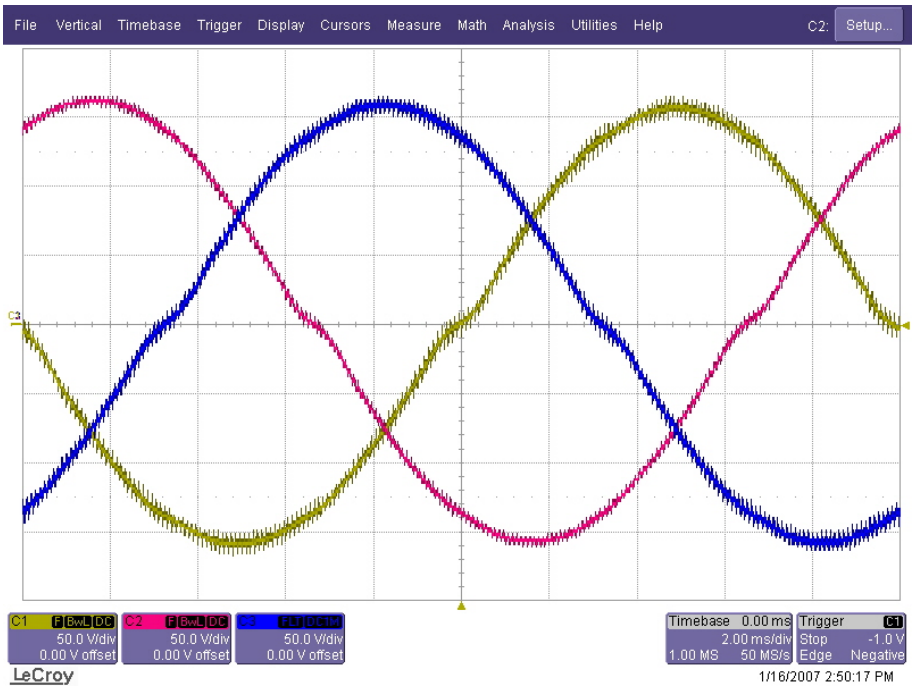


Figure 5.26 Steady-state three-phase output voltages during open-loop operation under linear balanced load (Scales: 50V/div, 2ms/div).

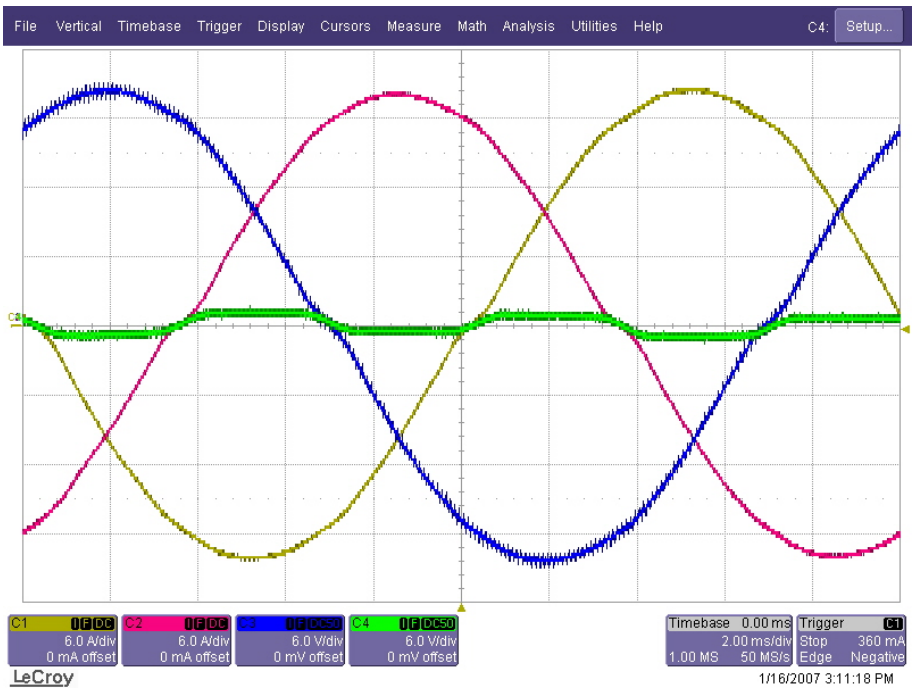


Figure 5.27 Steady-state load currents during open-loop operation under linear balanced load (Scales: 6A/div, 2ms/div).

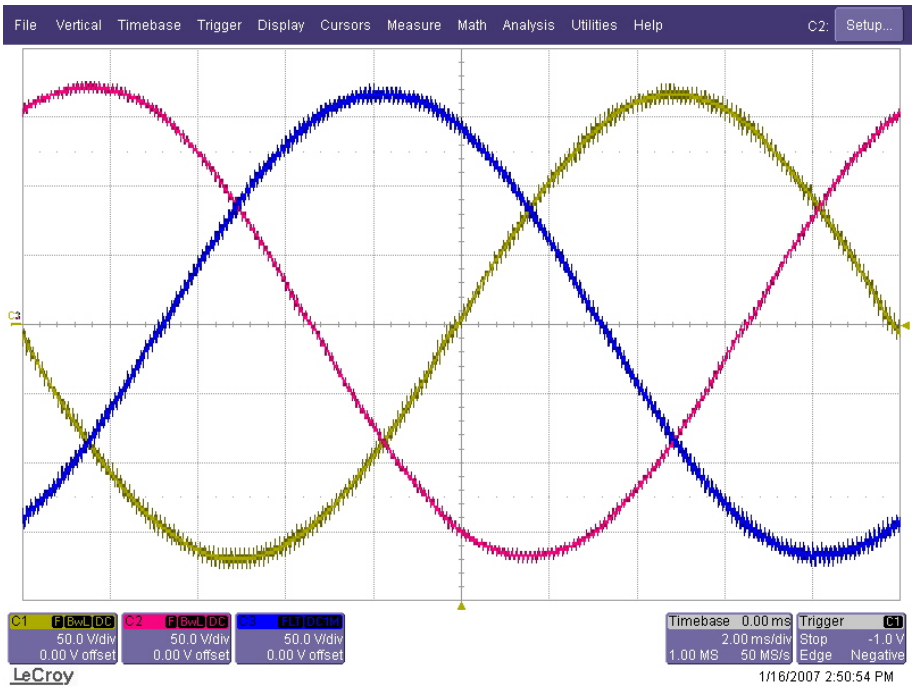


Figure 5.28 Steady-state three-phase output voltages during closed-loop operation under linear balanced load (Scales: 50V/div, 2ms/div).

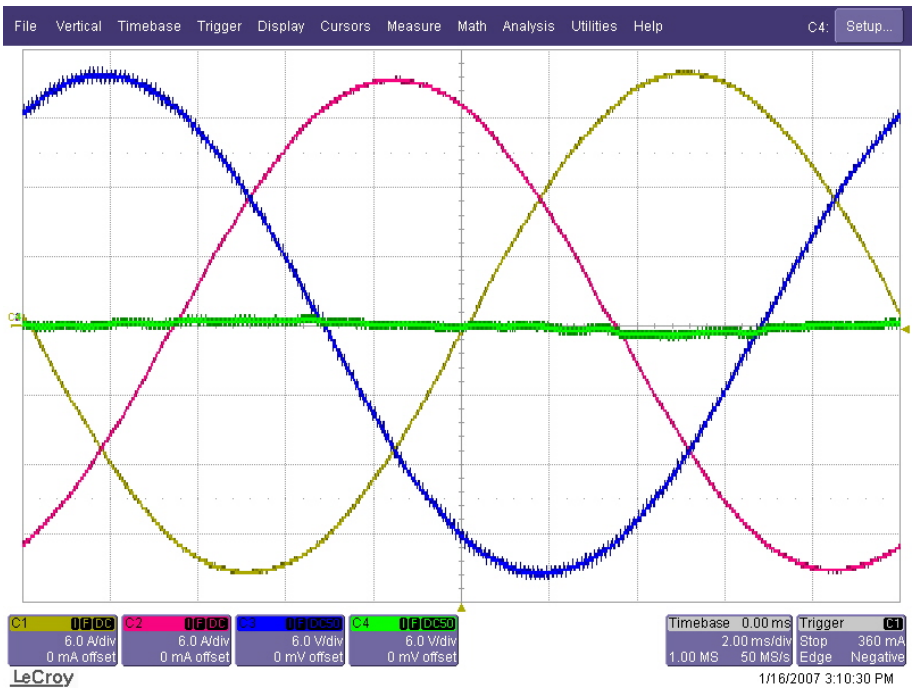


Figure 5.29 Steady-state load currents during closed-loop operation under linear balanced load (Scales: 6A/div, 2ms/div).

Figure 5.30 Steady-state three-phase output voltages during open-loop operation under linear line-neutral unbalanced load (Scales: 50V/div, 2ms/div).

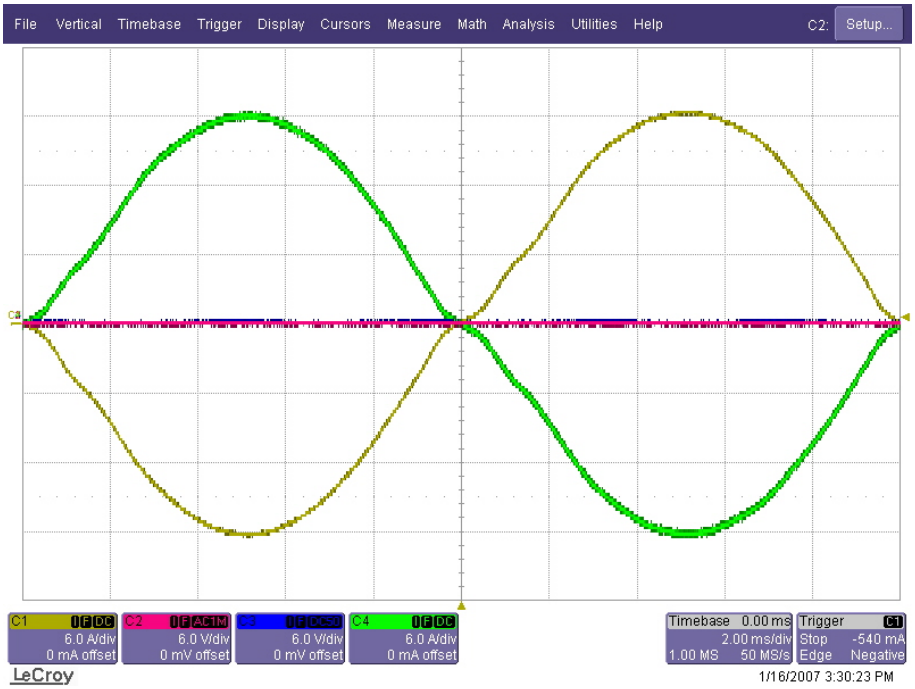


Figure 5.31 Steady-state load currents during open-loop operation under linear line-neutral unbalanced load (Scales: 6A/div, 2ms/div).

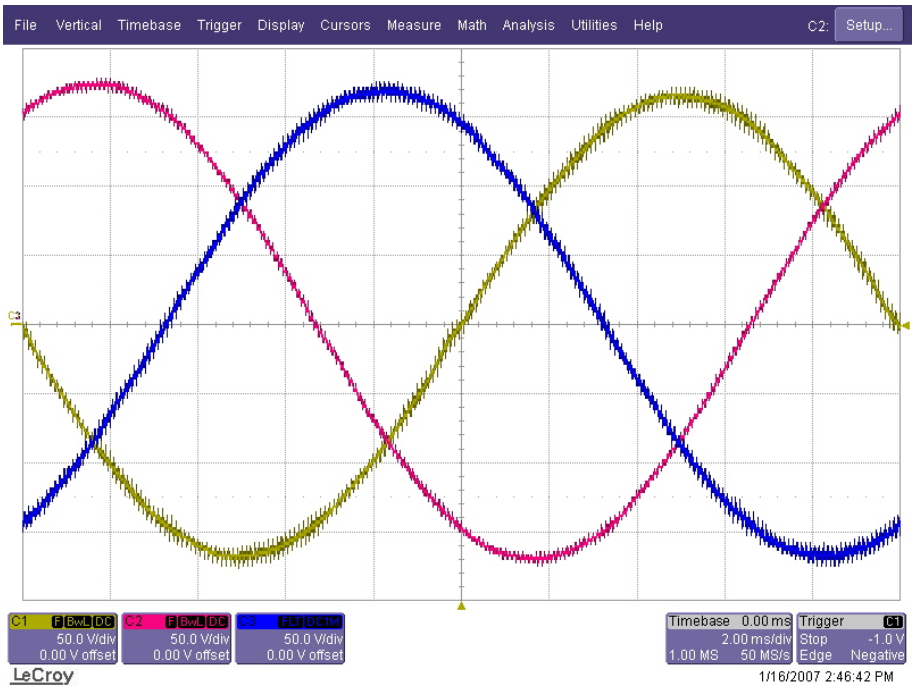


Figure 5.32 Steady-state three-phase output voltages during closed-loop operation under linear line-neutral unbalanced load (Scales: **50V**/div, 2ms/div).

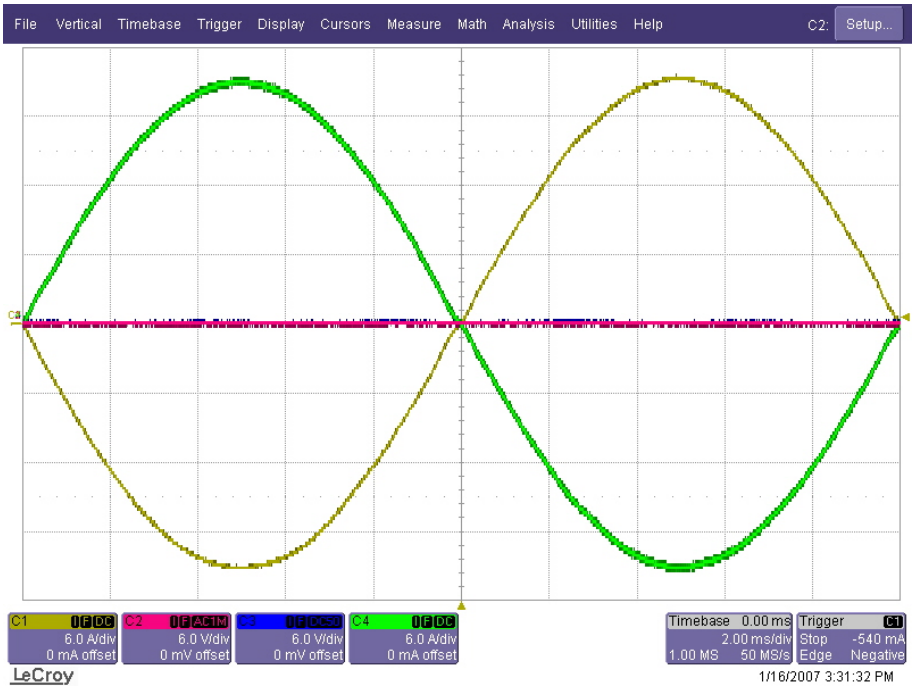


Figure 5.33 Steady-state load currents during closed-loop operation under linear line-neutral unbalanced load (Scales: 6A/div, 2ms/div).

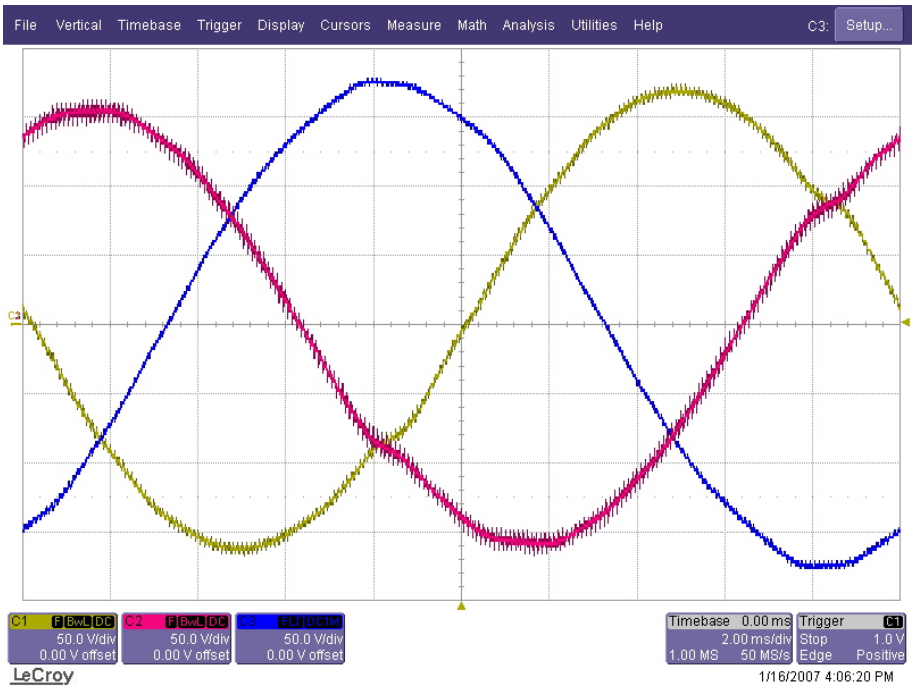


Figure 5.34 Steady-state three-phase output voltages during open-loop operation under linear line-line unbalanced load (Scales: **50V**/div, 2ms/div).

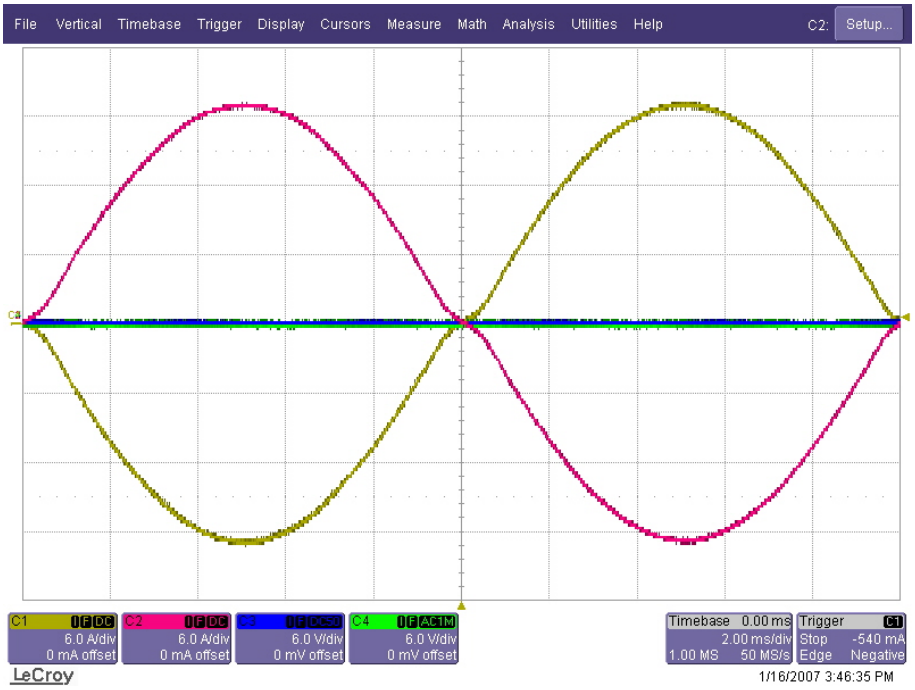


Figure 5.35 Steady-state load currents during open-loop operation under linear line-line unbalanced load (Scales: 6A/div, 2ms/div).

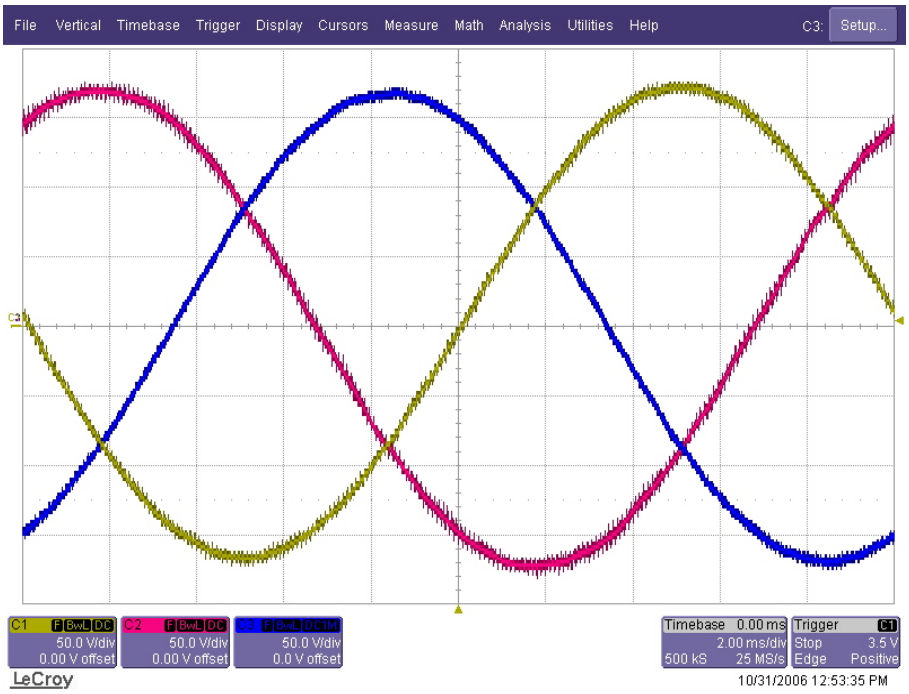


Figure 5.36 Steady-state three-phase output voltages during closed-loop operation under linear line-line unbalanced load (Scales: 50V/div, 2ms/div).

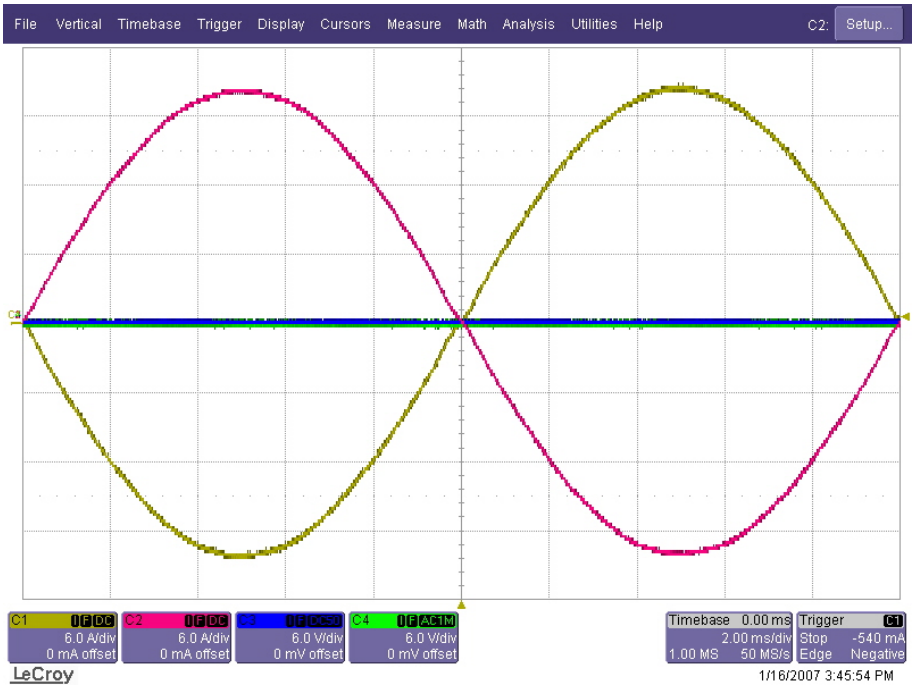


Figure 5.37 Steady-state load currents during closed-loop operation under linear line-line unbalanced load (Scales: 6A/div, 2ms/div).

Table 5.7 The steady-state performance at nonlinear load conditions

(A range is given when noticeable differences exist among the three-phase quantities)

		Open loop	Without capacitor current feedback		With capacitor current feedback	
			The fundamental component is controlled (A)	The fundamental and harmonic components are controlled (B)	The fundamental component is controlled (C)	The fundamental and harmonic components are controlled (D)
Nonlinear balanced load	CF	1.68	1.76	2.20	1.90	2.60
	VR (%)	5.12	0.45	0.24	0.08	0.04
	THD_V (%)	11.4	12.60	3.50	6.30	1.80
	V_{neg} (%)	0.2	0.3	0.3	0.3	0.3
	V_{zero} (%)	0.3	0.5	0.5	0.4	0.5
	I_{neg} (%)	3.5	9.1	4.4	5.9	4.1
	I_{zero} (%)	0.1	0.3	0.2	0.2	0.2
Nonlinear line-neutral unbalanced load	CF	2.27	2.38	2.75	2.54	3.25
	VR (%)	6.85~9.80	0.16~0.24	0.08	0.08~0.42	0.0~0.25
	THD_V (%)	4.9~13.6	6.0~14.7	1.7~4.4	3.3~9.2	0.9~2.4
	V_{neg} (%)	2.9	0.3	0.3	0.4	0.3
	V_{zero} (%)	8.6	0.6	0.6	0.6	0.6
	I_{neg} (%)	100	100	100	100	100
	I_{zero} (%)	100	100	100	100	100
Nonlinear line-line unbalanced load	CF	2.30	2.35	2.77	2.52	3.24
	VR (%)	2.6~3.85	0.08~0.42	0.08~0.17	0.08~0.16	0.08~0.16
	THD_V (%)	1.6~11.2	1.7~12.2	1.0~4.1	0.7~6.5	0.6~1.9
	V_{neg} (%)	4.6	0.2	0.2	0.3	0.3
	V_{zero} (%)	1.6	0.5	0.4	0.4	0.4
	I_{neg} (%)	100	100	100	100	100
	I_{zero} (%)	0.2	0.2	0.1	0.1	0.3

For the nonlinear full-load balanced operation the open-loop control method gives a poor output voltage waveform with poor regulation (THD_v=11.4% and VR=5.12%, Figure 5.38). As a result the load current crest factor becomes poor (1.68). Closed-loop operation yields superior results (THD_v=1.8% and VR<0.1%, Figure 5.39). With closed-loop control the output voltage waveform becomes a cleaner waveform yielding a load current crest factor of 2.6. this result illustrates the order of reduction in the UPS output impedance.

Similar to the linear load under load unbalance case, the nonlinear unbalanced load has the same detrimental effect on the output voltage during open-loop operation, be it line-to-neutral or line-to-line load unbalance. For the line-to-neutral nonlinear unbalanced load the open-loop operating condition yields nearly a square shaped output voltage waveform on the loaded phase (Figure 5.40). The triplen harmonics become dominant on the waveform. The voltage THD for this phase is 13.6% while it is less in the other phases. In this case the crest factor is approximately 2.27. Since this is a single-phase type load, the zero sequence unbalance of the output voltage is 8.6% compared to the negative sequence unbalance of 2.9%. With closed-loop control, the output voltage distortion could be decreased to less than 2.4% for the loaded phase and significantly less in the other phases. In this case the crest factor increases to approximately 3.25 which means the UPS output impedance has been lowered by means of the resonant filter banks. In this case the output voltage unbalance is below 1% for both zero and negative sequence unbalance (Figure 5.41). The nonlinear line-to-line unbalanced rated load for open-loop control yields an output voltage distortion of 10% and a poor regulation of 4%. This results in a crest factor of 2.3 for the load current (Figure 5.42). Closed-loop operation restores the output voltage distortion to 1.9% and the voltage regulation to less than 0.16. The crest factor increases to 3.24 indicating again significant reduction in the UPS output impedance (Figure 5.43).

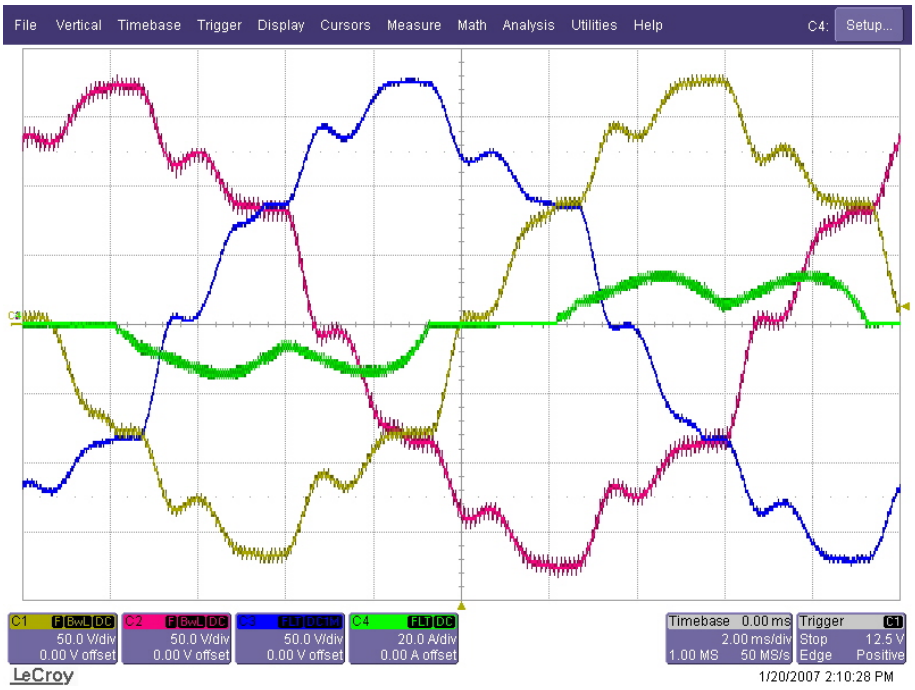


Figure 5.38 Steady-state three-phase output voltages and one phase load current during open-loop operation under nonlinear balanced load (Scales: 50V/div, 20A/div, 2ms/div).

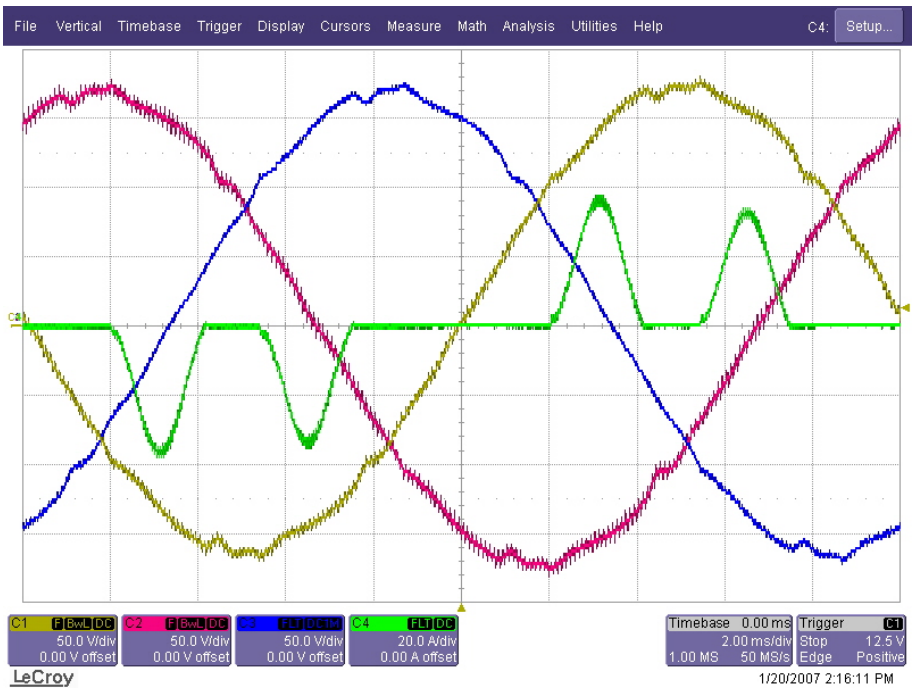


Figure 5.39 Steady-state three-phase output voltages and one phase load current during closed-loop operation under nonlinear balanced load (Scales: 50V/div, 20A/div, 2ms/div).

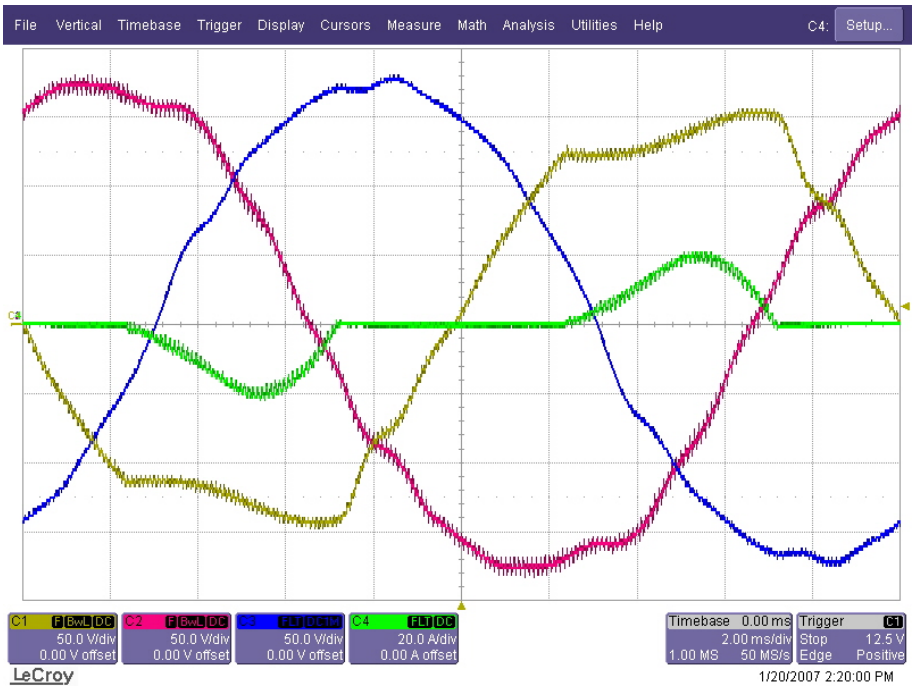


Figure 5.40 Steady-state three-phase output voltages and one phase load current during open-loop operation under nonlinear line-neutral unbalanced load (Scales: 50V/div, 20A/div, 2ms/div).

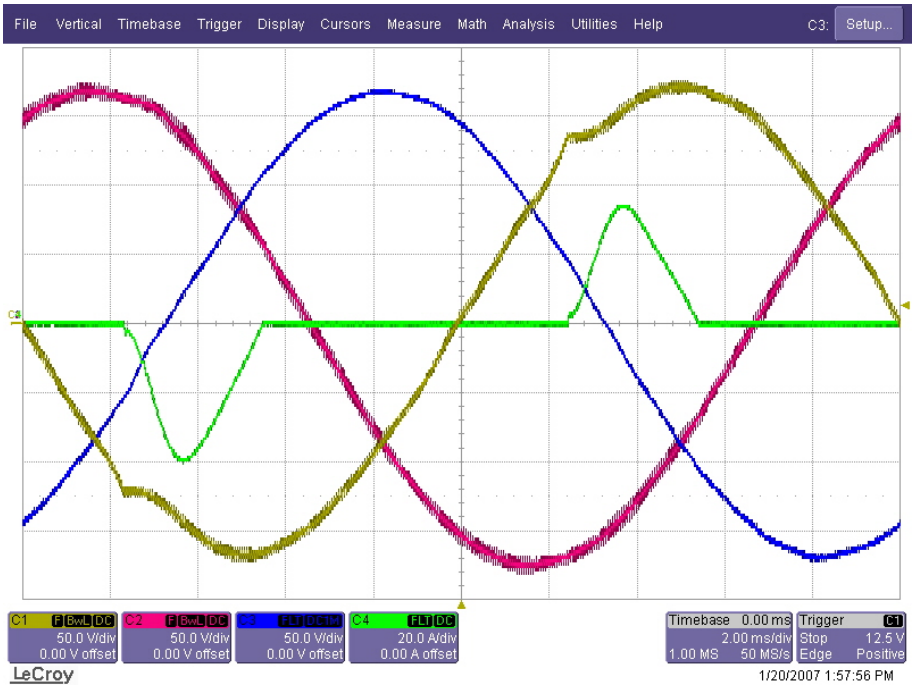


Figure 5.41 Steady-state three-phase output voltages and one phase load current during closed-loop operation under nonlinear line-neutral unbalanced load (Scales: 50V/div, 20A/div, 2ms/div).

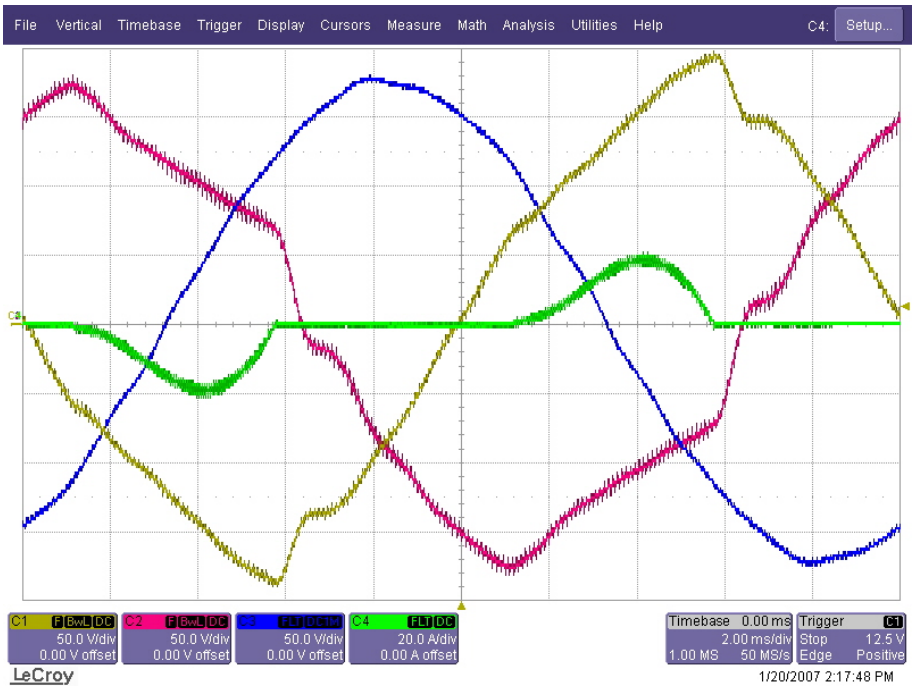


Figure 5.42 Steady-state three-phase output voltages and one phase load current during open-loop operation under nonlinear line-to-line unbalanced load (Scales: 50V/div, 20A/div, 2ms/div).

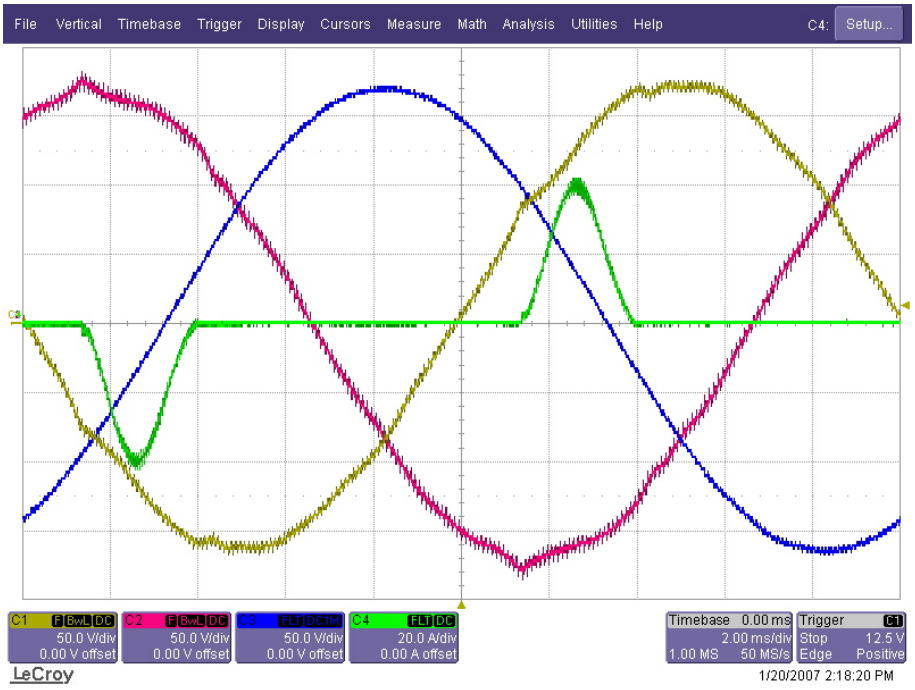


Figure 5.43 Steady-state three-phase output voltages and one phase load current during closed-loop operation under nonlinear line-line unbalanced load (Scales: 50V/div, 20A/div, 2ms/div).

Based on the experimental studies of this section, it can be concluded that the high performance output voltage controller involving resonant filter banks provides satisfactory performance over a wide range of loads. In the experiments in addition to the THD and VR, the output voltage and load current unbalance quantities could be measured and compared to the standards. Based on the test data it can be clearly seen that the output voltage regulation and waveform quality are within the high performance UPS standard values. Thus, it can be stated that the method helps the practical UPS approximate the ideal UPS which has zero internal impedance and ideal internal voltage which equals the rated voltage under all operating conditions.

5.3.3. Dynamic Performance Investigation of The Four-Leg Inverter Based Three-Phase UPS System

In the computer simulation studies of dynamic performance evaluation in section 4.3.3 of Chapter 4, the importance, the performance measurement method, and the performance criteria of dynamic performance were discussed. In this section the computer simulation based dynamic performance studies are verified by means of experiments.

The experimental dynamic performance test is the same as discussed in the simulations. However, some practical differences exist. One such difference involves the instant of loading during the test. In the simulations, the load switch was turned on at the instant where the output voltage is at its maximum level in one phase in order to start the transient at the worst case loading operating condition. However, in the experiments this condition can not be exactly met as the switches utilized are neither fast nor precise in terms of defining the loading instant. In the experimental setup, a three-phase contactor has been utilized to enable and disable the load. The experiment for each test condition could only be created by various trials until the worst case (at the peak of the voltage waveform for one phase) loading condition could be obtained. However, the positioning is not precise and it only gives an approximate result for the dynamic performance.

The experimental system has also limitations in terms of controller structure. Since the capacitor current feedback is an important quantity strongly influencing the system dynamics, its measurement accuracy and speed determine the dynamic response of the practical system. The simulation model assumed for the current transformer, which measures the capacitor current, has been found too optimistic in terms of bandwidth. In the experiment it has been found that the bandwidth is less than 20 kHz which is the assumed value in the simulations. The low bandwidth is expected to decrease the effect of active damping loop compared to that of the simulation.

Considering the above two performance limitations of the experimental system, the experimental dynamic performance of the UPS system is expected to be slightly inferior to that of the simulation model. The experimental dynamic performance tests are conducted in the same manner as in the computer simulations. The performance results and their test conditions are listed in Table 5.8 and the important waveforms associated with these test conditions are illustrated in Figure 5.44 to Figure 5.48.

Based on Table 5.8 and the related experimental waveforms, it can be concluded that the active damping loop improves the dynamic performance significantly, but not to the same degree as in the computer simulations due to the above described capacitor current feedback measurement delay. It can be seen from the table that when the active damping loop disabled (Figure 5.44 and Figure 5.45) the voltage dip is in the range of 85-95V while with the loop enabled (Figure 5.46, Figure 5.47, and Figure 5.48) the voltage dip ranges around 65-85V. The fact that there exists a range rather than solid numbers is related to the loading instant determination difficulties described above. However, it can be clearly seen that on the average there exists about 20% decrease in the voltage dip with the active damping loop. The proportional gain helps improve the dynamic performance as predicted by the simulations (Figure 5.47). Finally, it can be seen that when all the control components are built into the system the dynamic performance of the UPS becomes satisfactory and at the final stage the experimental results match those of the simulations (Figure 5.48). In the experiments in Case 16 the lost volt-seconds are

21mVs as shown in Table 5.8 as compared to Case 16 in the simulations with the value of 20mVs in Table 4.7.

The above experimental studies illustrate that the active damping loop is vital for the dynamic performance of the UPS. Not only the steady-state waveforms improve, the controller gains can be increased due to enhanced stability, but the impact loading transients can be efficiently manipulated. Thus, a high UPS performance with very small lost volt-seconds during loading transients can be achieved. All the simulation studies regarding dynamic performance have been correlated with the experimental study.

Table 5.8 Gains, controller components, and performance characteristics of the UPS system during the dynamic loading tests

	Fundamental component controller		Harmonic component controllers	K_{ad}	Δt (ms)	ΔV (V)	∫vdt (V·ms)
	K_{iv}	K_{pv}					
Case 1	0	0.00	Uncontrolled	0.00	1.02	105	53.55
Case 2	0	0.00	Controlled	0.00	0.97	89	43.16
Case 3	100	0.00	Uncontrolled	0.00	1.25	87	54.38
Case 4	100	0.00	Controlled	0.00	1.27	88	55.88
Case 5	0	0.05	Uncontrolled	0.00	1.12	94	52.64
Case 6	0	0.05	Controlled	0.00	1.3	87	56.55
Case 7	100	0.05	Uncontrolled	0.00	1.0	90	45.0
Case 8	100	0.05	Controlled	0.00	1.0	95	47.50
Case 9	0	0.00	Uncontrolled	15.00	1.0	87	43.50
Case 10	0	0.00	Controlled	15.00	1.29	75	48.38
Case 11	100	0.00	Uncontrolled	15.00	1.04	72	37.44
Case 12	100	0.00	Controlled	15.00	1.35	69	46.58
Case 13	0	1.00	Uncontrolled	15.00	0.85	79	33.58
Case 14	0	1.00	Controlled	15.00	0.65	81	26.33
Case 15	100	1.00	Uncontrolled	15.00	0.68	77	26.18
Case 16	100	1.00	Controlled	15.00	0.65	65	21.13

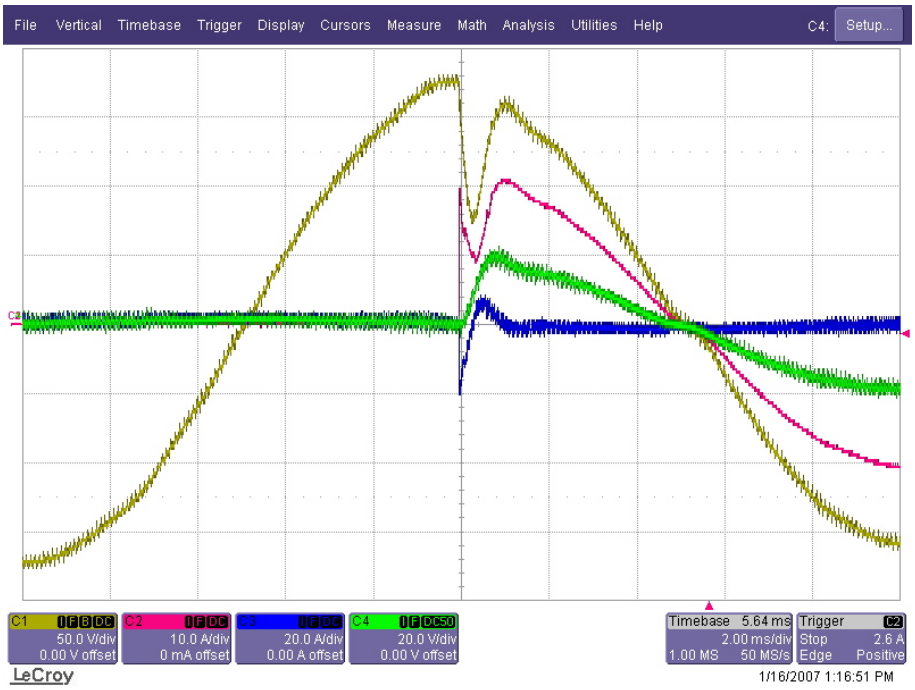


Figure 5.44 Output voltage (yellow), load current (red, x2), inductor current (green), capacitor current (blue) transients of the open-loop controlled UPS during loading transient (Case 1 of Table 5.8) (Scales: 50V/div, 20A/div, 2ms/div).

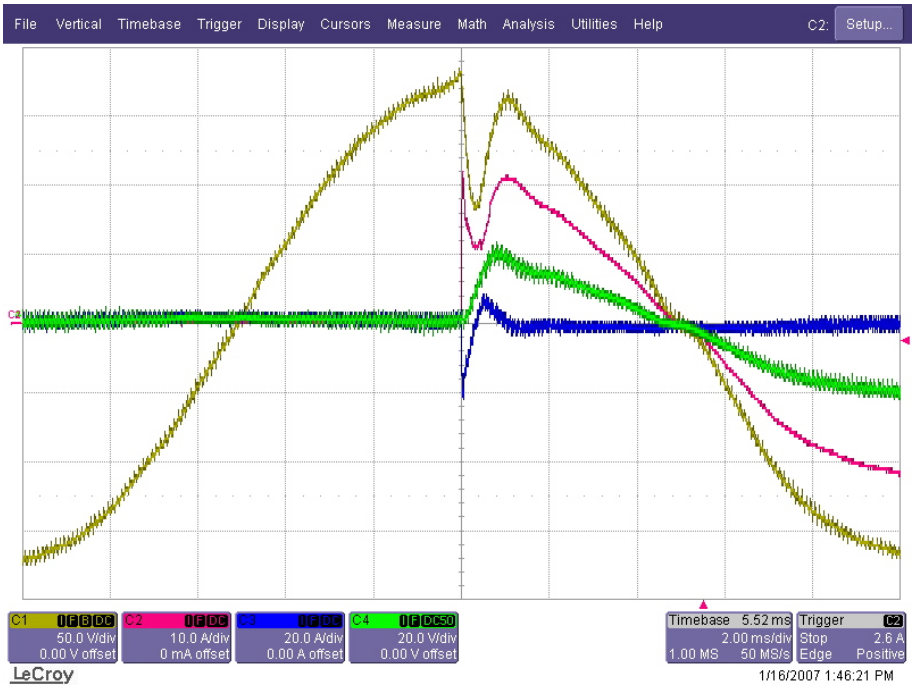


Figure 5.45 Output voltage (yellow), load current (red, x2), inductor current (green), capacitor current (blue) transients of the proposed controller during loading at the peak of output voltage (Case 8 of Table 5.8) (Scales: 50V/div, 20A/div, 2ms/div).

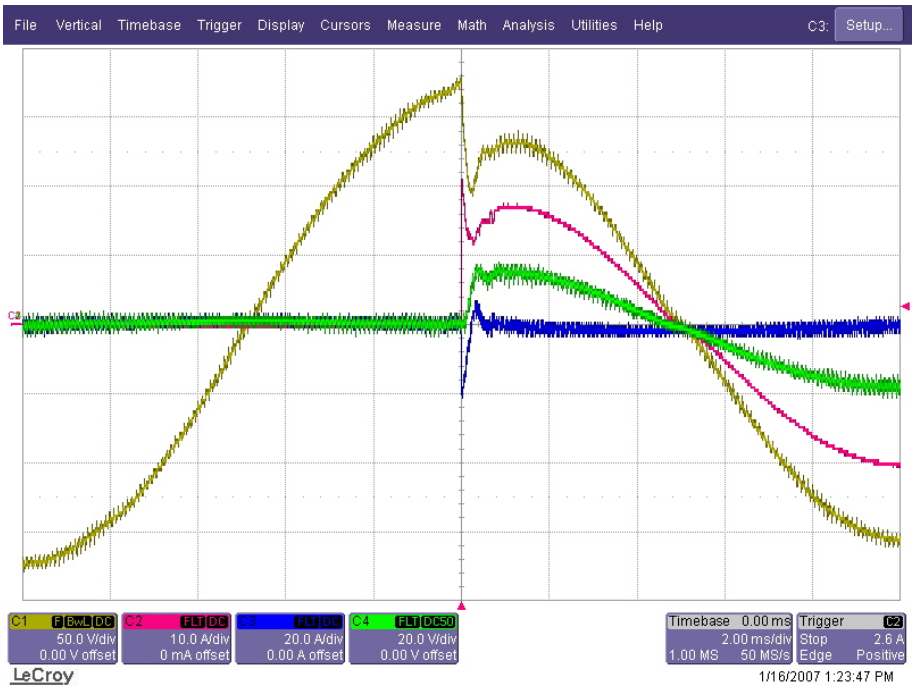


Figure 5.46 Output voltage (yellow), load current (red, x2), inductor current (green), capacitor current (blue) transients of the proposed controller during loading at the peak of output voltage (Case 9 of Table 5.8) (Scales: 50V/div, 20A/div, 2ms/div).

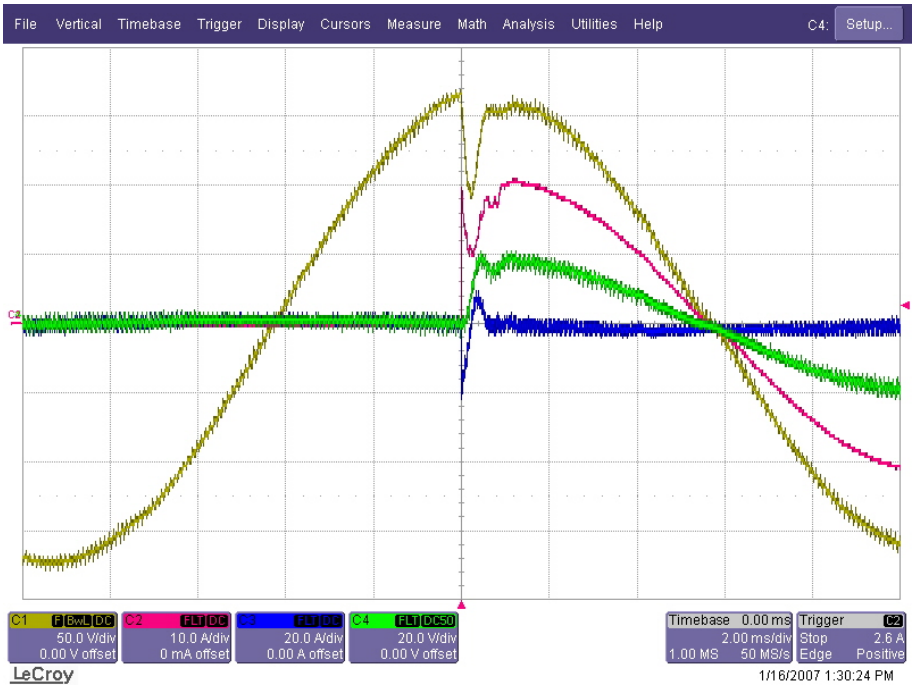


Figure 5.47 Output voltage (yellow), load current (red, x2), inductor current (green), capacitor current (blue) transients of the proposed controller during loading at the peak of output voltage (Case 13 of Table 5.8) (Scales: 50V/div, 20A/div, 2ms/div).

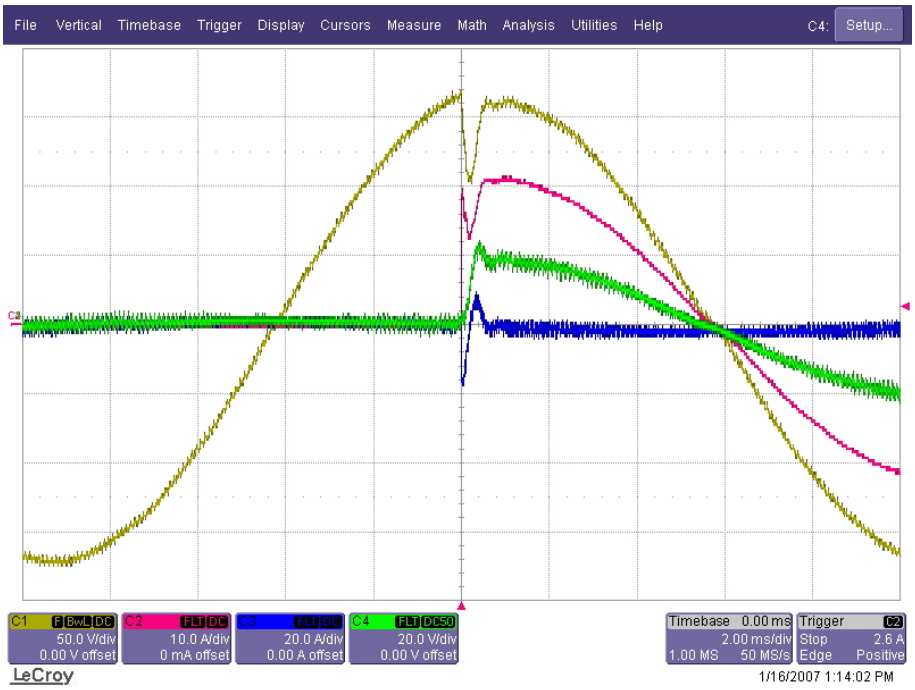


Figure 5.48 Output voltage (yellow), load current (red, x2), inductor current (green), capacitor current (blue) transients of the proposed controller during loading at the peak of output voltage (Case 16 of Table 5.8) (Scales: 50V/div, 20A/div, 2ms/div).

5.3.4. Experimental Investigation of Switching Ripple and Switching Loss Characteristics of Various PWM Methods

This section experimentally investigates the modulator switching ripple and loss characteristics for SVPWM, DPWM1, and MLDPWM. Based on the study results the modulator performances are evaluated and compared. The methods will be evaluated for linear balanced resistive, for line to neutral unbalanced linear resistive load, for nonlinear balanced and single-phase unbalanced load. For the linear load case the full-load power operating condition is tested. For the nonlinear balanced and unbalanced loads, the power rating is half the UPS power rating.

Throughout the modulator performance studies closed-loop control is involved and the high performance resonant filter controller structure shown in Figure 3.19 is utilized. The controller coefficients are the same as those of Stage IX of Table 5.5.

The carrier frequency is 20 kHz and the sampling rate is also the same as the carrier frequency (single update mode).

In the study first the balanced load operating conditions are considered and modulators are compared in terms of their switching ripple and losses. Then single-phase loading, in other words, the line-to-neutral unbalanced loading case is considered. Both linear and nonlinear load cases will be considered. The aim of this study is to illustrate the loss mechanism of each modulator and show the significant differences between MLDPWM and other modulators.

In the experiments focus is placed on visual illustration of the modulator performance characteristics rather than rigorous methods. The ripple of various PWM methods is compared visually. The switching loss is also evaluated based on the observation of the switch signals of the IGBTs. Since the loss measurement is an involved issue, it is not pursued at this stage. Therefore, the discussion of switching loss will be in terms of the switch signals and the currents that flow in the associated switches. For example, if a phase carries a large current and it switches at the carrier frequency, its losses are considered high. If the switch ceases to switch in a specific interval, then the switching losses are considered low. Therefore, if a PWM method that clamps the largest current carrying phase is locked to either side of the DC rail for a considerable number of PWM periods, the switching losses of the PWM method under investigation are expected to be low and the method is supposed to be superior.

For the balanced linear load case the SVPWM method PWM ripple current is small (Figure 5.49). The fourth leg ripple current is larger than the phase current ripple (Figure 5.50). Since the operation is in the linear region, the modulation is continuous implying the carrier frequency and average switching frequency are the same and the switching losses are high. For the same operating condition DPWM1 and MLDPWM methods result in the same switching pattern and behavior. Thus, only MLDPWM will be discussed. As can be seen from Figure 5.51 the phase current ripple is larger than the SVPWM case, in particular within the interval of

switch position lock out. The ripple current on the fourth leg again is larger than the phase legs (Figure 5.52). For linear line-to-neutral unbalanced load, the SVPWM waveform indicates that the ripple is still small. The ripple and switching characteristics remain the same as the balanced load case (Figure 5.53). For the DPWM1 and MLDPWM cases the characteristics change. The phase carrying the unbalance current in the MLDPWM case ceases to switch for a longer time interval in the MLDPWM case (Figure 5.56 and Figure 5.57) compared to the DPWM1 case (Figure 5.54 and Figure 5.55). This attribute of the modulator was also shown in the simulations (compare to Figure 4.72). The current ripple of the associated phase increases to a larger value over the longer time interval where switching ceases.

For the nonlinear balanced load operating condition, the SVPWM exhibits standard performance as shown in Figure 5.58. The DPWM1 method regularly locks $2x60^{o}$ intervals (Figure 5.59). In the MLDPWM method case, the largest currents define the lock-out interval. As Figure 5.60 illustrates, since the currents are discontinuous, the interval that a lock-out occurs is shorter than that of DPWM1. For the unbalanced nonlinear load case, SVPWM commutates every PWM cycle as always (Figure 5.61). The DPWM method lock-out interval is still $2x60^{o}$ (Figure 5.62). The MLDPWM method in this case exhibits a short interval lock-out behavior (Figure 5.63) as predicted by the simulation.

With the study of experimental modulation waveform characteristics, this chapter concludes. In this chapter, it has been shown by means of detailed laboratory experiments that the high performance resonant filter bank controller with active damping provides a superior solution for UPS output voltage control. Also in the final section the study involving modulation types has illustrated that the MLDPWM method has comparable PWM ripple to SVPWM but has lower switching losses than any other method. Thus, it should be favored in practical applications, specifically UPS applications where nonlinear and unbalanced loads are typical. The experimental results are in strong correlation with the theoretical studies of Chapter 2 and Chapter 3, and computer simulation studies of Chapter 4. With the experimental results of this chapter the feasibility of the proposed methods has been proven.

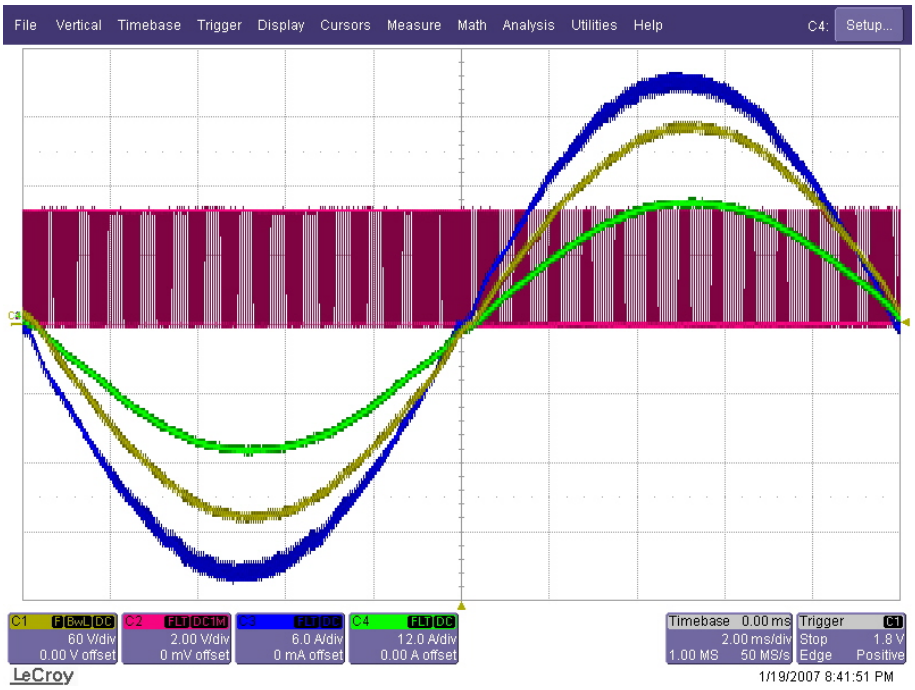


Figure 5.49 The steady-state inductor current (blue, x2), output voltage (yellow), load current (green), switch signal (red, x30) during SVPWM operation under linear balanced load (Scales: 60V/div, 12A/div, 2ms/div).

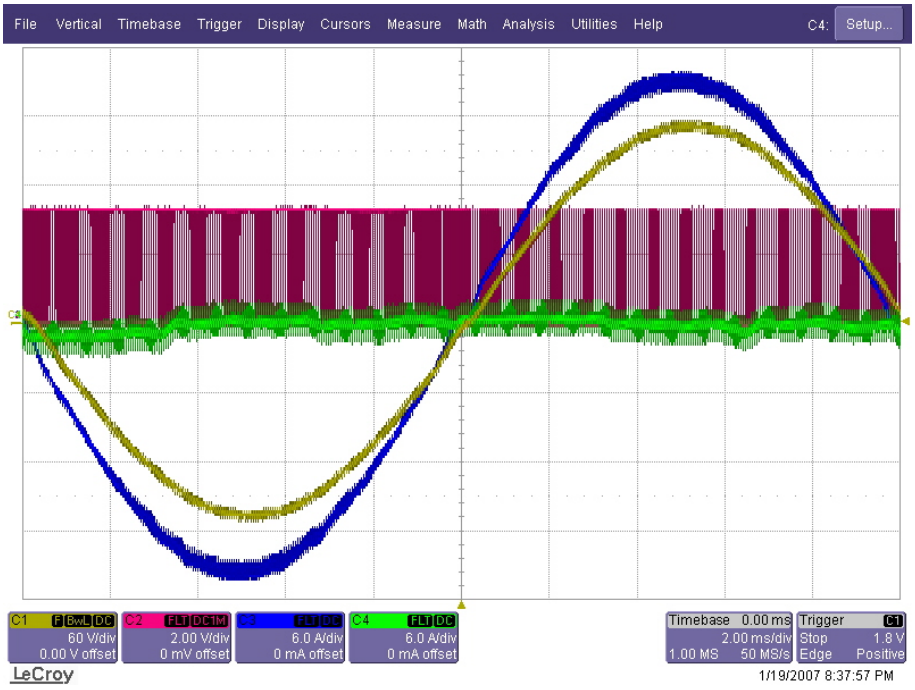


Figure 5.50 The steady-state inductor current (blue), output voltage (yellow), neutral inductor current (green), switch signal (red, x30) during SVPWM operation under linear balanced load (Scales: 60V/div, 6A/div, 2ms/div).

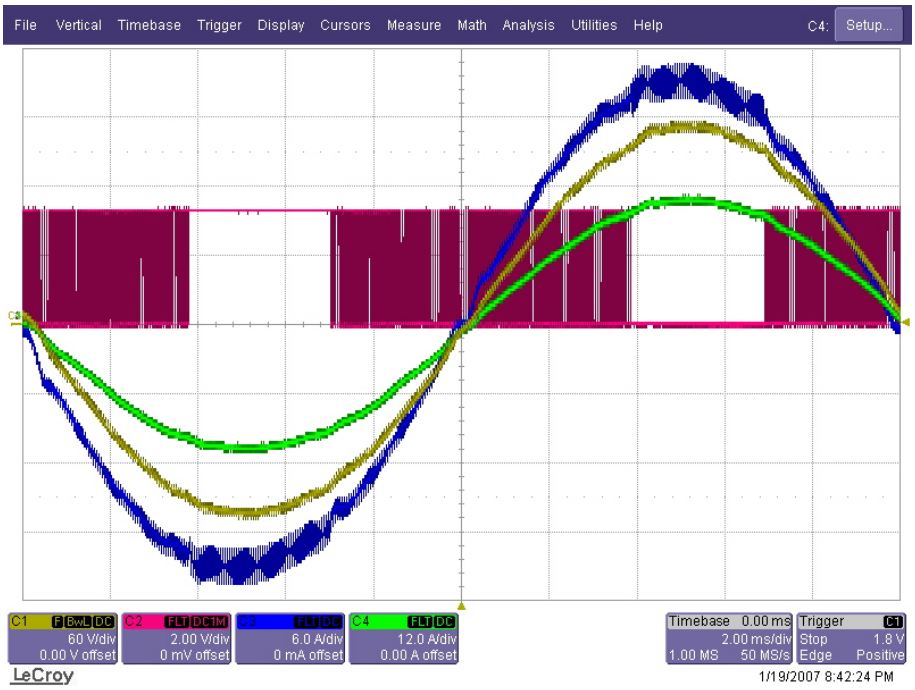


Figure 5.51 The steady-state inductor current (blue, x2), output voltage (yellow), load current (green), switch signal (red, x30) during MLDPWM operation under linear balanced load (Scales: 60V/div, 12A/div 2ms/div).

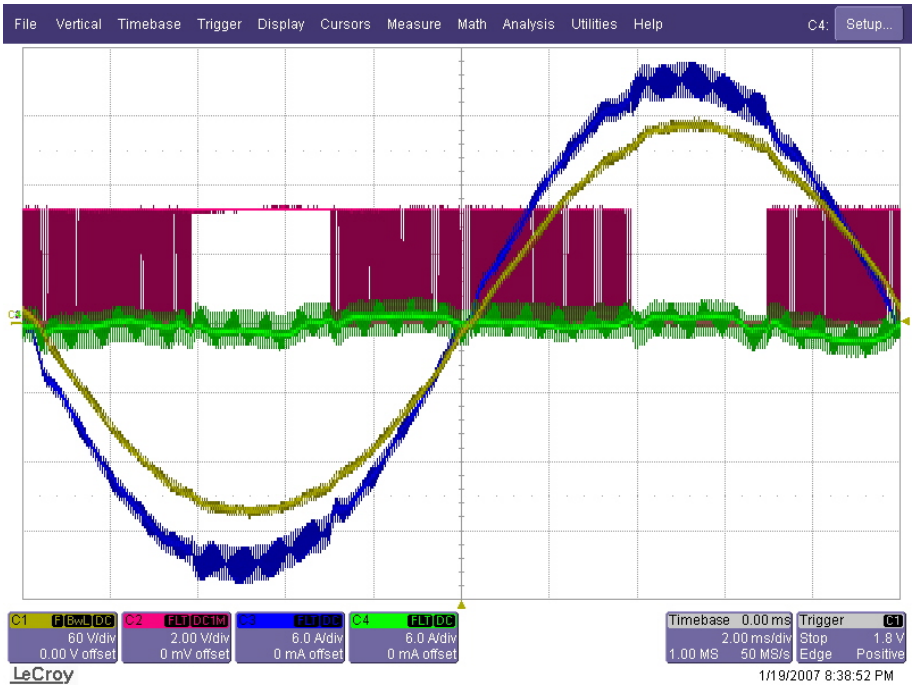


Figure 5.52 The steady-state inductor current (blue), output voltage (yellow), neutral inductor current (green), switch signal (red, x30) during MLDPWM operation under linear balanced load (Scales: 60V/div, 6A/div 2ms/div).

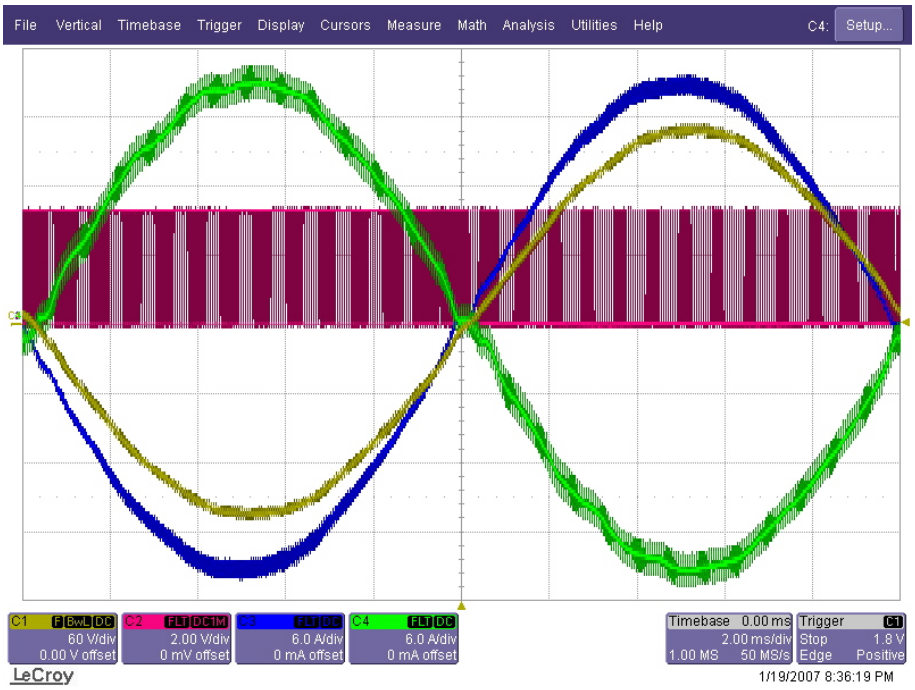


Figure 5.53 The steady-state inductor current (blue), output voltage(yellow), neutral inductor current (green), switch signal (red, x30) during SVPWM operation under linear line-to-neutral unbalanced load (Scales: 60V/div, 6A/div, 2ms/div).

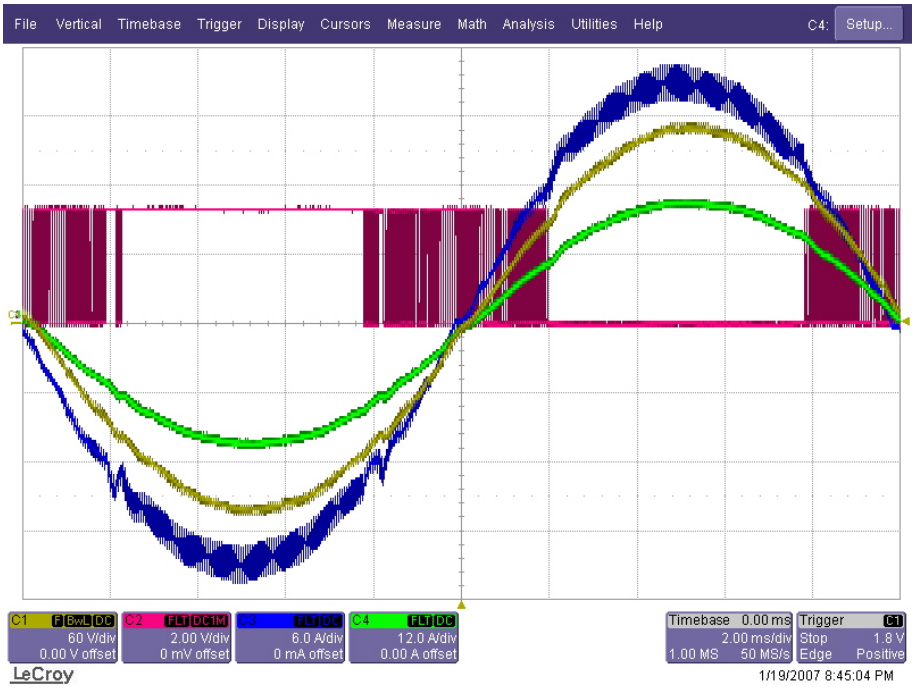


Figure 5.54 The steady-state inductor current (blue, x2), output voltage (yellow), load current (green), switch signal (red, x30) during DPWM1 operation under linear line-to-neutral unbalanced load (Scales: 60V/div, 12A/div, 2ms/div).

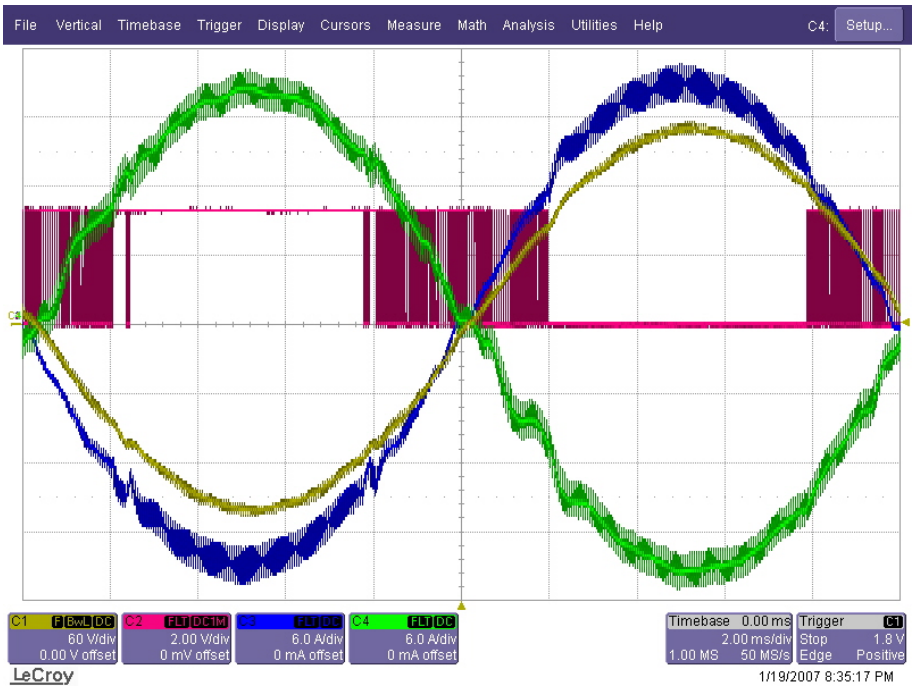


Figure 5.55 The steady-state inductor current (blue), output voltage (yellow), neutral inductor current (green), switch signal (red, x30) during DPWM1 operation under linear line-to-neutral unbalanced load (Scales: 60V/div, 6A/div, 2ms/div).

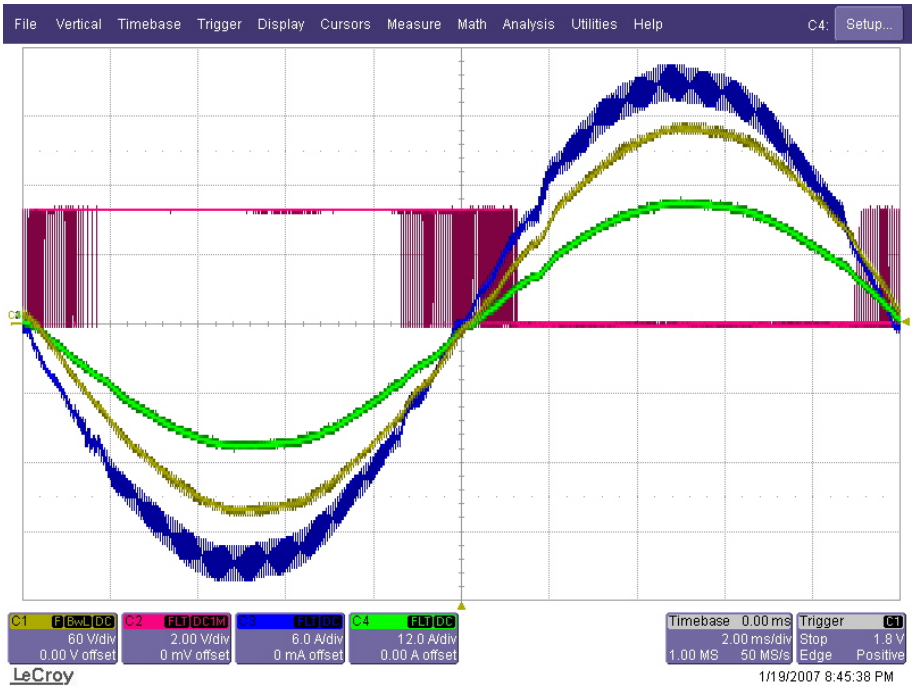


Figure 5.56 The steady-state inductor current (blue, x2), output voltage (yellow), load current (green), switch signal (red, x30) during MLDPWM operation under linear line-to-neutral unbalanced load (Scales: 60V/div, 12A/div, 2ms/div).

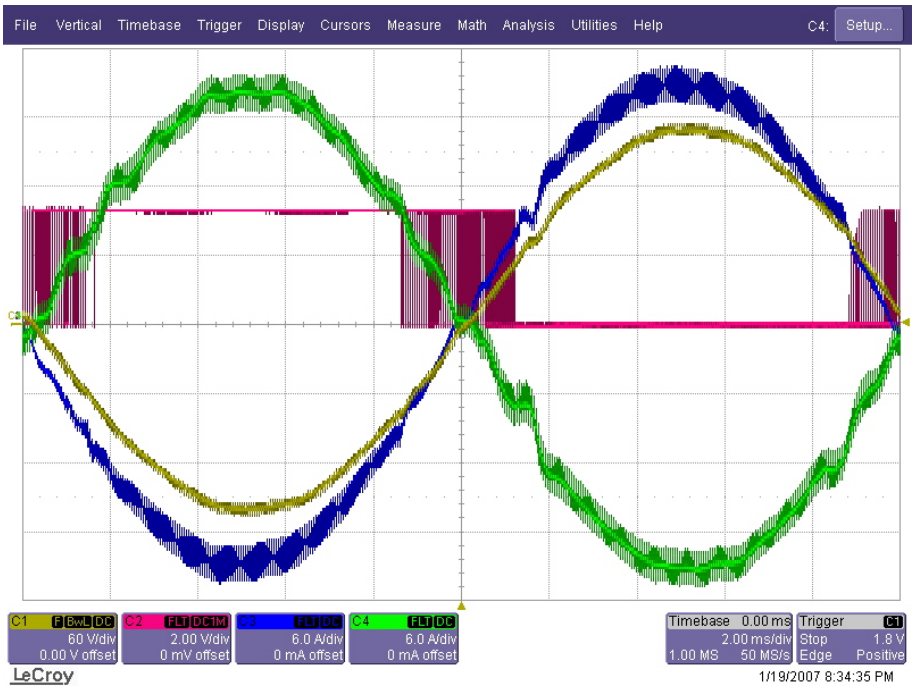


Figure 5.57 The steady-state inductor current (blue), output voltage (yellow), neutral inductor current (green), switch signal (red, x30) during MLDPWM operation under linear line-neutral unbalanced load (Scales: 60V/div, 6A/div, 2ms/div).

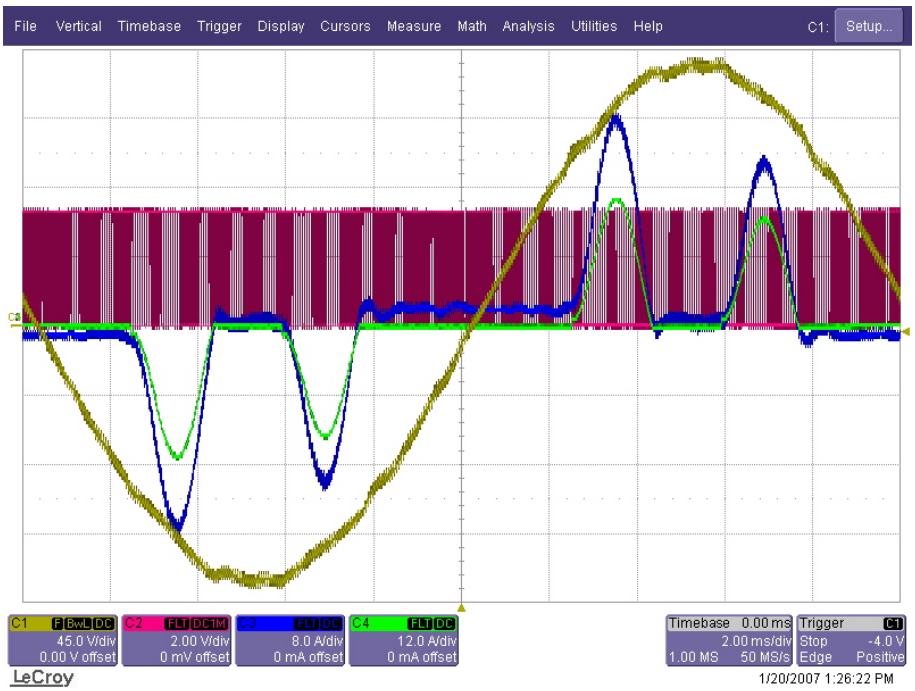


Figure 5.58 The steady-state inductor current (blue, x1.5), output voltage (yellow), load current (green), switch signal (red, x22.5) during SVPWM operation under nonlinear balanced load (Scales: 45V/div, 12A/div, 2ms/div).

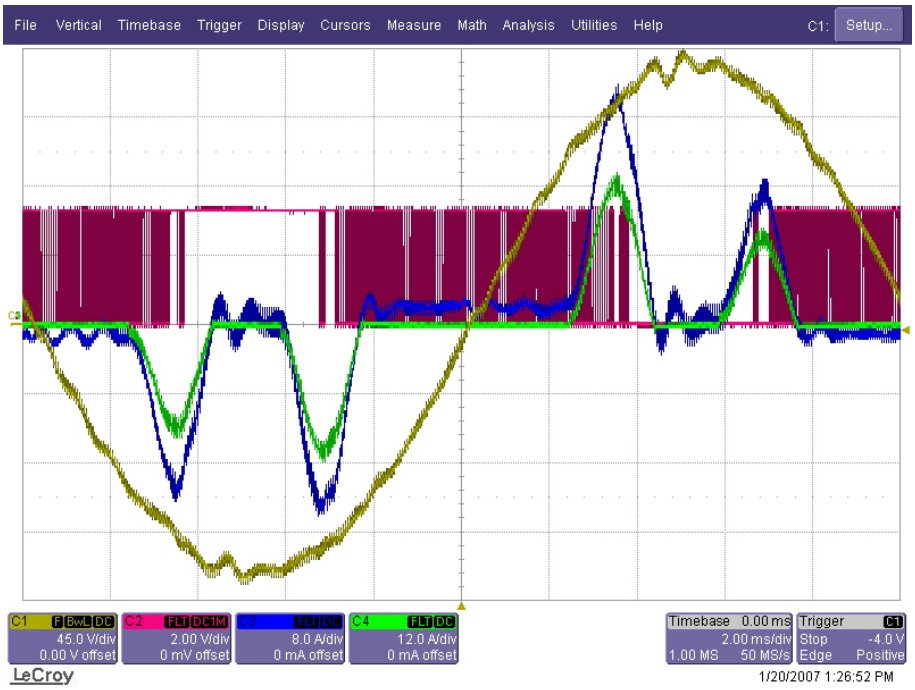


Figure 5.59 The steady-state inductor current (blue, x1.5), output voltage (yellow), load current (green), switch signal (red, x22.5) during DPWM1 operation under nonlinear balanced load (Scales: 45V/div, 12A/div, 2ms/div).

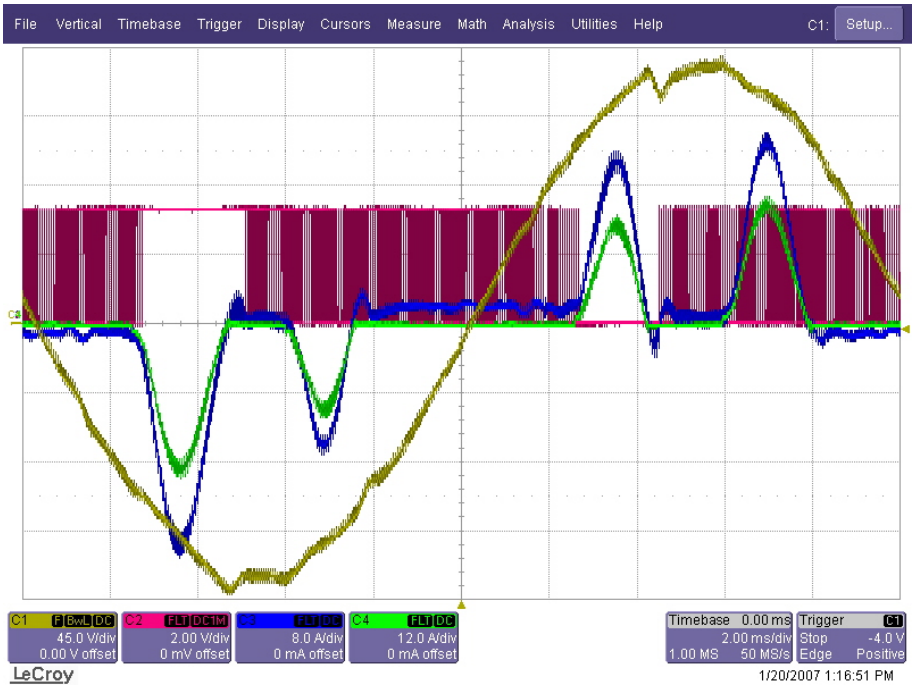


Figure 5.60 The steady-state inductor current (blue, x1.5), output voltage (yellow), load current (green), switch signal (red, x22.5) during MLDPWM operation under nonlinear balanced load (Scales: 45V/div, 12A/div, 2ms/div).

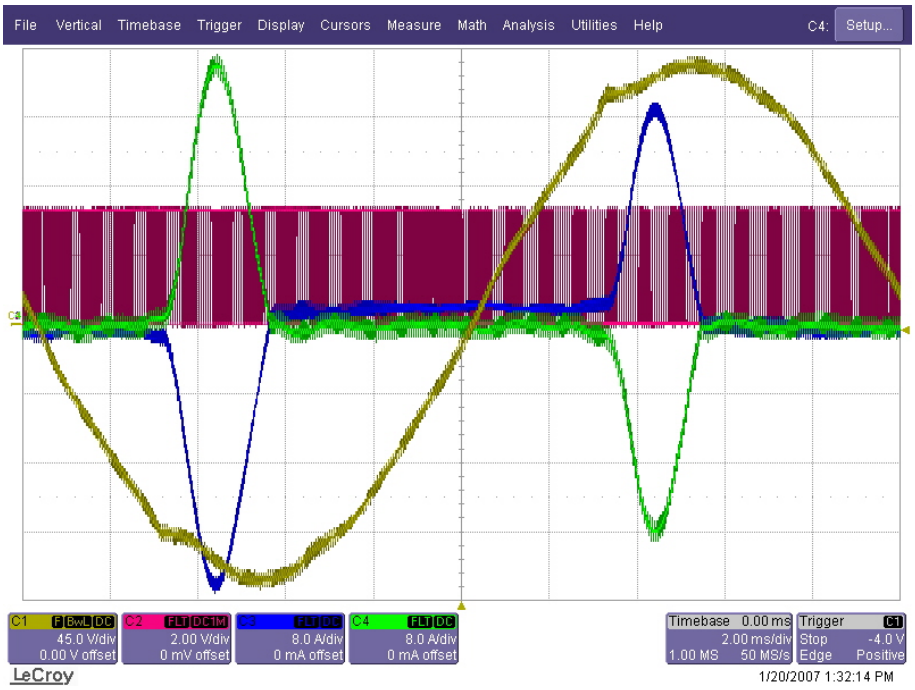


Figure 5.61 The steady-state inductor current (blue), output voltage (yellow), neutral inductor current (green), switch signal (red, x30) during SVPWM operation under nonlinear line-neutral unbalanced load (Scales: 45V/div, 8A/div, 2ms/div).

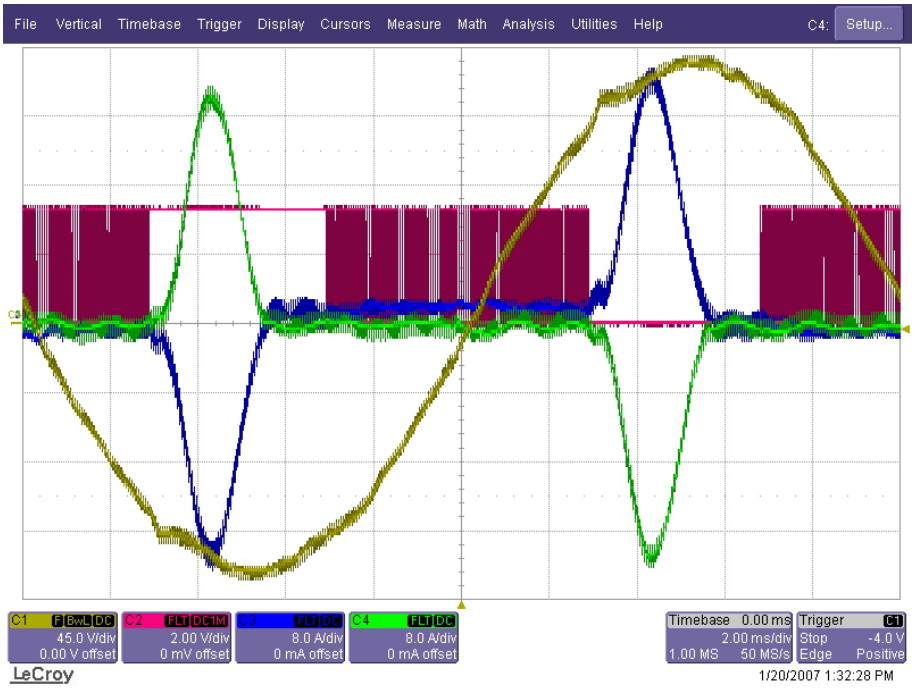


Figure 5.62 The steady-state inductor current (blue), output voltage (yellow), neutral inductor current (green), switch signal (red, x30) during DPWM1 operation under nonlinear line-neutral unbalanced load (Scales: 45V/div, 8A/div, 2ms/div).

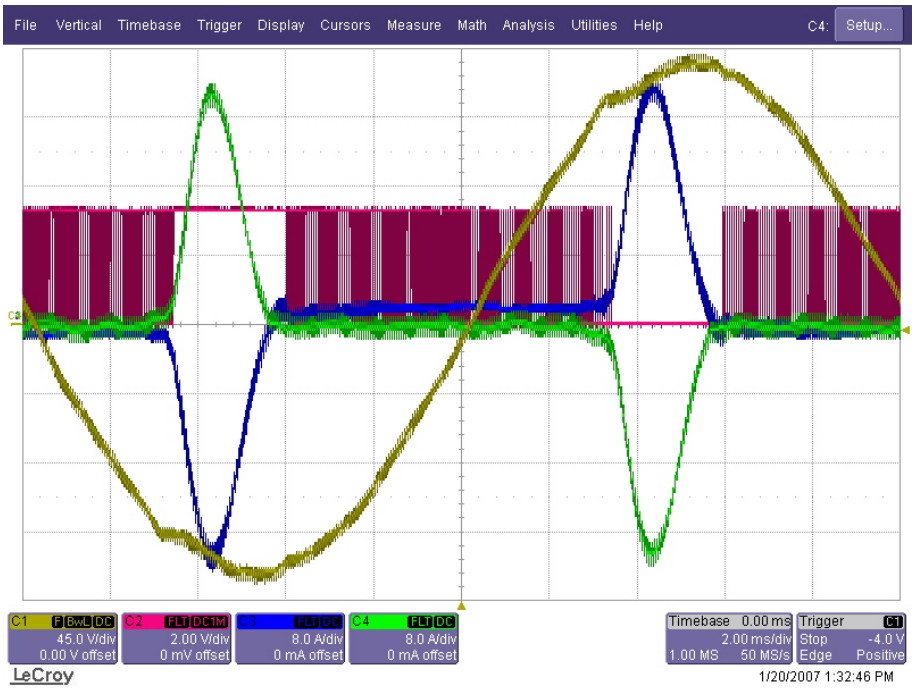


Figure 5.63 The steady-state inductor current (blue), output voltage (yellow), neutral inductor current (green), switch signal (red, x30) during MLDPWM operation under nonlinear line-neutral unbalanced load (Scales: 45V/div, 8A/div, 2ms/div).

CHAPTER 6

CONCLUSIONS

The four-leg inverter based UPS is a high performance UPS due to lower DC bus voltage requirement and availability of the zero sequence current flow path through the fourth leg. In the transformerless UPS application it provides better than 10% reduction in the DC bus voltage (when compared to the half-bridge inverter based classical topology). As a result, switching losses and voltage stresses on the circuit components are reduced. Further, providing a path for the load zero sequence current through the fourth leg, the DC bus center point is not loaded and neither the battery nor the DC bus capacitors are loaded with the zero sequence current. Thus, it can be claimed that the four-leg inverter based UPS topology is the ideal transformerless UPS topology.

This thesis investigated the PWM and control methods for the four-leg inverter based UPS. Since the four-leg inverter has one more leg than the conventional three-leg inverter, its PWM and control algorithms are seemingly complex. The 3-D space vector based PWM approach is conceptually difficult to understand and practically very difficult to implement due to the sector/region identification procedure which involves large number of comparisons/computations. Thus, the general impression on the four-leg inverter involves complexity in structure and implementation. Although large number of control methods are developed for the single-phase and three-phase/three-wire inverter based UPSs, the control of the four-leg inverter based UPS also involves difficulties involving transformation of the UPS model to d-q-0 components and control in rotating and stationary (mixed) coordinates. Thus the control of the four-leg inverter based UPS also is seemingly complex.

This thesis has contributed towards significant simplification of the PWM and control methods of the four-leg inverter based UPS. In order to simplify the PWM signal generation procedure, the scalar PWM approach is adopted and this provides ease of understanding and simplification in the implementation stage. Also employing the zero state partitioning variable, the scalar PWM methods for the four-leg inverter are unified under one umbrella. This approach simplifies the implementation and more importantly enhances the understanding of the scalar modulation techniqe. Based on the method adopted a clear understanding of switching loss mechanism of modulation methods could be established. Based on this knowledge, a reduced switching loss PWM method, MLDPWM, has been developed. In order to simplify the output voltage control procedure without sacrification from performance, the resonant filter bank approach complemented with the capacitor current feedback based active damping loop has been adopted. With such a control structure, neither a coordinate transformation, nor complex computations and algorithms become necessary. The resonant filter controller design has been carefully conducted and emphasis was placed on the filter damping and delay compensation. Rules for the filter design involving filter selectivity have been established. Thus, the resonant filter bank design procedure has been methodically established. As a result, the four-leg inverter based UPS becomes an easy to understand, design, and control UPS system with superior performance when compared to other topologies.

In the development stage of the scalar PWM approach, a general approach is carried from the concept used in the three-leg inverter scalar PWM approach and an offset voltage which represents the degree of freedom in selecting the PWM pulse pattern has been considered as the free variable. Also the zero vector state partitioning function has been developed and shown to provide an equivalent degree of freedom. Showing the equivalency both degrees of freedom, by selecting various zero state partitioning function values, PWM methods equivalent to SVPWM and DPWM1 methods which are widely utilized in the three-phase three-wire inverters could be obtained. In addition, a modulation algorithm, which provides minimum switching losses, the Minimum Loss DPWM (MLDPWM) method has been developed in this

theses. Although it exhibits similar behavior to DPWM1 and more generally generalized DPWM (GDPWM) methods, it performs differently under unbalanced load operating conditions. With the UPS applications involving unbalanced loads as usual loads, MLDPWM becomes a favorable for such applications. Thus, high performance PWM methods could be derived from the offset voltage injection or equivalently zero state partitioing function optimization. While the SVPWM method could be utilized for its low PWM ripple, the DPWM1 method could be utilized due to its reduced switching losses (by at least 33%) and low PWM ripple performance at high modulation index which is the typical UPS operating range. Futhermore, the MLDPWM method provides even a superior method when compared to DPWM1 and should be favored over these methods for the UPS application. Thus, using the scalar PWM approach, simple and high performance PWM algorithms could be developed. Generating such pulse patterns only involves several comparisons and basic addition and subtraction steps which are all light duties for the modern microcontrollers and digital signal processor chips available in the market. As a result, the difficulties in optimizing the PWM pulse pattern and implementing such pulse pattern in the four-leg inverter based UPS system have been greatly overcome.

Employing the resonant filter bank based controller and complementing it with the reference voltage feedforward and capacitor current feedback based active damping loop, the UPS output voltage could be precisely regulated under steady-state and dynamic loading conditions for linear, nonlinear, balanced, unbalanced operation. Since the controller is implemented per phase and in the stationary frame, the control complexity is low and full resolution of the signal processor is utilized as there is no coordinate transformations, no mixture of controllers for positive/negative/zero sequence components. The resonant filter bank approach involves a simple structure and its careful implementation provides precise output regulation with high bandwidth. In the thesis the design of the controller involving practical implementations and operating conditions has been carefully investigated. The filter selectivity and delay compensation parameters have been found critical for the success of the controller. For this purpose a detailed study involving the selectivity, damping and delay compensation has been conducted. Based on the study it has been

found that the delay compensation plays a major role for controlling the high frequency harmonic distortion. It also has been found that the selectivity should be decreased at high frequencies for the filter to be successfully compensate for the harmonics. Rules of thumb for the filter design could be obtained and the design has been demonstrated via numerical examples. Thus, the second major difficulty involving the practical realization of the four-leg inverter based UPS has been overcome.

The theoretical work developed in this thesis has been supported by detailed system modelling and computer simulation studies. First the UPS system model has been analytically established in the Laplace domain, its computer simulation model has been built and then computer simulations for various control and PWM algorithms have been conducted. The computer simulation results involve the steady-state and dynamic operating conditions and all practical loading conditions which put stress on the UPS output voltage regulation have been considered and studied in detail. It has been shown that the computer simulation results are in well agreement with the theoretical study and the proposed PWM and control methods provide high steady-state and dynamic performance. A UPS output voltage THD less than 2% under a nonlinear load with crest factor higher than 2.5 could be obtained. The output voltage fundamental component regulation with less than 1% error is always guaranteed. In the dynamic performance study it has been shown that the instantaneous loading at the maximum voltage point (worst case) has been compensated for in less than 600μs which corresponds to several PWM cycles. The voltage dip and settling time delays are minimal compared to alternative methods. Thus the computer simulations have thoroughly verified the performance of the proposed methods. In the simulation studies it has also been shown that DPWM1 and MLDPWM methods perform comparably to the SVPWM method in terms of PWM ripple, but due to reduction in switching losses both are superior. Of the DPWM1 and MLDPWM methods, the latter has been shown to fit the UPS application better due to its capability of providing lower losses under changing power factor and more importantly unbalanced load operating conditions. Thus, MLDPWM should be the method of choice in practical implementations.

Finally, the feasibility of the proposed PWM and control algorithms proven by theory and simulation studies, has been verified by the 5-kVA, 50-Hz, 120-Vrms rating four-leg inverter based UPS prototype laboratory tests. A state of the art DSP chip has been utilized as the control and PWM platform and the inverter employed the standard IGBT modules. A prototype UPS was built and tested under various operating conditions to illustrate the feasibility of the methods proposed. Experimental studies have been in good agreement with the theory and simulations. Thus, the feasibility of the proposed methods has been proven.

Overall, this thesis has contributed to the control and PWM algorithm method development for the four-leg inverter based UPS system. The main contribution is towards implementation simplification without performance sacrification. The contributions regarding the control algorithms involve analytical evaluation, design and implementation. The contributions regarding PWM involve detailed analysis, unification for simplification and development of the MLDPWM method for high performance. With the results of this research, it can be claimed that the four-leg inverter based UPS is at least as easy and perhaps easier to control than the three-leg inverter based UPS which either employs passive means of zero sequence path (via a zig-zag transformer in the transformer based application) or active means of zero sequence path (the DC bus center point in the transformerless application). As a result, it is expected that the four-leg inverter based UPS systems will have increase in utilization and provide high power quality at higher energy efficiency and lower cost than the present competitors which are either transformer based UPS or half-bridge based transformerless UPS.

Future work relating to the subject study of this thesis involves several issues. Since the DSP chip utilized has implementation constraints the PWM pulse pattern could not be generated in the best manner, as discussed in the experimental studies. With more appropriate DSP chips, the PWM algorithms proposed should be implemented and tested to demonstrate the superior performance of the proposed methods to a higher degree. In terms of the modulator performance, the losses should be experimentally investigated to quantify the energy efficiency superiority of the

method. Since the loss formulation and device models employed in the thesis are naive, the switching loss characteristics of the discussed PWM methods could only be analytically discussed in the thesis. Thus, these studies must be verified by experimental work.

The influence of the fourth leg inductor on the PWM ripple is another issue that needs to be addressed. The sizing of the fourth leg inductor should be studied subject to the unbalanced operating conditions, modulation index, etc. variables to determine the best value for this inductor.

In the control aspect, utilizing the load current instead of the capacitor current in the active damping loop provides an important cost reduction. Because in practical UPS systems the load current is measured for various purposes such as short-circuit or overload protection, customer demand, etc. The filter inductor current is also measured for the short-circuit or overload protection. With these two currents known, the capacitor current information can be considered redundant. Thus, it is necessary to incorporate the two measured quantities into one and account for the measurement delay to estimate the capacitor current and provide the feedback through this signal. Thus, significant cost reduction and reliability increase can be achieved. The method of estimating the capacitor current and applying active damping loop requires dedicated attention. Likewise, control methods such as deadbeat control in stationary coordinates should be considered for higher performance.

REFERENCES

[1] R.C. Dugan, M.F. McGranaghan, S. Santoso, H.W. Beaty, "Electrical power systems quality," McGraw-Hill, 2nd editon, 2002.

[2] A. King, W. Knight, "Uninterruptible power supplies and standby power systems," McGraw-Hill, 1st edition, 2003.

[3] R.A. Gannett, "Control strategies for high power four-Leg voltage source inverters," M.Sc. Dissertation, Virginia Polytechnic Institute, July 2001.

[4] Motors and generators, NEMA Standards Publication no MG 1-1993.

[5] A. Juanne, B. Banerjee, "Assessment of voltage unbalance," IEEE Transaction On Power Delivery, Vol. 16, No. 4, pp. 782-790, Oct. 2001.

[6] R. Zhang, "High performance power converter systems for nonlinear and unbalanced load/source," Ph.D. Dissertation, Virginia Polytechnic Institute, November 1998.

[7] IEEE Standard 100-1992, "IEEE Standard dictionary of electrical and electronic terms."

[8] IEC 61000-4-30 77A/356/CDV, "Power quality measurement methods," 2001.

[9] A.M. Hava, "Carrier Based PWM-VSI Drives in the Overmodulation Region," Ph.D. Dissertation, University of Wisconsin-Madison, 1998.

[10] A.M. Hava, R.J. Kerkman, T.A. Lipo, “Simple analytical and graphical methods for carrier based PWM-VSI drives,” *IEEE Transactions On Power Electronics*, vol. 14, pp. 49-61, January 1999.

[11] R. Zhang, V.H. Prasad, D. Boroyevich, F.C. Lee, “Three-dimensional space vector modulation for four leg voltage source converters,” *IEEE Transactions On Power Electronics*, vol.17, pp. 314-326, May 2002.

[12] J. Kim, S. Sul, “A carrier-based PWM method for three-phase four-leg voltage source converters,” *IEEE Transactions on Power Electronics*, vol. 19, pp. 66-75, January 2004.

[13] J. Kim, S. Sul, H. Kim, J. Ji, “A PWM strategy for four-leg voltage source converters and applications to a novel line interactive UPS in a three-phase four-wire system,” IAC, vol. 4, pp. 2202-2209, October 2004.

[14] N.M. Abdel-Rahim, J.E. Quaicoe, “Analysis and design of a multiple feedback loop control strategy for single-phase voltage source UPS inverters,” *IEEE Transactions On Power Electronics*, vol. 11, pp. 532-541, July 1996.

[15] M.J. Ryan, W.E. Brumsickle, R.D. Lorenz, “Control topology options for single phase UPS inverters,” *IEEE Transactions On Industry Applications*, vol. 33, pp. 493-501, March/April 1997.

[16] F. Kamran, “A new UPS topology and deadbeat control techniques for improved utility interface compatibility,” Ph.D. Dissertation, Georgia Institute Of Technology, October 1995.

[17] O. Kükrer, “Deadbeat control of a three-phase inverter with an output LC filter,” *IEEE Transactions On Power Electronics*, vol. 11, pp. 16-23, January 1996.

[18] O. Kükrer, H. Kömürcügil, “Deadbeat control method for single phase UPS inverters with compensation of computation delay,” *IEE Proceeding-Electronics Power Application*, vol. 146, pp. 123-128, January 1999.

[19] U. Borup, P.N. Enjeti, F. Blaabjerg, “A new space-vector-based control method for UPS systems powering nonlinear and unbalanced loads,” *IEEE Transactions On Industry Applications*, vol. 37, pp. 1864-1870, November/December 2001.

[20] K. Zhang, Y. Kang, J. Xiong, J. Chen, “Direct repetitive control of SPWM inverter for UPS purpose,” *IEEE Transactions On Power Electronics*, vol. 18, pp. 784-792, May 2003.

[21] S. Çetinkaya, “Repetitive control of a three-phase uninterruptible power supply with isolation transformer,” M.Sc. Dissertation, Middle East Technical University, 2006.

[22] K. Kim, N. Park, D. Hyun, “Advanced synchronous reference frame controller for three-phase UPS powering unbalanced and nonlinear loads,” IEEE PESC Conference, pp. 1699-1704, 2005.

[23] P.C. Loh, M.J. Newman, D.N. Zmood, D.G. Holmes, “A comparative analysis of multiloop voltage regulation strategies for single and three-phase UPS systems,” *IEEE Transactions On Power Electronics*, vol. 18, pp. 1176-1185, September 2003.

[24] P. Mattavelli, “Synchronous-frame harmonic control for high-performance AC power supplies,” *IEEE Transactions On Industry Applications*, vol. 37, pp. 864-872, May/June 2001.

[25] T.M. Rowan, R.J. Kerkman, "A new synchronous current regulator and an analysis of current-regulated PWM inverters," *IEEE Transactions On Industry Applications*, vol. 22, pp. 678-690, July/August 1986.

[26] Y. Sato, T. Ishizuka, K. Nezu, T. Katako "A new control strategy for voltage-type PWM rectifiers to realize zero steady-state control error in input current," *IEEE Transactions On Industry Applications*, vol. 34, pp. 480-486, May/June 1998.

[27] X. Yuan, W. Merk, H. Stemmler, J. Allmeling, "Stationary-frame generalized integrators for current control of active power filters with zero steady-state error for current harmonics of concern under unbalanced and distorted operating conditions," *IEEE Transactions On Industry Applications*, vol. 38, pp. 142-150, March/April 2002.

[28] D.N. Zmood, D.G. Holmes, G.H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Transactions On Industry Applications*, vol. 37, pp. 601-610, April 2001.

[29] D.N. Zmood, D.G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Transactions On Power Electronics*, vol. 18, pp. 814-82, May 2003.

[30] H.W. Van Der Broeck, H.C. Skundelny, G.V. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Transactions On Industry Applications*, vol. 24, pp. 142-150, January/February 1988.

[31] A.M. Hava, R.J. Kerkman, T.A. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Transactions On Industry Applications*, vol. 34, pp. 1059-1071, September/October 1998.

[32] J.B. Cruz, M.E.V. Valkenburg, "Signals in linear circuits," Houghton Mifflin Company, Boston, 1974.

[33] K. Ogata, "Modern control engineering," Prentice-Hall Inc., 3rd Ed., 1997.

[34] K.J. Aström, T. Hägglund, "Automatic tuning of PID controllers," Research triangle park, NC, Instrument Society of America, 1988.

[35] L. Harnefors, H.P. Nee, "Model-based current control of AC machines using the internal model control method," *IEEE Transactions On Industry Applications*, vol. 34, pp. 133-141, January/February 1998.

[36] M.J. Ryan, "Analysis, Modeling and control of three-phase, four-wire sine wave inverter systems," Ph.D. Dissertation, Wisconsin-Madison, 1997.

[37] M.J. Ryan, R.W.D. Doncker, R.D. Lorenz, "Decoupled control of a four-leg inverter via a new 4x4 transformation matrix," *IEEE Transactions On Power Electronics*, vol. 16, pp. 694-701, January 2001.

[38] J.G. Tracy, H.E. Pfitzer, "Achieving high efficiency in a double conversion transformerless UPS," IECON Conf., Raleigh, NC, 2005, pp. 942-945.

[39] Matlab 6.5. A numerical computation software, Mathworks Inc., 2002.

[40] Ansoft-Simplorer V7.0. A power electronics simulation software, Ansoft Corporation, 2004.

[41] "eZdsp™ F2812 Technical Reference," Spectrum Digital, September 2003.

[42] "TMS320x281x DSP Event Manager Reference Guide," Texas Instruments, November 2004.

[43] “Code Composer Studio Getting Started Guide,” Texas Instruments, November 2001.