DEVELOPMENT OF ELECTROCHEMICAL ETCH-STOP TECHNIQUES FOR INTEGRATED MEMS SENSORS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF NATURAL AND APPLIED SCIENCES
OF
MIDDLE EAST TECHNICAL UNIVERSITY

BY

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IN PARTICULAR FULFILLMENT OF THE REQUIREMENTS
FOR
THE DEGREE OF MASTER OF SCIENCE
IN
ELECTRICAL AND ELECTRONICS ENGINEERING

SEPTEMBER 2006

Approval of Graduate School of Natural and Applied Sciences

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ABSTRACT

DEVELOPMENT OF ELECTROCHEMICAL ETCH-STOP TECHNIQUES FOR INTEGRATED MEMS SENSORS

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September 2006, 184 pages

This thesis presents the development of electrochemical etch-stop techniques (ECES) to achieve high precision 3-dimensional integrated MEMS sensors with wet anisotropic etching by applying proper voltages to various regions in silicon. The anisotropic etchant is selected as tetra methyl ammonium hydroxide, TMAH, considering its high silicon etch rate, selectivity towards SiO_2, and CMOS compatibility, especially during front-side etching of the chip/wafer. A number of parameters affecting the etching are investigated, including the effect of temperature, illumination, and concentration of the etchant over the etch rate of silicon, surface roughness, and biasing voltages. The biasing voltages for passivating the n-well and

enhancing the etching reactions on p-substrate are determined as -0.5V and -1.6V, respectively, after a series of current-voltage characteristic experiments. The surface roughness due to TMAH etching is prevented with the addition of ammonium peroxodisulfate, AP. A proper etching process is achieved using a 10wt.% TMAH at 85°C with 10gr/lt. AP.

Different silicon etch samples are produced in METU-MET facilities to understand and optimize ECES parameters that can be used for CMOS microbolometers. The etch samples are fabricated using various processes, including thermal oxidation, boron and phosphorus diffusions, aluminum and silicon nitride layer deposition processes. Etching with the prepared samples shows the dependency of the depletion layer between p-substrate and n-well, explaining the reason of the previous failures during post-CMOS etching of CMOS microbolometers from the front side. Succesfully etched CMOS microbolometers are achieved with back side etching in 6M KOH at 90°C, where -3.5V and 1.5V are applied to the p-substrate and n-well. In summary, this study provides an extensive understanding of the ECES process for successful implementations of integrated MEMS sensors.

Key words: Electrochemical etch stop technique, anisotropic wet etching, TMAH.

ÖZ

ENTEGRE MEMS DUYARGALARI İÇİN ELEKTROKİMYASAL AŞINDIRMA-DURDURMA TEKNİKLERİ GELİŞTİRİLMESİ

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Eylül 2006, 184 sayfa

Bu tez silikonun çeşitli bölgelerine uygun voltaj değerleri uygulayarak ıslak anizotropik aşındırma ile 3 boyutlu yüksek kesinlikli entegre MEMS duyargaları elde etmek için elektrokimyasal aşındırma-durdurma teknikleri geliştirilmesini sunmaktadır (EKAD). Anizotropik aşındırıcı olarak, özellikle yonga/pul'un önden aşındırması sırasında, yüksek silikon aşındırma oranı, SiO_2'ye karşı seçiciliği, ve CMOS'a uygunluğu göz önünde bulundurularak tetra metil amonyum hidroksit, TMAH, seçilmiştir. Aşındırmayı etkileyen aşındırıcının sıcaklığı, konsantrasyonu, ve aydınlatılması gibi parametrelerin, aşındırıcının silikonu aşındırma oranı, yüzey pürüzlülüğü ve uygulanan voltajlar üzerindeki etkileri araştırılmıştır. Bir sıra akım-voltaj karakterizasyon deneyi sonrası n-tipi kuyu bölgesini oksitleyen ve

p-tabakada aşındırma reaksiyonlarını geliştiren voltajlar, -0.5V ve -1.6V olarak sırasıyla belirlenmiştir. TMAH aşındırması sırasında oluşan yüzey pürüzlülüğü amonyum peroksodisülfat, AP katılarak engellenmiştir. 85°C'de, 10gr/lt. AP katılmış %10 TMAH solüsyonu kullanılarak uygun aşındırma süreci gerçekleştirilmiştir.

CMOS mikrobolometrelerde kullanılmak üzere, EKAD parametrelerini anlamak ve en iyi şekilde kullanmak için METU-MET tesislerinde çeşitli silikon aşındırma örnekleri üretilmiştir. Aşındırma örnekleri termal oksidasyon, boron ve fosfor difüzyon, alüminyum ve silikon nitrit serme gibi süreçler kullanılarak üretilmiştir. Aşındırma örnekleri ile yapılan aşındırmalar daha önceden yapılan CMOS mikrobolometrelerin CMOS sonrası önden aşındırmaları sırasındaki başarısızıkların sebebinin p-tabaka ve n-tipi kuyu arasındaki tükenmiş bölgeye bağlı olduğunu göstermiştir. Başarıyla aşındırılmış CMOS mikrobolometreleri 90°C'de 6M KOH kullanılarak, p-tabakaya -3.5V ve n-tipi kuyuya 1.5V uygulayarak arkadan yapılan aşındırma süreci ile sağlanmıştır. Özetle, bu çalışma entegre MEMS duyargaları için başarılı EKAD süreci uygulamayı geniş bir çerçevede anlatmaktadır.

Anahtar Kelimeler: Elektrokimyasal aşındırma-durdurma tekniği, anizotropik ıslak aşındırma, TMAH.

To My Family

ACKNOWLEDGEMENTS

First and foremost, I would like to express my deep and sincere gratitude to my thesis supervisor, Prof. Dr. Tayfun Akın, for his sustained guidance and support that enlightens me throughout the development of this thesis and during the whole time of my graduate study.

I would like to present my sincere thanks to Orhan Akar for encouraging me throughout the design and fabrication steps of my thesis with his valuable discussions and perceptiveness. I also would like to thank to Harun Tanık, Murat Ünal, Ebru Sağıroğlu Topallı and Akın Aydemir from METU-MET facilities for their effort and for sharing their extensive experience on fabrication processes.

I would like to gratefully acknowledge the support of Mahmud Yusuf Tanrıkulu, Erkan Alpman and Şafak Demirci. I want to thank to Yüksel Temiz and İlker Ender Ocak for their help during the measurements of the experiments results. I am also thankfull to all my friends in METU MEMS VLSI group for their encouragement and friendship.

I would like to thank to Yalçın Küçükerdönmez for his understanding, endless patience, and encouragement when it was most required.

Last but not least, I would like to give my endless gratitude to my family, who endured this long process with me and supported me with their patience, understanding, and love.

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CHAPTER 1

INTRODUCTION

The micromachining and Micro Electro-Mechanical Systems (MEMS) technology serves humanity in all aspects by means of automotive, defense, biomedical, and scientific applications. Every development in MEMS advances the efficiency, availability, performance, and implementation of MEMS devices, and therefore, directly affects the quality of life of the mankind. Researchers gather the knowledge and utilize them in fabrication of microstructures. Every research extends the limits of design of microstructures for more performance and less cost. However, this also brings enhancement to the fabrication techniques of the microstructures, which can obviously change the point of view or the stipulated cost and performance.

The principal issue in fabrication is to have a reproducible process, which is especially substantial for batch production. Every issue about the process parameters should be considered before exposing the devices to the processes. Otherwise, a great loss of time can come across to the engineers, as well as huge financial problems. Therefore, the optimization of the fabrication process is a "must" on microstructure fabrication.

One of the most important MEMS processes that needs a precise optimization is the wet anisotropic etching process of the silicon. The wet anisotropic etching process is a key technology to fabricate various important MEMS sensors, like microbolometers, pressure sensors, and gyroscopes. The process is an aggressive process towards its target, and determining the end point of the etching reactions by

etch stopping techniques is very critical for a reliable and reproducible device fabrication.

This thesis presents the studies done for extensive understanding of the ECES processes for successful implementations of integrated MEMS sensors. A number of parameters affecting the etching are investigated, including the effect of temperature, illumination, and concentration of the etchant over the etch rate of silicon, surface roughness, and biasing voltages. Different silicon etch samples are produced in METU-MET facilities to understand and optimize ECES parameters that can be used for CMOS microbolometers. A stable wet anisotropic etching process is developed for proper application of the electrochemical etch-stop (ECES) technique. This study has allowed understanding and succesfull implementation of CMOS microbolometers at Middle East Technical University.

This chapter is organized as follows: Section 1.1 explains the silicon as a substrate and anisotropic properties of single crystal silicon with an explanation of the Miller indices representation. It underlines the unique properties of crystalline silicon which makes it useful for many microelectronic sensor structures. Section 1.2 describes the wet anisotropic etching process including, etching behavior on various protection masks, etch stopping techniques, and anisotropic etchants. Section 1.3 reviews the enhanced microstructure examples fabricated by the anisotropic wet etching process and the electrochemical etch-stop technique, and it summarizes thermal detection mechanisms and microbolometer detectors with structural analysis of the CMOS microbolometer previously developed at Middle East Technical University. Section 1.4 concludes this chapter with the research objectives and thesis organization.

1.1. An Overview of Silicon

Silicon, with its magnificent properties, excites and welcomes all the creations in the micromachining world. Its nature offers significant electrical and mechanical advantages [1]. Silicon is a suitable platform, on which electronics as well as mechanical, thermal, optical and even fluid flow functions can be integrated. Mechanically, silicon is an elastic and robust material. Furthermore, it is a good thermal conductor with conductivity approximately one hundred times larger than that of glass. This property of silicon is utilized a lot in the thermal detectors and microbolometers. The low cost of these substances makes them attractive for the fabrication of micromechanical components and systems

Silicon is a strong substance. MEMS devices become more invulnerable to shape deformations during operation of the devices because of the high Young's Modulus of silicon. Its Young's modulus value can increase to 190 GPa (which is very close to of steel's), depending on the orientation of the crystal silicon structure [2-4]. Another feather of silicon that makes it unique among other materials is it's highly stress sensitive structure.

The properties of silicon vary according to its material structure. Silicon can be grown in crystalline, polycrystalline, and amorphous forms. In amorphous silicon, atoms are randomly located. There is no order in the lattice of the amorphous silicon. However, it is used in wide electrical and industrial areas. It can be deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) systems. Amorphous silicon is used in various areas like thin-film transistors, microbolometer sensors [5-7]. Polycrystalline silicon is formed with grains which are individually in crystalline from and has been used as the conducting gate material in MOSFET and CMOS processing technologies. It can be deposited by Low Pressure Chemical Vapor Deposition (LPCVD) systems [8]. Among polycrystalline and amorphous structures, crystalline silicon is in concern of the wet anisotropic etching process.

1.1.1. Crystalline Silicon Structure

Crystalline silicon has atoms in an arranged order. The total lattice can be defined with the basic unit cell that is repeated periodically in all 3 dimensions. Generally, examining the unit cell properties, placement and number of the atoms, lattice constant, is enough to comment on the material. Figure 1.1 gives the unit cell of the single silicon crystal. It is a cube, having a lattice constant of 5.43 Å [3, 4]. This arrangement of atoms is also known as "Diamond Lattice Unit" because of the same characteristics that diamond crystal has.

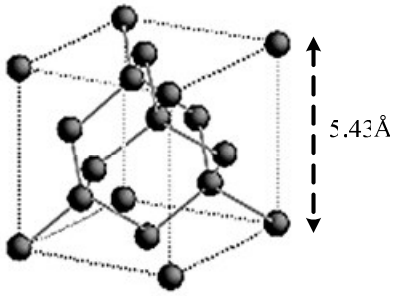


Figure 1.1: The unit cell of crystal silicon with its lattice constant [3].

The crystalline silicon can be grown from melted metallurgical grade silicon by "Czochralski Growth" or "Flat Zone Growth" [2-4]. The melted silicon is purified and then, electronic grade silicon, which is used in micromachining processes, is formed in a long ingot shape. Another technique is the "Epitaxial Growth Technique" [2-4]. The important point is that; the grown silicon takes the exact same characteristic of the below silicon layer during the "Epitaxial Growth Process". Therefore, it can only be done over another crystalline silicon layer.

1.1.2. Miller Indices

The unit cell of the single crystalline silicon can be examined according to its crystallographic planes and directions by referring them separately [3, 4]. Miller indices are used to represent these planes and directions. Figure 1.2 shows some of the crystal planes of the silicon unit cell. Following steps show how to define the Miller indices of a plane;

- First, define the coordinates for the plane. (x, y, z)
- Then, take the reciprocal of each coordinate. $(1/x, 1/y, 1/z)$
- Finally, multiply the coordinates with the smallest common denominator of the three reciprocals. $(y.z/x, x.z/y, x.y/z)$

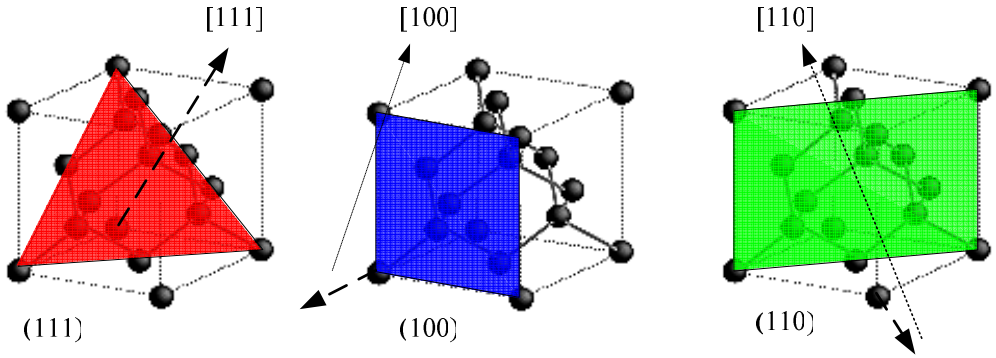


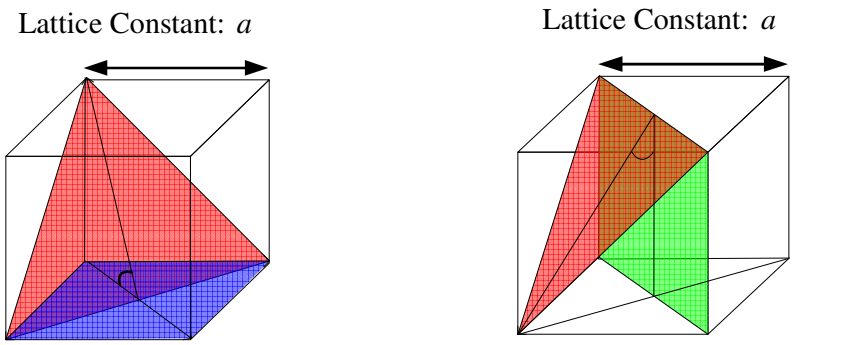
Figure 1.2: Basic planes and their directions of the silicon unit cell.

Since the silicon unit cell is a cubic structure, some planes and their directions have the same characteristic with each other. This makes defining and grouping the characteristic behaviors of the crystallographic planes and their directions easier.

Following notations are used to define these planes. A cap mark is put on top of the coordinate number to indicate the inverse coordinate.

- (100): indicates the crystal planes.
- {100}: indicates all the equivalent planes. The cube faces of the unit cell have the identical atom arrangements coming from the crystal symmetry. That is (100), (010), (001), $(\bar{1}00)$, $(0\bar{1}0)$, $(00\bar{1})$ are equivalent planes.
- [100]: indicates crystal directions. The vector of the defined plane is represented by the direction notation.
- <100>: indicates all equivalent directions.

The angles between planes are important in designing the structures according to the wet anisotropic etching process. Figure 1.3 explains the angles between the defined planes. Since the anisotropic etchants act selectively towards orientation, these angle values define the slope of the outcome structure.



The angle between (100) and (111) plane is: $\alpha = 54.7°$

(a)

The angle between (110) and (111) plane is: $\beta = 35.26°$

(b)

Figure 1.3: Notation of the angle between crystallographic planes of (a) (100) and (111) planes, and (b) (110) and (111) planes.

1.2. Wet Anisotropic Etching

The silicon bulk micromachining technology involves removing silicon from substrate in order to get 3-dimensional mechanical structures [1, 2, 4]. Different etching techniques make it possible to etch the silicon substrate to a depth of hundreds of micrometers and to obtain thin membranes, cantilevers and bridges. The primary tool used in achieving 3-dimensional devices with the bulk micromachining is the wet anisotropic etching process. Anisotropic etchants act selectively towards different orientations of single crystal silicon wafer, producing 3-dimensional structures with only a 2 dimensional protective masking layer.

The etch characteristic of certain etchants over the single crystal silicon substrate differs according to the crystallographic orientation of the substrate surface. The etch rate of (111) plane is significantly low on the contrary of (110) and (100) planes etch rates. Various explanations had been brought for this situation, but none is clear enough. The common sense is due to the different atom density on the surface of each plane. {111} has the highest atom density, and also, has the lowest dangling bond, which are defined as the non-complete covalent bonds [9, 10]. The crystallographic planes expose different numbers of non-complete bonds to the surface. More non-complete bonds enables the etching and increases the etch rate.

Figure 1.4 and Figure 1.5 give cross-sectional views of simulation results after the wet anisotropic etching process of p-type <100> silicon samples. Simulations were done in AniSe IntelliSuite 8.0 tool. Isotropic etchants attacks all planes at the same etch rate, on the other hand; anisotropic etchants make an angle of 54.7º to the (100) oriented substrate, which is the angle between (100) and (111) plane. The same rule goes for (110) oriented silicon samples. During the etching process, the angle between the (110) and (100) planes occurs as 45º. When (111) planes cross, the angle between (110) and (111) can be measured as 35.26º [1-4].

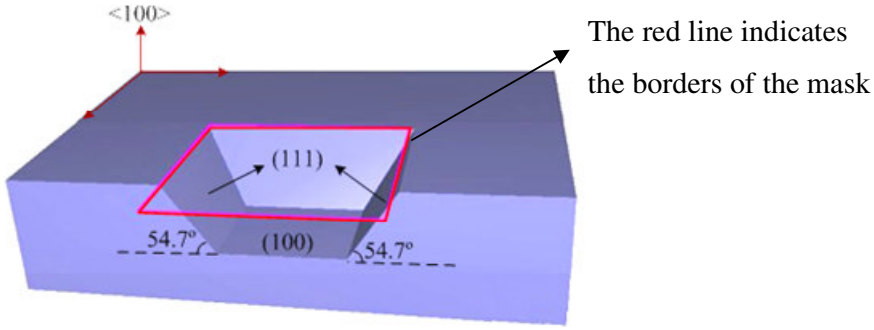


Figure 1.4: Cross section view of anisotropic etching process simulation on (100) oriented silicon wafer.

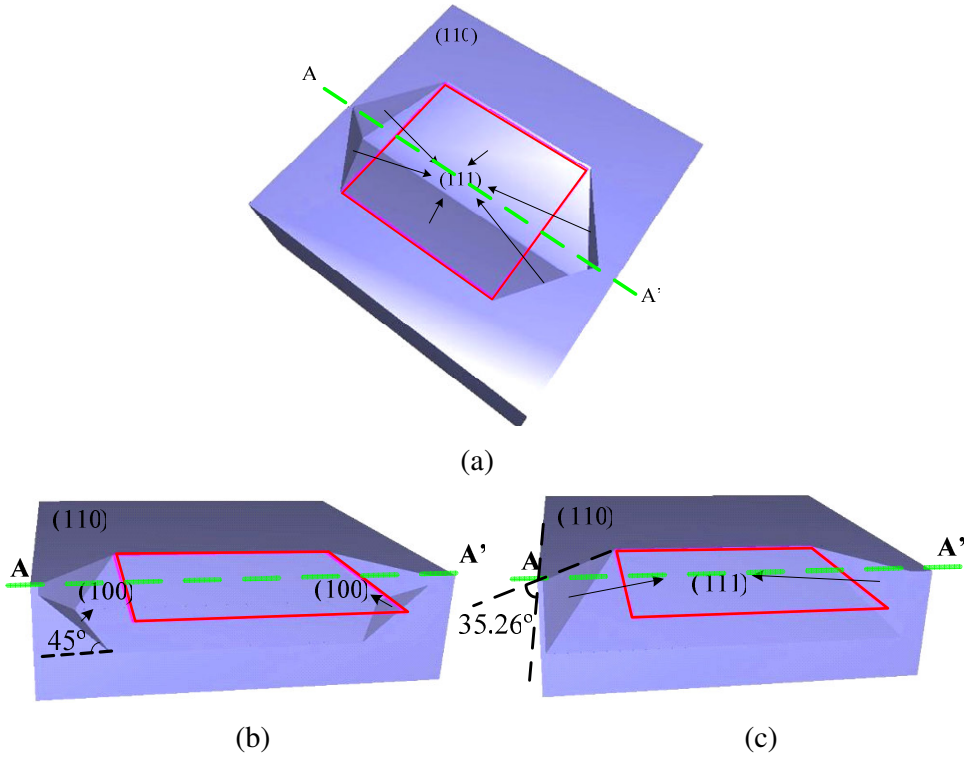
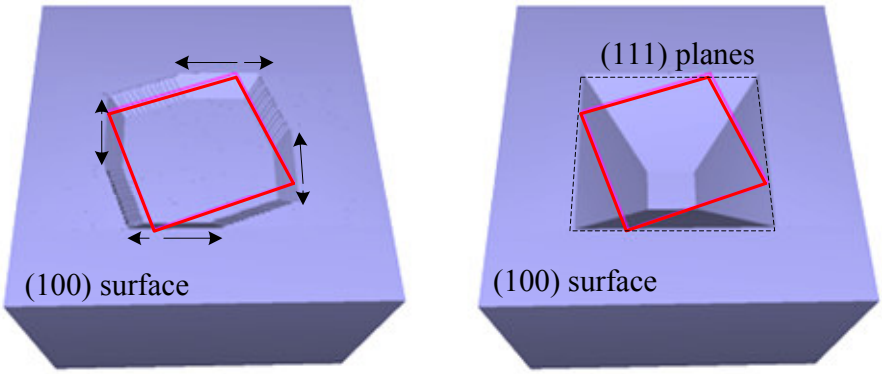


Figure 1.5: Anisotropic etching process simulation on (110) oriented silicon wafer: (a) upper view of the (110) plane after etching. (b) Cross-sectional view of (110) oriented wafer during etching. (c) Cross-sectional view of (110) oriented wafer at the end of the etching.

Since the etching directions are dominated by crystallographic planes, the process masks of the designed structures are needed to be arranged according to these planes. A dislocation of the mask may cause a deformation of the expected etched area. As the etchant reaches to a more resistive plane, the etching of silicon continues all the way of this plane, unless etchant comes across to another resistive plane, which is produced by the mask.

Figure 1.6 illustrates an example of a misaligned masking layer and afterwards, the outcome of the wet anisotropic etching process. The red squares show the boundaries of the masking layer. Side of the masking layer does not aligned according to the (111) planes. Unfortunately, the dimensions and the direction of the etched silicon are not compatible with the masking layers dimensions and direction. The etching continued until the (111) plane resistance which was defined by the corners of the square mask.



(a) (b)

Figure 1.6: Simulation of an anisotropic etching process with a mask, misaligned according to (111) plane: (a) after short etching process and (b) after longer etching process.

Due to these effects, a round structure is impossible to obtain with the anisotropic etching process. An anisotropic etching process was carried out on p-type (100) oriented silicon sample with a round and a randomly shaped silicon nitride masks in order to illustrate the outcome. Process is done in tetra methyl ammonium hydroxide (TMAH) which is an anisotropic etchant. Figure 1.7 and Figure 1.8 give the outcomes of these experiments. Following structures were obtained after 1 hour of etching process with 10wt.% TMAH solution. The thin silicon nitrate film is a transparent material, providing to see the silicon surface beneath it. The side walls of these rectangles are (111) planes. It is also important to mention that the etching reaction continues until the (111) planes intersect on a concave edge. If any convex edge occurs, then these edges are removed with high etch rates.

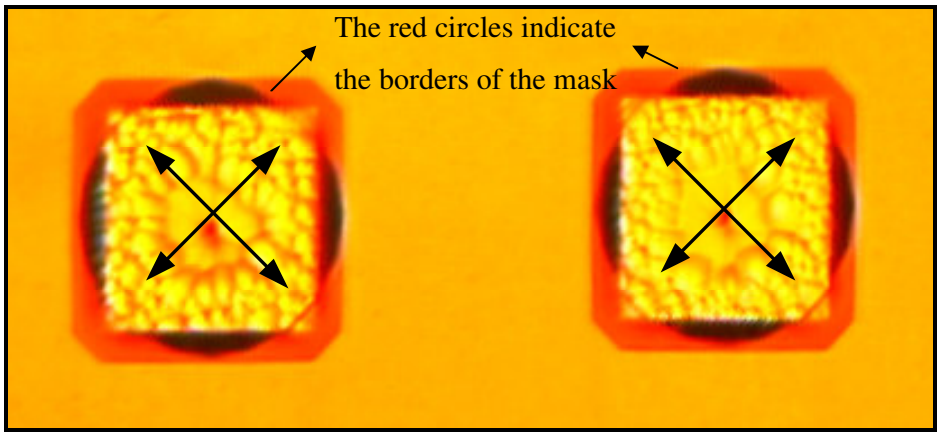


Figure 1.7: The outcome of the anisotropic etching process of a p-type (100) oriented silicon sample with a round silicon nitrade mask.

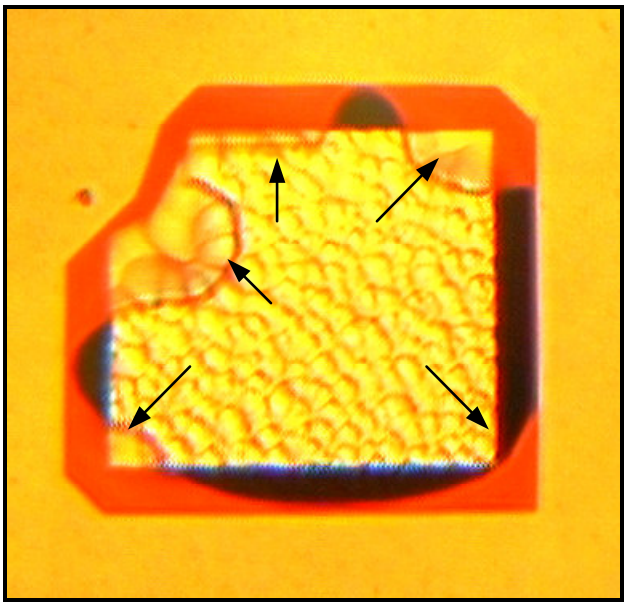


Figure 1.8: The outcome of the anisotropic etching process of a p-type (100) oriented silicon sample with an irregular shaped silicon nitrade mask.

The etch rate of convex edges is higher than any plane on the silicon surface. The high etch rate of the convex edges is an important feature for mask design parameters. Most 3-dimensional structures are designed according to this fast edge removal feature. Cantilevers, bridges and thin membranes can be obtained easily. Figure 1.9 demonstrates steps of the removal of the convex edges.

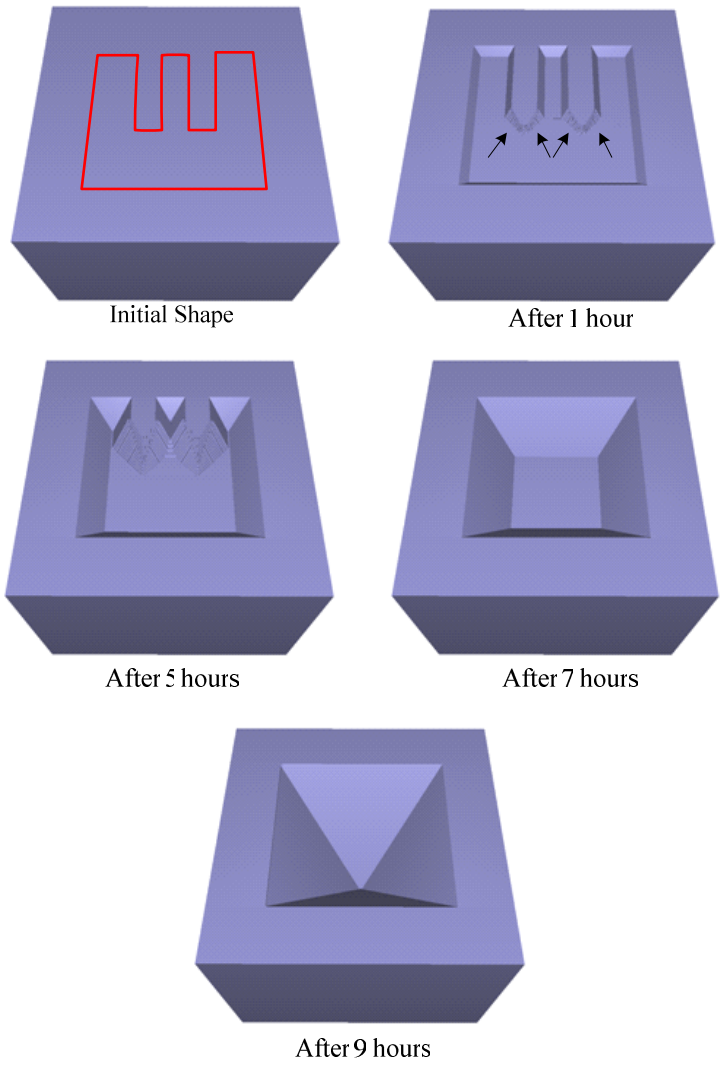


Figure 1.9: Steps of the removal of the convex edges.

The removal of convex edges is illustrated with a silicon etching experiment. The experiment was done with a p-type (100) oriented silicon sample. The etching process took 30 minutes. Figure 1.10 shows the outcome of the anisotropic etching process of p-type (100) oriented silicon sample showing the high etch rate of convex edges. The different etch rates of the crystallographic planes of the silicon can also be examined clearly.

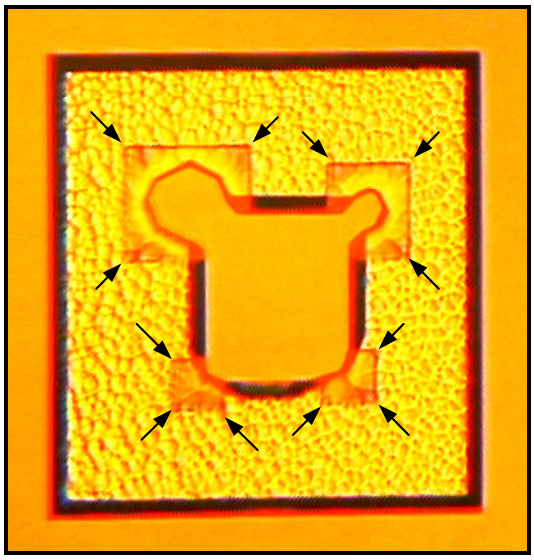


Figure 1.10: The outcome of the anisotropic etching process of a p-type (100) oriented silicon sample showing the high etch rate of convex edges.

1.2.1. Anisotropic Etchants

Any solution, which has a larger pH value of 12, can be used as an anisotropic etchant. Main issues, concerned about an anisotropic etchant, are; high etch rate of silicon, high etch rate dependency of the crystallographic planes, smooth etched surface, low etch rate of the masking material, compatibility with the CMOS process, low toxicology and easy handling [11].

Anisotropic etchants are aqueous alkaline solutions which can be divided into two groups, according to its main component: (1) inorganic aqueous solutions, like potassium hydroxide (KOH), Sodium hydroxide (NaOH), Cesium hydroxide (CsOH), Ammonium hydroxide (NH_4OH), and hydrazine; (2) organic aqueous solutions, like tetra methyl ammonium hydroxide (TMAH, $(CH_3)_4NOH$),

ethylenediamine ($NH_2(CH_2)_2NH_2$), and choline ($((CH_3)_3N(CH_2CH_2OH)OH$) [2, 12]. Ethylenediamine is used in process with the addition of certain amount of water and pyrocatechol. This compound is called EDP. Among these etchants, following sections provides more information on KOH, TMAH, and EDP. These etchants are mostly preferred in the wet anisotropic etching process applications.

1.2.1.1. KOH: Potassium Hydroxide

KOH has a high (100)/(111) etch rate ratio compared to TMAH and EDP [11]. However, the etching selectivity of KOH against SiO_2 is not high enough for making SiO_2 as a masking layer for KOH etching processes. Instead, silicon nitrate films are preferred as a masking layer. Also, KOH is not compatible with the CMOS process since the mobile alkali ions contaminate the oxide layer. Therefore, it is especially preferred with backside anisotropic etching of silicon. If not enough attention and precautions are satisfied during the etching process, KOH can cause blindness [12]. However, KOH is easy to handle compared to EDP. Table 1.1 gives the <100> silicon etch rates in various concentration of KOH [9]. The etch rates of silicon are highly dependent to temperature. Moreover, they also vary according to the concentration of KOH solution.

Table 1.1: (100) oriented silicon etch rates of KOH solutions according to different concentrations and different temperature values [9].

	Temperature			
%KOH	**60ºC**	**70ºC**	**80ºC**	**90ºC**
10	0.425 um/min	0.76 um/ min	1.36 um/min	2.33 um/min
15	0.4416 um/min	0.81 um/min	1.43 um/min	2.45 um/min
20	0.445 um/min	0.81 um/min	1.43 um/min	2.46 um/min

1.2.1.2. EDP: Ethylenediamine, Water & Pyrocatechol

EDP has a wide variety of masking materials like SiO_2, Si_3N_4, Au, Cr, and Cu [10, 13]. The process is far away from alkali ions contamination. However, pyrocatechol used in EDP is known as a very toxic and corrosive material [12]. High safety must be satisfied for the process engineer. Also, the process materials should be kept separated from other materials and should not be mixed in any other processes. The reason is that a vapor is developed as a side product during the EDP etching process. It leaves a dark brown residue on where it contacts. Cleaning this residue and sterilizing the process materials are somehow impossible. Furthermore, it is very hazardous for health, if it is breathed. Therefore, handling EDP is very hard, which makes EDP less popular among other etchants. Nevertheless, EDP produces a smooth etched surface, which is a very important problem for surfaces etched with anisotropic etchants [13, 14]. Also, EDP is the best choice for heavy boron diffused etch stop techniques, as will be explained later [14].

1.2.1.3. TMAH: Tetra Methyl Ammonium Hydroxide

TMAH is the most popular etchant among others. The reason is coming, mostly, from its compatibility with CMOS process [11, 15-17]. It can be easily utilized in clean room processes. Furthermore, TMAH is not toxic, and it is easy to handle the process [11, 16, 17]. The disadvantages that TMAH brought to the process are low silicon etch rate, high aluminum etch rate, and rough silicon surface outcome [17]. These problems can be solved by adding the proper surfactant to the TMAH solution at precise order. High aluminum etch rate can be lowered by doping the TMAH solution with certain amount of silicon or silicic acid. The surface roughness can be prevented by adding surfactants like isopropyl alcohol or ammonium peroxodisulfate. SiO_2 can be a trustable masking layer towards TMAH etching.

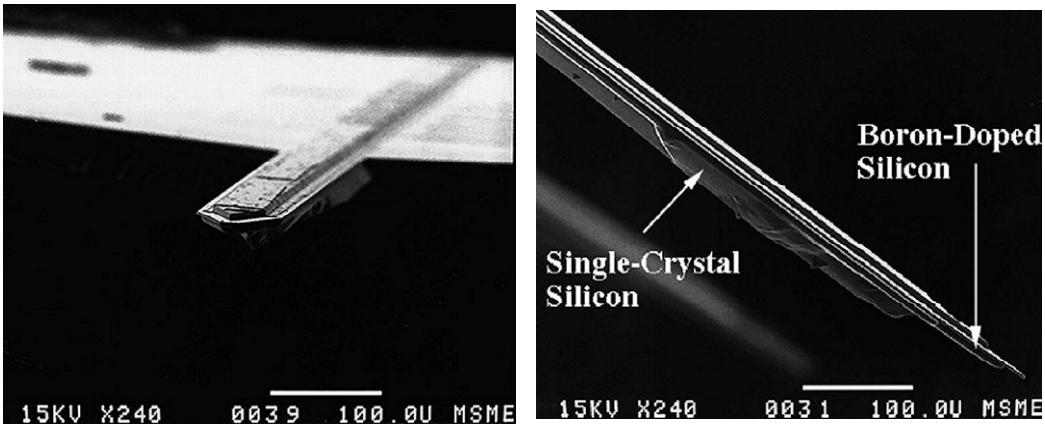
Furthermore, Si_3N_4 shows excellent resistance against TMAH, with an etch rate of nearly 0Å [12].

1.2.2. Etch-Stop Techniques

The main problem in the wet etching process is the preciseness of the etch stopping region. Critical structures always preferred to be etched with dry plasma etchants so always etch-stop mechanisms can be controllable. In the wet anisotropic etching process, two etch-stop techniques presents this control to the process engineers [2, 4, 12]: (1) the heavily boron diffused etch-stop technique, and (2) the electrochemical etch-stop technique.

1.2.2.1. Heavy Boron Diffused Etch-Stop Technique

A heavily boron doped silicon layer is a barrier layer for anisotropic etchants. The etch rates of crystallographic planes of boron doped silicon substrate decrease drastically starting at boron concentrations of approximately 10^{-19} cm^{-3} [10]. This technique enables fabrication of 3-16μm-thick thin membranes with boron diffusion in boron diffusion furnaces. It is also possible to obtain very thin membranes of 200nm with the help of ion implantation process. A shallow, highly boron doped areas can be formed with precise ion implantation processes [18-20]. Figure 1.11 shows a free-standing silicon processed microneedles produced by EDP etching process with the control of heavy boron doped etch stop technique [19]. However, the heavily doped silicon degenerates and makes it impossible to construct electronic devices on it. The electrochemical etch-stop technique exceeds this problem and brings another point of view, as it is explained in next section.



(a) (b)

Figure 1.11: Free-standing silicon processed microneedles produced by EDP etching process with the control of heavy boron doped etch-stop technique [19]: (a). near "head-on" view of a free-standing microneedle, and (b) side view of a whole microneedle.

1.2.2.2. Electrochemical Etch-Stop Technique (ECES)

The electrochemical etch-stop technique intends to control the etching process by applying appropriate voltages to silicon surface; the etching reactions can either be stopped or be enhanced by biasing the silicon surface [9, 11, 12]. Preventing the etching reactions can be possible by oxidizing the silicon surface. Applying the precise voltage during the wet anisotropic etching process can oxidize the silicon surface, which is called anodic oxidation. This technique can control the etching reactions on phosphorus doped and boron doped regions of a silicon substrate, separately. One can easily prevent etching reactions on the n-diffused area by growing an oxide layer on its surface where it is exposed to the etchant, meanwhile; enhancing the etching reactions on the p-diffused area by biasing them individually at specific voltages. This technique is very common since it does not have a

drawback like the heavily boron doped etch stop technique. However, mechanism of anisotropic etching and the applied voltage values should be determined precisely, and the variables of the etchant should be controlled well. Figure 1.12 and Figure 1.13 shows two microstructures formed by using electrochemical etch-stop technique.

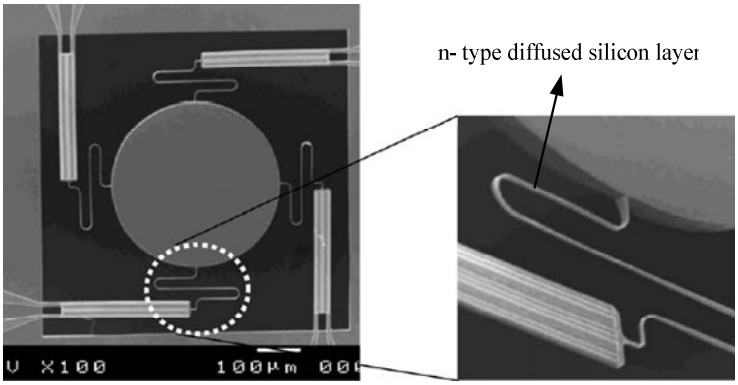


Figure 1.12: 3D free space thermally actuated micromirror hanging on four actuators and four springs produced by etching process with the control of electrochemical etch-stop technique [21].

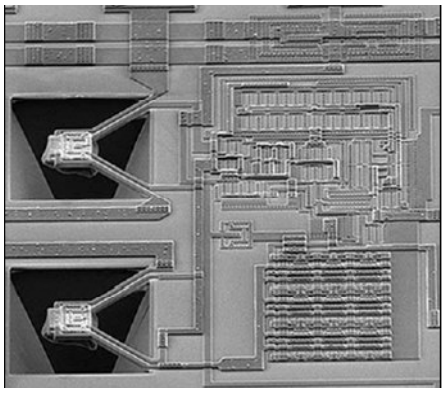


Figure 1.13: Diode-based thermal RMS converter with on-chip circuitry fabricated using electrochemical etch-stop technique [22].

The detailed investigation about the electrochemical etch-stop technique is the main theme of this thesis and covered in forthcoming chapters. The main objective about investigating variables of electrochemical etch-stop technique is to have a successful, controllable and a stable anisotropic wet etching process which can be used in the production step of an integrated MEMS sensor. Therefore, an optimization of the anisotropic etching process with the electrochemical etch-stop technique application is done with the proper anisotropic etchant. Then, the optimized procedure is applied to the microbolometers which were designed in METU MEMS-VLSI group as a demonstration.

Figure 1.14 illustrates an SEM picture of previously achieved microbolometer structure by using a wet anisotropic etching process together with the electrochemical etch-stop technique. Following section gives a brief summary of the structure and working principle of the microbolometers as an introduction.

1.3. Thermal Detection Mechanisms: Microbolometer Detectors

Detecting an object depends on sensing the radiation it emits. Despite the natural illumination, human eye is not capable of sensing long and small wavelengths emitted from the object like infrared radiation. It is known that; every object above absolute zero (0 Kelvin) releases infrared radiation. By making these radiation variations measurable, detection of any objects can be possible, even in dark or smoke. These benefits of infrared image detection are widely used in military, civilian, and medical applications.

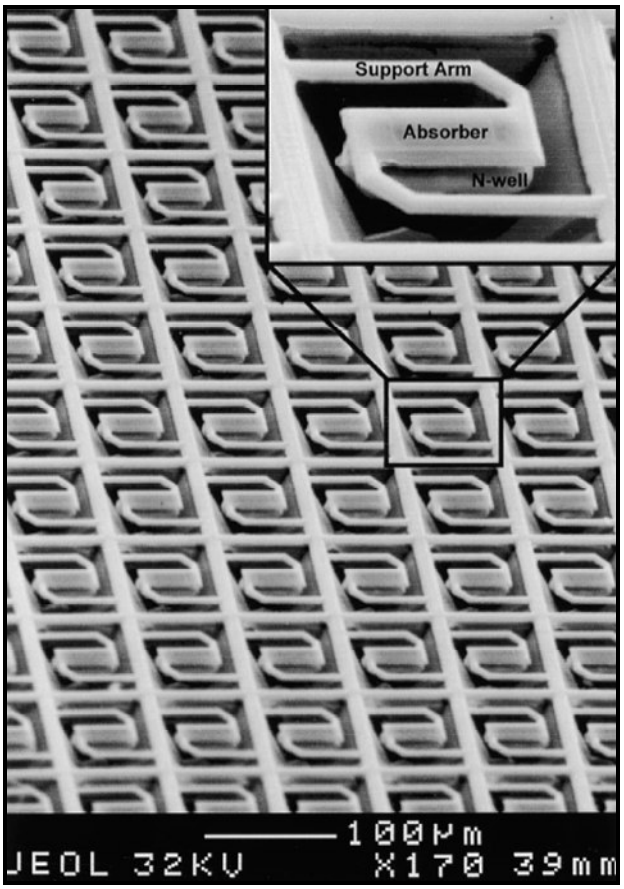


Figure 1.14: Array of infrared microbolometer detector, achieved by using a wet anisotropic etching process together with the electrochemical etch-stop technique. Here, the etching of the n-well under the absorber area is prevented by applying a passivation voltage [23].

One of the most important mechanisms for infrared detection is thermal detection. The main advantage of this mechanism is its low cost. In thermal detectors, the effect of the temperature change over the sensitive material properties, caused by the absorbed radiation, is measured. These variations due to radiation are converted to electrical signals with proper circuits.

There are 4 types of thermal detection mechanism: (1) microbolometers, (2) pyroelectric detectors, (3) ferroelectric detectors, and (4) thermoelectric detectors. In order to have very low-cost detectors with high performance, diode type microbolometers are designed and implemented in METU.

1.3.1. Diode Type Microbolometer Structure

Thermal detectors, designed as diode type microbolometers, have a sensitive area with an n-well/ p^+-active diode structure [24]. An oxide layer, which covers the sensitive area, absorbs the incident radiation causing a temperature increase on the pixel. This increase directly affects the temperature of the buried diode structure. The bolometer pixels measure the variations in either the diode current or the diode voltage as a result of the variations in pixel temperature, depending on the biasing methods. One measurement method is to bias the pixel diodes with constant current and to measure the change in the diode's forward-bias voltage due to incident radiation, with respect to a reference voltage. The diode's forward-bias voltage changes are related with the temperature coefficient of the sensitive area of the pixel, which is related with the diode structure. The increase in the detector temperature, which is sensed by this sensitive area, is due to radiation of the target object. Therefore, the diode structure must be thermally isolated from the substrate for measurements with high detectivity.

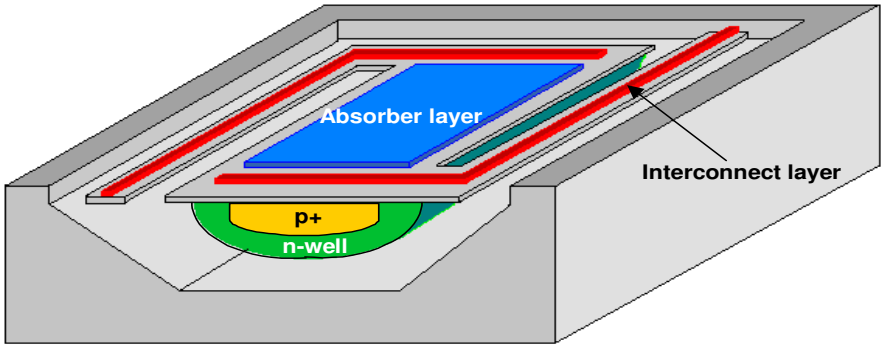


Figure 1.15: Diode-type microbolometer pixel structure [25].

Figure 1.15 shows a diode-type microbolometer pixel structure. The diode structure is occurred in the p-type substrate with an ion implantation process. The suspended sensitive part is carried with the supporting arms, which also have the electrical connections from the diode structure. However, the design of the arms must be made by carefully considering the amount of heat transferred to the substrate from the suspended area through the arm connections. Thin arms, carrying the interconnect layer, are rounded from the corner of the sensitive area and they are made as thin as possible to reduce the thermal conductance between the suspended region and the substrate. For the same purpose, the interconnect layer is selected to be polysilicon, which has lower thermal conductance compared to metal layers. Figure 1.16 gives the cross-sectional views of each step of the post processing of a microbolometer pixel [24]. Figure 1.16a shows the cross-sectional view of the pixels after the CMOS fabrication. The metallization layer and silicon surface is protected by a thick oxide layer. First, to reach the silicon substrate, the oxide layer is etched with the dry plasma etching process, having exact controllability of anisotropy on one direction from the etch openings. Figure 1.16b illustrates the result of the dry plasma etching process. Then, silicon substrate is etched with the wet anisotropic etching process. Figure 1.16c demonstrates the cavity that satisfies a thermal isolation for the diode structure. The electrochemical etch-stop technique is applied to the n-well region of

the diode structure. With this technique, the etching reaction of the p-substrate from the etch openings is enhanced by a proper bias applied to the bulk silicon substrate.

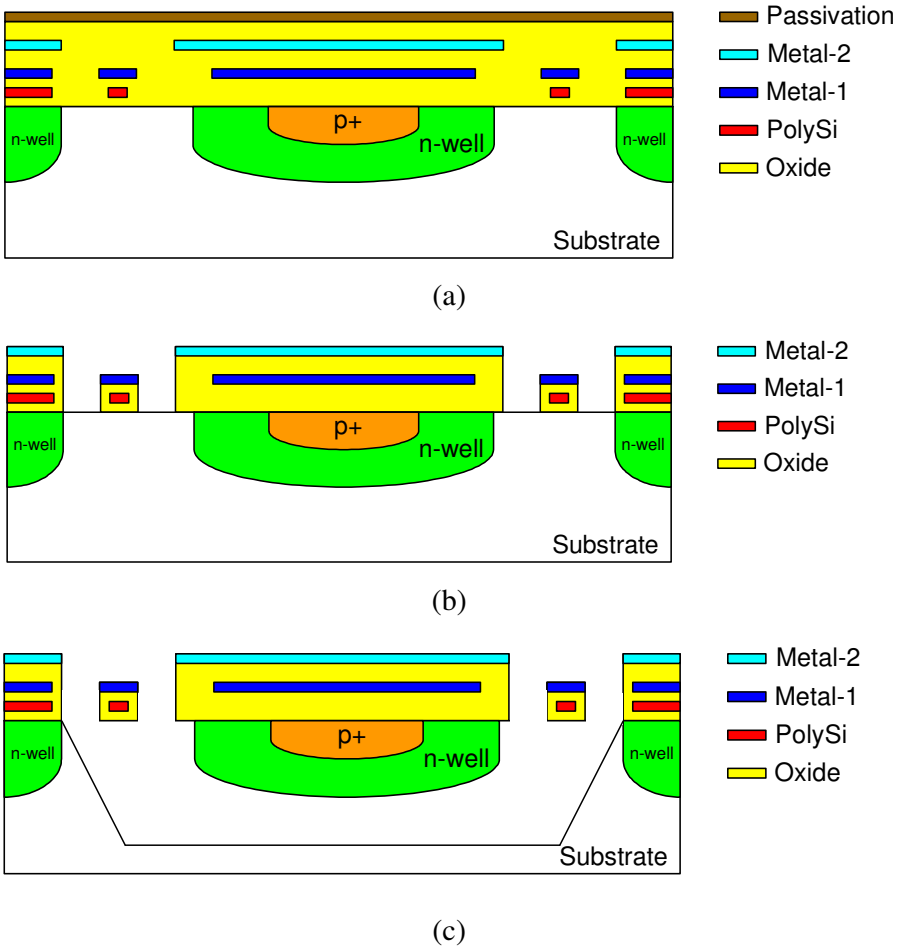


Figure 1.16: Cross-section view of microbolometer pixel [24]. (a) The microbolometer pixel after the CMOS fabrication process. (b) The microbolometer pixel after dry plasma etching process. (c) The microbolometer pixel after wet anisotropic etching process with the control of electrochemical etch-stop technique.

1.3.2. Selection of Anisotropic Etchant Utilized over CMOS Microbolometers

The most important point in the selection of the etchant for the wet anisotropic etching process of the CMOS microbolometers is whether the etching process is done from the front side of the pixels or from the back side of the wafer. The back side etching can be done by using a single masking layer, which is drawn according to the anisotropy between (100) and (111) plains. If the design of the microbolometers is made for a front side anisotropic etching, then the etchant selection is done according to the property of CMOS compatibility of the etchant. Moreover, a low etch rate for SiO_2 is very critical. These necessities lead us to select the TMAH solution as the anisotropic etchant. Above all, TMAH satisfies most of the vital requirements like ease of handling and low toxicity. However, there are also some drawbacks, as previously mentioned. If a back side anisotropic etching is suitable for the fabrication process, then KOH can be the best choice for the process.

Previously, many anisotropic etching processes with TMAH solutions by applying the electrochemical etch-stop technique were done [24-26]. Some of them succeeded, and suspended absorber areas with protected n-well regions were obtained. But, on the other hand, applying the electrochemical etch-stop technique becomes harder to implement when the design of the microbolometers enhances. Determining the important variables that affect the fabrication of the devices is essential for the reproducibility of the devices and the etching processes.

1.4. Research Objectives and Thesis Organization

The goal of this thesis is to investigate the electrochemical etch-stop technique under the determination of the characteristic of TMAH solution. The specific objectives can be listed as follows:

- Characterization of TMAH under the definition of the anodic passivation theory. The effects of temperature and concentration of the etchant to the etch rate and surface smoothness are studied. An optimization of the TMAH solution is done in order to apply it for future works.

- Design and fabrication of etch samples, which are used in the investigation of etching process and ECES implementation on microbolometer with the TMAH solution. The effect of the structural design is studied with these etch samples.

- Study and comment on the results of the designed samples etched with previously optimized TMAH solution. The effect of applied voltages over the etch-stop layer thickness, the effect of the n-well diffused areas to each other when a passivating voltage is applied to them are investigated. The post-CMOS etching process of a microbolometer is done with the optimized TMAH solution as a demonstration.

This thesis is organized as follows:

The study has begun with the investigation of the theory of the electrochemical etch-stop technique and determining the etching reactions that takes place on the surface

of the silicon. Chapter 2 presents the basic theory of anodic oxidation. Detailed investigation about previously selected anisotropic etchant, TMAH is given. Effect of etchant temperature, etchant concentration and illumination is explained with experimental results. This chapter gives an optimized TMAH solution for anisotropic etching processes.

Chapter 3 tells the design and fabrication of etch samples in order to study the consequences of etching process and ECES implementation on microbolometer structures. Each fabrication step is explained in detail.

Chapter 4 includes the results of applying the electrochemical etch-stop technique to the fabricated samples. Fabrication of the microbolometers with the optimized TMAH solution is given as the device fabrication with the electrochemical etch-stop technique.

Finally, Chapter 5 summarizes the achievements, presents the conclusion of this research, and gives suggestions for future studies.

CHAPTER 2

THEORY OF ELECTROCHEMICAL ETCH-STOP TECHNIQUE AND TMAH OPTIMIZATION STUDIES

This chapter explains the theory of the electrochemical etch-stop (ECES) technique and the optimization of the TMAH solution for the wet anisotropic etching process. Section 2.1 gives information about the anodic passivation of silicon which is the base of the ECES technique. The section discusses the control of the etching process by applying bias between the silicon and the TMAH solution. Section 2.2 explains the I-V curve experiments; setup and sample preparation. The outcomes of these experiments determine the passivation potentials and open circuit potentials needed for controlling the etch reactions on the silicon surface. Section 2.3 discusses the optimization of TMAH solution. The section investigates the behavior of the TMAH solution under the effect of temperature and concentration. Moreover, in order to enhance the etching process with TMAH, the effect of the daylight over the etching profile, high aluminum etch rateof TMAH, and the prevention of the surface roughness are studied. Section 2.4 gives the details of ECES setup and implementation information. Finally, Section 2.5 concludes the chapter by summarizing the theory of ECES technique and defining the outcome of the TMAH solution optimization.

2.1. Anodic Passivation of Silicon

The ECES technique is based on the anodic passivation process of the silicon. This ability provides preventing the etching reactions by applying potential to the silicon surface with respect to the etchant. This section first provides short information on anodic passivation of silicon. Then it gives the results of experiments for characterization of anodic passivation of silicon within the framework of this study.

The removal of the silicon atom in an alkaline solution happens as an outcome of a reduction–oxidation (RED-OX) reaction. The main reactants of the etchant are water molecules and the hydroxide ions. After the immersion of a silicon sample into the etchant, no matter whether it is n-type or p-type doped, a negative excess charge develops on the surface of the silicon due to the higher Fermi level of the RED-OX couple H_2O/OH^- with respect to the Fermi level of the silicon sample [9, 27]. Following reactions take place, respectively.

1. Hydroxide ions, which are in the strong base etchant, form a silicon hydroxide complex by affecting on silicon surface [27]. Equation 2.1 shows the first step of the reaction. The OH^- ions continues the reaction on the complex that results with the oxidation of the silicon compound on the surface. Equation 2.2 gives the outcome of the reaction with OH^- ions. The continuing OH^- attachment to the dangling bonds of the silicon causes the silicon atom to be removed from the surface. Thus, the etching is accomplished. Four electrons are generated due to the oxidation reactions.

$$Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 2e^- \qquad 2.1$$

$$Si(OH)_2^{2+} + 2OH^- \rightarrow Si(OH)_4 + 2e^- \qquad 2.2$$

2. The generated electrons are directly used in the reduction of the water molecules. This reaction takes place on the surface of the silicon [27]. As an outcome, OH^- ions and H_2 molecules are produced. Equation 2.3 and 2.4 shows the steps of reduction of the water molecules.

$$4\ H_2O + 2e^- \rightarrow 4\ H_2O^- \qquad 2.3$$

$$4\ H_2O^- \rightarrow 4OH^- + 2H_2 \qquad 2.4$$

Since the silicon surface is negatively charged due to the difference between the Fermi levels of silicon and the etchant, silicon surface prevents and drives back the hydroxide ions coming from the etchant [9]. For this reason, hydroxide ions used in the oxidation of silicon are not from the strong base etchant. Instead, these hydroxide ions are generated at the reduction step and located within the surface of the silicon. Only the beginning of the oxidation reaction is done by the hydroxide ions coming from the etchant [9, 27, 28]. Otherwise, the etch rate of the solution would be extremely dependent to the OH^- concentration of the solution. But, the fact is that the etch rate of EDP solution, which has an OH^- concentration of 0.034mol/lt., is nearly as large as KOH solutions with an OH^- concentration of 5-10 mol/lt.[9]. Continuous OH^- ion generation develops a continuous silicon atom removal from the surface.

Another product of the reactions is H_2 molecules. The hydrogen bubbles occur on the surface of the silicon, and if they are not diverged from the surface, they cause the etch rate to fall. Many surfactants may be used in order to repel these bubbles from the silicon surface.

These oxidation and reduction reactions happen without applying any voltage to the sample. At this point, a potential which is called open circuit potential, (OCP), is observed between the silicon and the etchant which forms from the difference of the Fermi levels of silicon and the etchant [28]. The DC current passing through the etchant is zero, and the system is in steady state condition at open circuit potential.

3. The reduction reaction produces the necessary OH^- ions for the oxidation of the silicon. If the reduction reaction is prevented, then the production of the OH^- ions will also be prevented, causing the silicate compound not to separate from the surface, but also generating a polymerization on the surface [9, 28]. Equation 2-5 gives the polymerization products on the silicon surface.

$$Si(OH)_4 \rightarrow SiO_2 + 2H_2O \qquad 2\text{-}5$$

Eliminating the electrons, which are generated in the oxidation step, can prevent the reduction reaction. Without any electrons, the reduction of water will be stopped, and the lack of OH^- ions will cause the silicate molecules not to dissolve in the solution. This can be satisfied by applying an anodic voltage, the passivation potential, (PP), to silicon with respect to the etchant. At this voltage value, anodic passivation of the silicon surface can be achieved and etching process will be stopped due to the generated oxide layer.

A current–voltage (I-V) curve is needed to be obtained in order to determine the OCP and PP values of an etchant. This experiment consists of measuring the current through the silicon substrate during a voltage sweep applied on silicon substrate with respect to the etchant. Following section explains the details of I-V curve experiments done in the framework of this study.

2.2. I-V Curve Experiments

Figure 2.1 shows the setup which is prepared for the I-V curve experiments to determine the open circuit potential and passivation potential. A conventional three-electrode set-up was employed using a platinum wire as a counter electrode, and a silver/silver chloride (Ag/AgCl/sat KCl) electrode as a reference electrode. The voltage is applied to the silicon substrate under the control of the potentiostat. Working electrode of the potentiostat biases silicon sample with respect to the reference electrode which monitors the etchant's potential. The applied voltage is increased at a rate of 1mV/sec., starting from -2V to 1V. During this voltage sweep, the current between silicon sample and the etchant is read by the multimeters directly connected to the computer. The current and voltage information is combined and I-V curve is obtained with the accessory of a PC.

The potentiostat (Elchema Model PS-205) applies a voltage of -2V to its working electrode with respect to reference electrode. This voltage is swept by the connected power supply (Agilent E3631A) which is controlled from a PC. The voltage increment is arranged to be 1mV/sec. by the HP VEE program. The current through silicon sample was measured by a digital multimeter (Agilent 34401A).

The reference electrode, RE, is responsible for reading the potential of the etchant. The working electrode biases the sample with respect to the solution, by the reference electrode. On the other hand, no current must flow from reference electrode in order to avoid depletion of the etchant. Hence, an ohmic contact to the solution is satisfied by the counter electrode, CE.

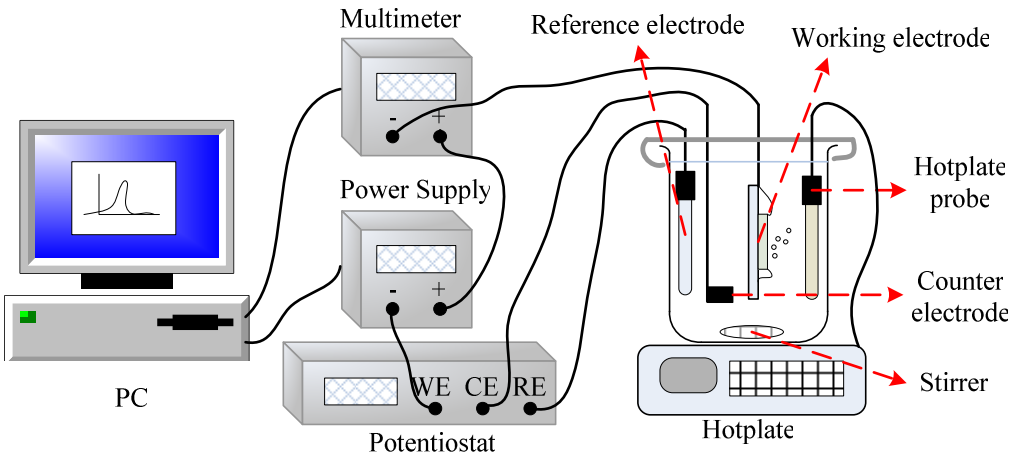


Figure 2.1: I-V curve experiment setup prepared to determine the open circuit potential and passivation potential.

I-V curve experiments were performed with samples from 4 inch (100) oriented n-type and p-type silicon wafers. Resistivity for the n- type wafer is 1-10Ωcm., where as resistivity of the p-type wafer is 5-10Ωcm. A silicon nitride layer was deposited on the wafers to serve as an etching mask. A photolithography process was applied in order to obtain 1.5mm X 1.5mm square openings to access to the silicon surface. The silicon nitride layer over these square openings was etched with the RIE process. The samples were diced and prepared for the etching process. Figure 2.2 gives the steps of sample preparation for I-V curve experiments.

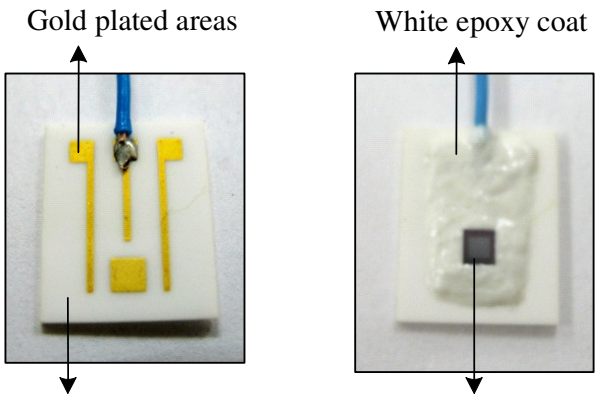


Figure 2.2: Sample preparation for I-V curve experiments: (a) an electrical connection is obtained from the gold-plated areas of the alumina substrate by soldering a wire, and (b) the sample is placed over the gold plated area, and a connection is done with silver epoxy. The sample is stabilized on the alumina substrate, and total gold-plated area is covered with white epoxy.

Samples were placed on an alumina substrate, which had a wire soldered to gold-plated area on it. A silver epoxy (Emerson & Cuming) was used to make contact with the substrate. Diced, square samples were placed on the gold-plated areas with the silver epoxy. However, the silver epoxy does not harden enough and would cause the etchant to be effected from the applied voltage. Therefore, the sample must be covered with the white epoxy (Dexter Company Hysol 1C). The white epoxy is an insulator, and it becomes very resistant to all types of acidic and basic solutions after a proper curing process. Gold coatings and soldered wire parts were completely covered with white epoxy in order to prevent the etchant to be effected from the applied voltage to the substrate. Samples were ready for chemical processes after 1 hour of curing at 120ºC on the hotplate.

These samples were cleaned before the etching process. For this purpose, firstly, samples were dipped in Trichloroethylene (TCE) for 2 minutes. TCE is used to remove the organic contamination. It is very hazardous and may even cause death if it is breathed at high levels. TCE dissolves very little in water; but it evaporates quickly in water, merges with air, and becomes more dangerous for health [29]. It may stick to particles and remains for a long time. Removing TCE from the surface can be possible with an acetone bath. Therefore, samples were dipped into acetone for 2 minutes. Afterwards, samples were immediately dipped into isopropyl alcohol (IPA) for 2 minutes in order to avoid stains caused by the fast evaporation of acetone. The native oxide layer over the exposed silicon area was needed to be stripped before the etching process. Dipping the samples in 5wt.% hydrofluoric acid (HF) solution for 20 seconds, would be enough for this purpose. HF is an aggressive silicon dioxide etchant and does not harm the silicon surface. A diluted HF solution is enough for stripping the native oxide layer.

The etching solutions were prepared to be 100ml at different ratios of TMAH solution and deionized water. The used TMAH is a product of MERCK. The etchant was heated on hotplate, while heating was controlled by the hotplate's probe. A stirrer was used to enhance the uniformity of both concentration and temperature of the solution. The top of the beaker was covered with aluminum foil in order to keep the concentration of the solution stable during the etching process.

Figure 2.3 shows the outcome of I-V curve experiments done with 25wt.% TMAH. The experiment was carried out with a p-type silicon sample. A 25wt.% TMAH solution was heated to 85°C. The obtained I-V curve is similar to those obtained in the literature [27, 30, 31]. Table 2.1 gives the open circuit potential (OCP), passivation potential (PP), and the flade potential (FP) values for p-type silicon sample, according to the I-V curve on Figure 2.3.

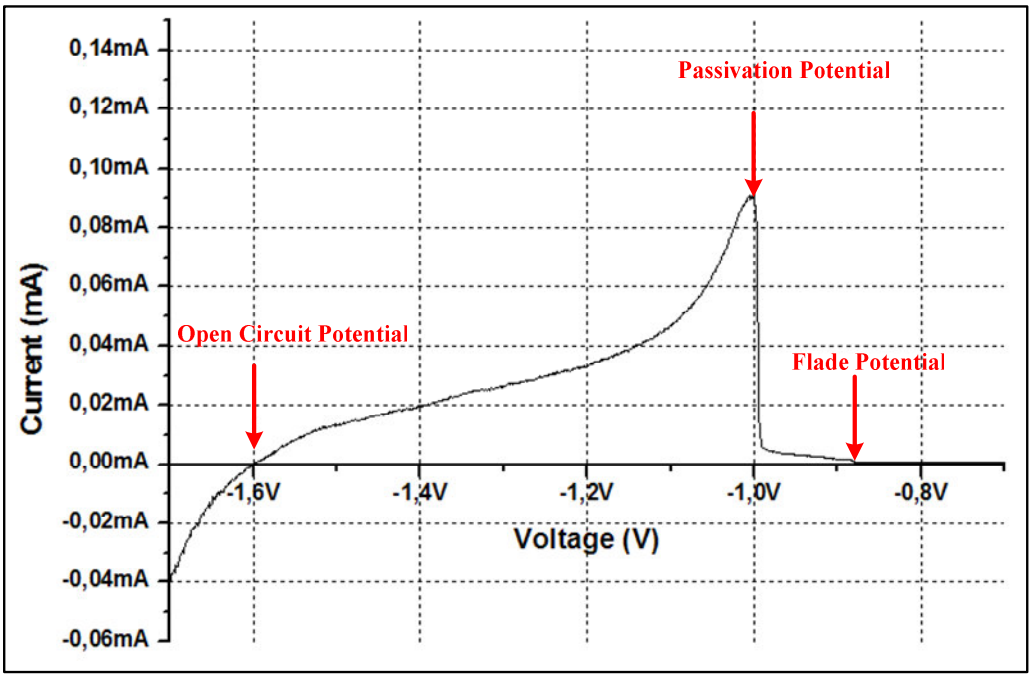


Figure 2.3: I-V curve of p-type (100) oriented silicon sample, obtained in a 25wt.% TMAH solution.

Table 2.1: Open circuit potential (OCP) and passivation potential (PP) values for p-type silicon sample, etched in 25wt.% TMAH at 85°C.

25wt.% TMAH at 85°C	**p-type silicon**
Open Circuit Potential	-1.59 V
Passivation Potential	-1.06 V
Flade Potential	-0.87 V
Etch Rate	0.75 µm/min.

Applying a negative voltage to the silicon with respect to OCP causes an increase on the conduction band electrons of the silicon, which creates an enhancement in the etching process. As the applied potential becomes more anodic than OCP, the electrons on the conduction band of the silicon start to be appealed. At the passivation potential, all electrons are eliminated, and thus, reduction of the water reaction is prevented due to the lack of conduction band electrons, causing the etch to be stopped. This can be observed with the sudden drop on the current at PP from Figure 2.3. The etching process is stopped at voltages higher than PP. The current decreases to a minimum value, which is called as Flade Potential.

After the PP value, the silicon surface is covered with a complex form of SiO_2. If passivation occurs on the silicon surface, the only way to continue the etching process is to dip the sample into hydrofluoric acid solution to get rid of the oxide layer on the silicon surface or to keep the sample in the etchant without applying any voltage until the chemical breakdown of the anodic oxide [31].

The following section explains the investigated titles under the facts coming from I-V curve experiments and SEM pictures of the results for TMAH solution.

2.3. Investigation on TMAH

The main issues that must be enlightened are the effect of daylight, temperature and the concentration of the TMAH solution. Determination of these factors and outcomes of etching processes are investigated in detail, as explained below.

2.3.1. Effect of daylight during etching process

The I-V curve of the silicon sample is affected from the daylight during the experiments. The daylight increases the maximum current measured from the working electrode of the silicon sample. The measured etch rates are clearly indicate that daylight improves the etch rate and the amount of H_2 bubbles. Figure 2.4 shows the effect of daylight on p-type silicon sample during etching with a 25wt.% TMAH. A change in the OCP values can be an expected outcome due to the effected Fermi levels of samples from the daylight [32]. Table 2.2 shows the silicon etch rate of TMAH solution, which is affected from the daylight during the I-V curve experiments.

Although daylight enhances the etching process, the variation of the passivation potential and the open circuit potential endangers the ECES application. If the etching process is decided to be done under daylight, then the same illumination amount must be satisfied during all etching processes. However, this may be a problem for etch setup and may threat the stability of the process. Thus, experiments and device fabrication processes are decided to be made under darkness.

Table 2.2: Silicon etch rates of TMAH solution, showing that the etch rate is affected from the daylight during the I-V curve experiments.

	25wt% TMAH at 85°C under daylight	**25wt% TMAH at 85°C without daylight**
Etch Rate of p-type silicon	0.97 µm/min.	0.75 µm/min.

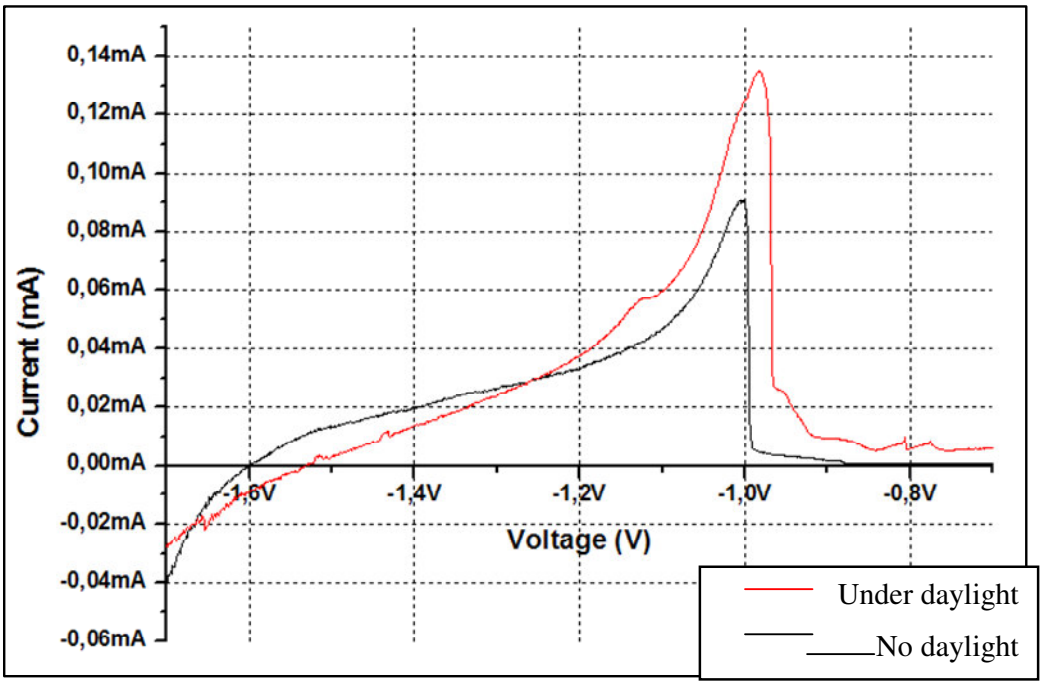


Figure 2.4: Variation of the I-V curve of p-type silicon sample in 25wt.% TMAH according to the applied daylight.

2.3.2. Effect of Temperature of the Etchant

The temperature of the TMAH directly affects the etch rate of the silicon surface. Figure 2.5 shows this effect for every concentration value. As the temperature of the etchant increases, the etch rate curve rises too [11]. The increased etch rate provides large silicon atom removal at a short time which is essential for the device fabrication. On the other hand, high temperature also increases the etch rate of SiO_2.

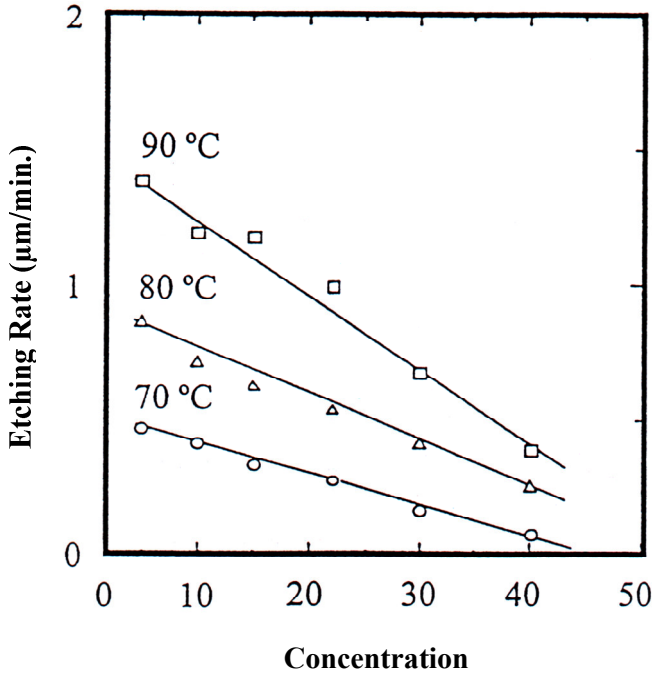


Figure 2.5: Temperature dependency of the etch rate of TMAH on (100) oriented wafers [11].

A series of experiments were carried out in the framework of this thesis in order to see the difference of the etch rates according to temperature variation. The concentration of the TMAH solution was kept constant at 25wt.% TMAH. Four dummy silicon samples were prepared for experiments. P-type (100) oriented, silicon nitride coated samples, which have 1.5mm X 1.5mm square openings, were placed on small lamella pieces with white epoxy. The white epoxy was cured at 120°C for 1 hour on the hotplate.

Then, these samples were cleaned inside the TCE, acetone and IPA solutions, respectively. Later, the native oxide over the etch opening was removed with a 5wt.% HF solution. The etching process was started after 15 minutes from the etchant reached to the necessary temperature in order to prevent any variation on the

temperature. The temperature of the solution was set to 55°C, 65°C, 75°C and 85°C, respectively. Each experiment took 20 minutes. Table 2.3 gives the results, where the increase in the etch rate is remarkable. According to these results the following optimization experiments were decided to be carried at 85°C.

Table 2.3: Etch rates of a 25wt.% TMAH solution of p-type (100) oriented silicon sample according to different temperatures.

Temperature	**Etch rates**
55°C	0.15 µm/min
65°C	0.37 µm/min.
75°C	0.62 µm/min.
85°C	0.75 µm/min.

The temperature of the etchant can be increased by using a pressure controlled set-up so a higher silicon etch rate can be satisfied

2.3.3. Effect of concentration of the TMAH solution

The TMAH concentration and etch rate of the silicon are inversely proportional until a certain concentration. As the concentration of the solution increases, the etch rate of silicon decreases drastically due to the reduction of the water amount [11, 30, 33]. Figure 2.5 shows that this reduction is consistent and does not change due to temperature variations.

Figure 2.6 gives etch rates measured from the recent studies. It is obvious that, however, at smaller concentrations than 5wt.% TMAH, the etch rate shows a drop,

instead of a rise. This is the outcome of the pyramidal structures, which are called hillocks that occur on the etched surface during the etching process [11]. Because of these hillocks, the etched surface becomes extremely rough. The size of the hillocks, even, may prevent obtaining the designed process parameters.

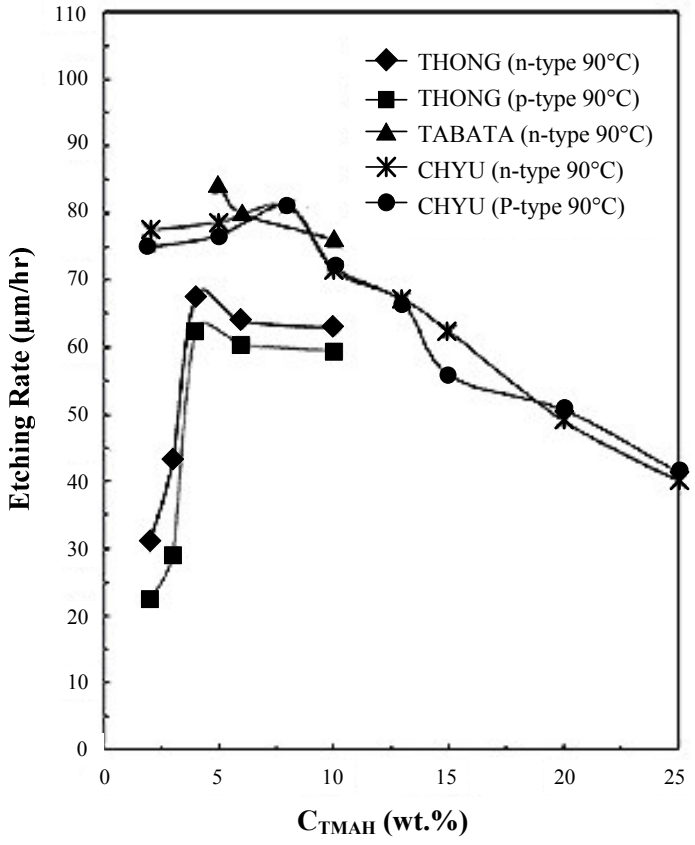


Figure 2.6: P-type silicon etch rates according to different TMAH concentrations in various works [33]. The figure also shows the results obtained by Thong et. al, Tabata et. al and Chyu et. al.

2.3.3.1. Surface Roughness

As previously explained, H_2 is a product of the etching reaction. This product is formed on the surface of the silicon. After formation of these H_2 bubbles, they must be immediately removed from the surface. Unless they are removed by mechanical agitation or by the help of a surfactant, they serve as a mask where they are attached to, as the etching reaction continues. Therefore, a pyramidal shape occurs due to the low etch rates of certain plains in the crystallographic structure. Figure 2.7 shows the behavior of H_2 bubbles during etching process.

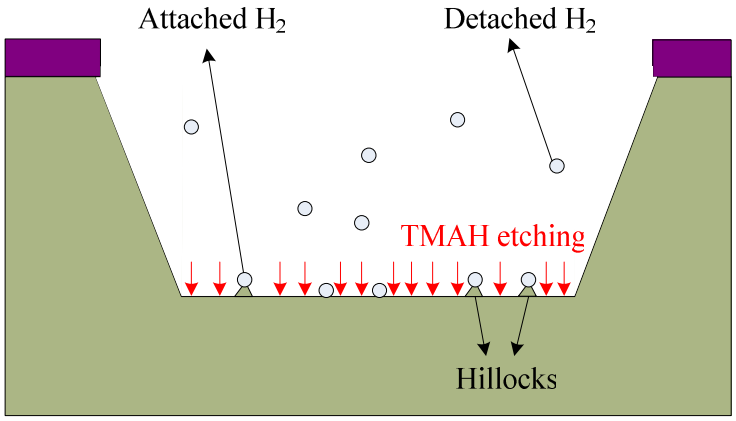


Figure 2.7 : Behavior of the etching product,H_2, bubbles during etching process.

However, at high concentrations of TMAH, the hillocks formation is nearly negligible, whereas at low concentrations hillocks height increases rapidly. The measured height of hillocks, occurred during 25wt.% TMAH etching, is 100nm [34]. On the other hand the height of hillocks increases to 5µm during 10wt.% TMAH etching process. Figure 2.8 shows the SEM picture of the etched (100) silicon surface by 10wt.% TMAH at 85°C for 20 minutes obtained in this study.

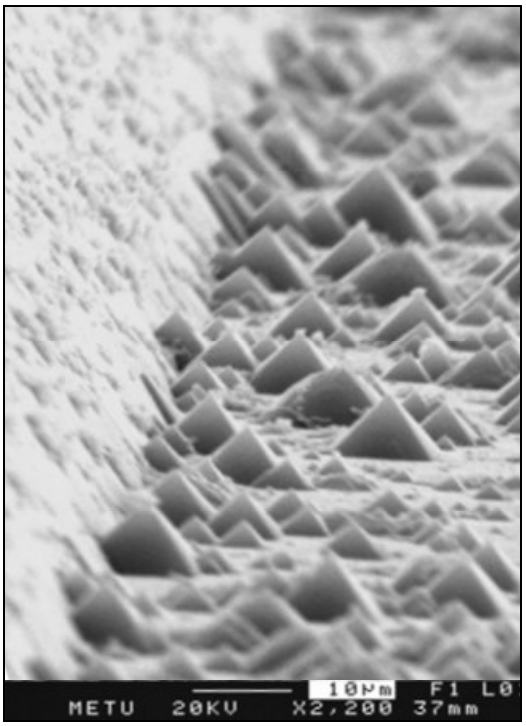


Figure 2.8: SEM picture of (100) oriented silicon surface after etching process with 10wt.% TMAH for 20 minutes, obtained in this study.

Hillock formation can be avoided by decreasing the amount of hillocks using proper surfactants or by ultrasonic agitation. The ultrasonic agitation technique can be applied to all types of anisotropic solutions. Applying ultrasonic waves to the solution enhances the detachment of both silicon atoms and H_2 bubbles from surface. Thus, the process increases the etch rate, and prevents the hillocks formation [35]. This can be a solution to surface roughness problem, but it can not be used in many device fabrications. For example, the vibrations caused by the ultrasonic agitation may destroy thin membranes. Adding oxidizers, such as ammonium peroxodisulfate ($(NH_4)_2S_2O_8$), AP) to the TMAH solution during etching process is a better solution for this problem [36]. It is claimed that, hillocks can be prevented by increasing the

(111)/(100) etch rate ratio [37]. Ammonium peroxodisulfate (AP) increases the detachment of H_2 from surface; hence, it acts a supporting role for the etching reactions. Therefore, it increases the etch rate of the solution.

Table 2.4 shows the etch rates of p-type silicon in 10wt.% TMAH solution adding different amounts of AP. However, it does not have an effect on the OCP and PP values. The drawback of this oxidizer is its low life time in anisotropic solutions. The oxidizer should be renewed at least every hour during the anisotropic etching [38, 39].

Table 2.4: 10wt.% TMAH etch rate of p-type (100) oriented silicon according to various AP amounts added to the solution.

AP amount	**Etch rate of 10wt% TMAH**
5 gr/lt. AP	1.0 µm/min.
10 gr/lt. AP	1.2 µm/min.
1.5 gr/lt. AP	1.35 µm/min.

The experiments showed that 10 gr/lt. of AP enhanced the etching rate, and decreased the hillocks formation. Figure 2.9 illustrates the enhancement on the surface roughness when 10 gr/lt. of AP was added to the 10wt.% TMAH solution. When AP amount increased further, AP did not dissolve in the solution fast, causing a white cloudy residue in the solution that could damage the samples by sticking on them.

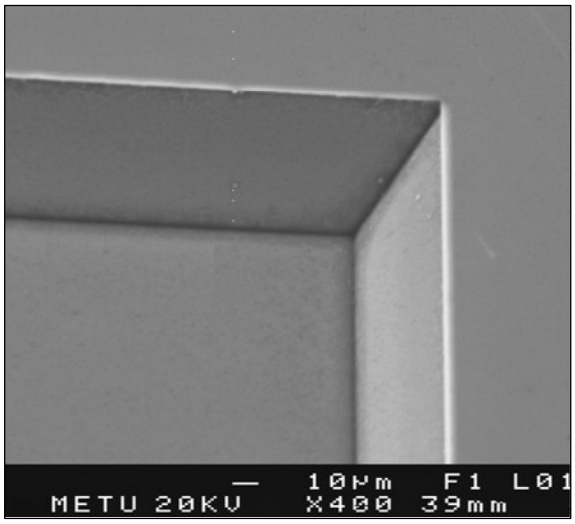


Figure 2.9: SEM picture of p-type (100) oriented silicon sample after the etching process with 10wt.% TMAH, added 1gr of AP, for 20 minutes.

2.3.3.2. Optimization of the TMAH concentration

A series of experiments were done with 5wt.%, 10wt.%, and 15wt.% TMAH concentrations in order to determine the concentration of the TMAH solution which has a high silicon etch rate and low surface roughness. Each concentration was optimized with the necessary AP amount. The highest etch rate at which a stable etching process can be done is preferred.

As the experiments for 25wt.% TMAH were done previously, the silicon etch rate for 25wt.% TMAH was significantly low. On the other hand, the silicon surface was smooth. The experiments continued with decreasing the concentration of the TMAH solution to 15wt.%. The surface roughness increased in this concentration, so the AP amount was first optimized for 15wt.% TMAH. A 5gr/lt. AP was determined to be used. Figure 2.10 shows the I-V curve of 15wt.% TMAH for both n-type and p-type

silicon samples. Table 2.5 gives the necessary voltage values for the n-type and p-type silicon etched in a 15wt.% TMAH. It is obvious that, the etch rate of silicon of 15wt.% TMAH is higher than the etch rate obtained previously from 25wt.% TMAH solution, as expected.

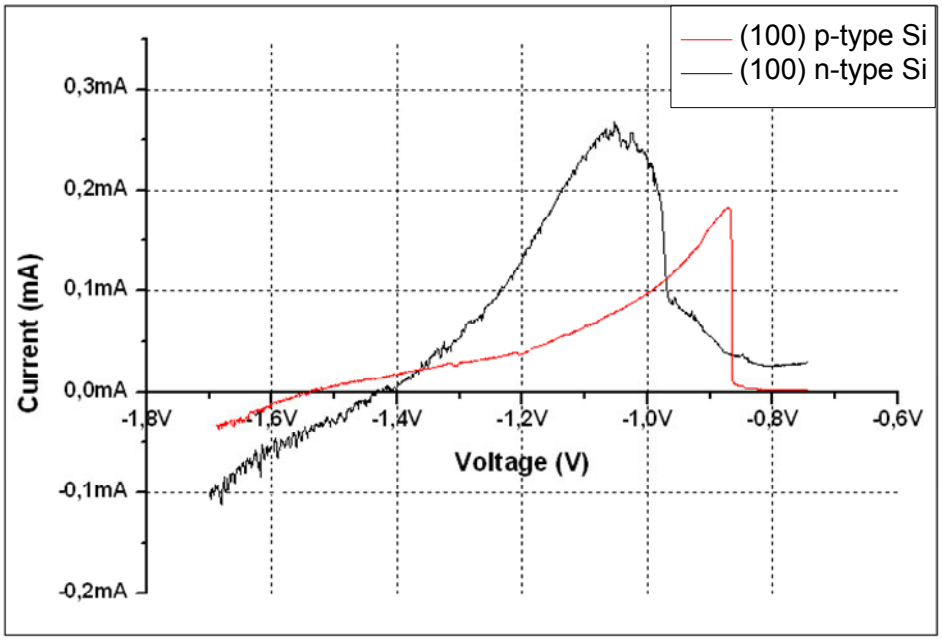


Figure 2.10 : I-V curve of p-type and n-type silicon samples in 15wt.% TMAH at 85°C. A 0.5gr AP was used for 100ml solution during the process.

Table 2.5: OCP and PP values for p-type and n-type silicon samples etched in 15wt.% TMAH at 85°C.

15wt.% TMAH at 85°C	**n-type silicon**	**p-type silicon**
Open Circuit Potential	-1.44V	-1.53V
Passivation Potential	-0.97V	-0.86V
Flade Potential	-0.8V	-0.82V
Etch Rate	0.88µm/min.	0.85 µm/min.

Figure 2.10 also shows the dependency of the I-V curve to the doping type of the silicon, where it is seen that the OCP and PP values differ. This difference can be explained by different Fermi levels of the n-type silicon and p-type silicon. Since OCP and PP depend on the difference of the Fermi levels of silicon substrate and the solution, the OCP and PP values of n-type silicon and p-type silicon may not be the same [28]. This effect is also seen on the different etch rates of n-type and p-type silicon samples. Moreover, the OCP and PP values of the etchant are extremely dependent to the doping concentration of the dopant. The OCP and PP values for a one type of silicon are not constant. Therefore, the determination of the OCP and PP values for the ECES implementation of a device must be done according to the doping concentration of the silicon used in that device. Otherwise, passivation of the silicon surface may fail. The optimization of the etchant must be done according to the same doping type and the same doping concentration of the device that would be fabricated.

The outcome of etching was successful with the 15wt.% TMAH. On the other hand, increasing the etch rate was still possible considering a further decrease on the concentration of the solution, therefore, the experiments continued with 10wt.% TMAH and 5wt.% TMAH solutions. Figure 2.11 shows the I-V curve of p-type and n-type silicon samples in 10wt.% TMAH at 85°C. 1gr AP was used for 100ml solution during the process. Table 2.6 gives the PP and OCP voltage values. The AP amount was optimized to 10gr/lt. It is important to mention that, the AP amount differs for each TMAH concentration. AP must be optimized for every concentration to obtain long term stability of the etching process.

The etch rate of 10wt.% TMAH against silicon was remarkably higher than the previous TMAH concentrations. Also, the stability of the etchant behavior against hillocks formation was satisfied by optimizing it with AP at an amount of 10gr/lt. However, it might still be possible to reach a higher etch rate with a smooth surface profile. Therefore, experiments continued with a 5wt.% TMAH concentration.

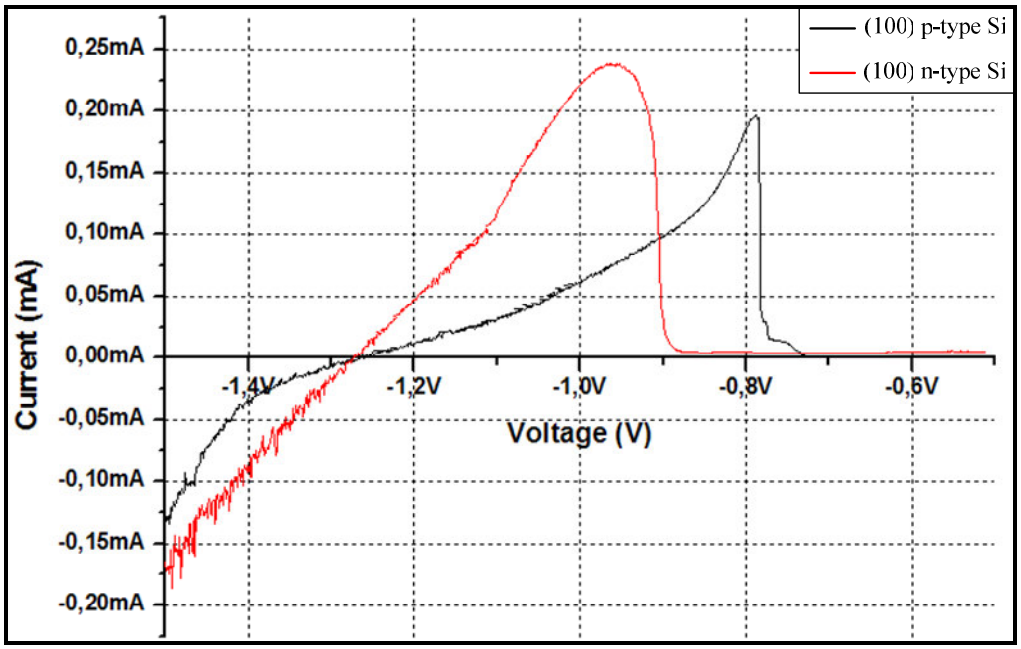


Figure 2.11: I-V curve of p-type and n-type silicon samples in 10wt% TMAH at 85°C. 1gr AP was used for 100ml solution during the process.

Table 2.6: OCP and PP values for p-type and n-type silicon samples etched in a 10wt% TMAH at 85°C.

10wt% TMAH at 85°C	n-type silicon	p-type silicon
Open Circuit Potential	--1.27V	-1.26V
Passivation Potential	-0.95V	-0.78V
Flade Potential	-0.89V	-0.72V
Etch Rate	1.23 µm/min.	1.2 µm/min.

Figure 2.12 and Table 2.7 give details about etching with 5wt.% TMAH solution. The etch rate is very high comparing with other concentrations of TMAH. On the other hand, the added AP amount increased too. But, unfortunately, the necessary stability of the process could not be achieved. The AP amount was not always satisfying the expected results. Furthermore, the etch time to obtain smooth surfaces at once time AP addition, varied, even, it could not pass over 20 minutes.

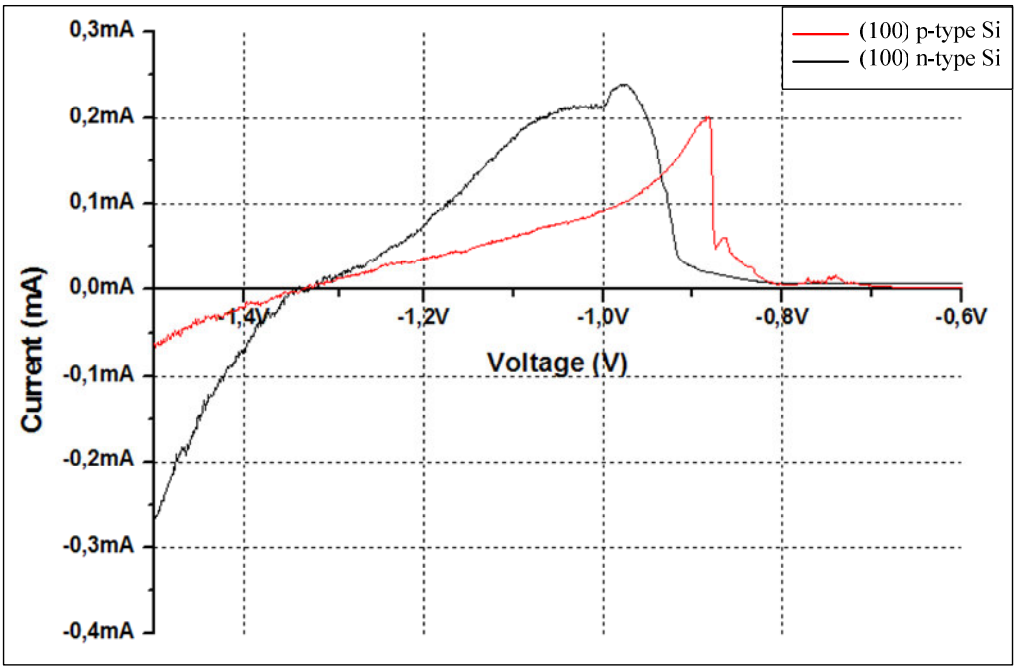


Figure 2.12: I-V curve of p-type and n-type silicon samples in 5wt% TMAH at 85°C. 1.3gr AP was used for 100ml solution during the process.

Table 2.7: OCP and PP values for p-type and n-type silicon samples etched in 5wt% TMAH at 85°C.

5wt% TMAH at 85°C	n-type silicon	p-type silicon
Open Circuit Potential	-1.34V	-1.34V
Passivation Potential	-0.95V	-0.87V
Flade Potential	-0.82	-0.8V
Etch Rate	1.43 µm/min.	1.37 µm/min.

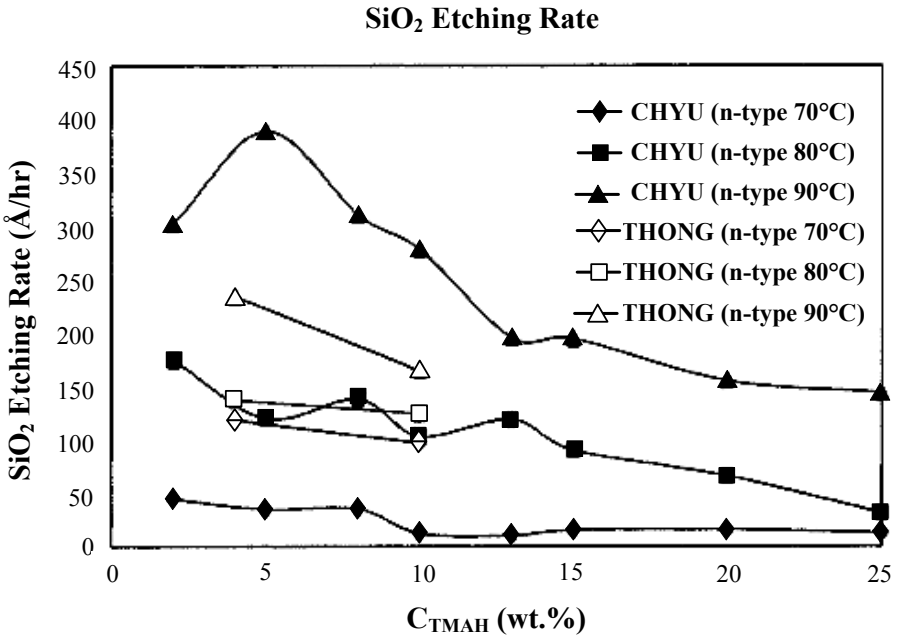


Figure 2.13 : SiO_2 etch rate versus TMAH concentration [33].

Another important point is the SiO_2 etch rate of the TMAH solution, especially when TMAH is used for front etching of CMOS processes wafers and dies. Figure 2.13

shows the SiO_2 etch rate of varying TMAH concentrations [33]. It is important to mention that, the highest etch rate of SiO_2 is obtained in etching with 5wt.% TMAH. As the concentration decreases, the etch rate curve also decreases slightly, and comes at a saturated point after 20wt.% TMAH [27]. Under these circumstances, using 10wt.% TMAH with 10g/lt. AP was decided to be used on device fabrications at METU.

2.3.4. Protection of the Aluminum layer from TMAH

TMAH attacks aluminum layers with a high etch rate due to its high pH value. However, the high pH value of TMAH can be lowered by dissolving silicon in the TMAH solution. According to previous studies, 3.2wt.% Si is needed to be used in 10wt.% TMAH [30, 37, 40].

Obtaining a silicon doped TMAH solution is a long and demanding procedure. Silicon pieces are kept in TMAH solution until they are dissolved completely. Both silicon wafer pieces and silicon powder can be used. However, if silicon powder is dissolved in the solution, the solution may foam and even may overflow of the beaker due to the high expose rate of silicon powder and TMAH solution. Therefore, a carefull handling is necessary considering that the process is an exothermic process.

The aluminum passivation was satisfied with the addition of 3.2wt.% Si but this procedure is not a solution for a long term anisotropic etching process. In order not to endanger the sample, all aluminum layers were sealed with Hysol 1C, white epoxy, before the etching process.

2.4. Electrochemical Etch-Stop Technique

The electrochemical etch-stop technique can be used properly after the optimization of the TMAH solution and the determination of the passivation potentials and the open circuit potentials for both n-type and p-type silicon. This study showed that an optimized TMAH solution could be achieved with 10wt.%.TMAH for the anisotropic wet etching processes. The etchant was heated to 85°C. 10gr/lt. AP was added to the TMAH solution in order to prevent hillocks formation. Also, stirrer was working during the etching process to help the H_2 bubbles detaching from the silicon surface. There was no daylight. The n-well area can be protected from etching reactions, and the substrate can be etched without a problem with an appropriate setup. For this purpose, both 3-electrode and 4-electrode ECES systems can be used.

The 3-electrode ECES system ensures to keep the n-well layer at a constant, well defined potential by applying this potential directly to the n-well area by an electrical contact. Figure 2.14 shows the 3-electrode ECES system configuration. However, the substrate potential is left floating at around OCP in the solution. The substrate will definitely be etched at OCP, nevertheless, leakage currents from p/n junction diode may produce voltage fluctuations in the p-substrate. These voltage fluctuations may even cause the substrate to passivate [41].

Another electrical connection to the substrate is added to overcome these problems. Figure 2.15 shows the 4-electrode ECES system configuration. The substrate potential can also be controlled by applying an anodic bias which ensures the substrate will stay at more cathodic voltage of passivation potential. This enables a control on the p-substrate and guaranties the etching reaction continuity. In this method, a working electrode is directly connected to the p-substrate. Biasing the n-well area is done by applying a forward-bias voltage between the n-well and p-substrate.

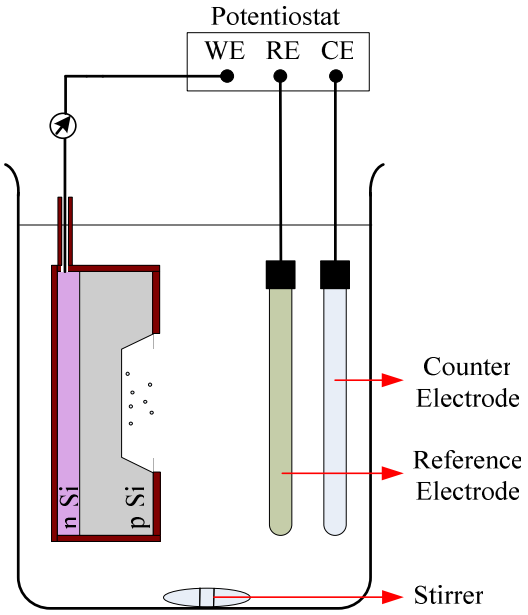


Figure 2.14: 3-electrode electrochemical etch-stop system configuration.

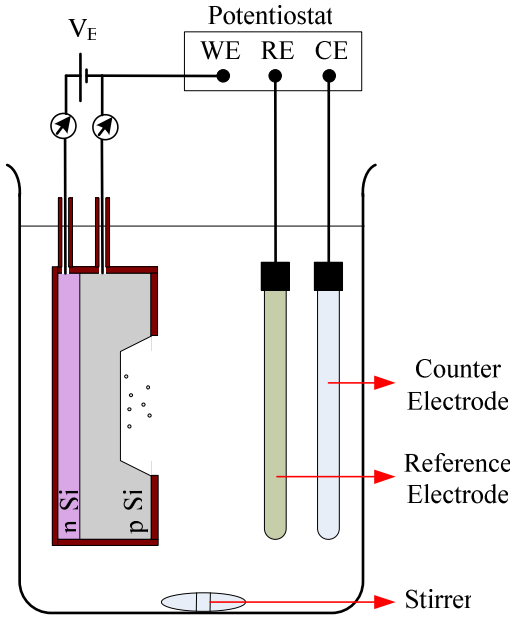


Figure 2.15: 4-electrode electrochemical etch-stop system configuration.

The 4-electrode ECES system configuration is chosen for providing high control on the biasing voltages and preventing leakage currents in this study. The n-well area of the device will be protected by biasing it with a sufficiently larger potential than the passivation potential of the n-type silicon in a 10wt.% TMAH solution. That is, the n-well area voltage is -0.5V, and the p-substrate is biased at -1.6V.

2.5. Conclusion

This chapter explained the theory of anodic oxidation, which is the rising point of the electrochemical etch-stop technique. The chemical reactions that took place on the surface of the silicon during the etching process were the reduction of the water molecules and then, the oxidation of the surface. The most important factor that keeps the etching process continuing was defined as the OH^- ions. These ions are not from the high pH valued solution, rather they are from the reduction reaction of the water molecules. Preventing this reduction reaction stopped removal of silicon atoms from surface, causing to form SiO_2 on the silicon surface. This prevention could be done by applying the passivation potential to the silicon.

Numerous experiments were performed in order to characterize the TMAH solution and to determine the passivation potential and open circuit potential. Experiments showed that the OCP and PP values depend on the difference of the Fermi levels of silicon substrate and the solution. That is the doping concentration and the dopant type changes the OCP and PP value. The effects of the concentration of the etchant are studied with the results obtained from the I-V curve experiments. The generation of hillocks at low concentration values was prevented with adding ammonium persulfate, AP, to the etchant. A high silicon etch rate was satisfied with a high TMAH temperature and a low TMAH concentration. Figure 2.16 demostrates the

variation on the silicon etching rate of the TMAH solution with respect to the varying the concentration.

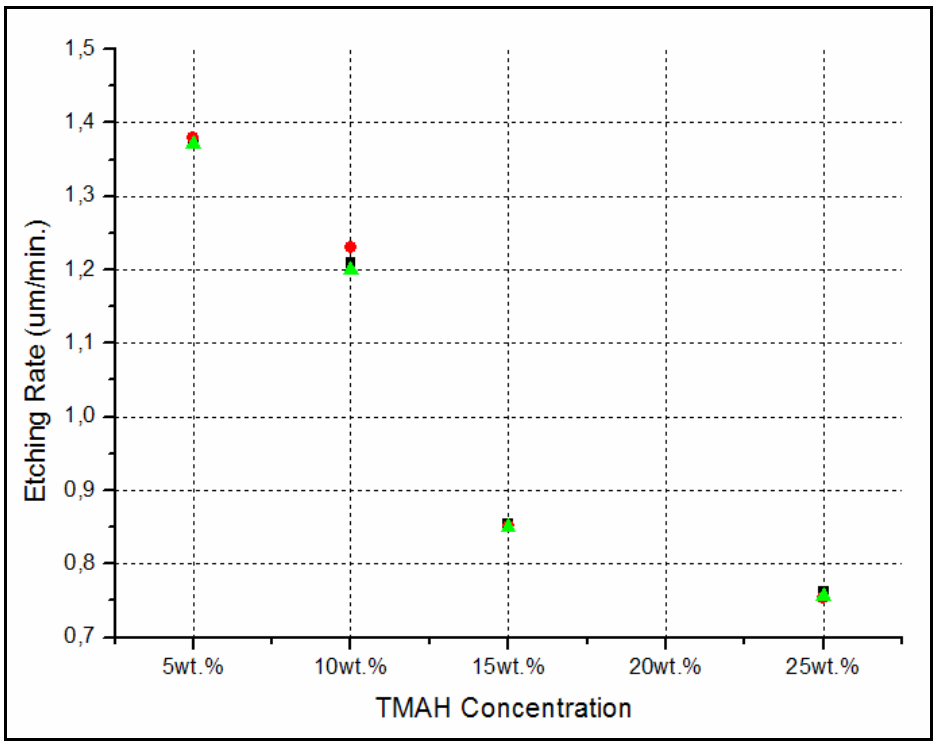


Figure 2.16: P-type silicon etch rates according to different TMAH concentrations obtained in this study. The experiments are repeated three times for the concentrations of interest.

A procedure for preventing the aluminum etching of TMAH was suggested but, since the procedure is not stable for all aluminum lines on the silicon substrate, the aluminum passivation was done by covering the lines with white epoxy. This chapter concluded with the explanation of the ECES system configurations. The best configuration was choosen as the 4-electrode ECES system configuration. Table 2.8 gives the optimized procedure used with the 4-electrode ECES sytem configuration.

The next chapter will present the design and fabrication of etch samples that can be used for optimization of post-etching of CMOS microbolometers. Before applying to the microbolometer chips, the effects of ECES implementation and consequences of the anisotropic etching will be investigated with these etch samples.

Table 2.8: Optimization results of the TMAH solution.

Property	**Value**
Concentration	10wt.% TMAH
Etching Temperature	85°C
Illumination	No
AP amount	10gr/lt.
Silicon doping	No
p-substrate etch voltage	-1.6V with respect to the etchant
n-well etch-stop voltage	-0.5V with respect to the etchant
Stirrer Rotation	200 rpm

CHAPTER 3

DESIGN AND FABRICATION OF ETCH SAMPLES

This chapter presents the design and fabrication of etch samples that can be used for the optimization of post-CMOS etching of CMOS microbolometers using electrochemical etch-stop (ECES) technique. Besides the effects of anisotropic etchant parameters, the structural design may also affect the etching reactions. Therefore, various etch samples are designed for the study of the ECES technique.

The etch samples are designed and fabricated in wafer-level with 5 photolithography masks. The fabrication processes for these etch samples are completely done in the METU-MET facilities. This chapter briefly describes the design and fabrication of these etch samples. The chapter is organized as follows: Section 3.1 gives the design considerations of these etch samples. Section 3.2 explains the measurement technique of diffusion parameters used in the optimization processes of phosphorus diffusion and boron diffusion and each fabrication step of these etch samples. Finally, Section 3.3 presented a conclusion for the fabrication of the etch samples.

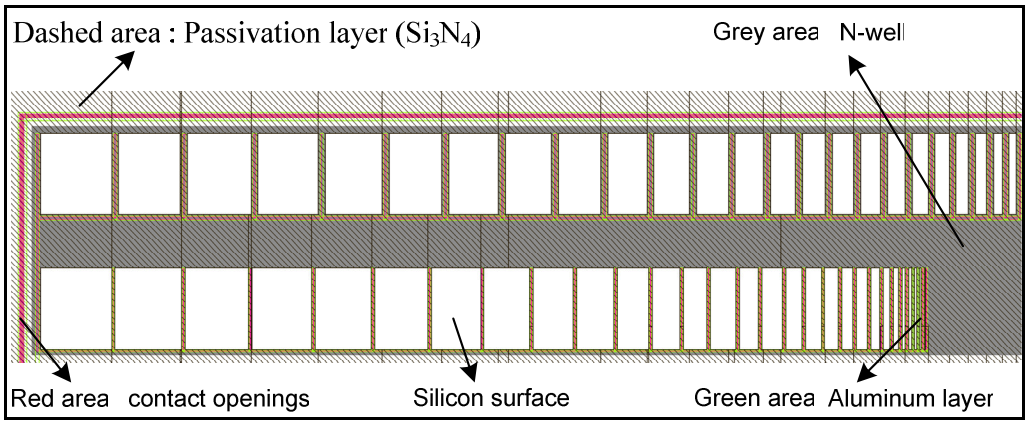
3.1. Design Considerations

Since the structures are used for obrimizing the etching process for microbolometers which were designed in AMS 0.8µm standard CMOS process, the designed structures were also designed considering the AMS 0.8µm standard CMOS process in CADENCE. 5 photolithography masks were drawn for the fabrication of 4 inch silicon wafers. Table 3.1 gives the descriptions of masks of the etch samples.

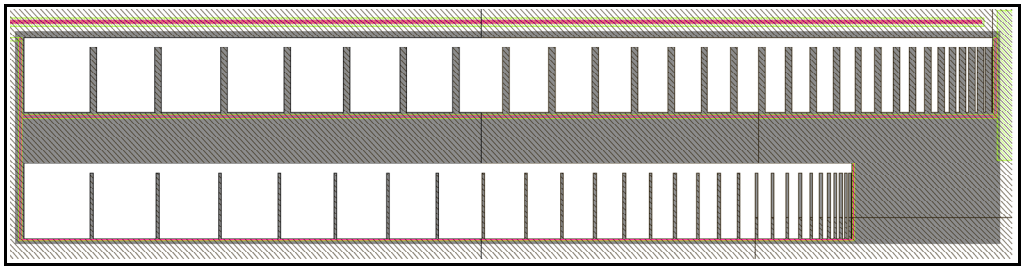
Table 3.1: Mask set for the etch samples.

MASK NO:	MASK DESCRIPTION
1	N-well diffused areas, dark-field mask
2	P^{++} diffused areas, dark-field mask
3	Contact openings, dark-field mask
4	Metallization lines, clear-field mask
5	Passivation layer, clear-field mask

A depletion region occurs at the metallurjical junctions of p/n doped areas after biasing the n-well and the p-substrate regions with the proper voltages. The n-well mask is drawn like comb and bridge structure on one of the dies to investigate the effect of this depletion region on the etching reactions. Figure 3.1a and Figure 3.1b show both comb like and bridge structures on this die designed for investigating the effect of depletion region formed between p/n junction to the etching reactions. While n-well area on comb and bridge like structures are being biased with the etch-stop voltage, the behaviour of p-substrate against the etchant can be examined. The distance between each bridge and comb varied between 2µm to 200µm. within each other.



(a)



(b)

Figure 3.1: Etch sample for investigating the effect of depletion region between p/n junction to the etching reactions. N-well diffusion is done like: (a) a bridge structure and (b) a comb structure.

The bolometer pixel structures, which were previously designed in METU MEMS VLSI group, were also included in this layout with many other pixel designs [24]. Since these processes were carried out in METU-MET facilities these pixel structures were designed with only 1 metallization layer. The reason is in this facility 2 metallization layer processes could not be achieved so far. That is why there is only n-well deposition on the absorber area and only 1 support arm of the absorber layer carries a metallization layer. By eliminating the p^{++} diffusion and metallization layers on the absorber area, 6 different pixel designs, with single and their array structures were added to study the influence of the electrochemical etch-

stop technique on array structures. Figure 3.2 illustrates one of these designed pixels, which is used as a reference pixel in order to see the consequences of anisotropic etching process. Reference pixels are used to prevent the effect of self-heating of the circuit and the effect of the temperature of the environment to the measurement of the infrared light.

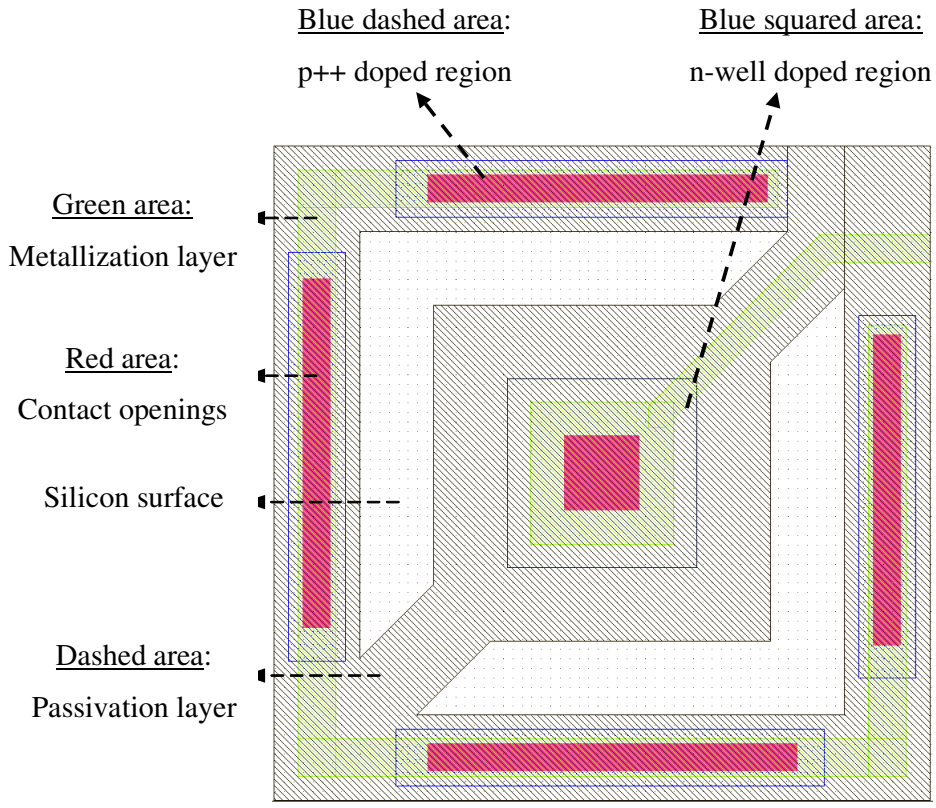


Figure 3.2: A reference pixel structure fabricated in order to see the consequences of anisotropic etching process.

As the previous chapter explains, the diffusion concentration affects the open circuit potential (OCP) and the passivation potential (PP) values. Since the optimized TMAH will be applied to the post-CMOS process of the microbolometers, the phosphorus and boron diffusion parameters of the etch samples that will be used for

the optimization of post-CMOS process of microbolometers should be fabricated according to the AMS 0.8 µm standard CMOS process parameters [42]. By this way, the consequences of the etching process and the ECES implementation on the microbolometers can be seen clearly, and the design of the pixels can be arranged according to these results of experiments with the etch samples. Table 3.2 gives the AMS 0.8 µm standard CMOS process parameters for phosphorus and boron diffusion process.

Table 3.2: AMS 0.8 µm standard CMOS process parameter [42].

	Minimum value	**Typical value**	**Maximum value**
n-well Junction Depth	-	3.5 µm	-
p^+ Junction Depth	-	0.4 µm	-
n-well Resistance	1.0k OHM/□	1.2k OHM/□	1.4k OHM/□
p^+ Resistance	25 OHM/□	40 OHM/□	60 OHM/□

Three structures were included for measuring the resistivity by the Van der Pauw technique to control the diffusion parameters of phosphorus and boron elements [43]. A rectangular structure, a cloverleaf like structure and a cross like structure were used in these measurements. Figure 3.3 illustrates these Van der Pauw resistivity measurement structures.

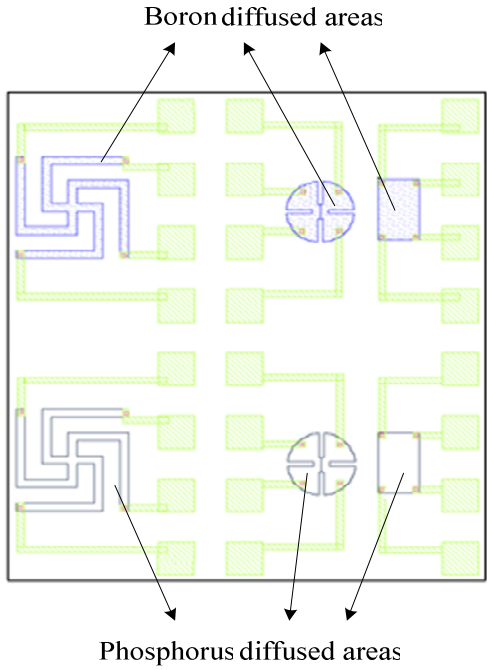


Figure 3.3: The Van der Pauw resistivity measurement structures.

3.2. Fabrication of the Etch Samples

As previously explained, five photolithograghy masks are needed for the fabrication of the etch samples. These masks are used during lithography steps of thermal oxidation, boron diffusion, phosphorus diffusion, aluminum, and silicon nitride layers. Section 3.2.1 explains measurement techniques of the diffusion parameters. Section 3.2.2 describes the process flow of the etch samples. Then, Section 3.3.2 presents the fabrication process in detail.

3.2.1. Measurement Techniques of Diffusion Parameters

The main parameters in a diffusion process are the resistivity of the diffused surface and the junction depth of the diffused layer. The Van der Pauw resistivity measurement structures can give the resistivity value at the end of the fabrication by biasing the structures from the metal pads, but the lack of phosphorus diffusion process optimization at needed resistivity value leads us a series of phosphorus diffusion test processes. Section 3.2.2 and Section 3.2.3 explain the measurement techniques of these parameters.

3.2.2. Four-Point Probe Technique

In four-point probe technique, 4 probes are landed on the sample as shown on Figure 3.4. A constant DC current, I (mA), is passed through the outer probes and voltage, V (mV), is measured between the inner probes.

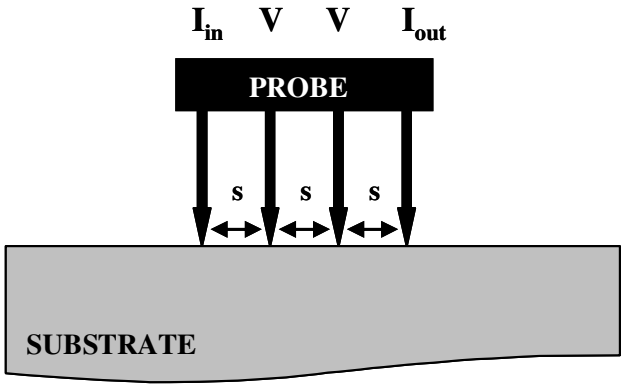


Figure 3.4: Structural view of the four-point probe technique used in the measurement of the phosphorus and boron doped wafers for the optimization of the diffusion processes.

The reliability of the measurements depends on the probe pressure, the current levels passing through the probes, and the shape of the measured sample [44, 45]. The probe pressure must be appropriate, not to deform the surface and exceed the junction depth but, only convenient to take connection from the surface of the deposited film. The sheet resistance, R_S is given as:

$$R_S = CF \ (V / I) \qquad 3.1$$

where, CF is the correction factor, I is the applied current and V is the measured voltage. The current levels should be arranged according to the expected resistivity. The shape of the surface affects the correction factor, CF, which the instrument automaticaly multiplies the calculated resistance value coming from the applied current and the measured voltage. If the sample has a circular shape, the correction factor depends on ratio of the diameter of the sample, d, to the probe spacing, s. If the sample is a rectangular sample, both parallel side to the probe line, d, and perpendicular side to the probe line, a, effects the correction factor. The dependency of the correction factor to the sample size and the position of the probe on the sample are needed to be decreased to a minimum size for a reliable measurement. Therefore, a high d/s value is needed to make the effect of this factor insignificant. Table 3.3 gives the correction factor list. This table is valid when only front side of the sample was deposited or the deposited back side is somehow removed or isolated from the front side. Otherwise, the correction factors will change.

Table 3.3: Correction factors used in sheet resistance measurements with the four-point probe technique [44]

	Circle	**Square**	**Rectangle**		
d/s		a/d**=1**	a/d**=2**	a/d**=3**	a/d**>=4**
1	-	-	-	0.9988	0.9994
1.25	-	-	-	1.2467	1.2248
1.5	-	-	1.4788	1.4893	1.4893
1.75	-	-	1.7196	1.7238	1.7238
2	-	-	1.9475	1.9475	1.9475
2.5	-	-	2.3532	2.3541	2.3541
3	2.2662	2.4575	2.7	2.7005	2.7005
4	2.9289	3.1127	3.2246	3.2248	3.2248
5	3.3625	3.5098	3.5749	3.575	3.575
7.5	3.9273	4.0095	4.0361	4.0362	4.0362
10	4.1716	4.2209	4.2357	4.2357	4.2357
15	4.3646	4.3882	4.3947	4.3947	4.3947
20	4.4364	4.4516	4.4553	4.4553	4.4553
40	4.5076	4.512	4.5129	4.5129	4.5129
Infinite	4.5324	4.5324	4.5325	4.5325	4.5325

3.2.3. Chemical Staining and Grooving

The junction depth of a diffusion layer can be measured from a groove made by a mechanical grinding process, which is proceeded in METU-MET facilities with the PHILTEC 2015 sectioner. The PHILTEC 2015 sectioner opens grooves whose depth can be controlled [44, 46]. From this groove a copper solution is pored for

staining the phosphorus doped area. The copper particles in the solution attract to the phosphorus diffused areas by highly illuminating it for 1 minute which causes the doped area to become darker. So, the junction depth's color changes by these cupper particles. Another approach is to use HF to stain the boron diffused areas. Figure 3.5 shows the cross-section of a groove which is used in junction depth measurements. To have a groove like this, the PHILTEC 2015 sectioner uses a tool having a radius of 19.050 µm, R. In addition to this, the PHILTEC 2015 sectioner defines a constant for the calculation of depth of the stained area which is 9.924, defined in the following equation [47].

$$x_j = \sqrt{(19.050\mu m)^2 - \left(\frac{W_2(\mu m)}{2} - 9.924\right)^2} - \sqrt{(19{,}050\mu m)^2 - \left(\frac{W_1(\mu m)}{2} - 9{,}924\right)^2} \qquad 3.2$$

where, W_1 and W_2 are defined as in Figure 3.5.

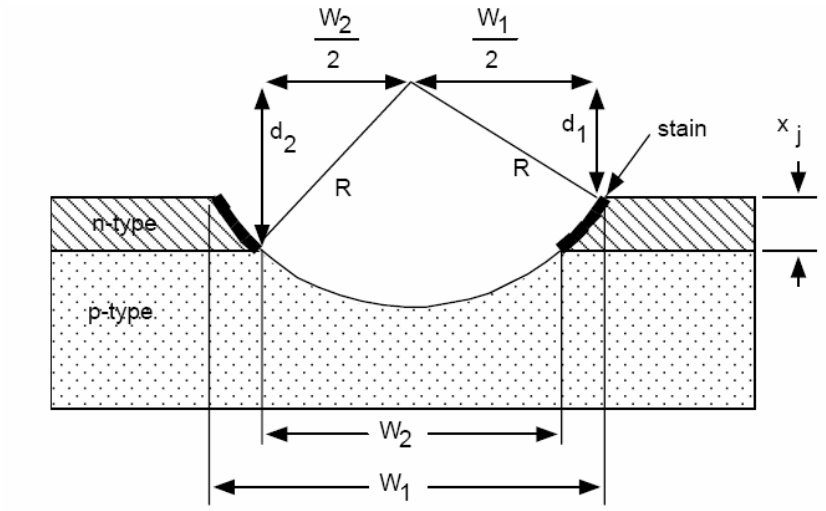


Figure 3.5: The cross-section of a groove which is used in junction depth measurements [47].

3.2.4. Process Flow of the Etch Samples

Figure 3.6 illustrates the process flow of the fabrication of the etch sample. The process is done with the p-type (100) oriented silicon wafers. First, the SiO_2 is grown with the thermal oxidation process (Figure 3.6b). Then, the oxide layer is etched according to the n-well diffusion mask (Figure 3.6c). Later, the phosphorus diffusion is done for generating the n-well areas (Figure 3.6d). The SiO_2 layer grown by the phosphorus process is etched for the boron diffusion process (Figure 3.6e). Next, boron diffusion is done to the silicon wafers (Figure 3.6f). The boron diffusion process also forms an oxide layer. The oxide layer formed during boron diffusion step is etched according to the mask of the contact openings where aluminum lines get contact to the silicon substrate (Figure 3.6g). The metallization of the etch samples are done by depositing aluminum (Figure 3.6h). The aluminum layer is etched according to the metallization mask (Figure 3.6i). After that, Si_3N_4 layer is deposited to the wafers in order to be used as the passivation layer against the TMAH (Figure 3.6j). Finally, reactive ion etching (RIE) process is done to reach the silicon layer for the anisotropic etching process. Both SiO_2 and Si_3N_4 layers are etched with RIE for obtaining the etch openings (Figure 3.6k).

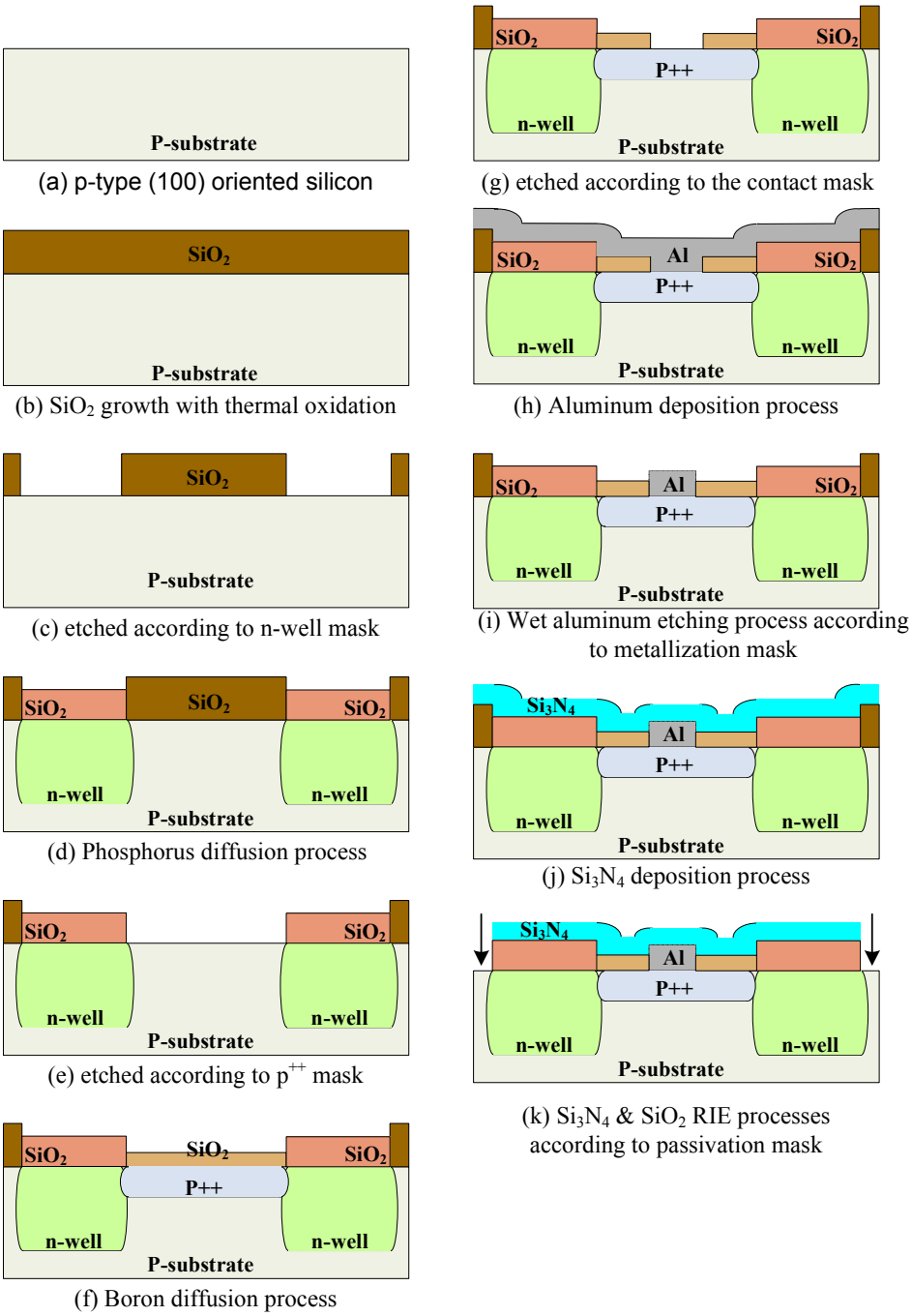


Figure 3.6: The process flow of the etch samples

APPENDIX A shows the whole process steps for the fabrication of the etch samples. The fabrication process starts with the cleaning of the process wafers. The wafers were 4 inch, p-type, (100) oriented wafers having a resistivity interval of 5-10Ω. Before involving them to the clean-room processes, wafers were cleaned with the piranha solution, as described below.

The piranha solution is used for removing organic residues from the wafer surface [48]. A standard piranha recipe was used in METU-MET clean-room which is 1:1 mixture of 49wt.% concentrated sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). As the hydrogen peroxide is added, the reaction starts immediately. It is an extremely exothermic reaction that rises the temperature of the mixture to 120ºC. Wafers were put in the piranha solution for 5 minutes. Then, the wafers were prepared for the first process of this study, which is the thermal oxidation process, by the RCA cleaning procedure.

3.2.5. RCA Cleaning

High temperature processes need extra attention and procedures for cleaning. Preventing the contamination of process equipment, especially the high temperature oxidation, diffusion, and deposition tubes is as important as the removal of the contaminants on the surface of silicon wafers in order to obtain highly reliable semiconductor devices. For this purpose, before the thermal oxidation process, the RCA cleaning is done to the wafers. The RCA cleaning is a standard procedure for removing contaminants from wafers [49]. Werner Kern developed this recipe in 1965 while working for RCA (Radio Corporation of America).
The RCA cleaning has 3 steps:

1. RCA-1 cleaning is used to remove organic residues from silicon wafers. In the process, it oxidizes the silicon and leaves a thin oxide on the surface of the wafer that must be removed. There is the pure silicon layer under this thin oxide. Following recipe is proceeded.

   H_2O_2 : NH_4OH : DI-H_2O = 1.5 : 1 : 6 at 70°C; for 7 minutes.

2. RCA-2 cleaning is used to remove ionic and heavy metal atomic contaminants. Following recipe is proceeded.

   H_2O_2: HCL: DI-H_2O = 1.5: 1: 6 at 70°C; for 7 minutes.

3. RCA-3 cleaning is used to remove the thin silicon dioxide layer which is a result of RCA-1. Metallic contaminants are cleaned with this removal process. Following recipe is proceeded.

   HF: DI-H_2O = 1: 10; for 20 seconds.

3.2.6. Thermal Processes

The fabrication of the etch samples continues with a series of thermal processes. These processes determine the field oxide layer, the n-well diffused and p^{++} diffused areas, and the dielectric layer between metallization lines and the silicon area. Since each thermal process after one affects the previous process parameters, each thermal process should be arranged carefully considering the temperatures which are above 500ºC. An oxidation process after a diffusion process changes parameters like the junction depth and resistivity, because the applied heat at a significant time increases the potential energy of the ions diffused in silicon and causes them to penetrate

deeper in silicon substrate, as a consequence, increases the junction depth and resistivity of the diffused area. Therefore, the whole thermal processes were simulated in a process simulator program, SUPREM, and the effects of each thermal process were observed, before the actual process started.

SUPREM is a process simulator which is developed for submicron silicon structures. It gives information about structures after ion implantation, diffusion, oxidation, and annealing processes on its cross sectional view. In this program many variables that play important role in thermal processes may be arranged according to the desired results. Depending to the outcomes of each step, optimizations of the resistivity and junction depth values can be analyzed more precisely. APPENDIX B gives the SUPREM script which is the outcome of the simulated thermal processes done for this study.

3.2.6.1. Thermal Oxidation: Field Oxide Growth

The fabrication of the etch samples involves 5 high thermal processes that are at temperatures above 500°C. The oxidation process for the growth of the field-oxide is the first step of this study. Cyclic oxidation was done at 1125ºC in three stage furnaces. The desired oxide thickness was 7000-8000 Å. This thickness can be obtained by wet oxidation process which has high oxide growth rate. The beginning of the thermal oxidation was done with the dry oxidation process in order to increase the quality of the Si-SiO_2 interface property. Ten p-type, (100) oriented wafers were placed on the quartz elephant. Each wafer's major wafer flats were looking to the top, so the gas flow through the wafers would not be interrupted, and the uniformity of the oxide over the wafers would not be affected. Figure 3.7 shows the placement of the wafers in the quartz elephant. Oxygen was sent to the oven for 30 minutes. After the dry oxidation step, a thick oxide growth was done with a wet oxidation technique, which is also called Pyrogenic wet oxidation. It was performed by

burning O_2 and H_2 at the input to the tube and given inside from the source. A 120 minutes of pyrogenic oxidation resulted in a 7000 Å thick oxide layer. This result is consistent with Figure 3.8, which shows the oxide thickness variation due to temperature and diffusion time [50].

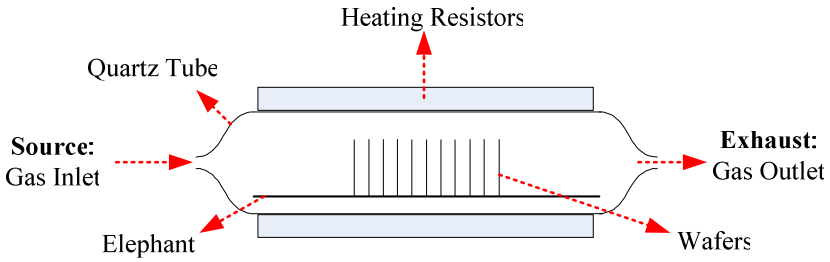
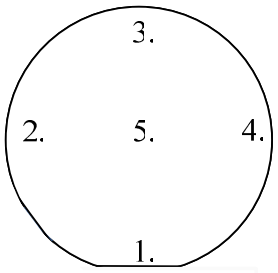


Figure 3.7: Thermal oxidation furnaces used for growing silicon oxide layer thermally.

To complete the cyclic oxidation, few tens of angstroms of the oxide layer were grown with the dry oxidation that gives a better quality oxide layer. The measured total SiO_2 thickness of the wafers was approximately 7100 Å. The measurements were done with the NANOTEK measurement device. Table 3.4 shows the oxide thickness measurement results at the five points on a wafer, which were taken from the source end and the exhaust end. H_2 and O_2 were burned in front of source and the vapor was sent from source end to the tube. The wafers at the source end may obviously have a greater thickness of oxide than others. Given measurements confirm this suggestion. The oxide thickness may vary approximately 300 Å among source and exhaust placed wafers, but the thickness uniformity on one wafer is very good.

Table 3.4: The oxide thickness measurement results at the five point on a wafer, which were taken from the source end and the exhaust end.



Source wafer	Exhaust wafer
1. 7395 Å	1. 6899 Å
2. 7063 Å	2. 6901 Å
3. 7050 Å	3. 6931 Å
4. 7086 Å	4. 6901 Å
5. 7105 Å	5. 6878 Å

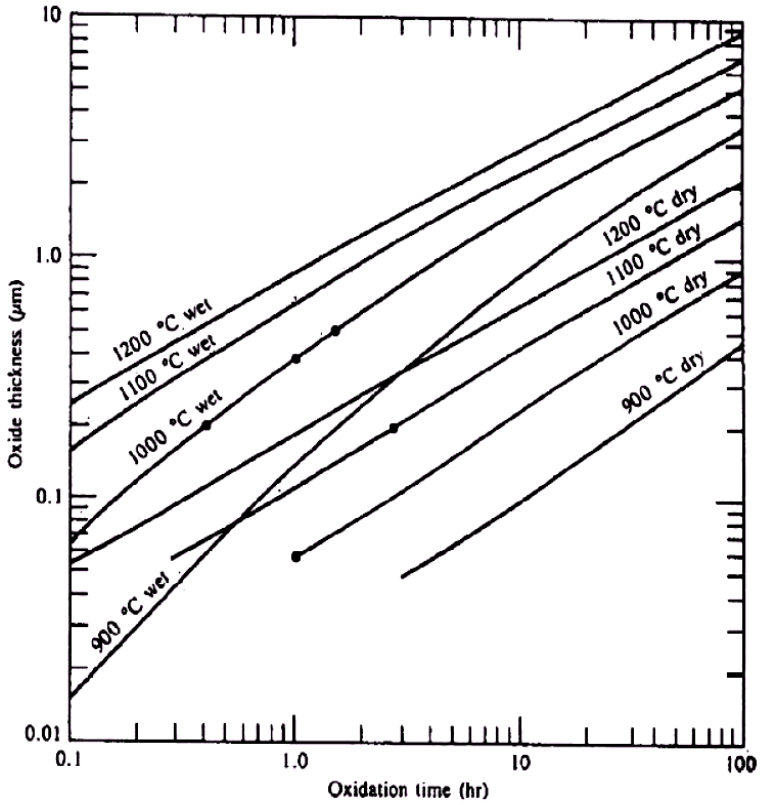


Figure 3.8: Wet and dry silicon dioxide growth curves with respect to time and temperature for (100) oriented silicon [50].

This grown oxide layer was used as the field oxide and also as a masking layer for the phosphorus diffusion process. Photolithography was done to the wafers with the n-well mask in order to etch the oxide layer to obtain n-well diffusion openings. Also, the backside oxide layer of the wafer was protected with the S1813 photoresist. After hard-bake process of the photoresist, the unprotected oxide layer was etched with a wet oxide etchant, i.e., the buffered HF (BHF) solution. The recipe for BHF can be given as NH_4F : HF = 7 : 1.

3.2.6.2. Phosphorus Diffusion Process: Pre-deposition and Drive-in

The first diffusion process in our process is the phosphorus diffusion process to form the n-well layer. The n-well layer should have a resistivity of 1.2kΩ/□ and a junction depth of 3.5µm. The optimization to achieve these values will be done considering the forthcoming thermal processes, namely n-well pre-deposition and drive-in processes. The phosphorus diffusion is done with a gas source, $POCL_3$. The gas is given to the quartz tubes from the source side and absorbed from the exhaust side. During optimization of the resistivity and junction depth of the dopant, the gas flow in the tube was kept constant, whereas the diffusion time, the drive-in process time, and the temperatures were optimized. At first, three inch wafers were used in the diffusion pocesses. After the pre-deposition of the three inch wafers, the measurements of the four-point probe technique showed that the size of the wafers did matter for the diffusion process, as it affects the flow of the gas through the five inch tubes causing non-uniformity on the wafer surface. Optimization studies continued with four inch wafers, which gave more uniform and precise results for my process.

The sheet resistance was arranged approximately 1000Ω/□, as this value would increase in further thermal oxidation steps, approaching to the target value of 1200Ω/□. Three optimization processes were done to satisfy this value. According

to the SUPREM simulations and the four-point probe measurements, the final pre-deposition was done at 805ºC for 10 minutes. A high temperature drive-in process was needed to activate the diffused ions. This process brings an activated region of diffused n-wells, and also arranged the junction depth. A high junction depth requires a long and high temperature process. The drive-in process was done at 1130ºC by exposing the wafer surface to pyrogenic wet oxidation for 60 minutes. This causes a new, doped oxide layer over the diffused areas and a field oxide, which will be used as the diffusion mask of boron diffusion process. Table 3.5 gives the measured resistivity and junction depths after drive-in process. The measurement results show that the sheet resistance is 980Ω/□ and the junction depth is 2.4 µm, which are very close to the target values.

Figure 3.9 shows the groove opened for junction measurements. The copper solution was used for staining, and the stained area appeared after 1 minute of illumination. Measurements were done with the VEECO surface profiler and PHILTEC 2015 Sectioner. Both results confirmed each other. After phosphorus diffusion, wafers were prepared for boron diffusion. The oxide layer was opened according to the p^{++} diffusion mask in photolithography step.

Table 3.5: Resistivity and junction depth measurements of phosphorus diffused area

	Sheet Resistance	**Junction Depth**
Phosphorus Diffused Area	980Ω/□	2.4µm

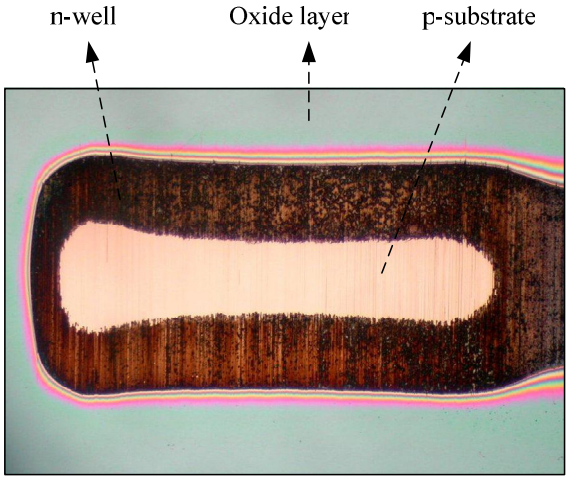


Figure 3.9: Chemical staining of phosphorus diffused sample for diffusion process optimizations.

3.2.6.3. Boron Diffusion Process: Pre-deposition and Drive-in

The boron diffusion was done with a liquid source using BBr_3. According to the simulations and previously settled processes in METU-MET facilities, the pre-deposition was done for 15 minutes at 1000ºC. Before the drive-in process, the boron silicate layer, which occurs after every boron deposition process, had to be removed from the surface. Otherwise, the silicate layer shows high resistivity to HF and could not be etched. For this purpose, a low temperature oxidation (LTO) was done to the wafers at 700ºC for 30 minutes. Then, the silicate layer was removed with the BHF solution.

For a low junction depth, the drive-in process needs to be short. Also, boron doped areas needs an oxide layer for metal isolation before the metallization process. This oxide layer should be no less than 1500 Å. Therefore, without making an extra oxidation step, only the drive-in process was done for both activating the diffused

ions and for oxide growth. The drive-in process was done at 1000ºC by exposing the wafer surface to pyrogenic wet oxidation for 25 minutes. Table 3.6 gives the final results of the thermal processes, whereas Figure 3.10 shows stained boron diffused area. After this step, any of the processes would not change the diffusion variables values.

The oxide thickness was measured as 2300 Å. Contact openings for metallization layer were exposed to photolithography with the third mask. The oxide layer was opened with Buffered HF solution.

Table 3.6: Sheet resistance and resistivity measurements of diffused areas.

	Sheet Resistance	**Junction Depth**
Phosphorus Diffused Area	1050 Ω/□	3.1 µm
Boron Diffused Area	75 Ω/□	0.7 µm

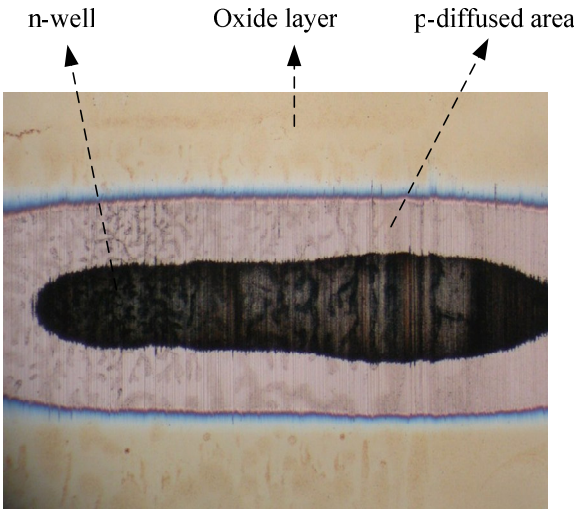


Figure 3.10: Chemical staining of boron diffused sample for diffusion process optimizations.

3.2.7. Metallization Process:

The metallization process of the etch samples is another challenging process. The hardest part is to obtain 1µm wide metallization lines. Those lines are necessary for implementing the etch stop voltage to the n-well regions in the absorber area of the bolometer pixels. Figure 3.11 shows one of the bolometer pixels. The black lines indicate the metal layer. The metal layer on the supporting arms, which is protected by the nitride layer indicated with blue mask, is 1µm. Every pixel structure has the same supporting arm thickness and metal layer thickness.

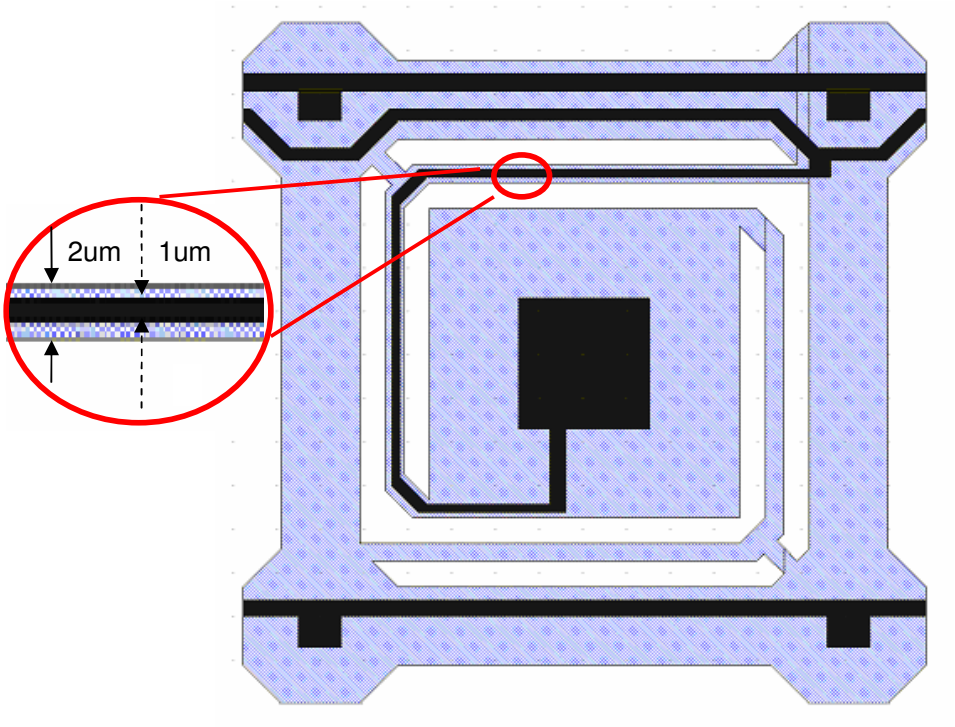


Figure 3.11: Passivation layer and metallization layer of the test bolometer pixel.

These lines had to survive from the metal wet etching process, which most of the metal etchant is highly isotropic etchant. The width of the lines was critical in the pixel design, since these lines were protected from etchant by Si_3N_4, nitride layer which was designed as 2µm, limiting the size of the metal width. Also, the width of the metal layer could not be decreased too much, considering the current which will pass over them, and considering the high undercut rate of the metal layer. Therefore, the mask of the metal layer was drawn as 1µm.

The most important requirements in contact metallization are stability of the metal throughout processing, reliability of the metal layer during utilization of the device, obtaining good ohmic contact, low resistivity, ease of process, and excellent adherence of the metal to the silicon. Considering these requirements, aluminum was chosen. But this choice leads us to a problem that occurs from the outcome of wet aluminum etching process, which is the high undercut rate of the aluminum etchant.

The metallization process, from the polarization of the metallization mask to the thickness of the aluminum layer, was needed to be optimized according to obtaining 1µm lines. Under these circumstances the mask of the metallization process was designed as clear field. A positive photoresist, S1813, was chosen among S1828, SPR220-3, MAN-1420, PI, and BCB. The reasons for this choice were the capability of achieving 1µm lines of S1813, the effective line width control during the processes over highly reflective substrates, decreased notching effect, perfect coating uniformity at 1.3µm thickness, and ease in stripping the resist with acetone and isopropyl alcohol. Hard-bake does not perturb the resist and shows excellent resistance to acidic solutions. Photolithography processes with S1813 were previously optimized.

A mistake was done in the mask order of the etch samples. The metallization mask came as dark field. The change in the polarity of the mask, forced us to change the

photoresist tone. Negative tone photoresist, MAN-1420 was used. Initially, an optimization process was needed to be done with MAN-1420 in order to obtain necessary feature size on aluminum coated wafers with a high yield. A number of optimization work are done including the thickness, the soft-bake time, the expose time, and the development time of the MAN-1420 and the thickness of the aluminum layer and aluminum wet etchant temperature, which are explained in the following subsections.

3.2.7.1. Optimization with Negative Photoresist, MAN-1420

This section will present the optimization work done for Negative Photoresist, MAN-1420, including its coating process, soft-bake time, expose time, development time, and hard-bake times.

Coating process of MAN-1420**:**

Figure 3.12 gives the spinning curve of MAN-1420 [51], provided by the manufacturer. Spinning the resist at 3000 rpm for 30 seconds gave us a uniform resist thickness of 2.1 µm. On further processes, it was understood that the resist thickness had to be thinned in order to get 1 µm, line width and to have 2µm, wide gaps between structures. The reason was that MAN-1420 did not have a perpendicular cross section view. There was a slight slope, whose size was extremely dependent to the expose time under the UV light of the mask aligner. The 2µm thick MAN-1420 also expanded and made obtaining thin and sharp features impossible. In order to be more precise with the expose time and to have neat structures, the spinning speed was increased to 7000 rpm. The acceleration time from the initial spin speed of 650 rpm to the coating spin speed of 7000 rpm was increased. This increase eased the propagation of the resist through the wafer. The thickness of MAN-1420 decreased to 1.6µm uniformly.

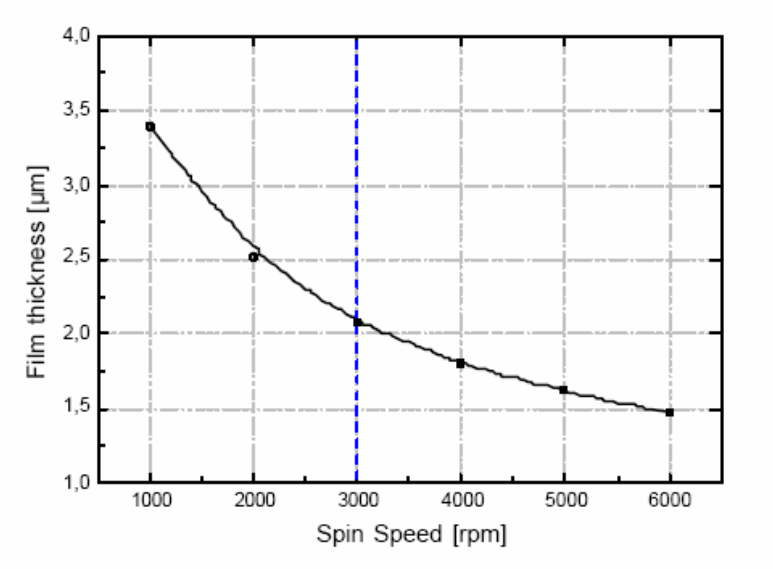


Figure 3.12: The spinning curve of MAN-1420 [51].

Soft-bake process of MAN-1420**:**

Soft-bake is done for vaporizing some of the solvent of the resist, so the resist hardens enough for UV-light exposure and for keeping the uniformity of the resist stable on the wafer surface. The soft-bake time and temperature were optimized in both oven and on hotplate surface. Curing on hotplate surface caused a non-uniform heating on the wafer surface, which was the reason for preferring the oven. The temperature and time was determined whether the resist stick to the mask surface during the vacuum contact, while exposing UV-light on mask aligner, or not. Determined soft-bake time was 60 minutes in 115ºC heated oven. This soft-bake time can be decreased to 5 minutes on the hotplate at 115ºC for wafers, where 5-10 mm of lost from the outer diameter of the wafer is tolerable.

Exposing of MAN-1420 with UV-light**:**

Since the tone of the photoresist was negative, the exposed part of the resist staid on wafer, whereas other parts were removed by the developer. If the expose time was too much, MAN-1420 became over-exposed and the resist topology started to expand laterally, which was illustrated on Figure 3.13. At a thickness of 1.6µm, the expose time was optimized to 15 seconds. At this rate, lines were slightly over-exposed, and 1µm lines were measured as 1.3µm. The intensity power of the EVG mask aligner was 18 mW/cm^2 during these exposure times.

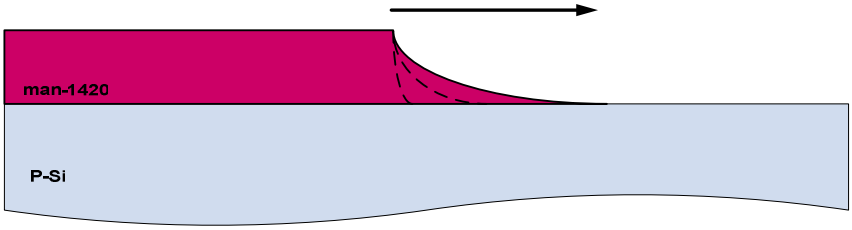


Figure 3.13: The lateral expansion of negative tone photoresist, MAN-1420. Expansion laterally increases as the expose time increases.

Developing the MAN-1420:

MAD-532S was used as the developer solution of MAN-1420 photoresist. The developer solution is a TMAH based solution. High pH value of 13.89 is not enough to prevent aluminum etch rate of the developer solution. As long as the developer was used, its pH value remained same, but solution got cloudy, as it is affected from aluminum particles. Developer of MAN-1420 was not compatible with processes done with the aluminum coated wafer. Therefore, the developer was renewed frequently. The process continued considering the aluminum layer will be slightly thinned in the developer.

Hard-bake process of the MAN-1420:

Before exposing the resist to aluminum etchant, wafers were put in oven at 120ºC for 1 hour. The hard-bake process was done for removing the solvents, completely. After the hard-bake process, the photoresist losted its tightened structure and melted down, so most structures were lost. MAN-1420 kept its resistivity against aluminum etchant without the hard-bake process. Therefore, hard-bake process was dismissed.

3.2.7.2. Aluminum Deposition and Wet Etching Optimizations

This section will present the work on Aluminum deposition and wet etching optimizations.

Aluminum Wet Etching Optimization**:**

These optimization processes were done on aluminum sputtered p-type silicon wafers. The aluminum etching process time needed to be decreased to obtain 1µm, wide aluminum line, because the Aluminum etchant did not have a good selectivity against lateral walls. Table 3.7 gives the etch rates of aluminum layers having different thicknesses. It etched isotropically which causes an undercut amount at high rates.

The Aluminum etching process was done at 25°C. At higher temperatures Aluminum etchant became more aggressive to the Aluminum layer, etching rate increased, thus undercut value of the etchant increased too. The etch rate falled drastically at lower temperatures. As the etch rate decreased, the effect of low selectivity of the etchant on the lateral walls appeared more obviously. Figure 3.14 shows the etch rates obtained in Aluminum etchant temperature optimization.

Among all, the most important issue, which affects the undercut rate and makes obtaining thin lines possible, was agitation. Etching the wafers with high agitation decreased the undercut amount. Eventually, the Aluminum etching was done with high agitation at 25ºC.

Table 3.7: Aluminum etch rates according to Aluminum thicknesses.

Aluminum Thickness	**Etching Time**	**Aluminum Etch Rate**
2800 Å Al layer	3 min 15 sec.	14,35 Å /sec.
3400 Å Al layer	3 min 46sec.	15.04 Å /sec.
5800 Å Al layer	6 min 21 sec.	15,22 Å /sec.

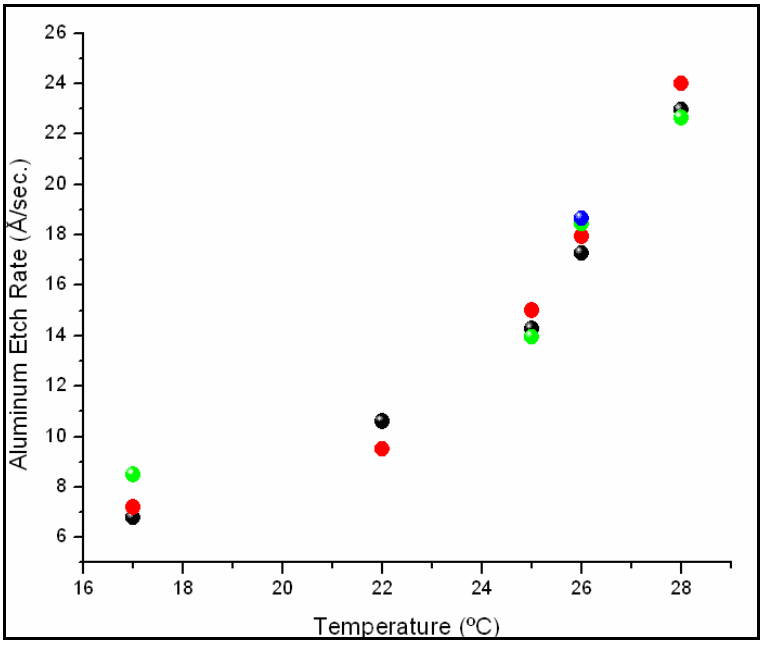


Figure 3.14: Aluminum etch rate versus Temperature.

Aluminum Deposition Process:

The aluminum layer is needed to be deposited as thin as possible to prevent the thin lines from an aggressive and high etch rate and to complete the etching process as soon as possible before the undercut increases. The deposited aluminum layer thickness was determined as 3000 Å. In METU-MET facilities, Aluminum can be deposited in two ways: (1) by resistive heating evaporation and (2) by sputtering.

The resistive heating evaporation is a method that heats the source material over its melting point, causing the material to evaporate. The method for heating the source is electrically, by applying large amounts of current over filaments. In the sputtering process, the atoms of the source material are removed by accelerated ions of Argon gas. By this way, the variety of the source material increases with respect to the resistive heating evaporation technique [52]. On the contrary, the evaporation system is a low cost system considering all its equipment and changes in source material. But, sputtering systems are preferred over evaporation systems, due to its advantages such as higher adhesion, better step coverage, and wider range of source materials [12].

The primary reason of preferring the sputtering system in METU-MET facilities is the behavior of the deposited aluminum layer against aluminum etchant during the aluminum wet etching process optimization. The etch rate of the layer and the undercut rate of the etchant increased dreadfully in aluminum coated wafers by evaporation process. The reason is the presence of little air bubbles and low density. These holes accelerate the etching process, causing uncontrolled high undercut rate. In sputtering technique, the density of the aluminum can be arranged according to the vacuum pressure. The etch time is high but undercut rate is more controllable. Increased etching time was compensated with decreased Aluminum layer thickness

and high agitation during etching process. The results were perfect. 1µm thickness of Aluminum lines was obtained on dummy wafers.

Unfortunately the optimized information about MAN-1420 did not work on the process wafers. The reason for that is the topology of the process wafers. Boron doping damaged the silicon surface. The roughness of the p^{++}-doped surface was noticed, when the aluminum layer, which was sputtered over the wafer, was etched with Aluminum etchant. The aluminum diffused the damaged surface and made it harder to be etched.

Figure 3.15 shows one of the 2 X 1 array structure of various pixel types. The pixels on the figure are same. On the left pixel, the boron doped layers are surrounded with red lines. The structure had 1µm wide aluminum lines. The aluminum etching time had to be arranged very precisely to be able to obtain 1µm wide line. When the thin lines were obtained, the overall etching of the wafer had to be ended. If etching continued, somehow, large undercut amounts occurred, and 1µm wide aluminum lines disappeared. Figure 3.15 was taken after etching the aluminum layer. Precise timing was satisfied, but this etching time was not enough for etching aluminum layer on the p^{++}-doped areas.

The negative resist MAN-1420 was over-exposed to obtain thicker lines in order to survive from long aluminum etching, as a solution to this problem. But this time, over exposed MAN-1420 kept the 1.8µm wide spaces between aluminum lines, which was indicated with a yellow circle in Figure 3.15, closed and undeveloped. Stripping the MAN-1420 was done with the oxygen plasma at 300W, 700mTorr. Each wafer was exposed to plasma for 45 minutes. However, exposing oxygen plasma for a long time deformed the aluminum surface and darkened its color.

A lot of problems had been encountered while processing with MAN-1420. Obtaining a reproducible aluminum etching process was very hard with this

photoresist. The insufficient minimum feature size of the MAN-1420 and the high undercut rate of aluminum etchant decreased the success of metallization process of this study. Therefore, the mask of the metallization process's polarity changed to clear-field and ordered again. The metallization processes restarted from the beginning.

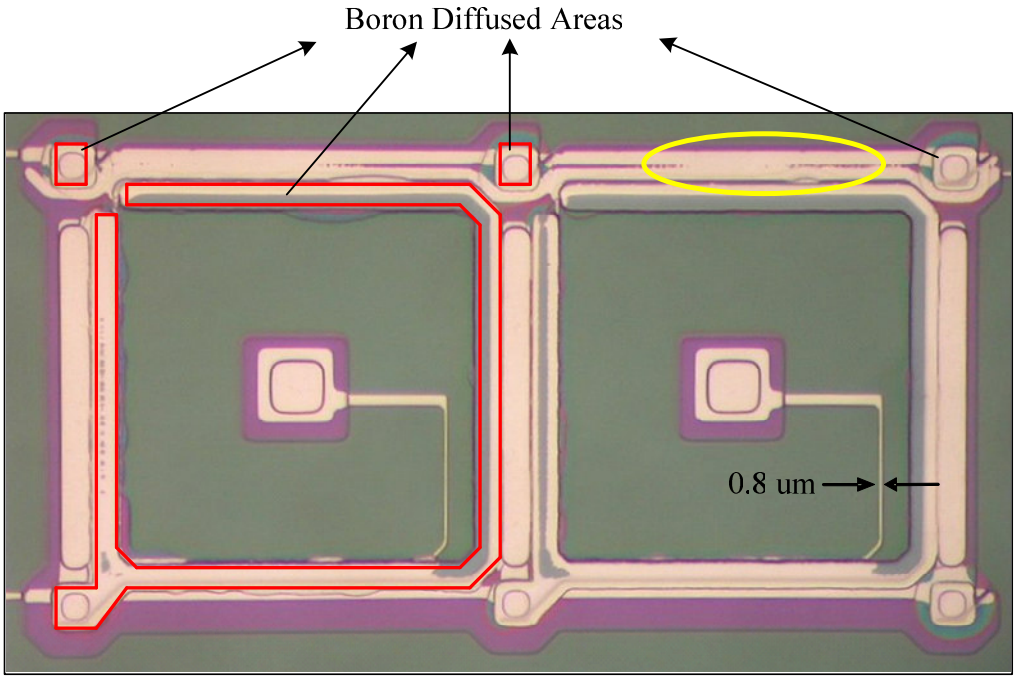


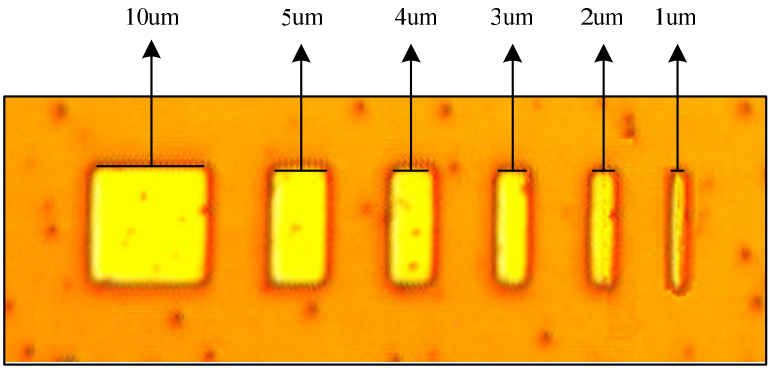
Figure 3.15: A 2 X 1 microbolometer array structure fabricated in this study, after the aluminum etching process. The photolithography was done with the negative photoresist, MAN-1420.

The native oxide layer on contact openings was cleaned by exposing the wafer into Buffered HF (BHF) solution for 10 seconds. The aluminum layer was deposited with the BESTEC Sputter device. Two pressure levels were used in the process. Arranging the argon amount, which was sent to the chamber, the sputtering process

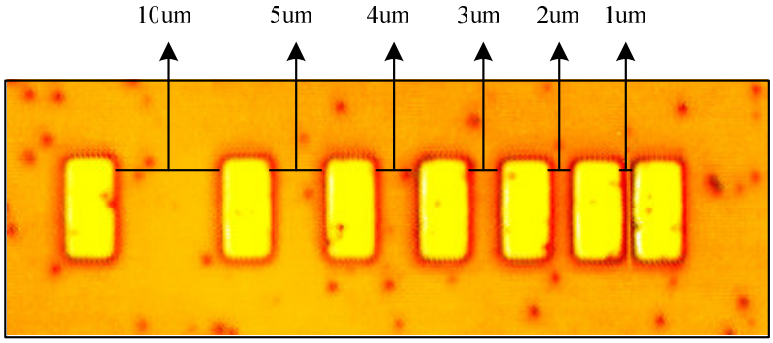
was done in $1.1x10^{-2}$ Torr for 200 seconds and $4.9x10^{-3}$ Torr for 400 seconds, giving an aluminum layer thickness of 3000 Å.

Since the mask of the metallization layer was a clear field mask, positive resist could be used this time. The positive resist which had the best resolution on minimum feature size of 1 µm was, S1813. So, S1813 was coated for the metallization photolithography. It was easy to obtain over-exposed, thicker S1813 lines with opened gaps at necessary places. Figure 3.16 illustrates aluminum lines, which have survived from the aluminum etching process. Aluminum lines on Figure 3.16(a) had varying thicknesses, from 1µm to 10 µm. On the other hand, Figure 3.16(b) shows the aluminum lines which had varying gaps between them from 1µm to 10µm. According to these pictures, the 1µm thick aluminum lines were successfully achieved. Also, it was possible to open a 1µm wide gap.

After the development of the resist, wafers were exposed to oxygen plasma before exposing the wafer to Al etchant. Here, the oxygen plasma was used to remove organic residues and contaminants that existed on some areas which might cause difficulty for the etchant to reach the surface. Thus, the plasma did some of the developer solution's job. Then, wafers were put in oven at 120°C for 30 minutes to increase the resistivity of the photoresist towards the Aluminum etchant. Eventually, the Aluminum etching process was done with high agitation at 25ºC for 3.5 minutes. The outcome is given on Figure 3.17, Figure 3.18, and Figure 3.19. These figures show that the etching optimizations are successful and the pixel structures in this study can be successfully obtained.



(a)



(b)

Figure 3.16: Aluminum lines, obtained after S1813 photolithography process and wet aluminum etching process.

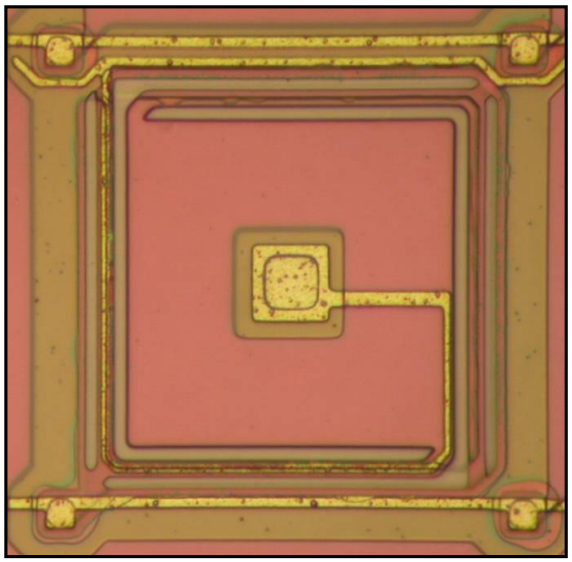


Figure 3.17: A pixel structure after Aluminum etching process. The photolithography was done with the positive photoresist, S1813.

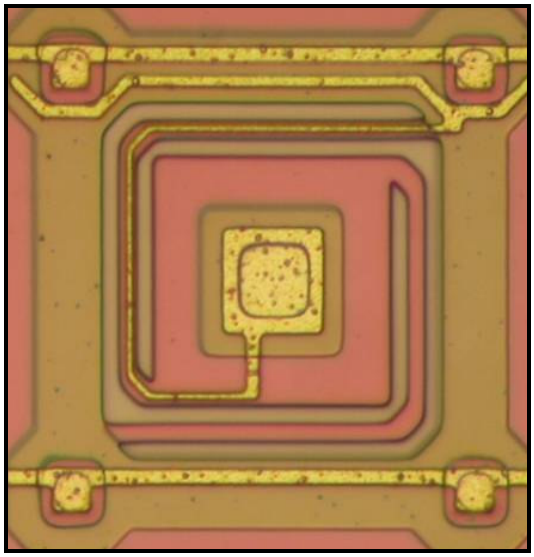


Figure 3.18: Another pixel structure after Aluminum etching process. The photolithography was done with the positive photoresist, S1813.

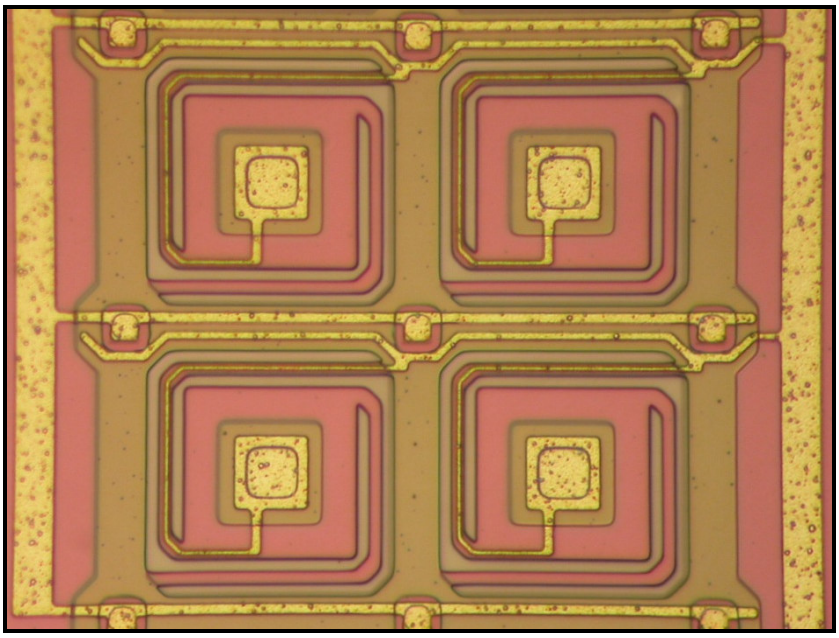


Figure 3.19: A 2 X 2 array structure fabricated in this study, after the Aluminum etching process. The photolithography was done with the positive photoresist, S1813.

Before this metallization process, many aluminum sputtering and aluminum etching processes were done over the same process wafers. Even, Au-Cr was deposited instead of aluminum, in order to escape from high undercut rate of aluminum. Before every metal deposition process, wafers were put in BHF solution in order to remove the thin native oxide; otherwise an ohmic contact to the layers could not be achieved. These etching processes caused the surface topology to chance. Especially the thickness of oxide around contact openings decreased.

The thickness of the oxide layer on the wafer showed variations according to its location on the wafer. The oxide thicknesses on the n-well deposited region, the p^{++}-deposited region, and the field oxide region were approximately 7000Å, 2000Å, and 9000Å, accordingly. The SiO_2 changed its color according to its thickness. As

the native oxide etching occurred on the wafer, some oxide layers especially corner and step oxide structures are etched too, causing different colors on the surface especially around the contact openings. The structure is explained on Figure 3.20 and Figure 3.21. Figure 3.22 shows the SEM pictures of the deformed oxide area. The topology occured a stair like structure of oxide layers. Etchant slowly etched these layers and caused the area to differ in color and in thickness.

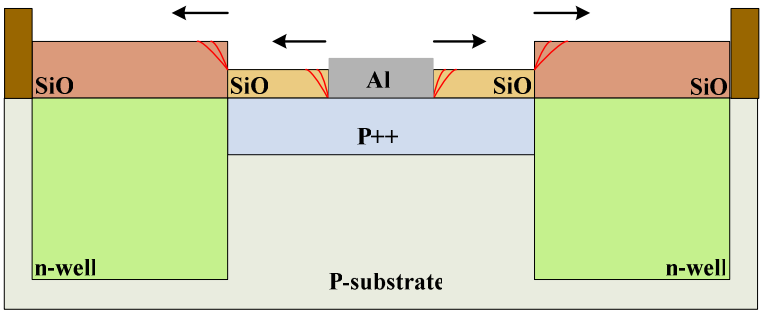
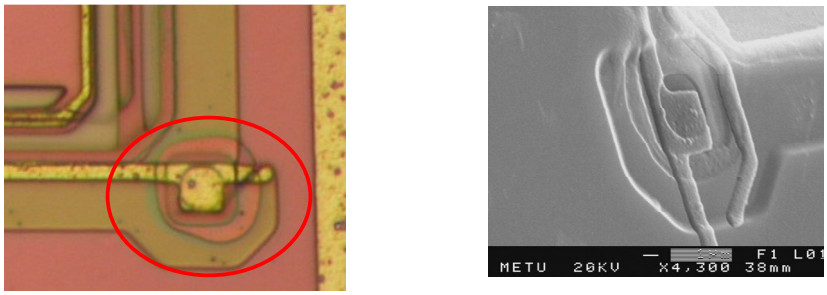


Figure 3.20: Consequences of oxide etching in BHF for native oxide removal.



(a) (b)

Figure 3.21: Oxide deformation around the contact openings: (a) the change of the colors due to the oxide layer deformation. (b) the SEM picture of the substrate contract of the pixels.

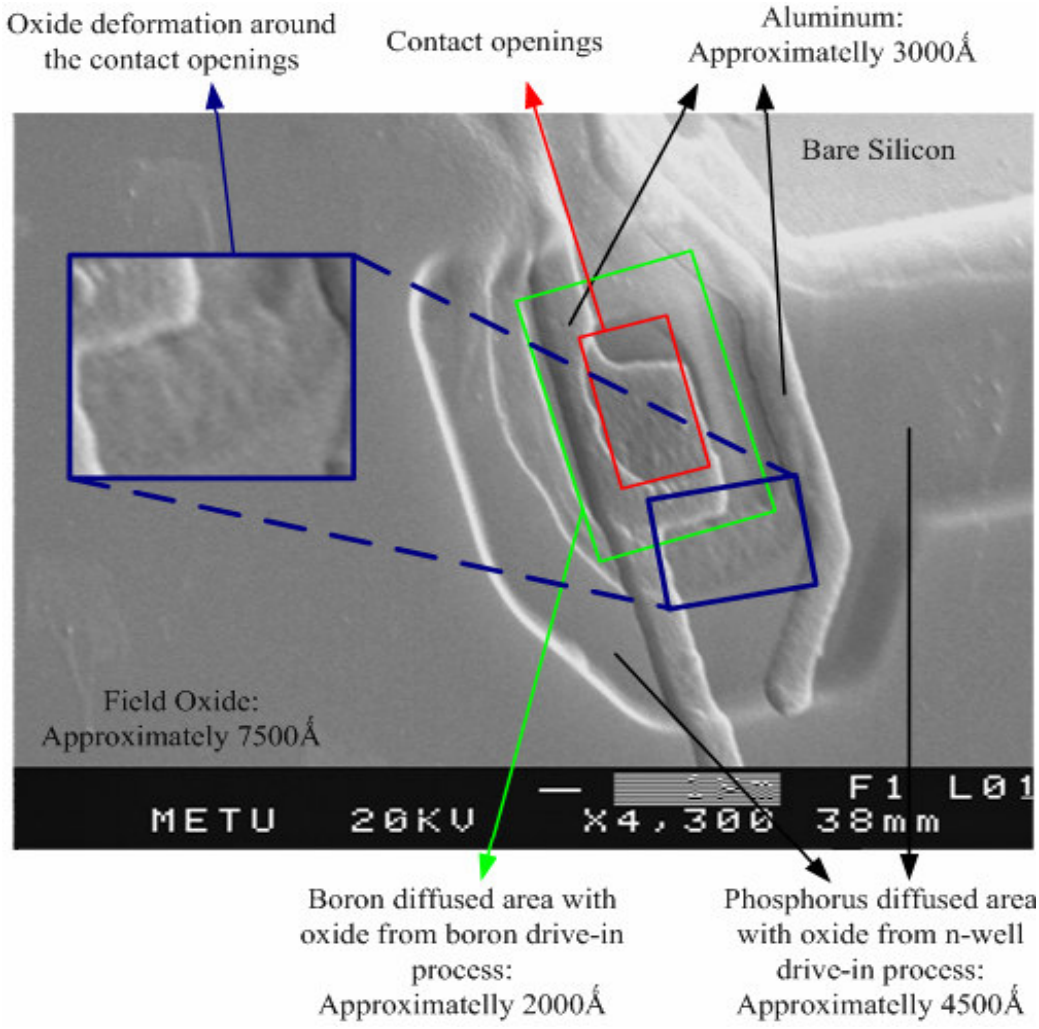


Figure 3.22: SEM pictures of the oxide deformation around the contact openings.

After the metallization process, annealing was done in furnaces. Aluminum annealing is necessary for decreasing the resistance value on contacts. The preciseness of the measured resistivity by the contacts depends on a good annealing. The process was done at 450 ºC for 30 minutes in oven.

3.2.8. Passivation Layer Deposition Process

A silicon nitride film was preferred as the passivation layer considering its low etch rate on TMAH. However, this layer had to be over metallization layer. Therefore, the temperature of the process must be low. For that reason, deposition was made by the pressure enhanced chemical vapor deposition (PECVD) system of Surface Technology Systems (STS), Inc. Main advantages of the PECVD among CVD processes are the lower substrate temperature, good adhesion, and good step coverage. These properties make PECVD suitable for depositing low temperature insulator regions over metals. The temperature of the substrate rises at most to 300-400ºC.

Before deposition, the etch rate of TMAH over different deposited nitrides were observed. Mixed frequency, low frequency, and high frequency deposited nitride dies were put in TMAH at 85ºC. Table 3.8 explains the results. The etch rates were unexpectedly high as compared to the ones on the literature. The lowest etch rate belongs to high frequency deposited silicon nitride.

Besides the low TMAH etch rate, the thin silicon nitride film must have low stress. Preventing the stress can be made by using the mixed frequency deposition. So, the mixed frequency type was used in this process. A 4000 Å thick silicon nitride was deposited over the wafers. Table 3.9 gives the details about process variables.

Table 3.8: Si_3N_4 thickness before and after TMAH etching.

Etching Times	Low Frequency Deposition	Mixed Frequency Deposition	High Frequency Deposition
Before etching	1061 Å	1373 Å	1056 Å
10 minutes	1021 Å	1269 Å	919 Å
20 minutes	943 Å	1185 Å	852 Å
30 minutes	932 Å	1117 Å	691 Å
40 minutes	901 Å	1047 Å	603 Å
Etch rates	5 Å/min.	8 Å/min.	12 Å/min.

Table 3.9: The process parameters using during the PECVD silicon nitride deposition.

Parameter	Value
SiH_4 flow rate	40 sccm
NH_3 flow rate	40 sccm
N_2 flow rate	1960 sccm
Mixed RF Power	20 W, 2 seconds low frequency 20 W, 6 seconds high frequency
Pressure	900 mT
Shower Temperature	250ºC
Platen Temperature	300ºC
Deposition Rate	350 Å/min.

3.2.9. SiO_2 and Si_3N_4 RIE Process

The passivation layer was supposed to be etched with the Reactive Ion Etching (RIE) process in STS devices. Wet etching of silicon nitride and silicon dioxide areas were extremely dangerous for this situation, since 2µm thick oxide and nitride deposited supporting arms had to survive without any undercut. Therefore, dry plasma etching was preferred in the first place.

Precise etching with high anisotropy is needed strongly in micromachining world. RIE responds to this need, allowing achieving etch holes with high depth and vertical straight walls. The gas which is in plasma form in the chamber is ionized and accelerated by an electric field toward the surface of the substrate. These ions move the molecules of the substrate by striking on them one after another. Directing the ions straight to the surface provides high anisotropy in trench etching.

The total layer thickness in the etch sample production wafers, which would be etched, was at most 11000Å including both SiO_2 and Si_3N_4. The coated photoresist needed to be resistive enough until the Reactive Ion Etching ends. Therefore, a thick resist with high resolution must be coated. S1813 was used in this photolithography. In order to thicken the resist, it was coated at 2000 rpm. The approximate S1813 thickness was 1.7µm. After hard-bake process, wafers were exposed to RIE. Silicon nitride RIE took 1 minute 21 seconds. Table 3.10 and Table 3.11 give the details about process variables. The outcome of the RIE process, which was the last step of the fabrication was illustrated with etch samples on Figure 3.23, Figure 3.24, and Figure 3.25.

Then the oxide layer under etched nitride was removed after 65 minutes of oxide RIE. Expose of the ions over the wafer in RIE processes, hardens the stripping of the photoresist. Long acetone and SVC-175 baths may be needed. Even it might be necessary to put the wafers into an oxygen plasma.

Table 3.10: The process parameters used during the Si_3N_4 RIE process.

Parameters	Value
CF_4 flow rate	60 sccm
CHF_3 flow rate	22 sccm
O_2 flow rate	10 sccm
RF Power	250 W
Pressure	70 mT
Etch Rate	3400 Å/min.

Table 3.11: The process parameters used during the SiO_2 RIE process

Parameters	Value
CF_4 flow rate	12 sccm
CHF_3 flow rate	38 sccm
RF Power	300 W
Pressure	100 mT
Etch Rate	1400 Å/min.

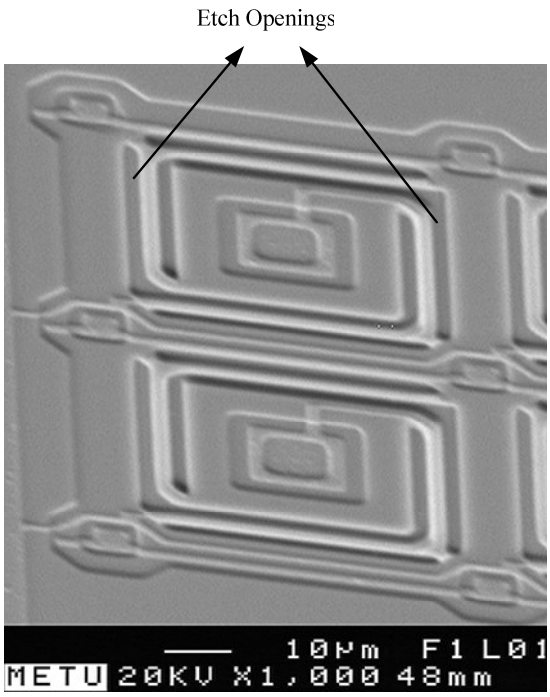


Figure 3.23: Etch samples fabricated for the ECES implementations in this study.

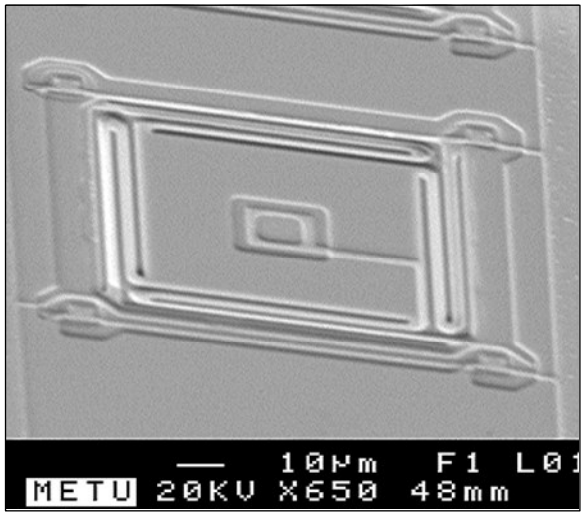


Figure 3.24: Another etch sample fabricated for the ECES implementations in this study.

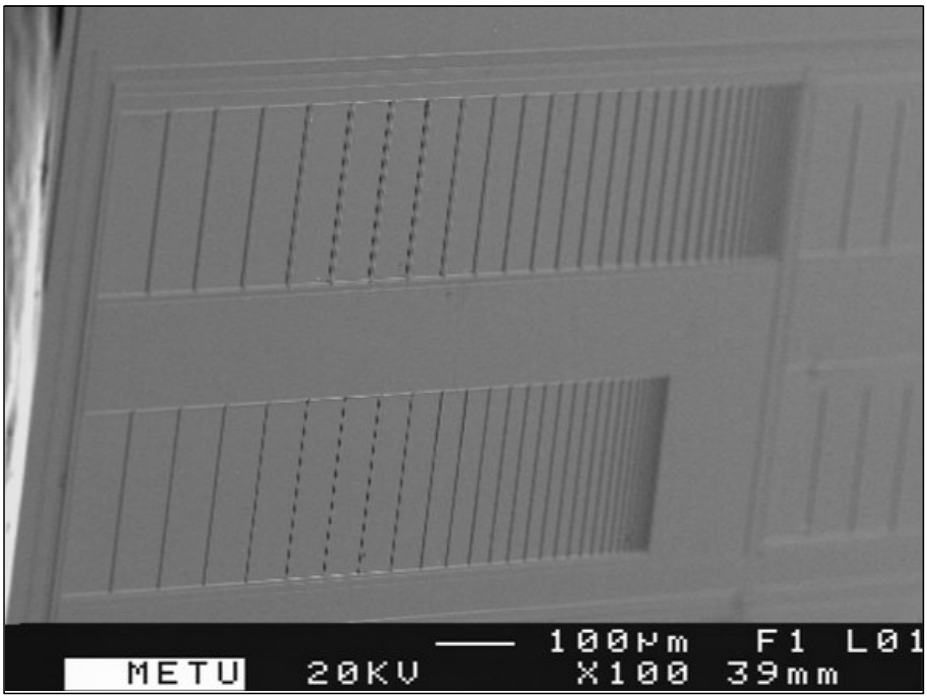


Figure 3.25: Bridge like structures fabricated for the ECES implementations in this study.

3.3. Conclusion

This chapter presented the fabrication process of the etch samples prepared for the ECES implementations. The fabrication processes involves thermal oxide growth, phosphorus diffusion, boron diffusion, metallization, silicon nitrade deposition and reactive ion etching processes. The thermal processes were carried according to the optimized parameters extracted from the SUPREM program results. Thus, the effect of thermal processes to each other was decreased to its minimum. The optimization of the phophorus and boron diffusion processes were done according to the four-point probe and chemical staining measurements. At the end of the thermal

processes the measurements told that the n-well and p^{++} process parameters were very close to those 0.8µm AMS standart CMOS process parameters have.

The metallization process of the etch samples were completely changed due to the wrong polarization of the metallization mask. The optimization of the negative photoresist MAN-1420 was done in order to obtain 1µm thick aluminum lines. Also, the aluminum wet etching was optimized to prevent the high undercut rate of aluminum. Since the topology of the wafer did not let the metallization process achieve, the project was continued with the original metallization mask. Obtaining 1µm lines was successfully obtained with the positive photoresist, S1813. Silicon nitride layer was deposited to the wafers as the passivation layer of the samples. Deposition process was done with PECVD. Finally, this chapter concludes the fabrication of the etch samples with the reactive ion etching process. This process was done for removing the nitride and oxide layer at the etch openings. The ECES experiments done with these etch samples will be explained in the next chapter.

CHAPTER 4

RESULTS AND DISCUSSIONS

This chapter gives the results of the experimental processes, done with the fabricated etch samples during this study. Also, the post-process of the microbolometer chips are done with etching the device in the optimized TMAH solution, under the effect of the ECES implementation.

Section 4.1 explains the results of the etching processes with the fabricated etch samples. The resistivity values of the doped areas of silicon are re-controlled by measuring the resistivity with the Van der Pauw resistivity measurement samples. Section 4.2 presents the implementation of ECES technique on microbolometer chips. Section 4.3 concludes this chapter by summarizing the outcomes of ECES implementation.

4.1. Etching Processes with the Fabricated Etch Samples

Firstly, the etch samples are examined after the fabrication process. The samples are needed to be tested weather an ohmic contact is satisfied with the aluminum layer or not. This can be done by the Van der Pauw resistivity measurement structures. The resistivities of the doped areas are measured from the contact pads of these

structures. The measured resistivity values are compared with the four-point probe measurements, which was done during diffusion process optimizations.

4.1.1. Resistivity Measurements

The resistivity of the phosphorous and boron doped areas of the fabricated etch samples were important. The diffusion processes were optimized according to the AMS 0.8 µm standard CMOS process parameters. The sheet resistances of the phosphorus diffusion and boron diffusion were controlled with the four-point probe measurements during those processes. Also, Van der Pauw resistivity measurement structures were added to the one of the etch samples in order to measure the resistivity after the fabrication of the devices. Figure 4.1 shows these structures.

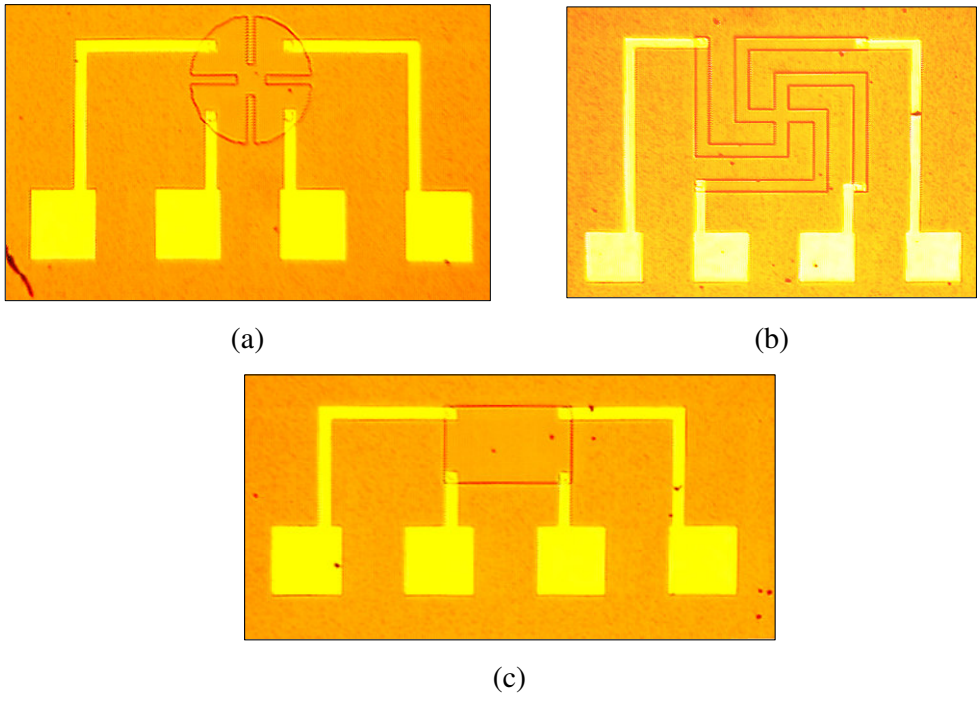


Figure 4.1: Van der Pauw resistivity measurement structures produsedin this study.

The sheet resistance of an arbitrary shaped sample can be calculated by the Van der Pauw technique [43]. Four contact pads along the periphery of the sample would be enough for these measurements. Figure 4.2 illustrates an arbitrary shaped sample with 4 contacts to the thin layer. The thickness of the sample needs to be very thin with respect to the width and length of the sample in order to prevent errors in calculations [43]. The Van der Pauw resistivity measurements consist of forcing a current flow through two adjacent contacts and measuring, the voltage across the other pair of contacts with a high impedance voltmeter [43, 44]. Considering the zero current flow through the voltage contacts, a contact resistance problem has no effect on the results [43]. A resistance can be found from these voltage and current values (Equation 4.1).

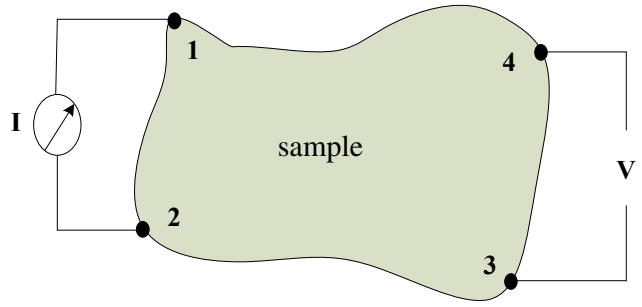


Figure 4.2: Measuring the resistivity of a sample with the Van der Pauw technique.

$$R_{12,34} = \frac{V_{34}}{I_{12}} \qquad 4.1$$

where, I_{12} is the current forced through contact 1 and contact 2, V_{34} is the voltage measured from contact 3 and contact 4. Horizontal and vertical resistances can be calculated as the Equation 4.2 and Equation 4.3 show. If the sample is symmetrical in shape, then there is no need for two calculations, as the horizontal and vertical resistance values would be equal to each other.

$$R_{horizontal} = R_{12,34} = \frac{V_{34}}{I_{12}} \qquad 4.2$$

$$R_{vertical} = R_{23,41} = \frac{V_{23}}{I_{41}} \qquad 4.3$$

The sheet resistance of the sample is calculated by the use of horizontal and vertical resistance values (Equation 4.4).

$$e^{-\pi R_{vertical}/R_S} + e^{-\pi R_{horizontal}/R_S} = 1 \qquad 4.4$$

where, Rs is the sheet resistance of the sample. As Figure 4.1 demonstrates, the measurements were done on three different structures. The calculated values are given on Table 4.2. The use of a cloverleaf structure for resistivity measurements is advised on the Van der Pauw technique. According to these results, the resistivity is successfully satisfied with a well-done aluminum deposition process, thus; ohmic contact is achieved.

Table 4.1: Resistivity values of phosphorus and boron doped areas compared with the AMS 0.8 standard CMOS process parameters.

	Sheet Resistance	
	4-Point Probe Meaurements	**CMOS process parameters**
Phosphorus Diffused Area	1050 Ω/□	1.2k OHM/□
Boron Diffused Area	75 Ω/□	40 OHM/□

Table 4.2: The Van der Pauw resistivity measurement results according to different measument samples.

	Sheet Resistances	
	n-well	**p++**
Rectangular sample	1230 Ω/□	-
Cloverleaf like sample	1065 Ω/□	70 Ω/□
Cross like sample	1085 Ω/□	78 Ω/□

4.1.2. Preparation of the Etch Sample for Etching Process

Each sample was prepared individually for the anisotropic wet etching process. Figure 4.3 gives the preparation steps of one of the samples. Firstly, the photoresist layer, which was coated before dicing process in order to protect the samples from contamination and damages, was stripped from the surface with long acetone and IPA baths. Later, the sample was placed on an alumina substrate, which was fabricated by Aselsan. The gold-plated areas of the alumina substrate were used as an interface to the sample pads. Thus, wires were soldered before the placement of the sample. Afterwards, samples were fixed on the alumina substrate with the help of the white epoxy. All white epoxy curing processes were done on the hotplate at 120°C for 1 hour.

Wire bonding of the sample was done to achieve electrical contact to the chip from the alumina substrate. Pads were connected to the gold layer on the alumina substrate. The white epoxy shows good resistivity against all kinds of high acidic and high basic solution; however, it applies a high stress to what it covers. Therefore, the bonded wires could not be covered with white epoxy, as the stress of the white epoxy breaks the wires bonds. A low stress filling material was needed to

cover the wire bonds. Instead of the white epoxy, Emerson & Cuming, Amicon 50500-1, black epoxy was used. The black epoxy has a very low viscosity, causing the epoxy to move until it is stopped by a wall. For this reason a cavity was built with white epoxy walls around the wires. Then, the black epoxy was applied to this cavity. The curing process of the black epoxy was done in oven. Another issue is that, this epoxy provides low stress but could not show resistance to the TMAH solution. Therefore, the black epoxy should be covered with white epoxy before any anisotropic etching process attempt.

A number of cleaning steps were done on the samples before the aniotropic etching. First, the samples were dipped in TCE, Acetone, and IPA solutions, respectively; sample stayed in each solution for 2 minutes. Then, samples were dipped into the 5wt.% HF solution for 15 seconds in order to get rid of the native oxide layer.

Figure 4.4 shows the 4-electrode electrochemical etch-stop system setup, prepared for the etching process. The power supply applies the V_E voltage, which was illusturated on Figure 2.15.

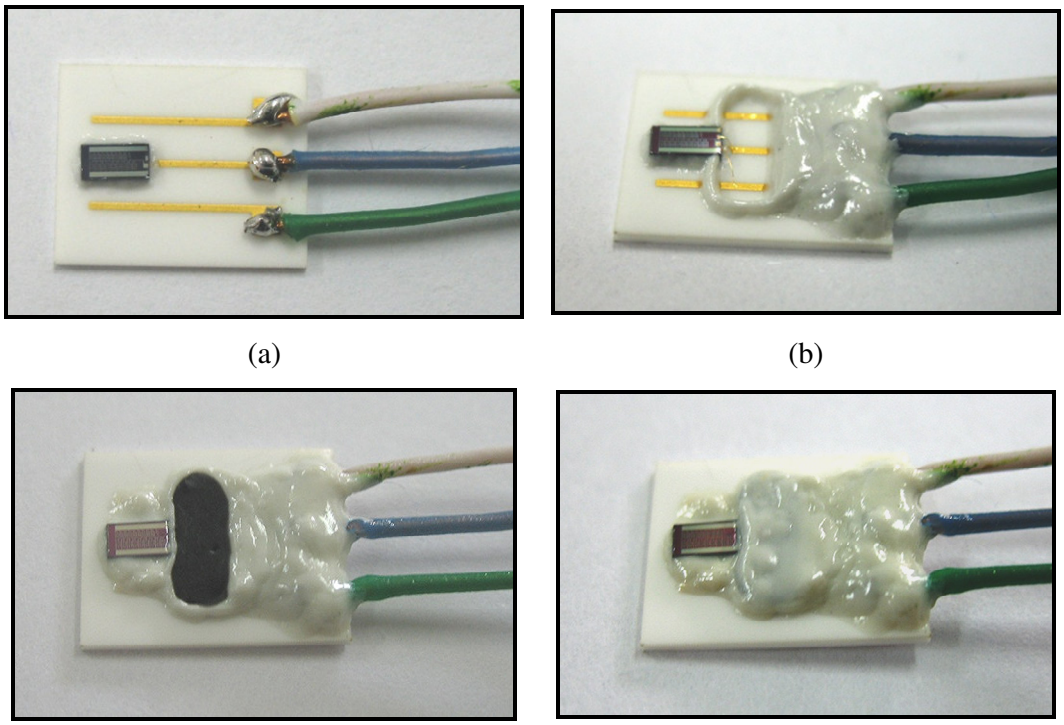
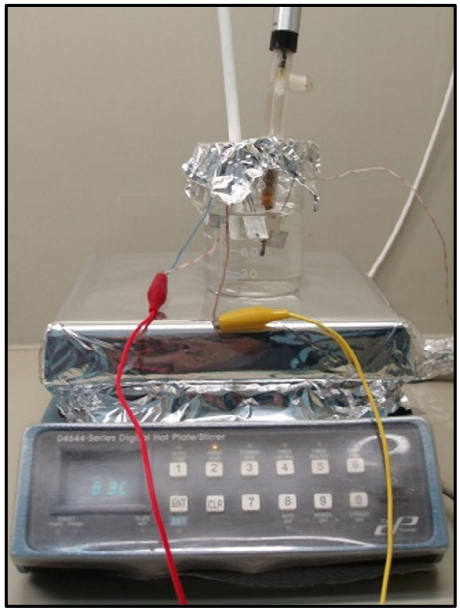


Figure 4.3: Preparation of the fabricated etch sample: (a) the sample is fixed on the alumina substrate with white epoxy. (b) A cavity is done with the white epoxy in order to surround and protect the wire bonding lines. (c) Bonded wires are protected with black epoxy, filling the cavity. (d) Black epoxy and all conductive layers on the alumina substrate are covered with white epoxy.



(a)

(b)

Figure 4.4: Anisotropic etching process, applied to the fabricated etch samples. Two multimeters are used for n-well, p^{++} and p-substrate current measurements.

The potentiaostat applied -1.6 V to working electrode which was directly connected to the p-substrate and p^{++}-doped areas contacts. A -0.5 V volateg was applied to the n-well doped regions. The multimeters measured the current passing through the p-substrate, p^{++} connections, and n-well connection. Figure 4.5 illustrates the current values taken for 1 hour. The p-substrate and p^{++} connection was applying a voltage that enhanced the etching process. That is the electron movement was towards the p-substrate and p^{++}-doped areas resulting a negative current value. The n-well doped regions were biased to appeal the electrons from the surface. The electron movement was backwards the n-well, causing a positive voltage value. These current signs ensured that the ECES technique could be properly applied.

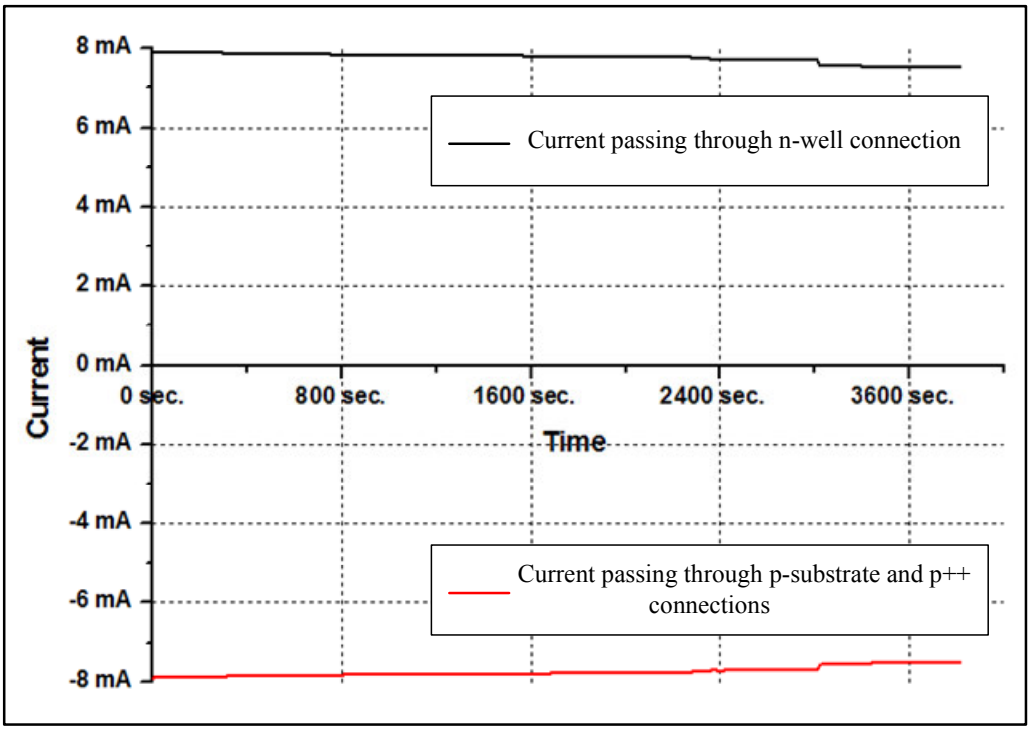


Figure 4.5: Currents flowing through biasing connections of p-substrate, p^{++} and n-well areas.

4.1.3. The Effect of Depletion Layer

The experiments show that the etching does not end at the metallurjical junction between n-well and p-substrate. The etching process is terminated before the metallurgical junction. The reason is the depletion region between n-well and p-substrate. The depletion region directly affects the etch reactions. Figure 4.6 gives the outcome of applying -1.6V to p-substrate and 1V to n-well doped area. After 30 minutes of etching, there are still un-etched regions because of the depletion region formed between n-well and p-substrate. The thickness of the combs is increased, and the n-well areas doped like combs can not be suspended after the etching process.

This effect can be large enough to prevent the etching of p-substrate between two n-well diffused areas. Figure 4.7 gives the SEM picture of all combs given in Figure 4.6. It is clearly seen that as the n-well combs get narrower, the etching reactions are prevented on the p-substrate. The smallest separation between n-well combs at which p-substrate continues to etch is determined as 80μm. The experiments were repeated with applying different n-well passivation potentials. Table 4.3 gives the minimum n-well separation that can be etched according to 1V, 0V and -0.5V n-well biases, where the minimum n-well separations that can be etched are determined as 80μm, 70 μm, and 50 μm, respectively.

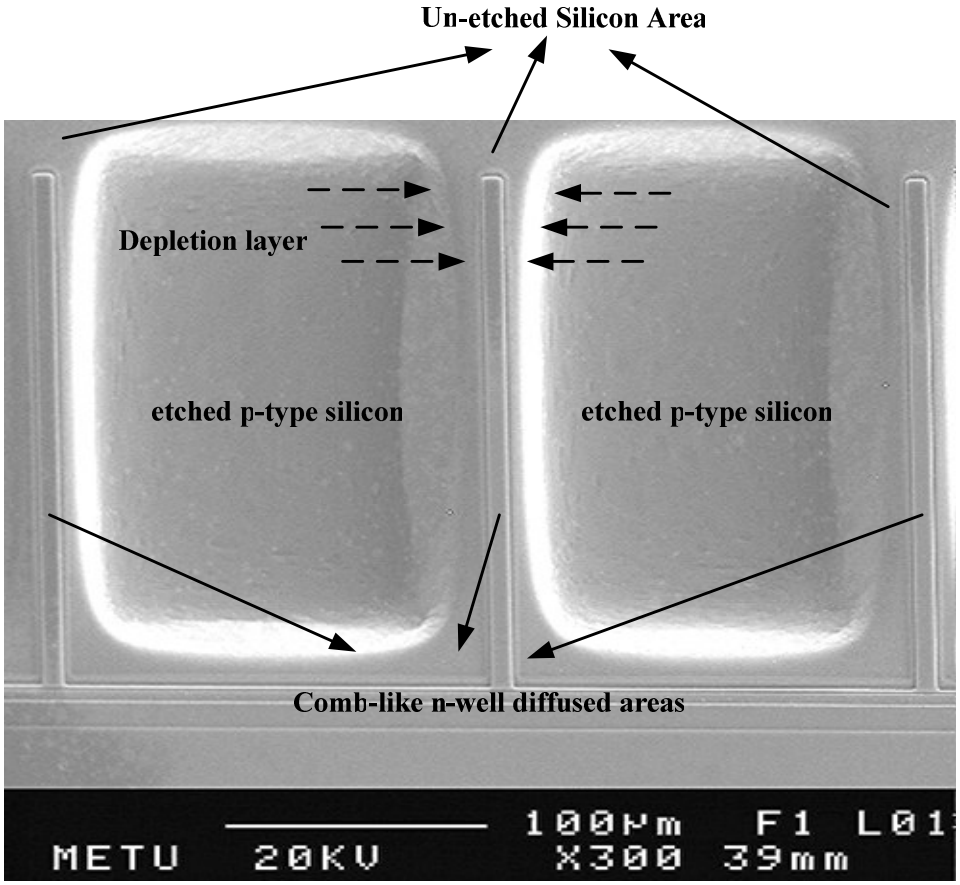


Figure 4.6: SEM picture of the etch sample, affected by the depletion region, i.e., the deposition regions are not etched in the TMAH solution.

Table 4.3: Minimum n-well separation that can be etched according to varying n-well bias.

n-well bias	Minimum n-well separation that can be etched
1V	80µm
0V	70µm
-0.5V	50µm

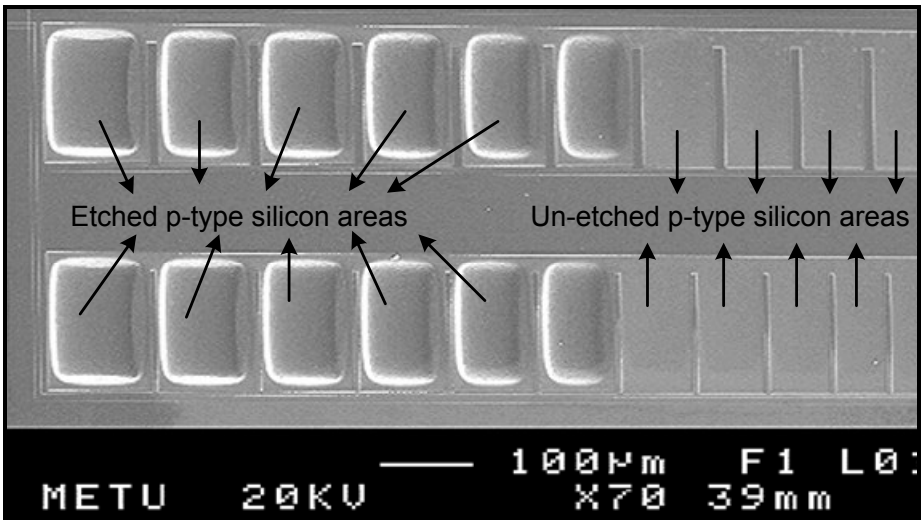
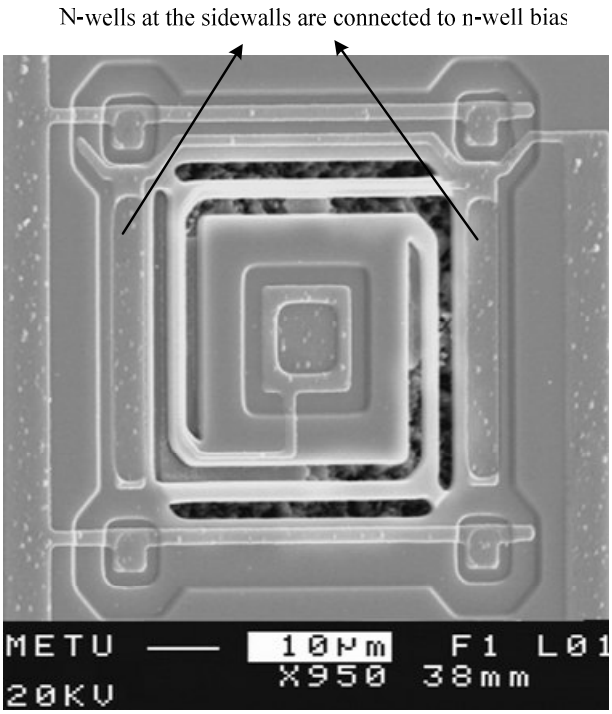


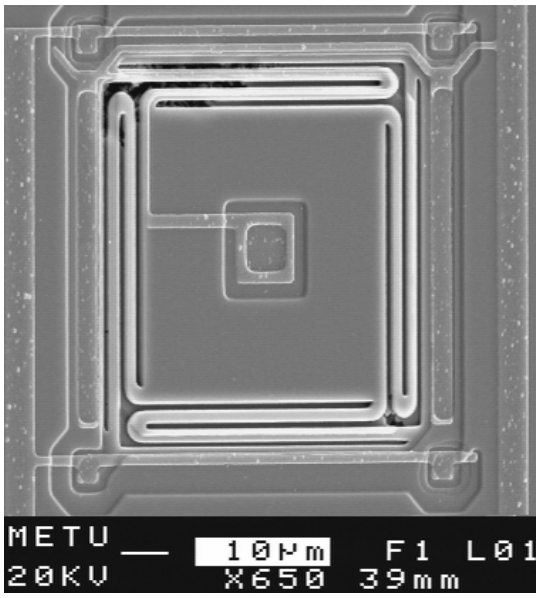
Figure 4.7: The effect of the depletion region to the etching reactions.

It is also important to mention that the corners of the etched areas are not sharp. This can be explained as the high current density through the silicon which passivates the n-well area [53, 54]. The increase of the electric field on the corners and edges causes the current density to be higher at those locations.

The etching processes with the etch samples having microbolometer pixel structures were done under the fact of depletion region effect. Decreasing the n-well bias could be possible, but there must be no doubt about whether the applied potential is anodic enough to passivate the n-well area. Therefore, the n-well was biased with -0.5V, whereas the p-substrate was biased with -1.6V. The etching took one hour. Figure 4.8 gives the SEM pictures of pixels having sidewalls connected to the n-well potential. It was seen that the pixels having their sidewalls biased with n-well potential did not etch. Even after one hour of etching process, only small deformations were seen on the etch surface.



(a)



(b)

Figure 4.8: Outcome of the etching process where sidewalls were biased with n-well potential. It is seen that the pixels are not etched properly.

On the other hand, the pixels having their sidewalls biased with p-substrate potential were etched at a high undercut rate. Figure 4.9 illustrates the SEM picture pixel having sidewalls connected to the p-substrate potential. The etching started properly from the etch openings.

There were also pixels without biasing their sidewalls. The outcome of the process on these pixels was as expected. The (111) walls underneath the sensitive area formed a pyramidial shape. A suspended structure was obtained. Figure 4.10 and Figure 4.11 shows the suspended structures

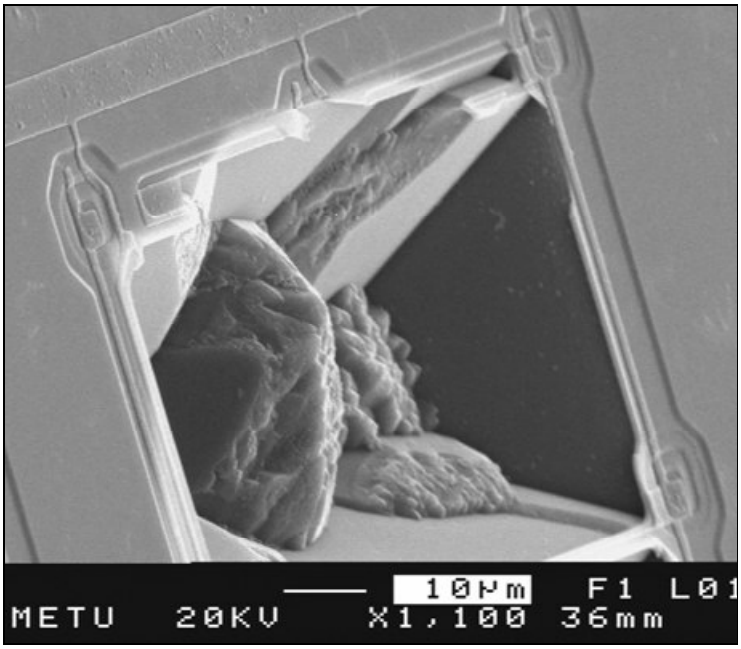


Figure 4.9: Outcome of the etching process where sidewalls were biased with p-substrate potential, where the top of the pixel is broken to see the cavity region. It is clear from this picture that the etching of the substrate is achieved successfully.

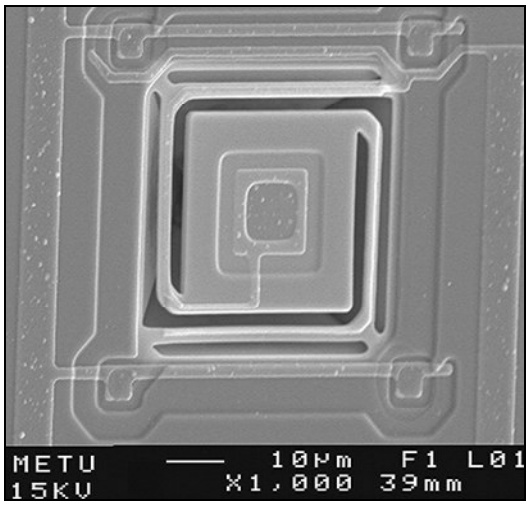


Figure 4.10: Outcome of the etching process where sidewalls were not biased. It is seen that the etching is successfully achieved.

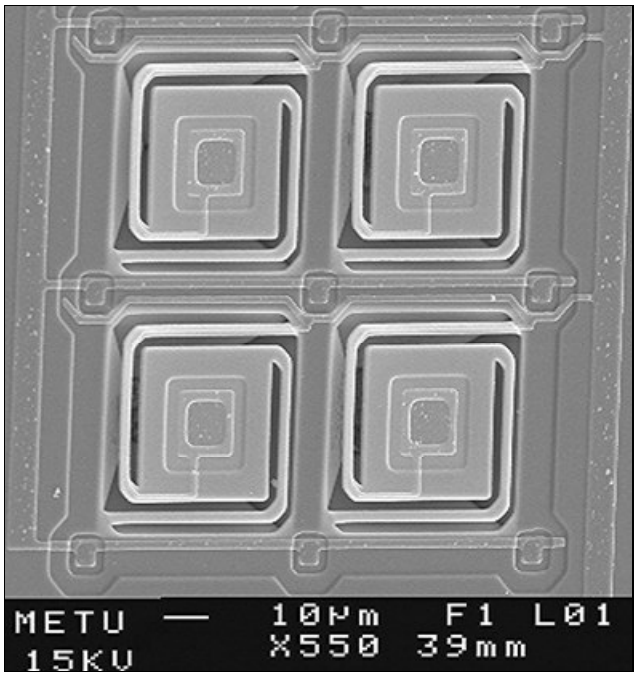
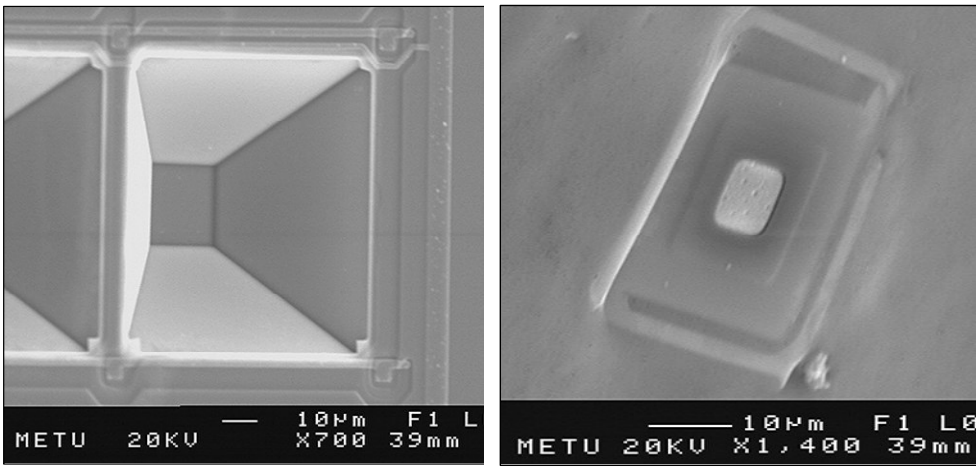


Figure 4.11: SEM picture of a 2 X 2 array of microbolometer pixels after the etching process. All of the four pixels etched properly.

4.1.4. Step Coverage of Si_3N_4

The suspended structures were obtained but the n-well are underneath the silicon nitride layer could not be protected from the etchant. A sticky tape was used to remove the silicon nitride to look under the structure. Figure 4.12 illustrates the SEM pictures of the pixel and the sensitive part of the pixel. The pyramidial shape formed because of the (111) planes were obvious without any hillocks on it. But, on the other hand, the bottom of sensitive part of the pixel did not have the n-well doped area. The reason of this problem is the low step coverage of the silicon nitride deposition process.

Silicon nitrade was a resistive film against TMAH. Thus, a 4000Å thick, Si_3N_4 layer was deposited as the masking layer for anisotropic etching process. But, unfortunately, the deposited nitrate layer could not stand against to TMAH solution for that much long. After one hour of the 10wt.% TMAH etching process, it is observed that the aluminum lines are exposed the solution and eventually etched by the TMAH solution at various parts. Figure 4.13 illustrates aluminum etched areas where the silicon nitrate coating was thinned and damaged. This situation causes the TMAH solution to expose to the applied potential. When the TMAH solution sees a potential, it is impossible to prevent etching on the n-well diffused area.



(a) (b)

Figure 4.12: SEM picture of (a) underneath of the silicon nitride layer, and (b) bottom of the silicon nitride layer, which was removed by a sticky tape.

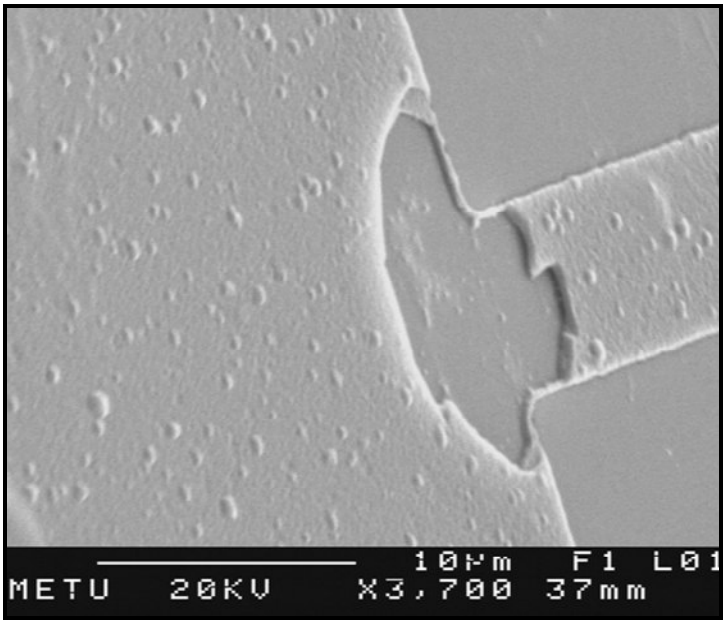
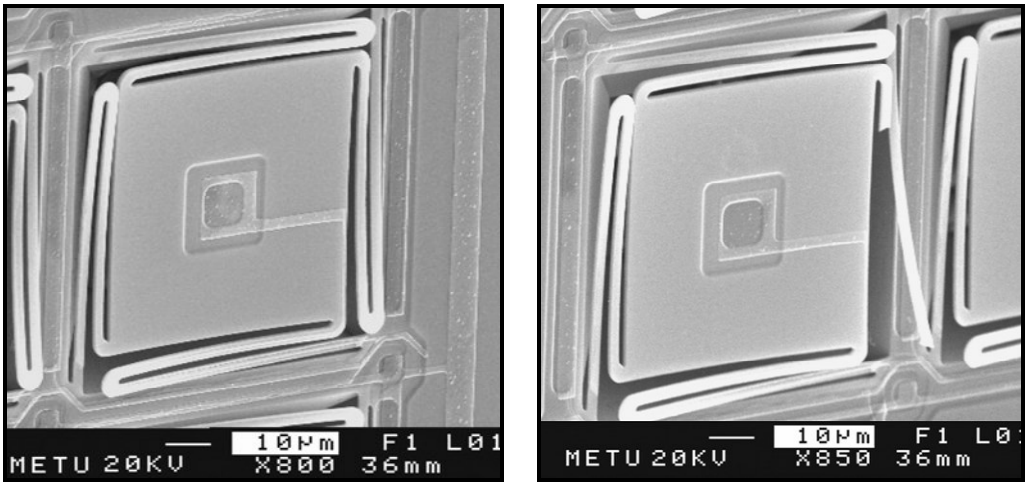


Figure 4.13: SEM pictures of aluminum lines, attacked by the TMAH solution.

4.1.5. High Thin Film Stress

The oxide layer, which acted as the masking layer of the silicon surface, was grown with a cyclic oxidation process. This process aimed reducing the stress of the oxide layer, and also enhancing the growth rate of the oxidation process. After the oxidation process, an additional Si_3N_4 layer was deposited as the TMAH masking layer. The silicon nitride deposition process was also carried out in mixed frequency in order to obtain a stress-free Si_3N_4 layer. However, the SEM pictures of the suspended pixels, which were taken after the TMAH etching process, showed the high tensile stress on the supporting arms. Figure 4.14 shows these SEM pictures.



(a) (b)

Figure 4.14: The tensile stress of the Si_3N_4: (a) the supporting arms of the pixels are affected from the tensile stress. (b) A very high tensile stress causing the supporting arms to break.

The bulk silicon under the pixels was etched with the TMAH solution. As the silicon layer was removed under the supporting arms, the effect of the tensile stress on the SiO_2 and Si_3N_4 was seen more obviously, such that some arms could not stand the tensile force and were broken. It is seen that the stress of the thin films deposited one on another should be considered together rather than optimizing their stresses individually. By this way, the stress of the films can be eliminated.

4.2. Post-Processing of Microbolometer Chip

The information about the ECES technique and TMAH etching processes were applied to microbolometer designs in the post-CMOS process of the devices. Section 4.2.1 will first explain the ECES setup for the front side microbolometer chip etching process. Then, Section 4.2.2 results of the post-process of the mirobolometer chip

4.2.1. ECES implementation of Microbolometer Chip for front side etching

The preparations of the mirobolometer chip for etching process was different from the preparation of the fabricated etch samples. Figure 4.15 gives the preparation steps of the microbolometer chip. The chip was placed into a standard 84 pin package (JLCC 84 with 0.3 inch x 0.3 inch square cavity) (Figure 4.15(a)). The cavity under the bondings was coated with the black epoxy, Emerson & Cuming, Amicon 50500-1 (Figure 4.15(b)). The pad connections were obtained by bonding each pad to this package (Figure 4.15(c)). The pads and bondings have to be covered with the black epoxy in order to keep them stress free. For this purpose, a very thin white epoxy is applied on the chip, next to the pads in order to prevent flow of the

black epoxy on to the pixels (Figure 4.15(d)). Then, the pads and bondings are covered with the black epoxy (Figure 4.15(e)). Finally, the white epoxy was carefully used to cover the black epoxy, pads of the package, and the surface of the chip except the array of pixels (Figure 4.15(f)). The epoxy was applied at high temperature in order to prevent it to leak.

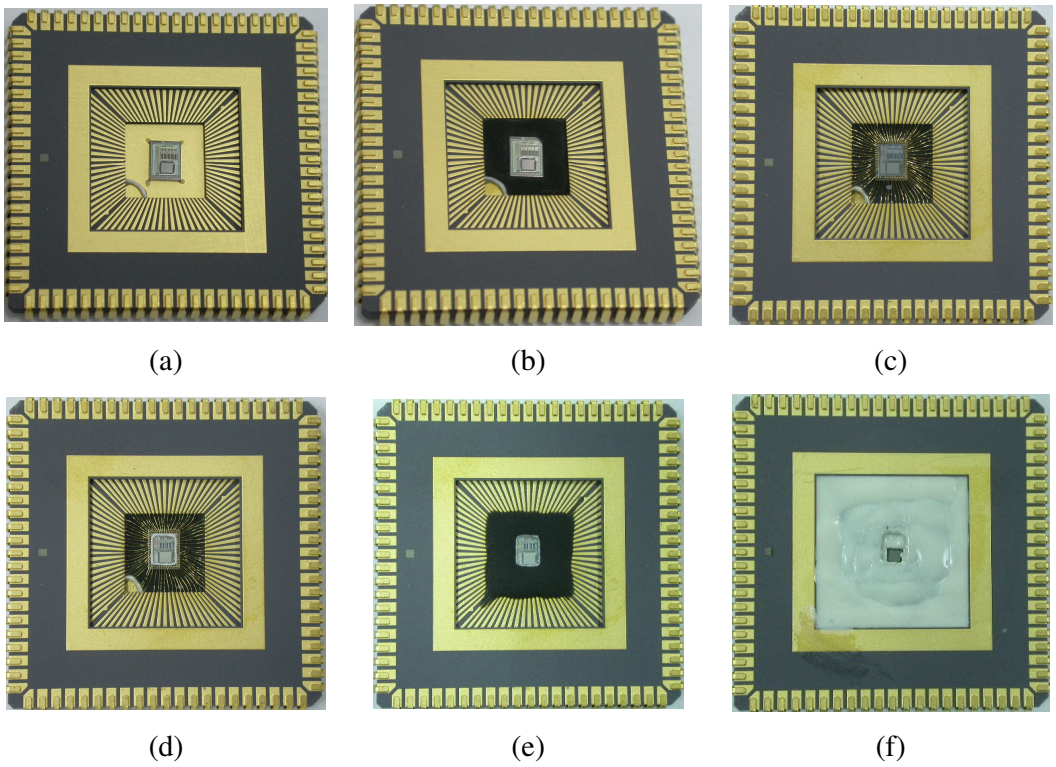


Figure 4.15: Preparation steps of the microbolometer chip for the etching process [24].

This package was placed into a socket which was protected with a steel etch setup and o-rings. Figure 4.16 and Figure 4.17 illustrates the etch setup and its structural design. The pins of the socket inside the etch setup were soldered with wires, that

pass through the long steel pipe and reach out. These wires are used to apply the biasing necessary for the ECES implementation. The o-rings prevented the TMAH leakage inside the etch setup. The prepared package was dipped into TCE, Acetone, and IPA, respectively. Then, the native oxide layer on the silicon surface was removed by dipping the package into the 5wt.% TMAH solution for 13seconds. Finally, the package was placed inside the socket. The o-rings were fixed on the surface with the screws. The etch setup was ready for the etching process.

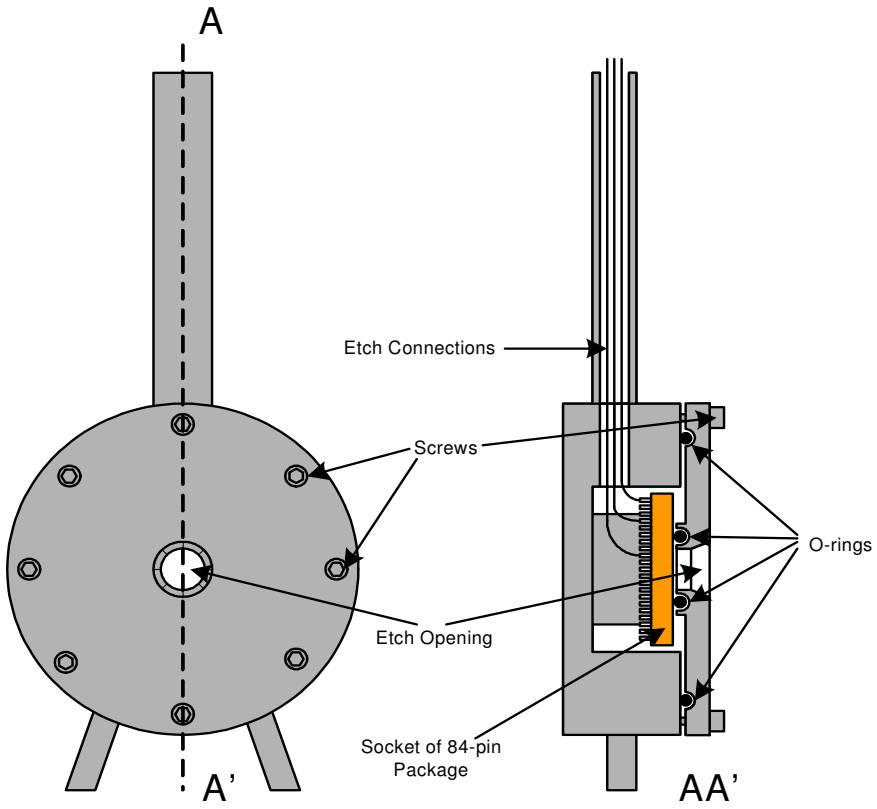


Figure 4.16: Structural and cross-sectional view of the etch setup [24].

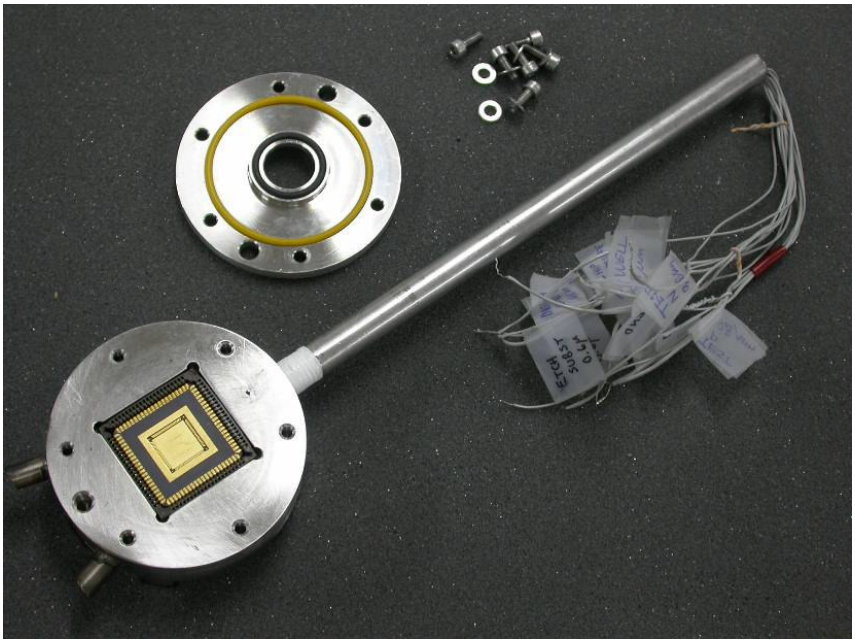


Figure 4.17: The etch setup of the microbolometer chip which applies ECES to the pixels [24].

A 300ml 10wt.% TMAH solution was prepared at 85°C, where 10gr/lt. AP was added to the solution just before the process started. The p-substrate was biased with -1.6V, on the other hand, sensitive areas having buried n-wells were biased with -0.5V. Unfortunatelly, the sidewalls of the pixels were biased with n-well potential because of the design of the pixels. The top of the beaker was covered with a specially designed Teflon cap. Previously, the necessary probe inlets were opened on this cap. Figure 4.18 and Figure 4.19 demonstrate the anisotropic etching process with the 4-electrode ECES system configuration applied to the microbolometer chip.

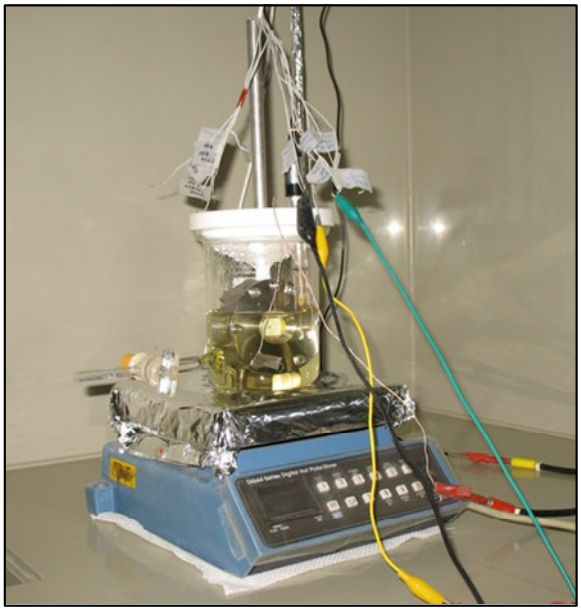


Figure 4.18: Anisotropic etching process applied to the microbolometer chip.

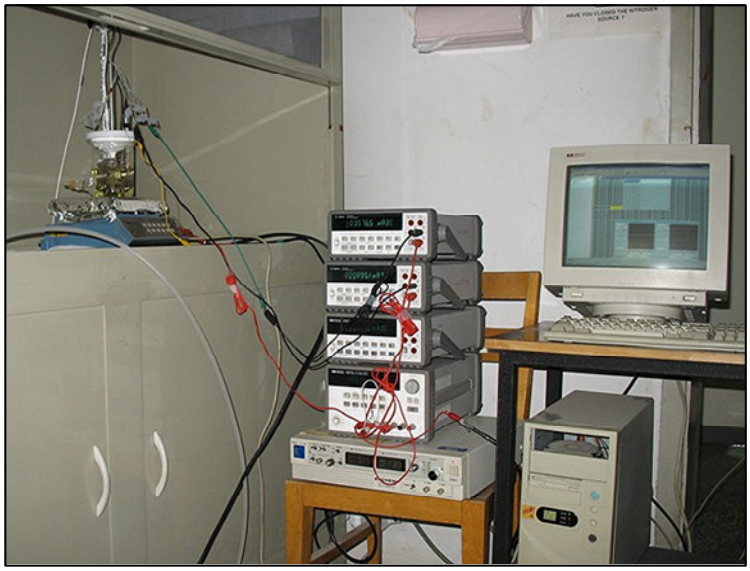


Figure 4.19: Anisotropic etching process applied to the microbolometer chip, where the computer setup is also seen.

4.2.2. Results of the front side etch of the microbolometer

Figure 4.20 and Figure 4.21 show the microbolometer and reference pixels after 1.5 hour of etching process.The depletion layer effect was seen on the pixels as expected. The silicon substrate did not etch because of the passivation voltage applied to the sidewalls. Increasing the etching process time is not a solution for situations like this. If the etching time is kept long from its usual process time, the masking layers, silicon nitride and silicon dioxide will be etched slowly, and they will drain resistivity against the etchant. Eventually, the etchant may reach the aluminum layer of the micobolometer chip.

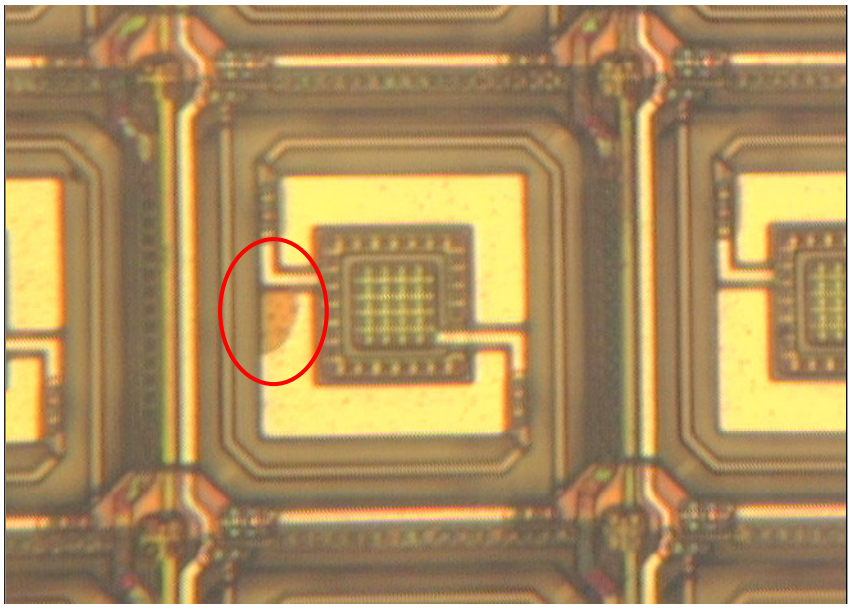


Figure 4.20: The microbolometer pixel after 1.5 hour of etching process. The metal layer on the sensitive area was damaged by the etchant.

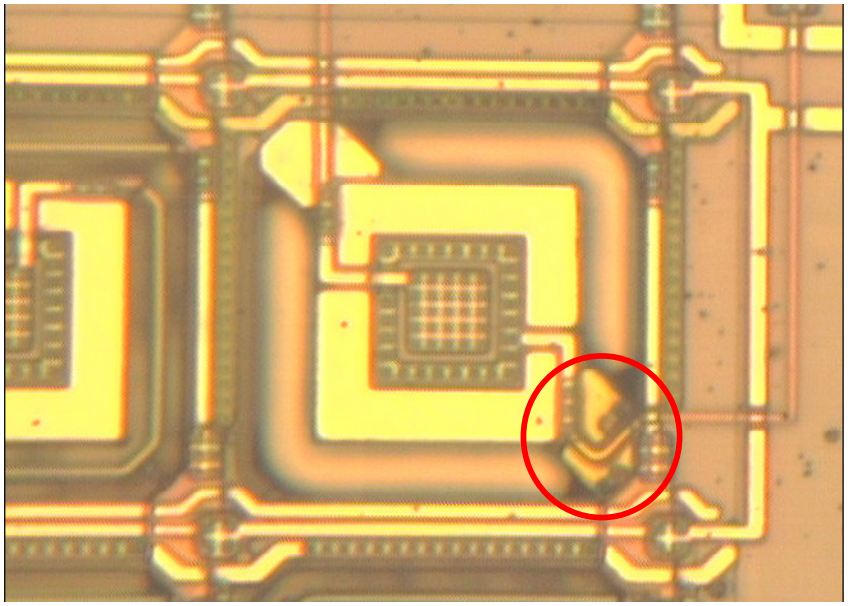


Figure 4.21: The reference pixel after 1.5 hour of etching process. The metal layer on the supporting arms of the pixel was damaged by the etchant.

4.2.3. ECES implementation of Microbolometer Chip for back side etching

These experiments show that applying passivation potential to the side walls indeed prevents the etching of the substrate. After these experiments, it is realized the reason for not being able to etch CMOS microbolometers. Infact, these findings were also confirmed with some other experiments performed on CMOS microbolometers with back side etchings.

The microbolometer prepared for back side etching is designed by Erkan Alpman and Şafak Demirci. The back side etching process of the microbolometers is designed as a wafer level process. The silicon area under the pixels is exposed to the

etchant with a proper mask. Figure 4.22 illustrates the cross-section of the desired result after the back side etching of the microbolometer chip.

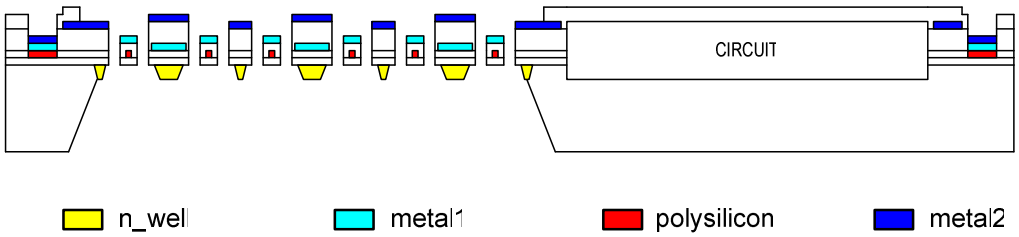


Figure 4.22: Cross-section of the desired result after back side etching of the microbolometer chip.

The back side anisotropic etching process with the ECES implementation was applied to this microbolometer by the ETH, Switzerland. Figure 4.23 gives the SEM picture of the etched back side of the microbolometer. The results showed that, there were still p-type silicon on the absorber area, and the supporting arms are still connected to the pixel itself. The problem is solved by applying an RIE process from the front-side of the pixels in order to open the areas next to the supporting arms. Figure 4.24 demostrates the suspended pixels obtained after the RIE process. However, the supporting arms still carry the un-etched p-type silicon under it. This causes problem for the detection mechanism.

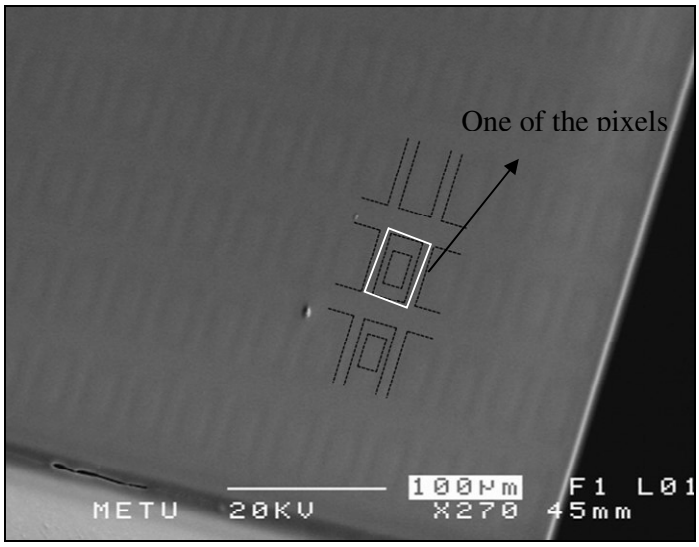


Figure 4.23: SEM picture of the etched back side of the pixels. It is seen that the bulk silicon was etched but the supporting arms were still connected to the pixel itself.

The back side anisotropic etching process of these microbolometers is repeated with disconnecting the n-well passivating voltage on the side walls of the pixels on another wafer. The etching process is done with 6M KOH solution at 90°C in a KOH tank. Figure 4.25 shows the KOH tank, where the wafer-level back side etching of the microbolometers was done.

The wafer is designed with two big pads which are needed for obtaining electrical contact with the electrode which has the n-well passivating voltage and p-substrate etch voltages contacts. Figure 4.26 illustrates the wafer and the preparation for the back side etching process in the electrode.

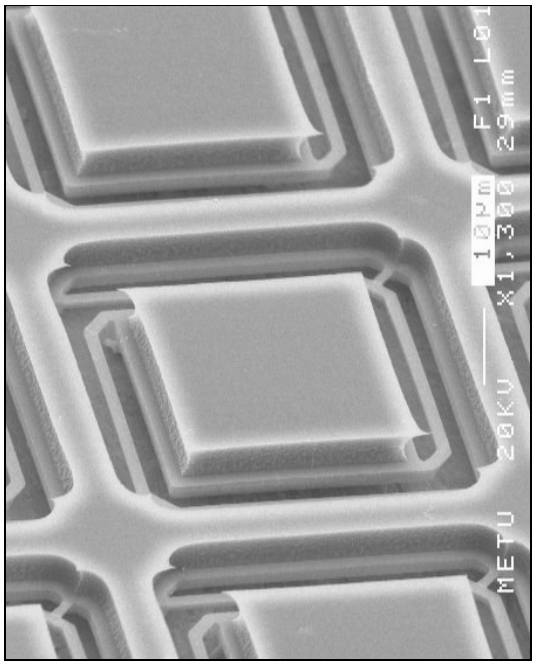
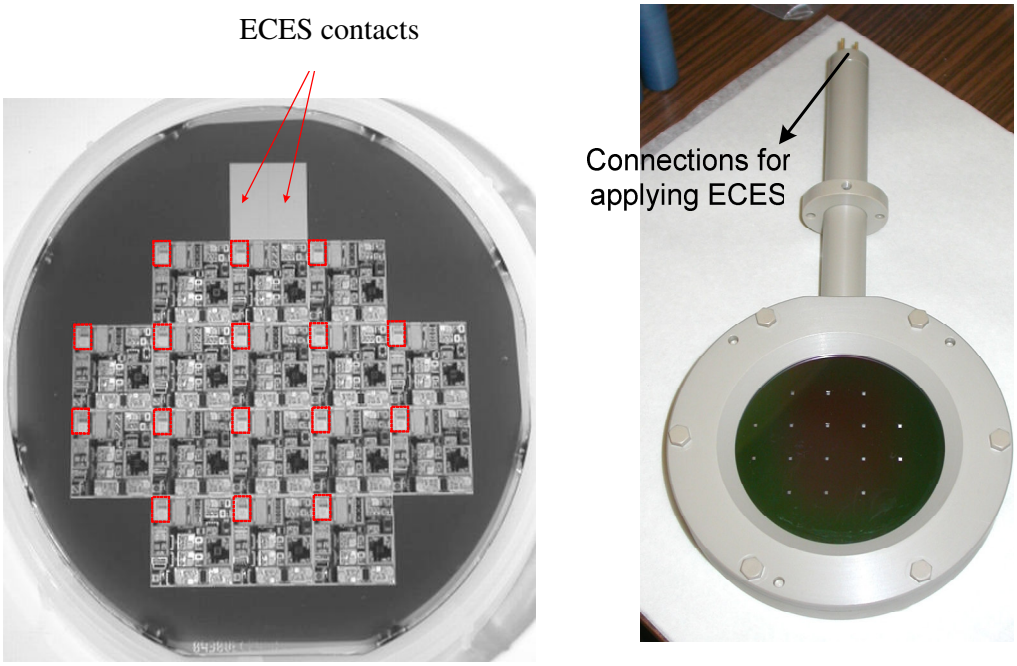


Figure 4.24: SEM picture of the front side of the microbolometers after the RIE process.

Figure 4.25: The KOH tank where the wafer-level back side etching of the microbolometers were done.



(a) (b)

Figure 4.26: The preparation of the wafer for back side etching process: (a) the wafer has two big pads, one is for n-well passivating voltage and the other is for the p-substrate etch voltage biasing, and (b) the wafer is placed according to these contacts in to the electrode.

In the etching process the n-well regions are biased with 1.5V, and p-substrate is biased with -3.5V. The process took 3 hours and 55 minutes. Figure 4.27 illustrates the SEM picture taken from the back side of the pixels after the etching process. It was seen that the etching started properly and the n-well areas were protected with a passivation layer generated by the passivating voltage.

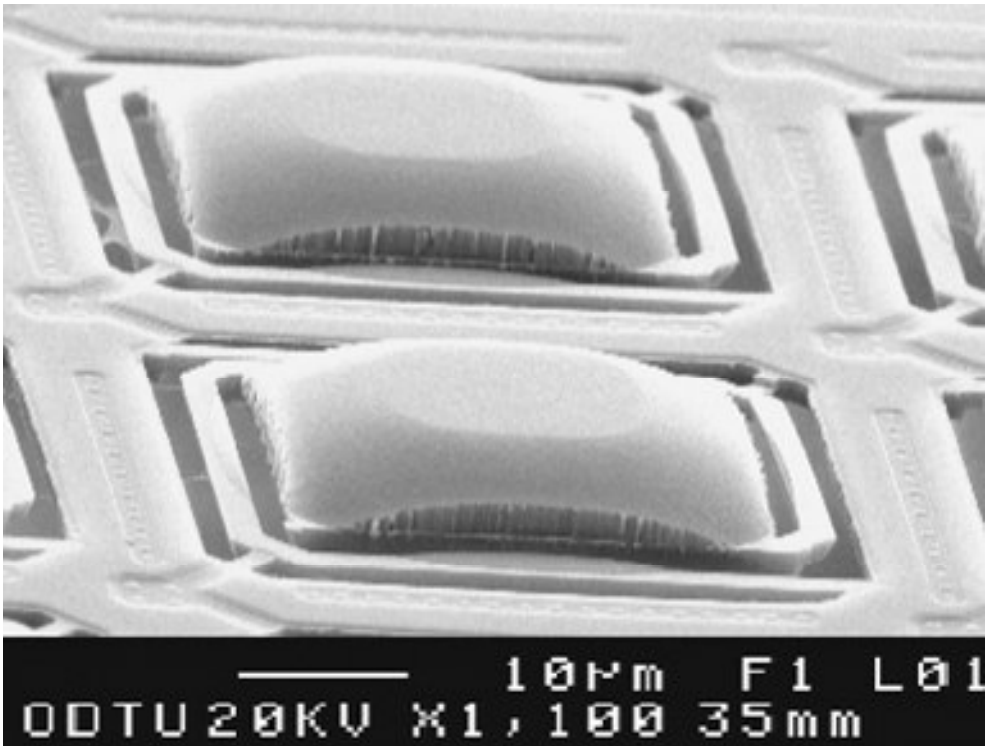


Figure 4.27: Back side of the pixels after the back side etching process with 6M KOH at 90°C.

4.3. Conclusion

This chapter gives the experimental results obtained after applying the ECES technique to the fabricated etch samples. Firstly, the sheet resistance values of the boron and phosphorus doped regions were measured by the Van der Pauw resistivity measurement structures. The measurements were close to those measured during the optimization of the diffusion processes by the four-point probe technique. This also showed that ohmic contact to the silicon was successfully satisfied by the aluminum deposition process.

The effect of the depletion region between n-well and p-substrate was investigated with the etch samples. Increasing the n-well voltage causes the p-substrate between two n-well doped areas to passivate. Decreasing the n-well voltage may also decrease the minimum distance that can be etched between n-well regions. However, the passivation of the n-well regions should be guarantied with a significant anodic voltage. The ECES implementation experiments shows that, to achieve a successful ECES implementation on the pixel structures, the sidewalls of the pixels should not be biased. Even though all the necessary conditions are satisfied for an ECES implementation, the aluminium layer on the supporting arms were affected from the etchant causing the n-well region under the sensitive area etch due to the low step coverage of the silicon nitride. This is a production problem, and can be solved in future experiments.

Another production problem which must be handled on further processes is the thin film stress of silicon nitrade. If these problems are considered and solved, a successful ECES implementation can be done with the the fabricated etch samples.

The post-CMOS etching process of the microbolometer chips is done with the developed ECES technique. Unfortunately, the design of the pixels includes n-well voltage biased side walls. The etching process was not successful due to the depletion effect which is proven on previous sections of this chapter. Further experiments with microbolometers with back side etching processes gave successful results. The n-well passivating voltage connections to the side walls are disconnected and the etching is done from the back side of the wafer with KOH. The experiments are succesfull. At the end of the etching the pixels were suspended and n-well regions were protected. ECES implementation parameters must be taken into consideration.

CONCLUSION AND FUTURE WORK

The research performed in the concept of this thesis involves the development of electrochemical etch-stop techniques for integrated MEMS sensors. The theory of the electrochemical etch-stop technique is explained in detail. The anisotropic etchant, TMAH, is investigated in order to obtain an optimized anisotropic wet etching process under control of ECES technique. The design and the fabrication of special etch samples are completed and the results of experiments done with etch samples are included in this thesis.

The achievements carried out during this research can be summarized as follows:

1. The anisotropic etchants are investigated according to their CMOS compatibility, selectivity towards SiO_2, high silicon etch rate, and low toxicity. As a result tetra methyl ammonium hydroxide (TMAH) is chosen for the anisotropic etching processes.

2. The theory of the anodic oxidation is explained in detail. The removal of the silicon atom is a consequence of a series of reduction-oxidation reactions. The continuity of the etching process depends on the reduction of the water caused by the electrons which are generated on the surface of the silicon by the oxidation reaction. The ECES technique involves drawing these electrons away from the surface by applying appropriate voltage to the surface to stop the etching of the surface.

3. The effect of the temperature of the etchant is studied with a series of etching experiments. Experiments show that, the etch rate of the silicon decreases drastically as the temperature decreases. A high etchant temperature is needed for high silicon etch rate, which is essential for all etching processes. However, as the temperature increases the etch rate of SiO_2 increases too. This may endanger the protecting SiO_2 mask of the samples, causing unwanted etching results. The temperature of the etchant is determined as 85°C.

4. The effect of the concentration of the etchant over the etch rate of silicon, surface roughness and biasing voltages are studied with the current-voltage experiments. The experiments show that, the etch rate of silicon decreases significantly as the concentration increases. However, at concentrations lower than 5wt.% TMAH, the silicon etch rate falls down because of the formation of the hillocks the on silicon surface. The hillocks caused by the low TMAH concentration are prevented with the addition of ammonium peroxodisulfate (AP). However, a stable process with a fixed AP amount can not be obtained with 5wt.% TMAH. 10wt.% TMAH with 10gr/lt. AP clearly provides a smooth silicon surface with high silicon etch rate. The passivating voltage for the n-well area and the etch voltage for the p-substrate are defined as -0.5V and -1.6V, respectively, for 10wt.% TMAH.

5. The effect of illumination over the silicon etch rate of the etchant is investigated. The experiments show that the illumination effects both silicon etch rate and the biasing voltages. Since the illumination causes a non-stable etching process, the experiments are done in total darkness.

6. Different silicon samples are designed in order to use in ECES experiments. Their masks are drawn with CADENCE according to the 0.8 AMS standard CMOS process design rules. The production of these samples was carried out

in METU-MET facilities. The process flow of these etch samples involves thermal processes at high temperature. Since the thermal processes affect the previously done process parameters, the simulation of all thermal processes is done with SUPREM simulation tool, before the process starts.

7. The boron and phosphorus diffusion processes are done according to the 0.8 AMS standard CMOS process parameters. After a series of optimization processes, the sheet resistance and the junction depth of the phosphorus and boron diffused areas are found very close to the 0.8 AMS standard CMOS process parameters.

8. Thermal oxidation, boron and phosphorus diffusions, aluminum and silicon nitride layer deposition processes are completed respectively. The metallization layer of the etch samples are obtained after a series of aluminum etching processes. The aluminum etchant temperature and etch time are optimized in order to get 1µm thick aluminum lines. Experiments give that, the undercut rate of the aluminum also increases as the temperature of the aluminum etchant increases. The undercut of the etchant is prevented with high agitation and low etchant temperature.

9. Experiments with the etch samples give that the minimum distance between n-well regions that enables etching is dependent to the depletion region width between p-substrate and n-well diffused areas. The width of the depletion region of a p/n junction is directly affected by the applied voltage and the sheet resistances of the diffused areas, causing the p-substrate to passivate. According to the experiments the minimum distance between n-well doped areas can be 80 µm when -0.5V is applied to the n-well area.

10. The post-CMOS front side etching process of a microbolometer is completed with the application of anisotropic etching process under control of the ECES

technique. However, the design of the used microbolometer failed due to the depletion layer effect explained previously.

11. The problem occurred due to the n-well passivating voltage application to th sidewalls of the pixels were solved with etching a new microbolometer with a back side etching design. The voltage through the side walls was disconnected and the etching was done from back side of the wafer with 6M KOH at 90°C. As a consequence, the pixels of the microbolometer were suspended and the n-well regions under the absorber area were protected.

This research gives above achievements on the ECES technique and its implementation. However, there is still need to study further on some points which can be performed as future work:

1. An investigation about the depletion layer effect under a constant and a controllable illumination can be done. The illumination may decrease the un-etched area which is caused by the depletion layer between n-well and p-substrate.

2. New device fabrications for gyroscopes or pressure sensors can be studied with the implementation of the ECES technique.

3. The low step coverage of the silicon nitride layer deposited in METU-MET facilities can be improved with an optimization of the deposition process variables.

REFERENCES

[1] K.E. Peterson, "Silicon as a mechanical material," *Proceedings of IEEE*, Volume 70, Issue 5, pp. 420–457, 1982.

[2] James D. Plummer, Michael D. Deal and Peter B. Griffin, "Silicon VLSI Technology, Fundamentals, Practice and Modeling," *Prentice Hall, Inc.*, 2000.

[3] Helmut F Wolf, "Silicon Semiconductor Data," *Oxford, New York, Pergamon Press*, 1969.

[4] Kenneth A. Jackson, "Silicon devices: Structures and Processing," *Weinheim: Wiley-VCH*, 1998.

[5] Cory Weber, "Amorphous Silicon Buried-Channel Thin Film Transistors," *IEEE Transactions on Electron Devices*, Vol. 45, No. 2, pp. 447-452, 1998.

[6] Mahmoud Almasri, "Amorphous Silicon Two-Color Microbolometer for Uncooled IR Detection," *IEEE Sensors Journal*, Vol. 6, No. 2, pp. 293- 300, 2006.

[7] Chi-Wen Chen, Ting-Chang Chang, Po-Tsun Liu, Hau-Yan Lu, Kao-Cheng Wang, Chen-Shuo Huang, Chia-Chun Ling, and Tesung-Yuen

Tseng, “High-Performance Hydrogenated Amorphous-Si TFT for AMLCD and AMOLED Applications,” *IEEE Electron Device Letters*, Vol. 26, No. 10, pp. 731- 733, 2005.

[8] Yuping Wang, Roberto Ballarini, Harold Kahn, and Arthur H. Heuer, “Determination of the Growth Strain of LPCVD Polysilicon,” *Journal of Microelectromechanical Systems*, Vol. 14, No. 1, pp. 160- 166, 2005.

[9] H. Seidel, “Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: I. Orientation Dependence and Behavior of Passivation Layers,” *J. Electrochem. Soc*., Vol. 137, No. 11, pp. 3612-3626, 1990.

[10] H. Seidel, “Anisotropic Etching of Crystalline Silicon in Alkaline Solutions: II. Influence of dopants,” *J. Electrochem. Soc*., Vol. 137, No. 11, 1990.

[11] O. Tabata, “Anisotropic Etching of Silicon in TMAH solution,” *Sensors and Materials*, pp.271-283, 2001.

[12] Marc J. Madou, “Fundamentals of Microfabrication: the science of miniaturization,” *CRC Press*, 2002.

[13] SC Chang, “Mesa Structure Formation Using Potassium Hydroxide and Ethylene Diamine Based Etchants,” *IEEE Technical Digest on Solid-State Sensor and Actuator Workshop*, pp. 102-103, 1988.

[14] Chunchie Huang and Khalil Najafi, “Fabrication of Ultrathin p^{++} Silicon Microstructures Using Ion Implantation and Boron Etch-Stop,” *Journal of Microelectromechanical Systems*, Vol. 10, No. 4, pp. 532-537, 2001.

[15] D. Starosvetsky, M. Kovler, and J. Yahalom, "Electrochemical Etching of Silicon in Aqueous Solutions," I, Vol. 3680, pp. 1083-1090, 1999.

[16] Mitsuhiro Shikida, Kazuo Sato, Kenji Tokoro and Daisuke Uchikawa, "Differences in Anisotropic Etching Properties of KOH and TMAH Solutions," *Sensors and Actuators A: Physical*, Vol. 80, Issue 2, pp. 179-188, 2000.

[17] K. Biswas, S. Das, D.K. Maurya, S. Kal and S.K. Lahiri, "Bulk Micromachining of Silicon in TMAH-Based Etchants for Aluminum Passivation and Smooth Surface," *Microelectronics Journal*, Vol. 37, Issue 4, pp. 321-327, 2006.

[18] T. Akin, K. Najafi, R. H. Smoke, and R. M. Bradley, "A Micromachined Silicon Sieve Electrode for Nerve Regeneration Applications," *IEEE Transactions on Biomedical Engineering*, Vol. 41, No. 4, pp. 305-313, 1994.

[19] L. Lin and A. P. Pisano, "Silicon-Processed Microneedles," *IEEE Journal of Microelectromechanical Systems*, Vol. 8, No. 1, pp. 78-84, 1999.

[20] K. J. Ma, " An Active Dissolved Wafer Process for The Fabrication of Integrated Sensors ," *Ph.D. dissertation, Univ. of Michigan, Ann Arbor*, 1994.

[21] Janak Singh, Terence Gan, Ajay Agarwal, Mohanraj and Saxon Liw, "3D Free Space Thermally Actuated Micromirror Device," *Sensors and Actuators A: Physical*, Vol. 123-124, pp. 468-475, 2005.

[22] A. E. H. Klaassen, R. J. Reay, and G. T. A. Kovacs, "Diode-based Thermal RMS Converter with On-Chip Circuitry Fabricated using CMOS Technology," *Sensors and Actuators A, Phys*., Vol. 52, pp. 33-40, 1996.

[23] D. Sabuncuoglu Tezcan, S. Eminoglu, and T. Akin, "A Low-Cost Uncooled Infrared Microbolometer Detector in Standard CMOS Technology," *IEEE Transactions on Electron Devices*, Vol. 50, No. 2, pp. 102-113, 2003.

[24] Erkan Alpman, "Development of Low-cost Uncooled Infrared Detector Arrays in Standard CMOS and SOI-CMOS Processes," *Dissertation for Degree of Master of Science, Middle East Technical University, Dept. of Electrical and Electronics Engineering*, September 2005.

[25] M. Y. Tanrıkulu, "A High Fill Factor CMOS Uncooled Infrared Microbolometer Detector," *Dissertation for the Degree of Master of Science, Middle East Technical University*, September 2002.

[26] Deniz Sabuncuoğlu Tezcan, "A CMOS compatible uncooled infrared detector focal plane array for night vision applications using MEMS Technology," *Dissertation for Degree of Doctor of Philosophy, Middle East Technical University, Dept. of Electrical and Electronics Engineering*, September 2003.

[27] H. Seidel, "The Mechanism of Anisotropic Electrochemical Silicon Etching in Alkaline Solutions," *IEEE Solid-State Sensor and Actuator Workshop*, pp. 86-91, 1990.

[28] Y. Nemirovsky and A. El-Bahar, "The non equilibrium band model of silicon in TMAH and in anisotropic electrochemical alkaline etching solutions," *Sensors and Actuators*, pp. 205–214, 1999.

[29] Agency for Toxic Substances and Disease Registry, ATSDR, http://www.atsdr.cdc.gov/tfacts19.html, Last access date: 16 August 2006.

[30] Paul G. Miney, and Vincent J. Cunnane, "A study of the passivation peak current density for (1 0 0) oriented silicon in tetramethylammonium hydroxide (TMAH): Effect of temperature, concentration and carrier type," *Electrochimica Acta.*, vol. 49, pp. 1009–1018, 2004.

[31] Paul G. Miney, Vincent J. Cunnane, "A study of the chemical breakdown of the anodic oxide formed on (100) oriented silicon in tetramethlyammonium hydroxide (TMAH) solutions," *Electrochimica Acta*, Vol. 48, Issue 11, pp. 1475-1482, 2003.

[32] R.Voss, H.Seidel, and H. Baumgartel, "Light-Controlled, Electrochemical, Anisotropic Etching of Silicon," *Int. Conf. on Solid-State Sensors and Actuators (TRANSDUCERS'91)*, pp.140-143, June 1991.

[33] Ping-Hei Chen, Hsin-Yah Peng, Chia-Ming Hsieh, and Minking K. Chyu, "The characteristic behavior of TMAH water solution for anisotropic etching on both Silicon substrate and SiO_2 layer," *Sensors and Actuators A: Physical*, Volume 93, Issue 2, pp: 132-137, 2001.

[34] Kalpathy B. Sundaram, Arun Vijayakumar and Ganesh Subramanian, "Smooth etching of silicon using TMAH and isopropyl alcohol for

MEMS applications," *Microelectronic Engineering*, Volume 77, Issues 3-4, pp. 230-241, 2005.

[35] Jing Chen, Litian Liu, Zhijian Li, Zhimin Tan, Qianshao Jiang, Huajun Fang, Yang Xu, and Yanxiang Liu, "Study of Anisotropic Etching of (1 0 0) Si with Ultrasonic Agitation," *Sensors and Actuators*, vol. 96,pp. 152–156, 2002.

[36] K. Biswas and S. Kal, "Etch Characteristics of KOH, TMAH and Dual Doped TMAH for Bulk Micromachining of Silicon," *Microelectronics Journal*, vol. 37, pp. 519–525, 2006.

[37] Norio Fujitsuka, Kanae Hamaguchi, Hirofumi Funabashi, Eishi Kawasaki, and Tsuyoshi Fukada, "Silicon anisotropic etching without attacking aluminum with Si and oxidizing agent dissolved in TMAH solution," *Sensors and Actuators A: Physical*, Volume 114, Issues 2-3, pp: 510-515, 2004.

[38] N. H. Tea, V. Milanovic, C. A. Zincke, J. S. Suehle, M. Gaitan, M. Zaghloul, M. E. Geist, "Hybrid Post-Processing Etching for CMOS-Compatible MEMS," *Journal of Microelectromechanical Systems*, Vol. 6, pp. 363-372, 1997.

[39] M. Paranjape, S. Brida, V. Guamieri, F. Giacomozzi, and M. Zen, "Characterization of TMAHW Silicon Etchant Using Ammonium Persulfate as an Oxidizing Agent," *Electrical and Computer Engineering, 1999 IEEE Canadian Conference*, Vol. 3, pp. 1627 – 1631, 1999.

[40] K. Lian, B. Stark, A. M. Gundlach, and A. J. Walton, "Aluminium Passivation for TMAH Based Anisotropic Etching for MEMS Applications," *Electronics Letters*, Vol. 35, No. 15, pp. 1266-1267, 1999.

[41] B Kloeck, S. D. Collins, N. F de Rooij, R. L. Smith, "Study of Electrochemical Etch-Stop for High-Precision Thickness Control of Silicon Membranes," *IEEE Transactions on Electron Devices*, Vol. 36, Issue 4, Part 2, pp. 663 – 669, 1989.

[42] 0.8 μm CMOS Process Parameters, Austrai Micro Systems, 2001.

[43] S. M. Sze, "VLSI Technology," *Mc Graw Hill, Inc*., 1988.

[44] Van der Pauw, "A method of measuring the resistivity and Hall coefficient on Lamellae of Arbitrary Shape," *Philips Technical Review*, Vol. 20, No. 8, pp. 220-224, 1958.

[45] W. R. Runyan, "Semiconductor Measurements and Instrumentation," *Mc Graw Hill, Inc.,* 1975.

[46] Ravi Subrahmanyan, Hisham Z. Massoud, and Richard B. Fair, "Experimental characterization of two dimentional dopant profiles in silicon using chemical staining," *Applied Physics Letters*, Vol 52, No. 25, 1988.

[47] Philtec Technical Manual

[48] Kirt R. Williams and Richard S. Muller, "Etch Rates for Micromachining Processing," *Journal of Microelectromechanical*

Systems, Vol. 5, No. 4, pp. 256-269, 1996.

[49] W. Kern and D.A. Puotinen, "Cleaning Solution Based on Hydrogen Peroxide for use in semiconductor technology," *RCA review*, pp. 187, 1970.

[50] Gary E. McGuire, "Semiconductor Materials and process Technology Handbook," *Noyes Publication*, 1988.

[51] Negative photoresist MAN-1420 datasheet.

[52] Stephen A. Campbell, "The Science and Engineering of Microelectronics Fabrication," *Oxford University Press*, 2001.

[53] Daniel Lapadatu, Gjermund Kittilsland, Martin Nese, Svein M. Nilsen and Henrik Jakobsen, "A model for the etch-stop location on reverse-biased pn junctions," *Sensors and Actuators A: Physical*, Vol. 60, Issues 1-3, pp. 191-196, 1997.

[54] Lars Wallman, Jonas Bengtsson, Nils Danielsen and Thomas Laurell, "Electrochemical Etch-Stop Technique for Silicon Membranes with p- and n-type Regions and Its Application to Neural Sieve Electrodes," *Journal of Micromechanics and Microengineering*, vol. 12, pp. 265-270, 2002.

APPENDICES

A. PROCESS STEPS FOR FABRICATION OF THE ETCH SAMPLES

Step	Process	Specification	Time
1	Prefurnace clean	Standard	
2	Thermal Oxidation	1. Ramp-Up to 1125 °C	
	Field Oxide Growth	2. Dry oxidation under O_2	30 min.
		3. Wet Oxidation under H_2 and O_2	120 min.
		4. Dry oxidation under O_2	20 min.
3	Protect backside	1. Dehydration under N_2, 120°C	30 min.
		2. Primer (HMDS) coating; 500rpm 10 sec. + 4000rpm 30 sec.	
		3. PR (S1813) coating; 500 rpm 10 sec. + 2000rpm 30 sec.	
		4. Softbake at 95°C	30 sec.
		5. Hardbake under N_2, 120°C	20 min.
4	Lithography	1. Dehydration under N_2, 120° C	30 min.
	N-well diffusion openings	2. Primer (HMDS) coating; 500rpm 10 sec. + 4000rpm 30 sec.	
		3. PR (S1813) coating; 500 rpm 10 sec. + 2000rpm 30 sec.	
		4. Softbake at 95°C	30 sec

		5. Align & Expose	
		6. Develop with MF-319	
		7. Rinse with DI H_2O	
		8. Dry by N_2	
		9. Hardbake under N_2 ,120°C	30 min.

5	Oxide etch	1. BHF; NH_4F (%40) : HF (%49) = 7:1	7.5 min
		2. Rinse with DI H_2O	
		3. Dry by N_2	

6	Strip photoresist	1. SVC-175 at 82ºC	15 min.
		2. Rinse with DI H_2O	
		3. Dry by N_2	

7	Prefurnace clean	1. HF : DI H_2O = 1: 4	30 sec.
		2. Rinse with DI H_2O	
		3. Dry by N_2	

8	N+ pre-deposition	1. Ramp-Up to 805 °C	
		2. Flow-1 : N_2, Low O_2	10 min.
		3. Flow-2 : N_2, Low O_2 $POCl_3$ Purge	2 min.
		4. Flow-3 : N_2, Low O_2, $POCl_3$	10 min.
		5. Flow-4 : N_2, Low O_2	10 min.

9	N+ drive-in	1. Ramp-Up to 1130 °C	
		2. Flow : H_2, O_2	60 min.

10	Lithography	1. Dehydration under N_2, 120°C	30 min.
	p+ diffusion openings	2. Primer (HMDS) coating; 500rpm 10 sec. + 4000rpm 30 sec.	
		3. PR (S1813) coating; 500 rpm 10 sec. + 2000rpm 30 sec.	
		4. Softbake at 95°C	30 sec.
		5. Align & Expose	

		6. Develop with MF-319	
		7. Rinse with DI H_2O	
		8. Dry by N_2	
		9. Hardbake under N_2 ,120°C	30 min.

11	Oxide etch	1. BHF; NH_4F (%40): HF (%49) = 7:1	14 min.
		2. Rinse with DI H_2O	
		3. Dry by N_2	

12	Strip photoresist	1. SVC-175 at 80ºC	15 min.
		2. Rinse with DI H_2O	
		3. Dry by N_2	

13	Prefurnace clean	1. HF : DI H_2O = 1:4	30 sec.
		2. Rinse with DI H_2O	
		3. Dry by N_2	

14	P+ pre-deposition	1. Ramp-Up to 1000 °C	
	Semi-deep boron diffusion	2. Flow-1 : N_2, Low O_2	5 min
		3. Flow-2 : N_2, Low O_2 BBr_3 Purge	2 min.
		4. Flow-3 : N_2, Low O_2, BBr_3	15 min.
		5. Flow-4 : N_2 , O_2.	5 min

15	LTO	1. Ramp-Up to 700°C	
		2. Flow-1 : H_2, O_2	30 min.

16	Oxide Etch	1. BHF; NH_4F (%40) : HF (%49) = 7:1	30 min
		2. Rinse with DI H_2O	

17	Oxidation (Drive-in)	1. Ramp-Up to 1000 °C	
		2. Flow-1 : O_2	6.5 min
		3. Flow-2 : H_2, O_2	25 min
		4. Flow-3 : O_2	5 min
		5. Measure oxide thickness 2000-2100 Å	

18	Lithography	1. Dehydration, N_2, 120°C	30 min
	Contact opening	2. Primer(HMDS), 500rpm 10 sec. + 4000rpm 20 sec.	
		3. S1813 PR, 500rpm 10 sec. + 4000rpm 20 sec.	
		4. Softbake 95°C, N_2	30 min.
		5. Align & Expose	
		6. Develop, MF-319	40sec.
		7. Rinse with DI H_2O	3 min.
		8. Dry by N_2	
		9. Hardbake 120°C	30 min.

19	Oxide etch	1. BHF; NH_4F%40 : HF%49, 7:1	14 min.
		2. Rinse with DI H_2O	
		3. Dry by N_2	

20	Strip photoresist	1. SVC-175, 80ºC	15 min.
		2. Rinse with DI H_2O	
		3. Dry by N2	

21	Aluminum Deposition	Transfer pressure : 3.e-6 Temp : None	600sec
	Sputter	1. Argon : 10sccm, Pressure : 1.1e-2, Rate : 0.6 Å/sec.	200 sec.
		2. Argon : 3.8sccm, Pressure : 4.9e-3, Rate : 1.1 Å/sec.	400 sec.

22	Lithography	1. Dehydration, N_2, 120°C	30 min
	Metallization layer	2. Primer(HMDS), 500rpm 10sec + 2000rpm 30 sec.	
		3. S1813 PR, 500rpm 10 sec. + 4000rpm 30 sec.	
		4. Soft-bake 115°C	60 sec.
		5. Align & Expose,	
		6. Develop, MF-319.	

		7. Rinse with DI H_2O	
		8. Dry by N_2	
		9. Oxygen Plasma 150mTorr, 300W.	2 min.
		10. Hardbake 120°C	30 min.

23	Al etch	Wet etching at 25°with High agitation	3,5 min

24	Strip photoresist	SVC-175	5 min

25	Aluminum annealling	Annealing at 450ºC	30 min

26	Nitride deposition	4000Å MF SiN	

27	Lithography	1. Dehydration, N_2, 120°C	30 min.
	passivation layer	2. Primer(HMDS), 500rpm 10 sec. + 2000rpm 30 sec.	
		3. S1813 PR, 500rpm 7 sec. + 2000rpm 30 sec.	
		4. Soft-bake 115°C	70 sec.
		5. Align & Expose	
		6. Develop, MF-319	65 sec.
		7. Rinse with DI H_2O	
		8. Dry by N_2	
		9. Oxygen Plasma 150mTorr, 300W.	2 min.
		10. Hard-bake 120°C	30 min

28	SiN RIE		1 min 21 sec.

27	SiO RIE		65 sec.

28	Strip photoresist	oxygen plasma	45 min.

29	Dicing		

B. SUPREM SIMULATION OF THE THERMAL PROCESSES OF ETCH SAMPLES

The code starts with wafer property definition and graphic axis definition. The oxide growth, the diffusion parameters depend on wafer type.

```
TITL    -- METU_ECESv1
GRID    DYSI=0.04, DPTH=12, YMAX=12
SUBS    ORNT=100, ELEM=B, CONC=5E14
PLOT    WIND=12, TOTL=TRUE, IDIV=FALSE

PRINT   HEAD=YES
PLOT    WIND=12, TOTL=TRUE, IDIV=FALSE
```

Modes are written according to the device parameters. These values are optimized in relation to the previous process results on those devices. Oxidation steps and diffusion steps differ as the time passes; the wafer surface oxidizes; the implant concentration of the wafer surface changes. These changes are reflected to the modes thus for each oxygen flow inside the tube, each high temperature process affecting another process variable is declared as a mode. MPH declares phosphorus diffusion, MBO declares boron diffusion, DRY declares dry oxidation and WET declares wet oxidation.

```
MODE    NAME=MPH1, DSXD=8E11, DOX0=2E11, SEG0=4
MODE    NAME=MPH2, DOX0=2.51939E9
MODE    NAME=MBO2, DSXD=3E11, DOX0=4.56E7, SEG0=10
MODE    NAME=MBO1, SEG0=110
MODE    NAME=MBO4, DSXD=800, DOX0=1.896E6, SEG0=1126
```

```
MODE    NAME=DRY3, LRTE=1.04838E5, PRES=0.10924
MODE    NAME=DRY1, LRTE=1.89E5
MODE    NAME=WET1, PRTE=4.14
MODE    NAME=WET5, PRTE=2.84
MODE    NAME=DRY4, PRTE=16
```

The n-well diffusion is defined as following. Temperature, time, type of element which is diffused, concentration of the element given for diffusion and model of the diffusion is written. The drive-in process modes directly are affected from the pre deposition process. In drive-in, both push and pull of the wafers through the tube are considered as dry oxidation and their effect is also included.

```
COMM    NWELL DEPOSITION
STEP    TYPE=OXID, TIME=3, TEMP=800, MODL=DRY0
STEP    TYPE=PDEP, ELEM=P, CONC=1E19, TIME=5, TEMP=800, MODL=MPH1
STEP    TYPE=OXID, TIME=5, TEMP=800, MODL=DRY4
COMM    NWELL DRIVE IN
STEP    TYPE=OXID, TIME=10, TEMP=1130, MODL=DRY1, MODL=MPH2
STEP    TYPE=OXID, TIME=200, TEMP=1130, MODL=WET1, MODL=MPH2
STEP    TYPE=OXID, TIME=7.5, TEMP=1130, MODL=DRY1, MODL=MPH2
```

The oxide layer occurred after drive-in process is stripped with an etching step.

```
STEP    TYPE=ETCH, TEMP=25
```

Boron diffusion is done over the phosphorus diffused area. Therefore in both pre-deposition and drive-in processes, a mode for phosphorus diffusion is added.

```
COMM    P++ DIFFUSION
STEP    TYPE=OXID, TIME=3, TEMP=1000, MODL=NIT0
STEP    TYPE=PDEP, ELEM=B, CONC=1.5E20, TIME=40, TEMP=1000, MODL=MBO0
        + MODL=MPH2
STEP    TYPE=OXID, TIME=3, TEMP=1000, MODL=DRY4, MODL=MPH2
```

LTO was done to ease the boron silicate removal which was occurred during boron diffusion.

```
COMM    LTO
STEP    TYPE=OXID, TIME=3, TEMP=700, MODL=DRY1
STEP    TYPE=OXID, TIME=30, TEMP=700, MODL=WET1
STEP    TYPE=OXID, TIME=3, TEMP=700, MODL=DRY1
```

The silicate layer was removed here

```
STEP    TYPE=ETCH, TEMP=25
```

The drive-in process of the boron diffusion was also the oxidation process for contact openings.

```
COMM    OXIDATION FOR CONTACT
STEP    TYPE=OXID, TIME=3, TEMP=1000, MODL=DRY0, MODL=MPH2,MODL=MBO4
STEP    TYPE=OXID, TIME=45, TEMP=1000, MODL=WET5
STEP    TYPE=OXID, TIME=5, TEMP=1000, MODL=DRY1
END
```

SUPREM SIMULATION RESULTS

```
NWELL DEPOSITION
STEP #  1
OXIDE THICKNESS     =    4.3057E-03 MICRONS
LINEAR    OXIDE GROWTH RATE =  1.581271E-03 MICRONS/MINUTE
PARABOLIC OXIDE GROWTH RATE =  6.690619E-05 MICRONS!2/MINUTE
OXIDE GROWTH PRESSURE       =   1.00000     ATMOSPHERES

                    I  OXIDE           I  SILICON         I                    I  SURFACE
                    I  DIFFUSION       I  DIFFUSION      I  SEGREGATION    I  TRANSPORT
                    I  COEFFICIENT  I  COEFFICIENT  I  COEFFICIENT     I  COEFFICIENT
 ---------------------------------------------------------------------------------------------------------------------
 BORON              I   1.29678E-09     I   3.66144E-05     I   .16589           I    3.67548E-04
SURFACE CONCENTRATION =  2.969953E+14 ATOMS/CM!3
```

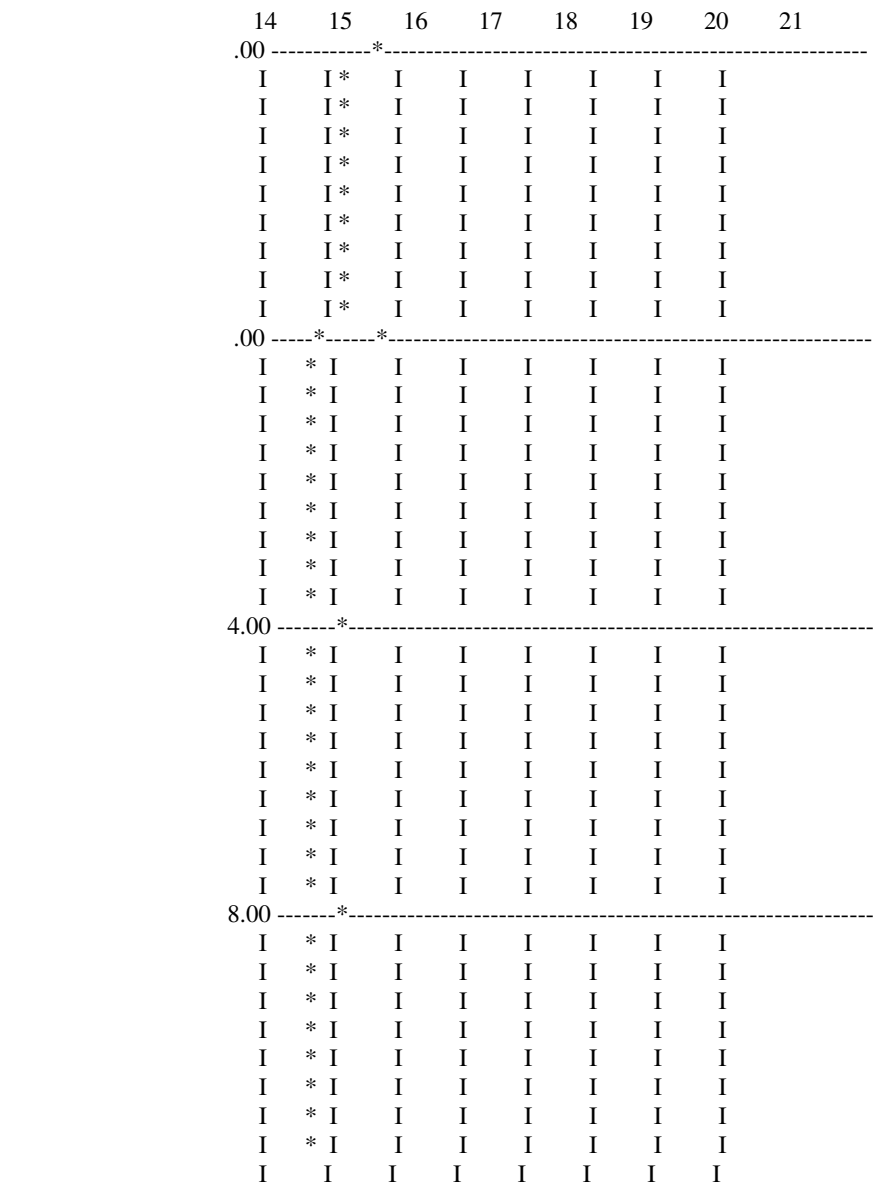
```
  JUNCTION DEPTH      I     SHEET RESISTANCE
 ---------------------------I-------------------------
                            I     21131.7     OHMS/SQUARE
```

NWELL DEPOSITION

STEP = 1

TIME =   3.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



NWELL DEPOSITION

STEP # 2

GASEOUS PREDEPOSITION

TOTAL STEP TIME = 5.0 MINUTES

INITIAL TEMPERATURE = 800.000 DEGREES C.

OXIDE THICKNESS = 4.3057E-03 MICRONS

PREDEPOSITION IMPURITY = PHOSPHORUS

GAS CONC. AT INTERFACE = 1.000000E+19 ATOMS/CC

	I OXIDE I DIFFUSION I COEFFICIENT	I SILICON I DIFFUSION I COEFFICIENT	I I SEGREGATION I COEFFICIENT	I SURFACE I TRANSPORT I COEFFICIENT I
BORON	I 5.00901E-11	I 2.72104E-07	I 6.84716E-02	I 3.73363E-05 I
PHOSPHORUS	I 7.30858E-06	I 5.18178E-06	I 4.0000	I 1.0000 I

SURFACE CONCENTRATION = -3.441887E+18 ATOMS/CM!3

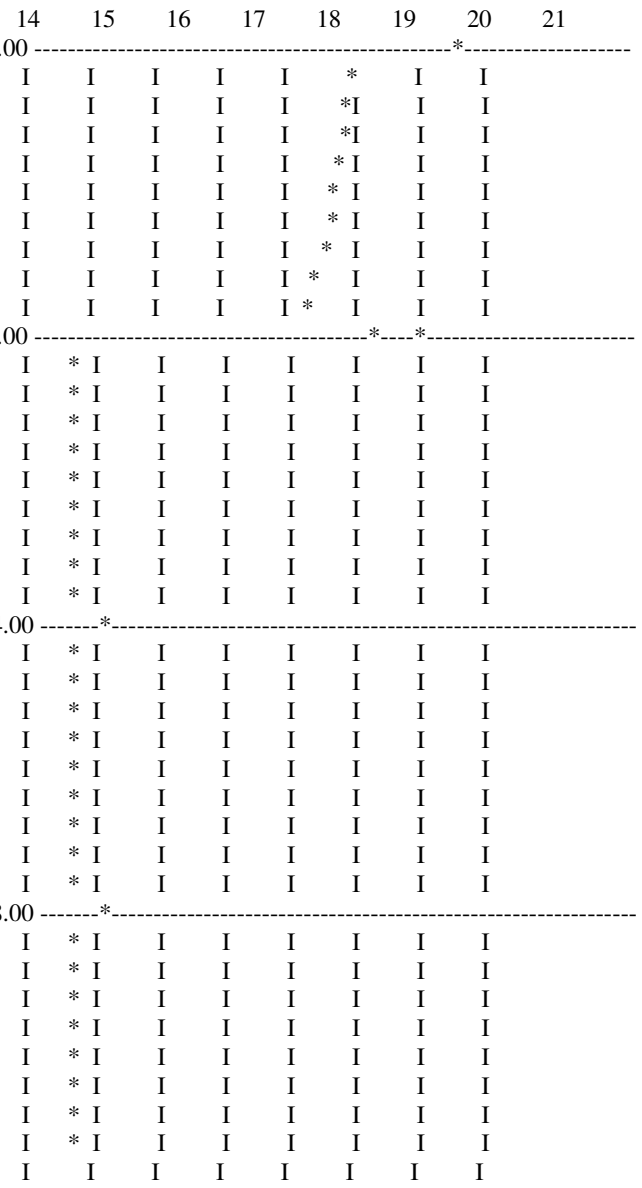
JUNCTION DEPTH	I	SHEET RESISTANCE
7.983582E-02 MICRONS	I 5381.76 OHMS/SQUARE	I 21237.2 OHMS/SQUARE

NWELL DEPOSITION

STEP = 2

TIME = 5.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



NWELL DEPOSITION

STEP # 3

OXIDATION IN DRY OXYGEN

TOTAL STEP TIME = 5.0 MINUTES

INITIAL TEMPERATURE = 900.000 DEGREES C.

OXIDE THICKNESS = 1.0477E-02 MICRONS

LINEAR OXIDE GROWTH RATE = 1.581271E-03 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 8.317786E-05 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = 1.00000 ATMOSPHERES

	I OXIDE I DIFFUSION I COEFFICIENT	I SILICON I DIFFUSION I COEFFICIENT	I I SEGREGATION I COEFFICIENT	I SURFACE I TRANSPORT I COEFFICIENT I
BORON	I 1.29678E-09	I 3.66144E-05	I .16589	I 3.67548E-04 I
PHOSPHORUS	I 1.84051E-04	I 1.51228E-04	I 4.0000	I 2.54185E-03 I

SURFACE CONCENTRATION = -1.922028E+18 ATOMS/CM!3

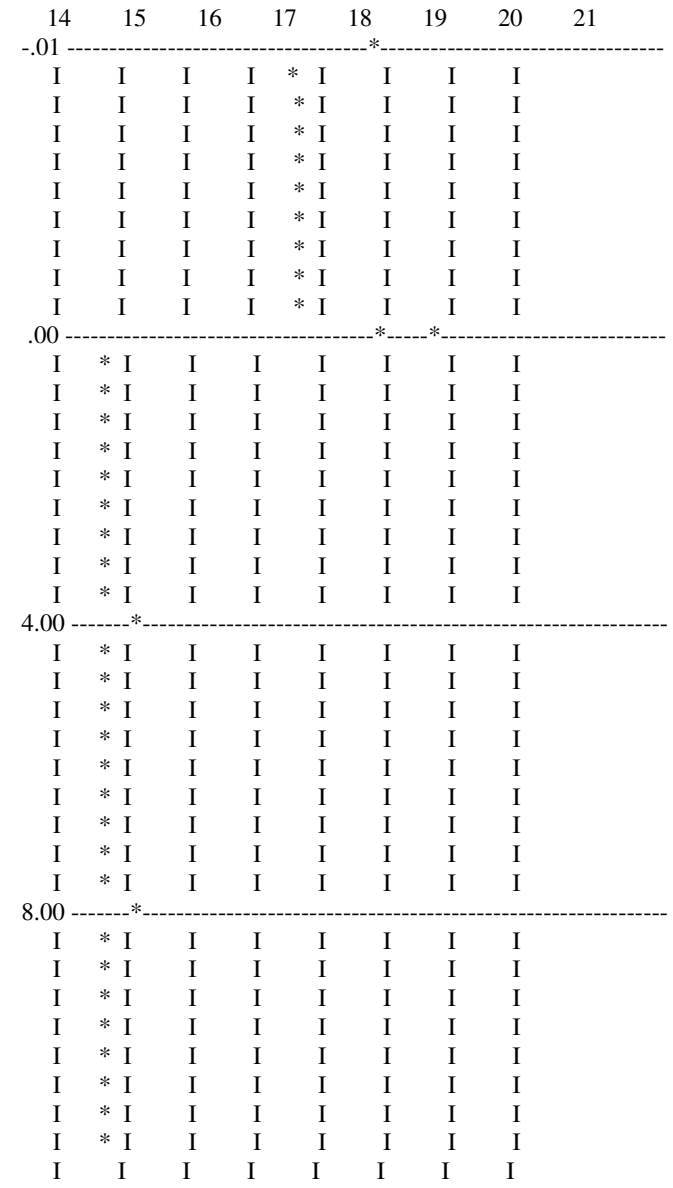
JUNCTION DEPTH	I	SHEET RESISTANCE
.224537 MICRONS	I	2785.96 OHMS/SQUARE I 21534.6 OHMS/SQUARE

NWELL DEPOSITION

STEP = 3

TIME = 5.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



NWELL DRIVE IN

STEP # 4

OXIDATION IN DRY OXYGEN

TOTAL STEP TIME = 10.0 MINUTES

INITIAL TEMPERATURE = 1130.00 DEGREES C.

OXIDE THICKNESS = 6.0085E-02 MICRONS

LINEAR OXIDE GROWTH RATE = 1.238174E-02 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 4.916039E-04 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = 1.00000 ATMOSPHERES

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT I
BORON	I 3.96866E-07	I 2.12144E-03	I .78674	I 2.05306E-02 I
PHOSPHORUS	I 6.75858E-04	I 2.96996E-03	I 10.000	I 6.40444E-02 I

SURFACE CONCENTRATION = -2.577700E+17 ATOMS/CM!3

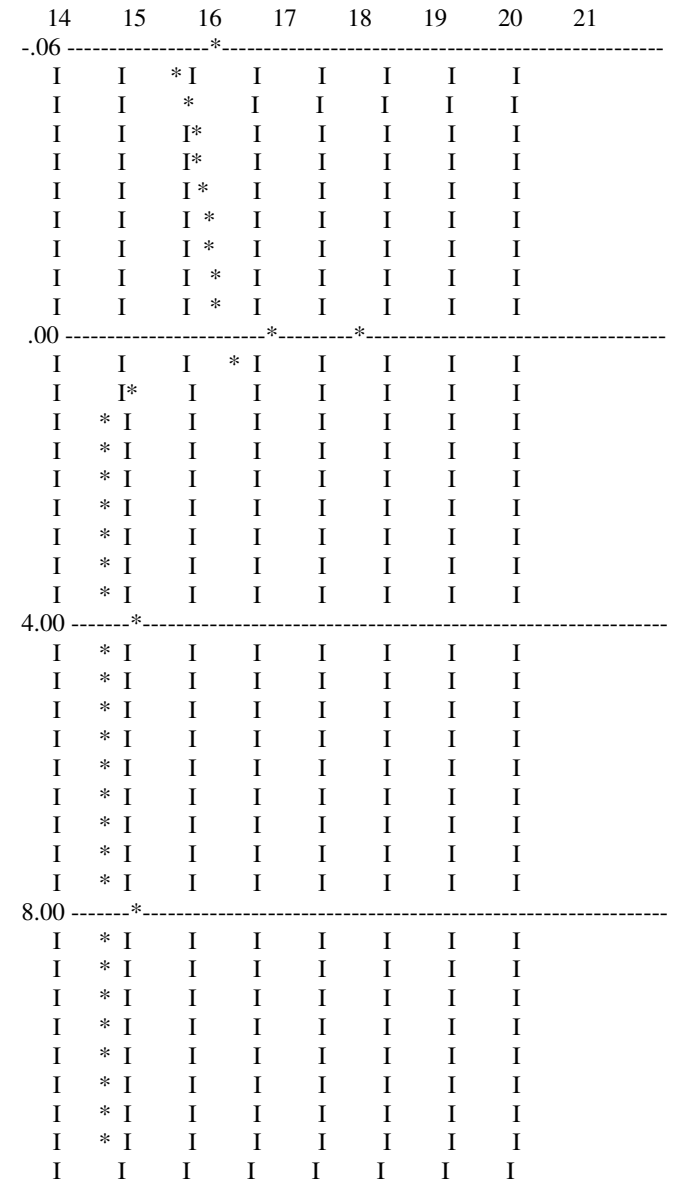
JUNCTION DEPTH	I	SHEET RESISTANCE
.925602 MICRONS	I 1446.19 OHMS/SQUARE	I 23123.0 OHMS/SQUARE

NWELL DRIVE IN

STEP = 4

TIME = 10.0 MINUTES.

DEPTH vs.CONCENTRATION (LOG ATOMS/CC) (UM)



NWELL DRIVE IN

STEP # 5

OXIDATION IN WET OXYGEN

TOTAL STEP TIME = 200.0 MINUTES

INITIAL TEMPERATURE = 1130.00 DEGREES C.

OXIDE THICKNESS = 1.008 MICRONS

LINEAR OXIDE GROWTH RATE = 5.899357E-02 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 5.504673E-03 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = .842105 ATMOSPHERES

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT I
BORON	I 3.96866E-07	I 2.12144E-03	I .78674	I 2.05306E-02 I
PHOSPHORUS	I 6.75858E-04	I 2.96996E-03	I 10.000	I 6.40444E-02 I

SURFACE CONCENTRATION = -5.528926E+16 ATOMS/CM!3

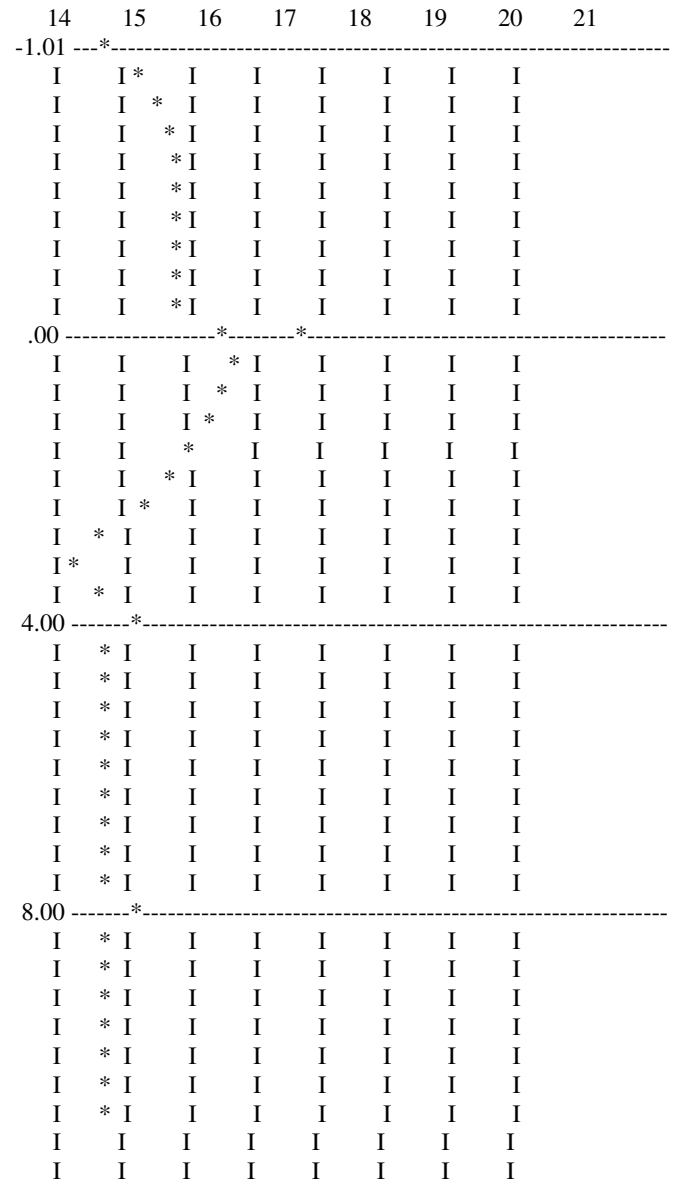
JUNCTION DEPTH	I	SHEET RESISTANCE
3.04246 MICRONS	I 1221.79 OHMS/SQUARE	I 31011.0 OHMS/SQUARE

NWELL DRIVE IN

STEP = 5

TIME = 200.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



NWELL DRIVE IN

STEP # 6

OXIDATION IN DRY OXYGEN

TOTAL STEP TIME = 7.5 MINUTES

INITIAL TEMPERATURE = 1130.00 DEGREES C.

OXIDE THICKNESS = 1.010 MICRONS

LINEAR OXIDE GROWTH RATE = 1.238174E-02 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 4.916039E-04 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = 1.00000 ATMOSPHERES

	I OXIDE I DIFFUSION I COEFFICIENT	I SILICON I DIFFUSION I COEFFICIENT	I SEGREGATION I COEFFICIENT	I SURFACE I TRANSPORT I COEFFICIENT I
BORON	I 3.96866E-07	I 2.12144E-03	I .78674	I 2.05306E-02 I
PHOSPHORUS	I 6.75858E-04	I 2.96996E-03	I 10.000	I 6.40444E-02 I

SURFACE CONCENTRATION = -5.234899E+16 ATOMS/CM!3

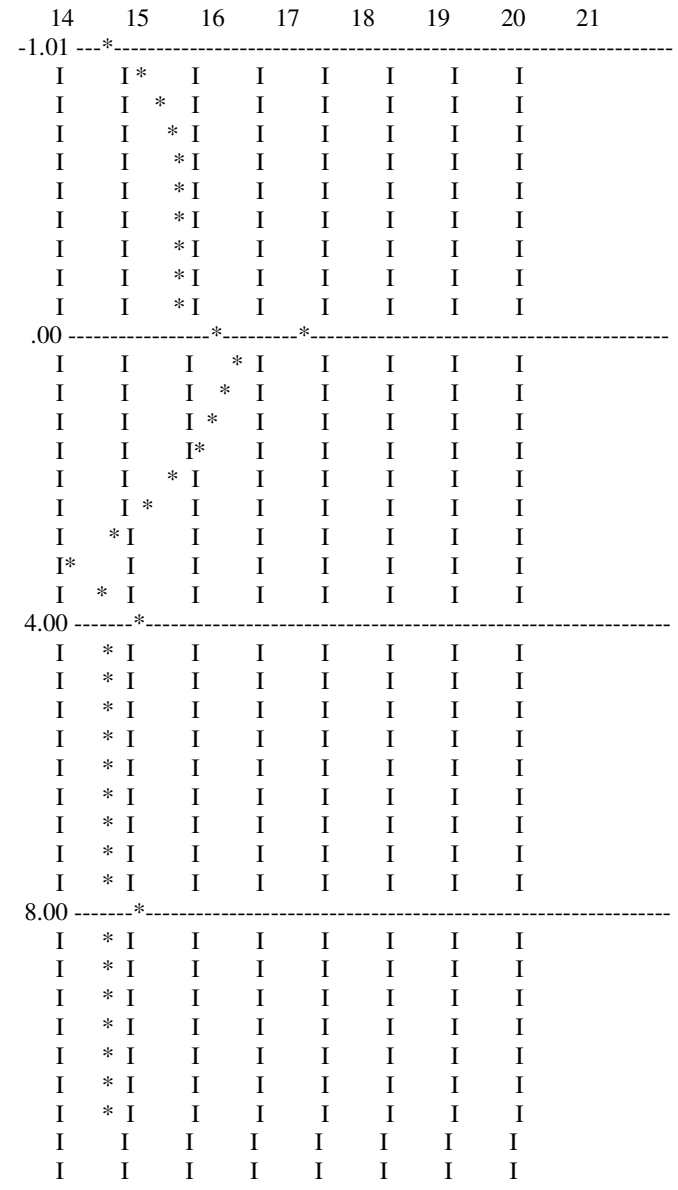
JUNCTION DEPTH	SHEET RESISTANCE
3.09650 MICRONS	I 1214.96 OHMS/SQUARE I 31211.8 OHMS/SQUARE

NWELL DRIVE IN

STEP = 6

TIME = 7.5 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



NWELL DRIVE IN

STEP # 7

ETCH STEP

ETCH TEMPERATURE = 25.0 DEGREES C.

ETCH TIME = .0 MINUTES

ETCH RATE = .0000 MICRONS/MINUTE

OXIDE THICKNESS = .0000 MICRONS

SURFACE CONCENTRATION = -5.234899E+16 ATOMS/CM!3

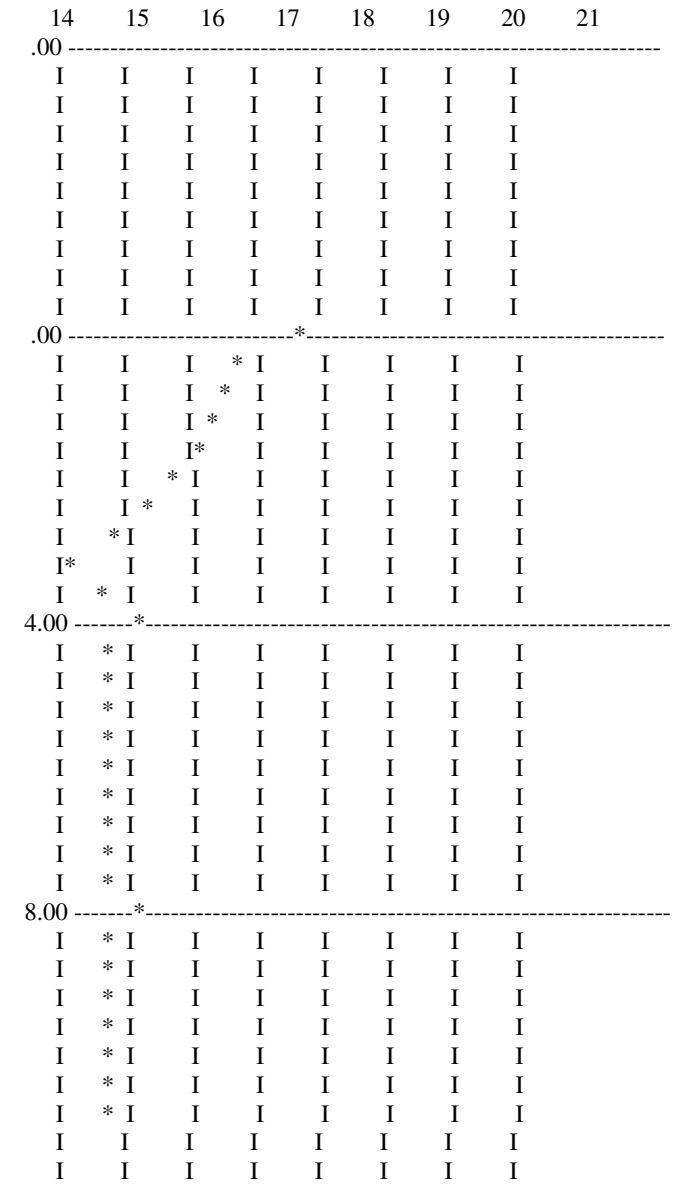
JUNCTION DEPTH	I	SHEET RESISTANCE
3.09650 MICRONS	I	1214.96 OHMS/SQUARE I 31211.8 OHMS/SQUARE

NWELL DRIVE IN

STEP = 7

TIME = .0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



P++ DIFFUSION

STEP # 8

OXIDATION IN DRY OXYGEN

TOTAL STEP TIME = 3.0 MINUTES

INITIAL TEMPERATURE = 800.000 DEGREES C.

OXIDE THICKNESS = 7.4431E-04 MICRONS

LINEAR OXIDE GROWTH RATE = 2.502507E-04 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 2.153168E-05 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = 1.00000 ATMOSPHERES

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT I
BORON	I 5.00901E-11	I 6.63569E-06	I 6.84716E-02	I 3.73363E-05 I
PHOSPHORUS	I 9.20658E-08	I 2.69323E-07	I 10.000	I 4.05997E-04 I

SURFACE CONCENTRATION = -5.276573E+16 ATOMS/CM!3

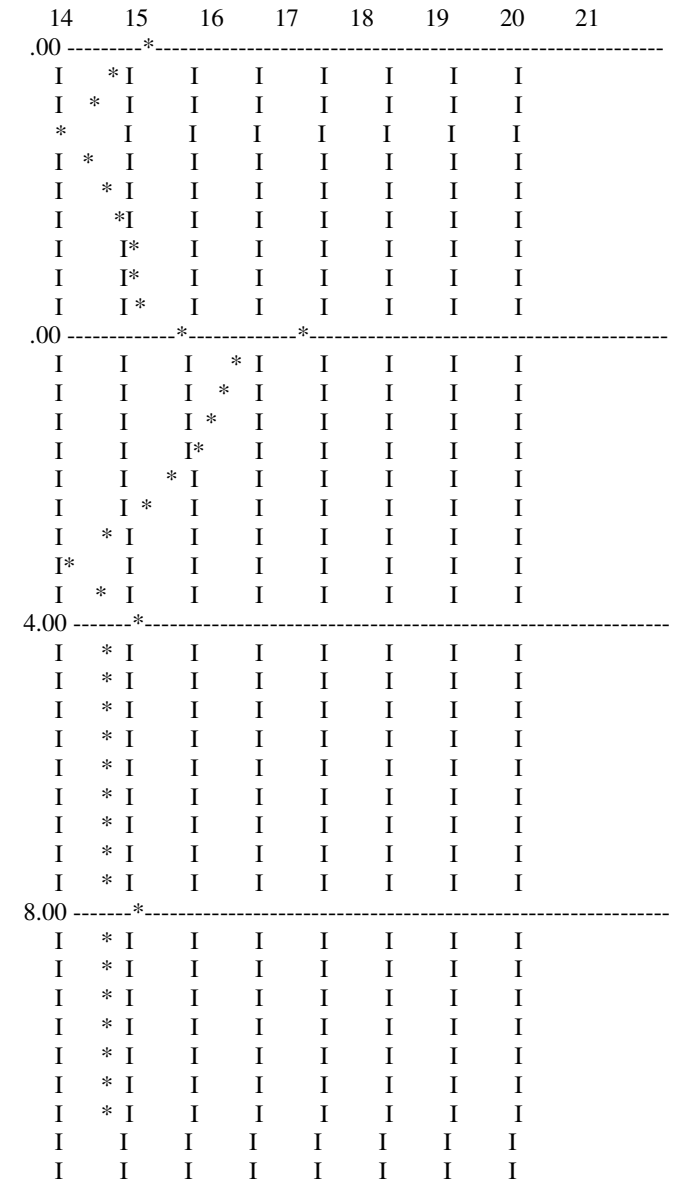
JUNCTION DEPTH	SHEET RESISTANCE
3.09617 MICRONS	I 1215.10 OHMS/SQUARE I 31212.4 OHMS/SQUARE

P++ DIFFUSION

STEP = 8

TIME = 3.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



P++ DIFFUSION

STEP # 9

GASEOUS PREDEPOSITION

TOTAL STEP TIME = 10.0 MINUTES

INITIAL TEMPERATURE = 780.000 DEGREES C.

OXIDE THICKNESS = 7.4431E-04 MICRONS

PREDEPOSITION IMPURITY = BORON

GAS CONC. AT INTERFACE = 1.000000E+20 ATOMS/CC

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT I
BORON	I 2.42619E-11	I 1.34653E-07	I 5.62203E-02	I 1.0000 I
PHOSPHORUS	I 4.48693E-08	I 1.27015E-07	I 10.000	I 2.69800E-04 I

SURFACE CONCENTRATION = -5.264634E+16 ATOMS/CM!3

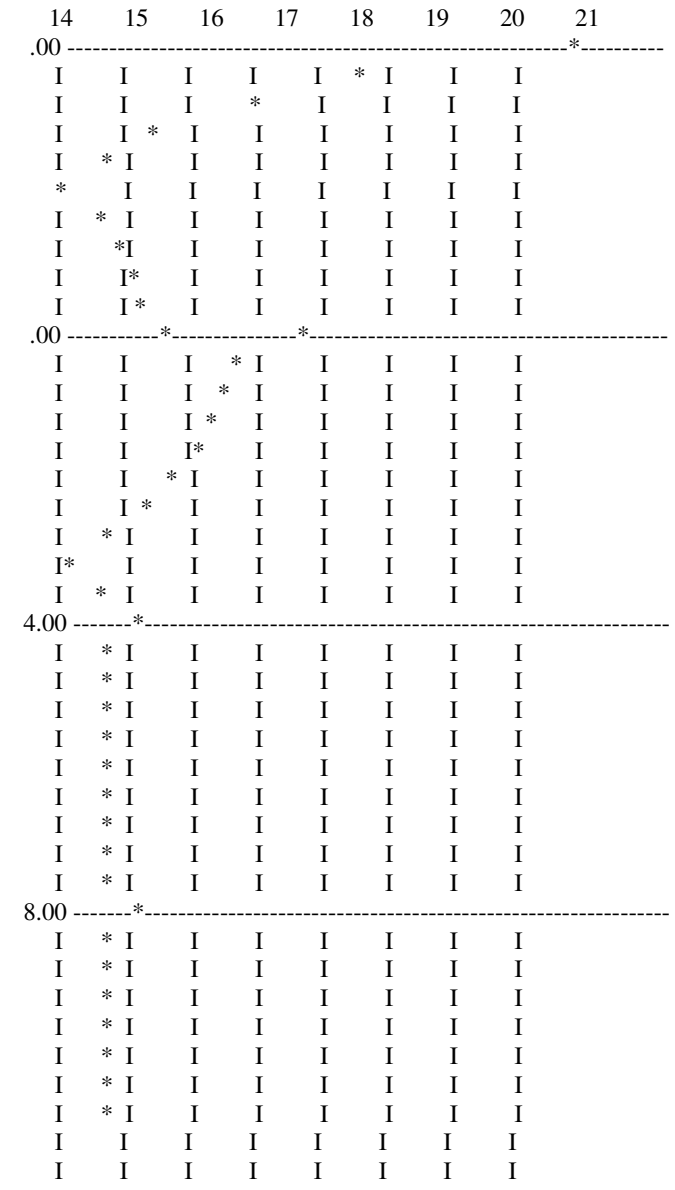
JUNCTION DEPTH	I	SHEET RESISTANCE
3.09617 MICRONS	I 1215.13 OHMS/SQUARE	I 31212.4 OHMS/SQUARE

P++ DIFFUSION

STEP = 9

TIME = 10.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



P++ DIFFUSION

STEP # 10

OXIDATION IN DRY OXYGEN

TOTAL STEP TIME = 3.0 MINUTES

INITIAL TEMPERATURE = 800.000 DEGREES C.

OXIDE THICKNESS = 1.4798E-03 MICRONS

LINEAR OXIDE GROWTH RATE = 2.502507E-04 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 2.676821E-05 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = 1.00000 ATMOSPHERES

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT I
BORON	I 5.00901E-11	I 6.63569E-06	I 6.84716E-02	I 3.73363E-05 I
PHOSPHORUS	I 9.20658E-08	I 2.69323E-07	I 10.000	I 4.05997E-04 I

SURFACE CONCENTRATION = -5.335560E+16 ATOMS/CM!3

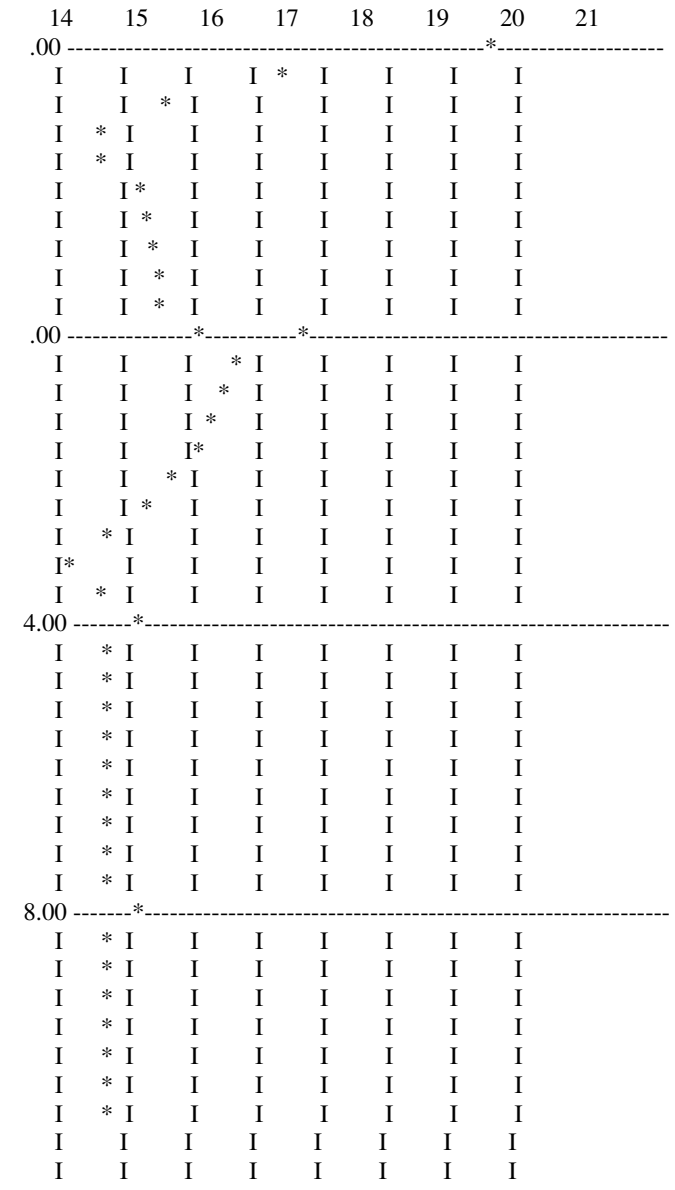
JUNCTION DEPTH	I	SHEET RESISTANCE
3.09585 MICRONS	I	1215.26 OHMS/SQUARE I 31212.8 OHMS/SQUARE

P++ DIFFUSION

STEP = 10

TIME = 3.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



LTO

STEP # 11

OXIDATION IN DRY OXYGEN

TOTAL STEP TIME = 3.0 MINUTES

INITIAL TEMPERATURE = 700.000 DEGREES C.

OXIDE THICKNESS = 1.7170E-03 MICRONS

LINEAR OXIDE GROWTH RATE = 8.290955E-05 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 5.489036E-06 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = 1.00000 ATMOSPHERES

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT I
BORON	9.91334E-13	9.79088E-07	2.35628E-02	2.37047E-06
PHOSPHORUS	1.88384E-09	4.61323E-09	10.000	4.44810E-05

SURFACE CONCENTRATION = -5.362569E+16 ATOMS/CM!3

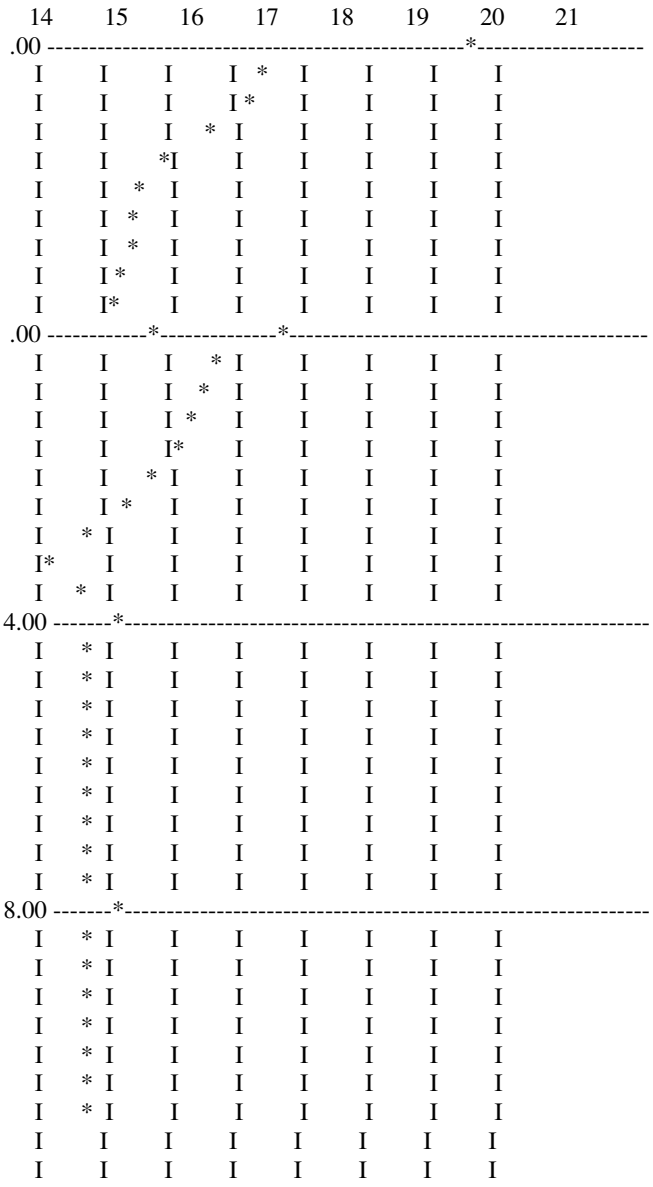
JUNCTION DEPTH	SHEET RESISTANCE
3.09575 MICRONS	1215.29 OHMS/SQUARE
	31212.9 OHMS/SQUARE

LTO

STEP = 11

TIME = 3.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC) (UM)



LTO

STEP # 12

OXIDATION IN WET OXYGEN

TOTAL STEP TIME = 30.0 MINUTES

INITIAL TEMPERATURE = 700.000 DEGREES C.

OXIDE THICKNESS = 2.7041E-03 MICRONS

LINEAR OXIDE GROWTH RATE = 3.290579E-05 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 3.182749E-04 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = .842105 ATMOSPHERES

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT I
BORON	I 9.91334E-13 I	9.79088E-07 I	2.35628E-02 I	2.37047E-06 I
PHOSPHORUS	I 1.88384E-09 I	4.61323E-09 I	10.000 I	4.44810E-05 I

SURFACE CONCENTRATION = -5.458129E+16 ATOMS/CM!3

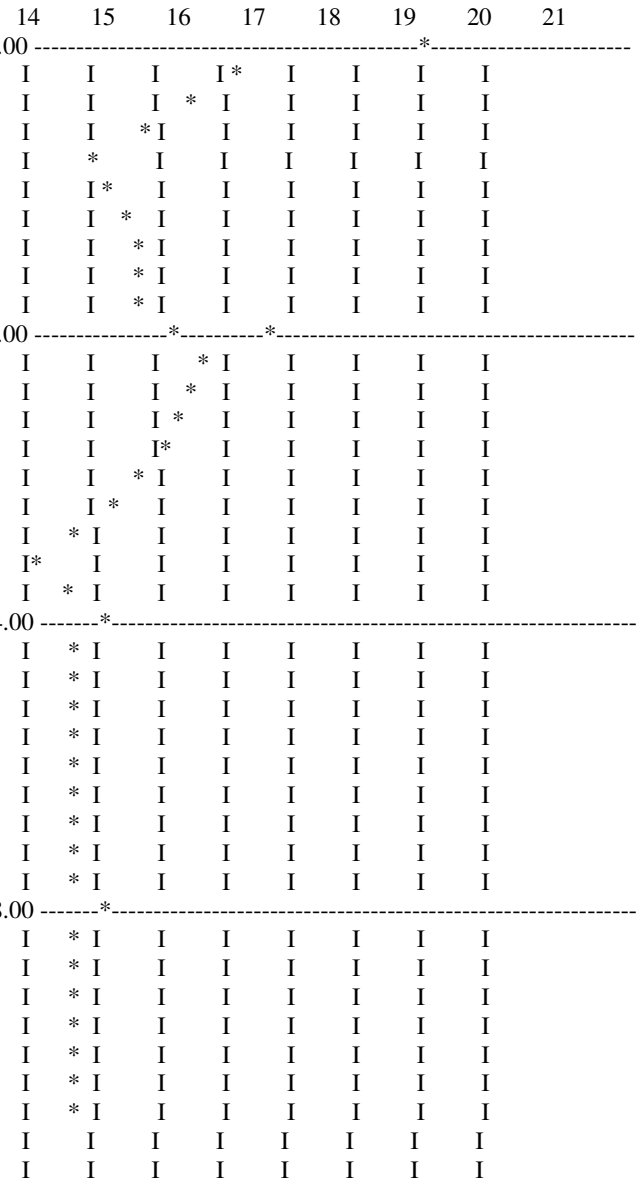
JUNCTION DEPTH	I	SHEET RESISTANCE
3.09531 MICRONS	I	1215.47 OHMS/SQUARE
	I	31213.7 OHMS/SQUARE

LTO

STEP # 12

TIME = 30.0 MINUTES.

DEPTH vs.CONCENTRATION (LOG ATOMS/CC)



LTO

STEP # 13

OXIDATION IN DRY OXYGEN

TOTAL STEP TIME = 3.0 MINUTES

INITIAL TEMPERATURE = 700.000 DEGREES C.

OXIDE THICKNESS = 2.9333E-03 MICRONS

LINEAR OXIDE GROWTH RATE = 8.290955E-05 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 5.489036E-06 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = 1.00000 ATMOSPHERES

	I OXIDE I DIFFUSION I COEFFICIENT	I SILICON I DIFFUSION I COEFFICIENT	I SEGREGATION I COEFFICIENT	I SURFACE I TRANSPORT I COEFFICIENT I
BORON	9.91334E-13	9.79088E-07	2.35628E-02	2.37047E-06
PHOSPHORUS	1.88384E-09	4.61323E-09	10.000	4.44810E-05

SURFACE CONCENTRATION = -5.479640E+16 ATOMS/CM!3

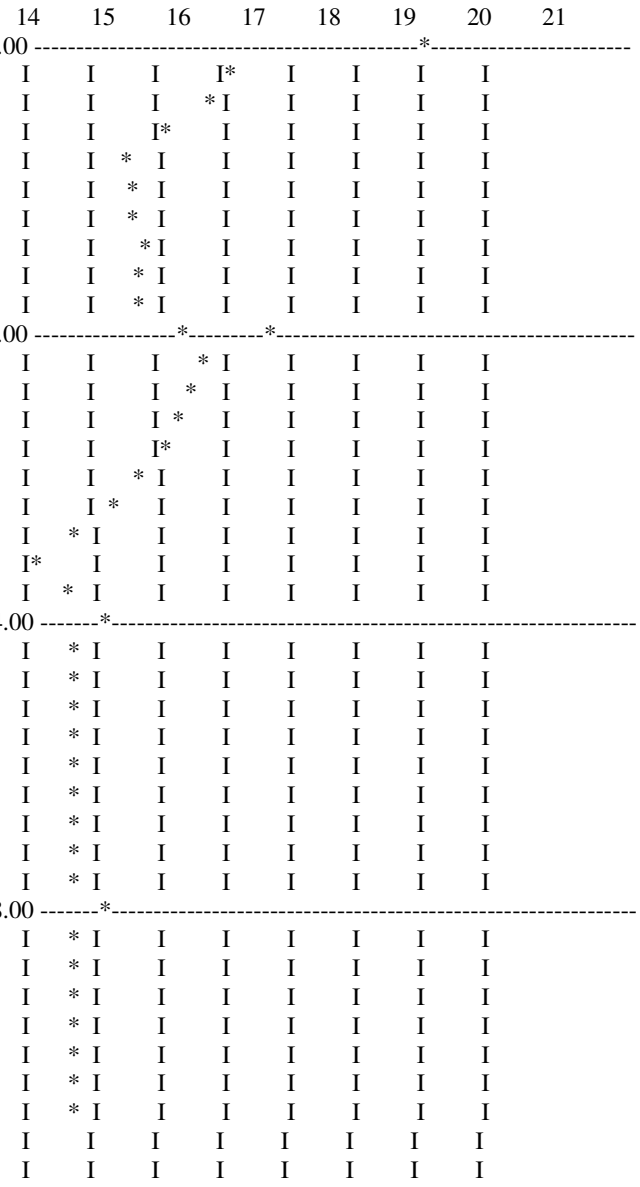
JUNCTION DEPTH	SHEET RESISTANCE
3.09521 MICRONS	1215.52 OHMS/SQUARE
	31213.8 OHMS/SQUARE

LTO

STEP #13

TIME = 3.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC)



LTO

STEP # 14

ETCH STEP

ETCH TEMPERATURE = 25.0 DEGREES C.

ETCH TIME = .0 MINUTES

ETCH RATE = .0000 MICRONS/MINUTE

OXIDE THICKNESS = .0000 MICRONS

SURFACE CONCENTRATION = -5.479640E+16 ATOMS/CM!3

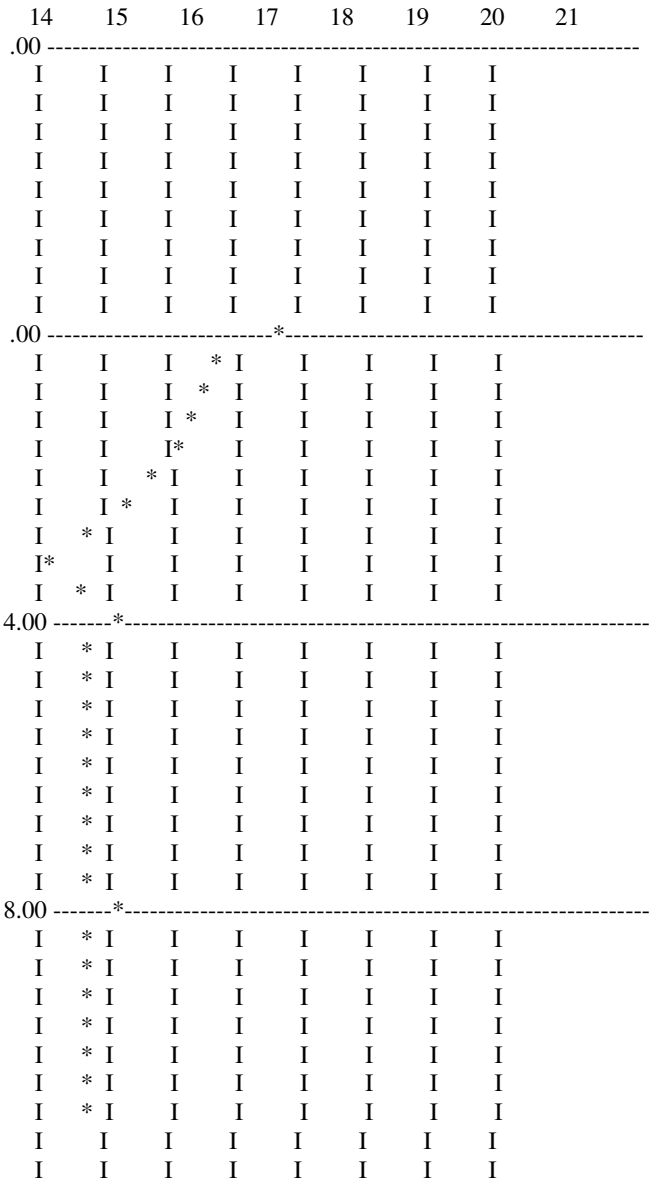
JUNCTION DEPTH	I	SHEET RESISTANCE
3.09521 MICRONS	I	1215.52 OHMS/SQUARE
	I	31213.8 OHMS/SQUARE

LTO

STEP #14

TIME 0 MINUTES.

DEPTH vs.CONCENTRATION (LOG ATOMS/CC)



OXIDATION FOR CONTACT
STEP # 15
OXIDATION IN DRY OXYGEN
TOTAL STEP TIME = 3.0 MINUTES
INITIAL TEMPERATURE = 1000.00 DEGREES C.
OXIDE THICKNESS = 1.4006E-02 MICRONS

LINEAR OXIDE GROWTH RATE = 7.479394E-03 MICRONS/MINUTE
PARABOLIC OXIDE GROWTH RATE = 1.739824E-04 MICRONS!2/MINUTE
OXIDE GROWTH PRESSURE = 1.00000 ATMOSPHERES

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT I
BORON	2.01370E-08	2.54949E-04	.17836	2.52627E-03
PHOSPHORUS	3.51730E-05	1.35028E-04	10.000	1.19299E-02

SURFACE CONCENTRATION = -5.808969E+16 ATOMS/CM!3

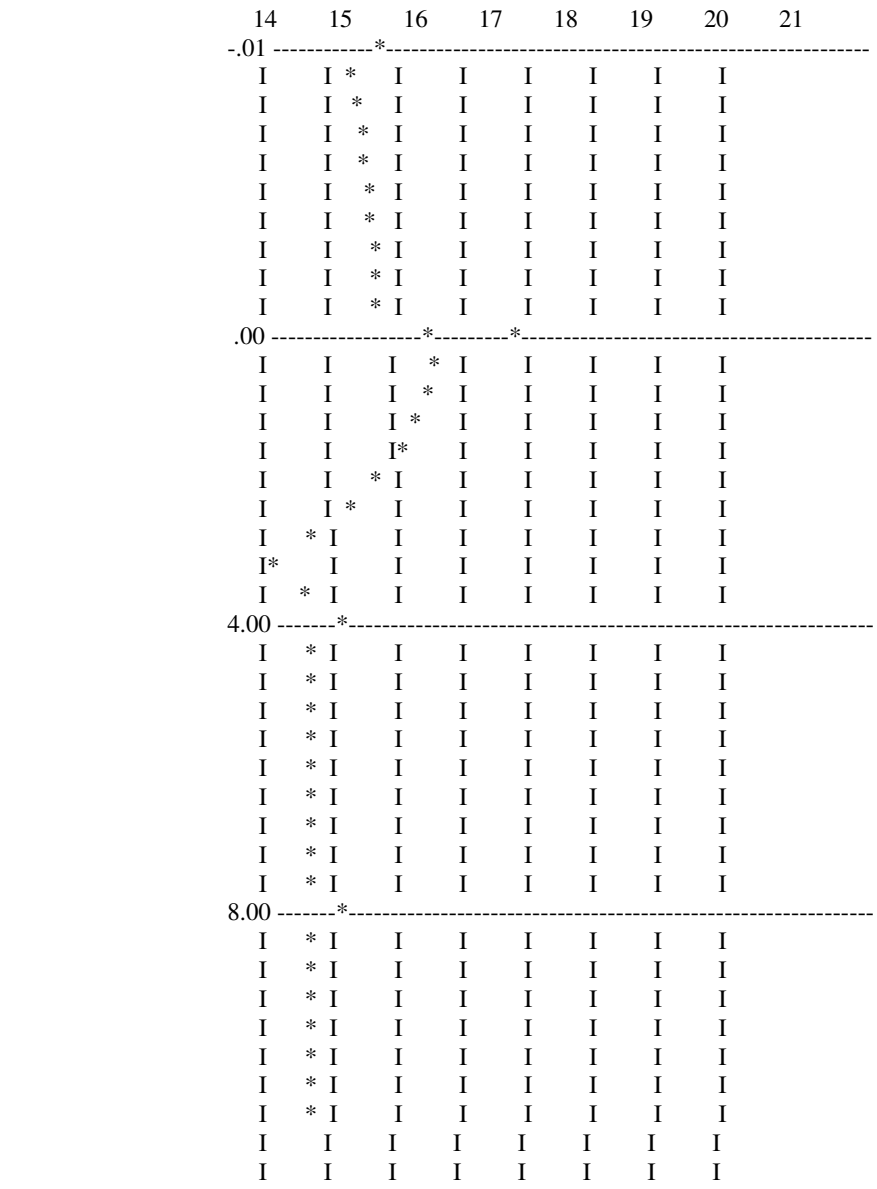
JUNCTION DEPTH	SHEET RESISTANCE
3.08997 MICRONS	1219.34 OHMS/SQUARE
	31226.1 OHMS/SQUARE

OXIDATION FOR CONTACT

STEP #15

TIME = 3.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC)



OXIDATION FOR CONTACT

STEP # 16

OXIDATION IN WET OXYGEN

TOTAL STEP TIME = 40.0 MINUTES

INITIAL TEMPERATURE = 1000.00 DEGREES C.

OXIDE THICKNESS = .2060 MICRONS

LINEAR OXIDE GROWTH RATE = 1.044611E-02 MICRONS/MINUTE

PARABOLIC OXIDE GROWTH RATE = 1.954248E-03 MICRONS!2/MINUTE

OXIDE GROWTH PRESSURE = .842105 ATMOSPHERES

	I OXIDE DIFFUSION COEFFICIENT	I SILICON DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE TRANSPORT COEFFICIENT I
BORON	I 2.01370E-08	I 2.03950E-04	I .17836	I 2.52627E-03 I
PHOSPHORUS	I 3.51730E-05	I 1.35028E-04	I 10.000	I 1.19299E-02 I

SURFACE CONCENTRATION = -9.815834E+16 ATOMS/CM!3

JUNCTION DEPTH	I	SHEET RESISTANCE
3.01851 MICRONS	I	1270.18 OHMS/SQUARE
	I	31261.3 OHMS/SQUARE

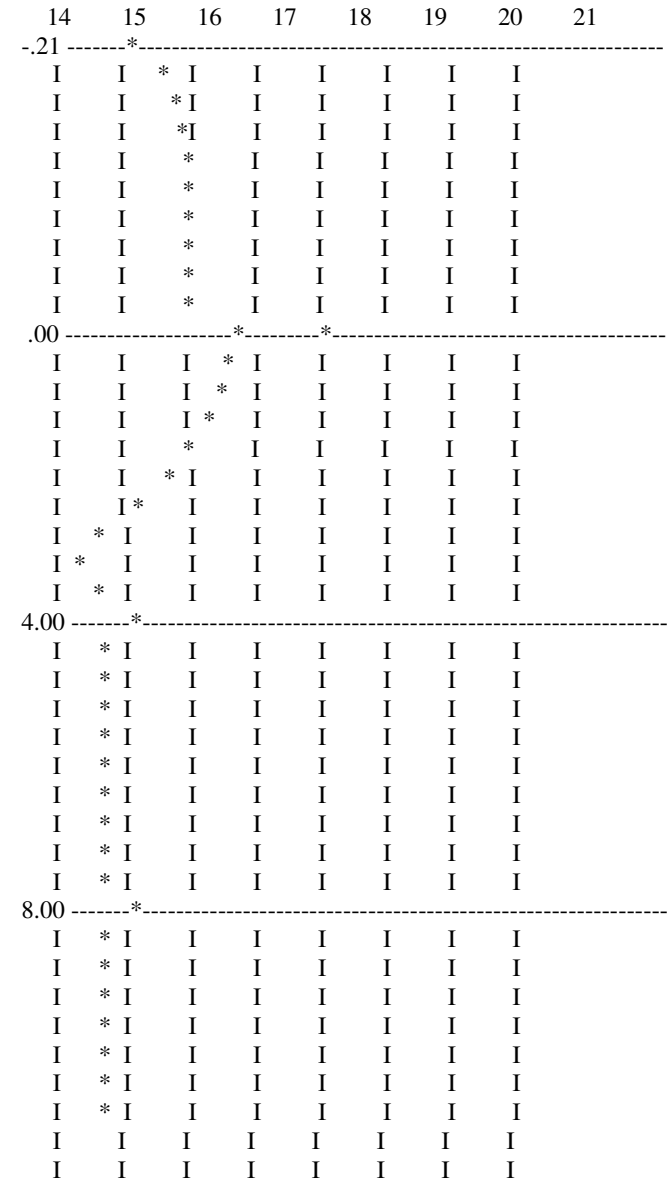
.

OXIDATION FOR CONTACT

STEP# 16

TIME = 40.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC)



OXIDATION FOR CONTACT
STEP # 17
OXIDATION IN DRY OXYGEN
TOTAL STEP TIME = 5.0 MINUTES
INITIAL TEMPERATURE = 1000.00 DEGREES C.
OXIDE THICKNESS = .2078 MICRONS

LINEAR OXIDE GROWTH RATE = 2.287017E-03 MICRONS/MINUTE
PARABOLIC OXIDE GROWTH RATE = 1.739824E-04 MICRONS!2/MINUTE
OXIDE GROWTH PRESSURE = 1.00000 ATMOSPHERES

	I OXIDE I DIFFUSION COEFFICIENT	I SILICON I DIFFUSION COEFFICIENT	I SEGREGATION COEFFICIENT	I SURFACE I TRANSPORT COEFFICIENT I
BORON	2.01370E-08	2.54949E-04	.17836	2.52627E-03
PHOSPHORUS	3.51730E-05	1.35028E-04	10.000	1.19299E-02

SURFACE CONCENTRATION = -8.803231E+16 ATOMS/CM!3

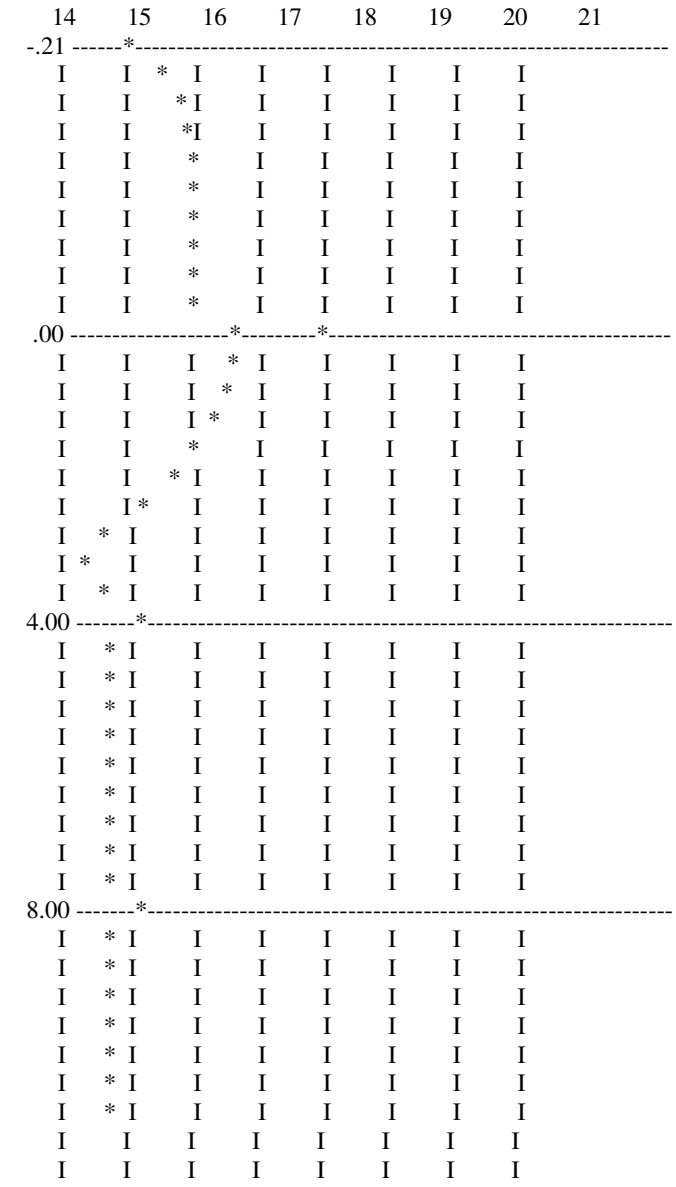
JUNCTION DEPTH	SHEET RESISTANCE
3.01933 MICRONS	1269.48 OHMS/SQUARE
	31266.1 OHMS/SQUARE

OXIDATION FOR CONTACT

STEP #17

TIME = 5.0 MINUTES.

DEPTH vs. CONCENTRATION (LOG ATOMS/CC)



SUPREM END.□