ANALYSIS, DESIGN, AND IMPLEMENTATION OF A TWO-SWITCH SINGLE PHASE ELECTRONIC LINE VOLTAGE REGULATOR

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ABSTRACT

ANALYSIS, DESIGN, AND IMPLEMENTATION
OF
A TWO-SWITCH SINGLE PHASE ELECTRONIC LINE VOLTAGE
REGULATOR

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Present day electrical equipment is rapidly becoming more and more sensitive to power quality problems, especially voltage sags. Various voltage sag correction devices are avaliable. This thesis analyzes a two-switch, single-phase electronic voltage regulator for correcting voltage sags. The theory of this voltage regulator has been investigated. An analytical method for sizing the energy storage capacitors has been established. The voltage regulator has been modeled and its steady-state and dynamic behavior has been studied by means of detailed computer simulations. A 220-V, 50-Hz, 1-kW rated regulator has been designed, simulated, and built. The results on the performance of voltage regulator and conclusions are also given.

Keywords: Power quality, voltage sags, power conditioning equipment, voltage regulator, energy storage capacitor.

ÖZ

ÇIFT ANAHTARLI VE TEK FAZLI BIR ELEKTRONIK SEBEKE GERILIM REGÜLATÖRÜNÜN ANALIZI, TASARIMI VE DENEYSEL UYGULAMASI

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Yüksek Lisans, Elektrik ve Elektronik Mühendisligi Bölümü

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Günümüzdeki elektrikli cihazlar giderek güç kalitesi problemlerine, özellikle gerilim düsümlerine karsi daha duyarli olmaktadirlar. Gerilim düsümlerini düzeltmek için çesitli cihazlar mevcuttur. Bu tez, gerilim düsümlerini düzeltmek için gelistirilmis çift anahtarli ve tek fazli bir elektronik gerilim regülatörünü analiz etmektedir. Bu gerilim regülatörünün teorisi arastirilmistir. Enerji depolama kondansatörlerinin boyutlandirilmasi için bir analitik yöntem gelistirilmistir. Ayrintili bilgisayar benzetimi yardimiyla bu gerilim regülatörü modellenmis ve kararli hal ve dinamik davranisi incelenmistir. 220-V, 50-Hz and l-kW anma degerlerinde bir gerilim regülatörünün tasarimi, benzetimi ve imalati yapilmistir. Bu gerilim regülatörünün basarimi ile ilgili sonuçlar ve son degerlendirmeler de tezin içerisinde verilmistir.

Anahtar Kelimeler: Güç kalitesi, gerilim düsümü, güç kalitesi düzeltme aygiti, gerilim regülatörü, enerji depolama kondansatörü.

To my daughter Inci,

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I would like to thank my husband and my mother for great support and understanding to complete this thesis.

I would like to thank my daughter Inci for her patience during this thesis.

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CHAPTER 1

INTRODUCTION

This thesis is related to power quality problems in the electric utility and the mitigation of these problems. With the increasing distortion and interference on the utility lines and also with the increasing use of sensitive equipment, power quality problems have become a major concern, especially for sensitive equipment. However, auxiliary equipment called power conditioning equipment may be utilized to mitigate power quality problems. Employing power conditioning equipment such as voltage regulators and uninterruptible power supplies, problems at the utility side may be prevented from distorting the voltage at the load side.

There are various power quality problems at the utility: Voltage sags, voltage swells, transients, voltage interruptions, etc. According to research by the Electric Power Research Institute (EPRI), in the USA, voltage sags down to 40-50 % of nominal voltage form 92 % of power quality problems [1]. In Europe and other countries similar findings have been reported. Therefore, this thesis focuses on voltage sags instead of other power quality problems. Voltage sags are defined as a decrease in the line voltage (below nominal) for a maximum duration of one minute. The subject of this thesis, the two-switch EVR (Electronic Voltage Regulator), is designed to correct these voltage sags. Since it involves minimum number of switch count, this topology will be referred to as “minimum” EVR and from here on, the term “MEVR” will refer to the Single-Phase Two-Switch Electronic Voltage Regulator which is investigated throughout this thesis.

This thesis is dedicated to analysis and design of the two-switch single phase MEVR. MEVR has two variations depending on the connection type of the filter capacitor. If the power stages of these voltage regulators are compared, both MEVR types have the same inverter circuit topology. The names of two variations are given below.

i. MEVR with series capacitor filter
ii. MEVR with parallel capacitor filter

MEVR is single-phase and two DC capacitors are used to store energy for the compensation. MEVR has some advantages compared to other solutions in the same category.

- Its size is small
- It does not need maintenance (there is no battery)
- Its cost of installation is low
- Its efficiency is high

Although MEVR is mainly utilized for correction of voltage sags, using proper control strategy and sizing the components appropriately, this voltage regulator can also be utilized to correct voltage swells.

The thesis consists of six chapters.

A brief information about power quality and voltage sags is given in chapter 2. Various power quality problems and their possible cures are outlined here as well.

The detailed MEVR theory, operating principle, and analysis is examined in chapter 3. The MEVR variations, circuit modes, storage capacitor sizing and inverter holding time (T_h) definition, voltage sag detection methods, phasor analysis, output filter design are discussed in chapter 3.

Three different control methods for these regulators are explained using block diagrams in chapter 3. They are:

i. In-phase injected voltage method
ii. Injected power minimization method
iii. Closed loop control method

In chapter 3, the inverter holding time (T_h), which is a time parameter that determines the ability of the regulator to sustain power quality at the output, is obtained via theoretical study and the results are verified with computer simulations. The inverter holding time vs. sag coefficient graphics are also given in this chapter. The inverter power rating and energy requirement is also analyzed in this chapter. The minimum energy method is analyzed and compared with the in-phase compensation approach. The inverter output low pass filter design is also examined in chapter 3. Finally a 1-kW rating MEVR is designed and the filter parameters are selected.

In chapter 4, the designed simulation circuit of MEVR is explained and results are given. The circuit simulations are run for various voltage sag conditions. Utilizing the simulation results, MEVR voltage sag correction performance is discussed. Also, momentary voltage sag condition is investigated in chapter 4.

A prototype of MEVR has been implemented in the laboratory. In chapter 5, the experimental studies are discussed. Control hardware and software for the prototype are described.

In chapter 6, overall conclusions of the thesis are given.

CHAPTER 2

POWER QUALITY AND VOLTAGE SAGS

2.1 POWER QUALITY

Power quality is quite frequently described as "voltage quality" because most power quality problems are voltage quality problems and generally power quality concerns the following groups: Utility, end users (residential, commercial, and industrial), sensitive equipment manufacturers, power conditioning equipment manufacturers, standard organizations (IEC, IEEE, ANSI), research organizations (EPRI, PEAC), consultants, monitoring and measuring equipment manufacturers, architect/engineer facility designers [2].

Also, power quality can be defined with respect to "clean power." "Clean power" refers to power that has sinusoidal voltage and current without any distortion and which is at the desired magnitude and frequency. Thus, "dirty power" could be described as a power that has a distorted sinusoidal voltage and current or which is outside the desired limits of voltage, current, and/or frequency [2].

"Power quality" or "clean power" is important and necessary especially for sensitive electronic devices designed and manufactured in state-of-the-art technology because these sensitive devices can not tolerate voltage variations as the non-electronic equipment. Non-electronic equipment used in the past such as motors, incandescent lights, and resistance heaters could tolerate voltage disturbances of ±5 % of nominal voltage [2]. Today, very sensitive equipment are

used and manufactured. Most of these sensitive equipments use microprocessors and computers.

Increasing the number of transistors on a chip or a microprocessor could be a reason for equipment sensitivity to voltage variations. The density of transistors in a very small package causes integrated circuits to have a low tolerance for voltage deviations. These voltage deviations cause electromagnetic interference (EMI). Due to this EMI, currents may flow which could damage the insulation between components. Moreover, computers use clock pulse voltages and timings produced by the power supply to store and process data in the microprocessor and memory. Any deviations from the specified voltage can cause the data to be corrupted or erased [2].

At this stage, "power quality problem" which is mentioned above as distortion or voltage deviations should be described. A phenomenon which causes any deviation in the magnitude, frequency or purity in the voltage is defined as a power quality problem.

These problems could be due to natural or man-made events. Lightnings, broken connections, and short circuits in the transmissions or distribution systems are examples for natural events. On the other hand, non-linear and unbalanced loads are common sources of man-made power quality problems. A non-linear load is defined as a load where the waveshape of the steady state current does not follow the waveshape of the applied voltage [2]. Non-linear loads often generate or amplify existing harmonic currents that distort the voltage waveform. Harmonics cause overheating of electrical equipments in the systems.

Some loads which are sources of harmonics or which amplify harmonics are: All types of electronic equipment that use switched-mode power supplies, adjustable speed drives which produce harmonics and cause nearby transformers to overheat and trip off, rectifiers converting ac to dc, inverters converting dc to ac, power-

factor-improving shunt capacitors, arc welders and arc furnaces, electronic and magnetic ballasts in fluorescent lighting, medical equipment such as MRI (Magnetic radiation imaging) and x-ray machines, UPS (Uninterruptible power supplies).

2.1.1 Categories of Power Quality Problems

Some important power quality problems are [3]:

1. Transients (Surges)
    a. Impulsive transients
    b. Oscillatory transients
2. Short duration variations
    a. Interruptions
    b. Sags (Dips)
    c. Swells
3. Long duration variations
    a. Undervoltages
    b. Overvoltages
4. Voltage unbalances
5. Harmonics

Figure 2.1 shows graphically all types of power quality problems. Studies show that, of all these problems, "short-duration variations" (which are defined as the phenomenon which last less than 1 minute) are the most common types of problems. The sag/swell problems investigated in this thesis belong to this group.

Short-duration voltage variations are caused by:

- fault conditions
- energization of large loads which require high starting currents
- intermittent loose connections in power wiring [3]

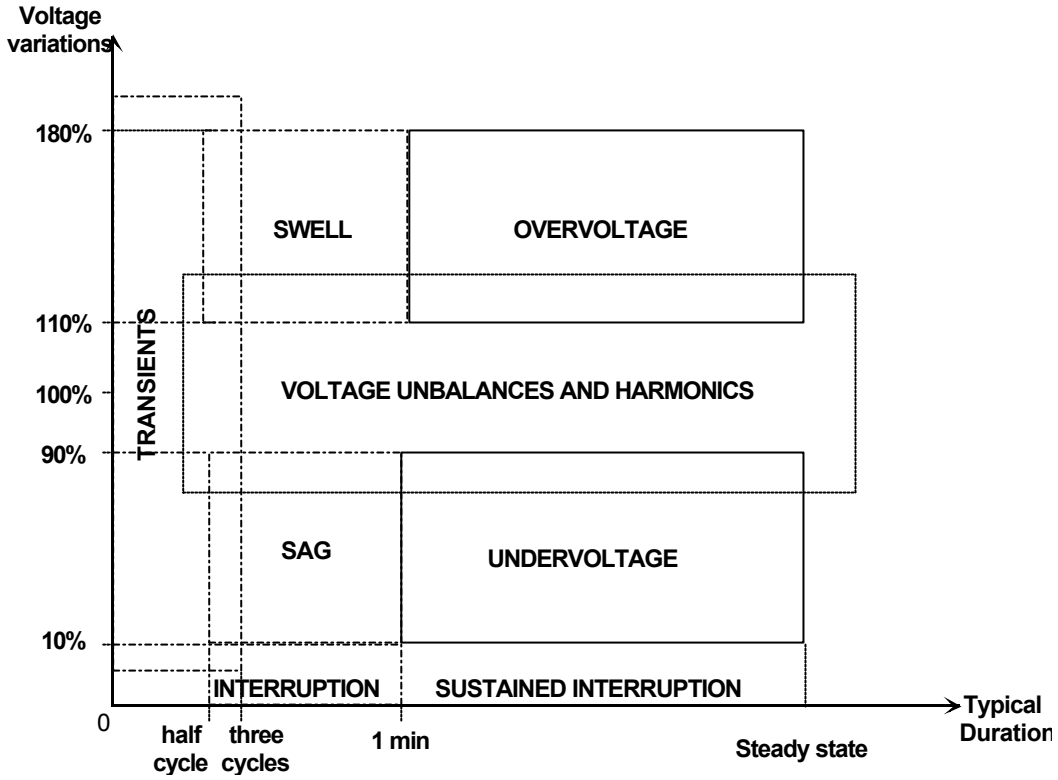


Figure 2.1. Categories of power quality problems.

Short-duration variations can be classified according to their voltage levels as follows:

- interruption (<0.1 pu)
- sag (0.1 – 0.9 pu)
- swell (1.1 – 1.8 pu)

Short-duration variations can also be classified according to their durations as [3]:

- instantaneous (0.5 to 30 cycles)
- momentary (30 cycles to 3 seconds)
- temporary (3 seconds to 1 minute)

2.2 VOLTAGE SAGS (DIPS)

Technically, a voltage sag is defined as: A decrease from nominal to between 0.1 and 0.9 pu in rms voltage or current at the power frequency for durations from 0.5 cycle to 1 minute.

Undervoltages that last less than one-half cycle can be considered as *transients.* Those that last longer than 1 minute can be considered as *long duration variations*.

Voltage sags are referred to as *voltage dips* in Europe. The IEC definition for this phenomenon is also dip. IEEE defines voltage sags as a reduction in voltage for a short time less than 1 minute but more than 8 milliseconds (0.5 cycle for 60 Hz frequency).

The magnitude of a voltage sag is defined as the missing voltage magnitude in the source voltage in this thesis. For example, if there is a 10 % voltage sag in the line voltage, it means that the line voltage at the mains is 0.9 pu. A "sag coefficient" (S_c) has been defined in this thesis, which is the per-unit value of the missing voltage. Therefore, a 10 % voltage sag corresponds to $S_c = 0.1$.

2.2.1 Causes and Results of Voltage Sags

Various events can cause voltage sags, but the most common causes are given below.

1. Faults (Single line to ground, line to line shortcircuit, etc.) on transmission or distribution system. The sag duration is about 5-6 cycles (100 ms for 50 Hz).
2. Energization of heavy loads or starting of large motors. In this case, sag duration is longer with respect to type 1 (typically from 0.5 s to several seconds).

The faults on a transmission or distribution system can be caused by utilities or end user. The end user is affected from faults according to its location. The fault could be on the same feeder or parallelled feeder with end user at the distribution system.

If there is a fault on the same feeder, the end user will experience a voltage sag during the fault followed by an interruption when the breaker opens to clear the fault. If the fault is temporary, a reclosing operation is done. This is true for an end user at feeder 4 with a single-line-to-ground fault, as shown in Figure 2.2 [3].

A fault on one of the other feeders from the substation, on a parallel feeder, or a fault somewhere on the transmission system is more common than the preceeding fault. When the breakers open to clear the fault, normal voltage is obtained by the end user. This is true for an end user at feeder 1, as shown in Figure 2.2 [3].

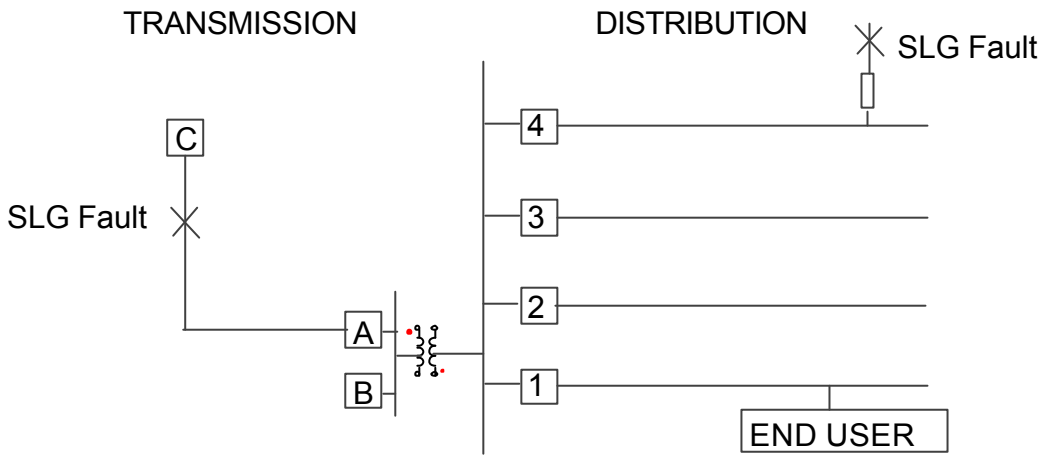


Figure 2.2. Typical reasons of voltage sags.

Transmission breakers typically clear a fault in 5 or 6 cycles. Distribution faults last longer than transmission faults.

A voltage sag is recognized with its effects or results on the end user. Some of the results of voltage sags can be given as follows:

i. Voltage sags reduce the energy being delivered to the end user for linear loads,
ii. Voltage sags cause computers to fail,
iii. Voltage sags cause adjustable speed drives to shut down,
iv. Voltage sags cause motors to stall and overheat,
v. Many manufacturing processes experience frequent shutdowns due to voltage sags,
vi. Most consumer products are affected by voltage sags and outages causing the electronic timer to shut down. These include digital clocks, microwave ovens, television sets, video cassette recorders, and stereo equipment.
vii. Incandescent lights often dim during a voltage sag. Lighting includes incandescent, high-intensity discharge, and fluorescent lights [3]
viii. For non-linear loads which include switch-mode power supplies, voltage sags cause increased currents to be drawn from the utility in order to draw constant power from the source.

Financial cost is one of the important results of the voltage sag, but exact cost of poor power quality can not be known with certainty. However, it is estimated that voltage sag disturbances cost billions of dollars every year in the USA [4]. Estimated cost of power quality problems to industry and commerce in the EU (European Union) is about 10 billion euros per year. However, the expenditure on preventative measures is less than 5 % (0.5 billion euros) of this amount [5]. Although, there are no detailed records for the power quality problems and effects in Turkey, it is well known that in addition to voltage sags, frequent interruptions occur.

To understand the effects of power quality problems involving voltage sags in industry, the following examples could be considered:

Paper is manufactured in a continuous process requiring precisely controlled speeds of hundreds of rollers in a machine. This may be over 500 meters in length. Any failure (interruption, sag, etc.) of the power supply will cause loss of synchronization and halt the process. All the processed paper and pulp must be cleared from the machine and the surrounding area before re-starting; this can take many hours. The negative results may be: Loss of products, waste of raw materials and manpower, the inability to deliver the customer orders, failure of the papermaker to deliver paper. As a result the publisher can not print news [5].

Another example involves the semiconductor industry, which is particularly sensitive to voltage sags, because wafers (PCB) require many manufacturing stages to be completed over several days. If a PCB which comes to the end of process is damaged, then all work done is wasted [5].

In Table 2.1, some numerical results on the costs of voltage sags are given.

Table 2.1. Financial impacts of voltage sags [5].

Industry	Typical Financial Loss per Event
Semiconductor production	3,800,000 Euro
Financial trading	6,000,000 Euro per hour
Computer centre	750,000 Euro
Telecommunications	30,000 Euro per minute
Steel works	350,000 Euro
Glass industry	250,000 Euro

2.2.2 Voltage Sag Standards

Voltage sag standards set voltage and current limits that sensitive electronic equipment can tolerate during electrical disturbances. Utilities need standards that set limits on the amount of voltage distortion their power systems can tolerate from harmonics produced by their customers with non-linear loads [2]. There are also standards on the performance of power conditioning equipment needed to prevent power quality disturbances from causing end-user equipment to misoperate.

Some important organizations which publish power quality standards are given in Table 2.2.

Table 2.2. Important organizations for power quality.

Organization	Abbreviation
American National Standards Institute	ANSI
European Union Standards Organization	CENELEC
Electric Power Research Institute	EPRI
International Electrotechnical Commission	IEC
Institute of Electrical and Electronics Engineers	IEEE
Information Technology Industry Council	ITIC (Formerly CBEMA)
Underwriters Laboratories,Inc.	UL

IEC standards refer to *power quality* standards as so called *Electromagnetic Compatibility (EMC) standards* [2]. Some important IEC and IEEE standards are given in Table 2.3.

Table 2.3. Important voltage sag standards [2].

Topic or disturbance	IEEE standard	IEC standard
Mitigation equipment	IEEE 446, 1035, 1100, 1250	None
Compatibility limits	IEEE 519	IEC 1000-3-2/4
Under-sag-environment	IEEE 1250	IEC 38,1000-2-4
Sag mitigation	IEEE 446, 1100, 1159	IEC 1000-5-X
Sag measurement	None	IEC 1000-4-1/11

IEEE 519-1992 (IEEE Recommended Practices And Requirements For Harmonic Control In Electric Power Systems) defines voltage distortion limits or THD (Total Harmonic Distortion) which utility can supply to the end user at the point of common coupling (PCC). Also it defines TDD (Total Demand Distortion) and sets limits on the harmonic current that the end user can inject into the utility's system at the PCC. This standard is important for this thesis because voltage regulators inject harmonic currents to utility.

The equation for calculating the THD for a voltage waveform where V_l is the fundamental voltage value and V_n (V_2, V_3, V_4,…) are harmonic voltage values is given in Eqn.2.1.

$$V_{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} (V_h)^2}}{V_1} \quad (2.1)$$

2.2.3 Voltage Sag Mitigation Methods

Power quality problems can not be avoided for the consumers (end users) who are directly connected together by the interconnected systems. Therefore, consumers must protect themselves from PQ problems with mitigation or power conditioning devices. It is researched by EPRI that 90 % of all power quality problems are voltage sags in the USA and it is assumed that the European power network exhibits similar attributes. In Turkey, the problem should be worse as the power grid is weak and frequent daily interruptions are not unusual. Therefore, the voltage sag correction solutions are the most important issue for consumers.

If protection from power quality problems is treated step by step, the following stages could be obtained.

1. Solutions during production of equipment

The basic and most cost effective solution is to strengthen sensitive devices against power quality problems during production. For example, IT (Information Technology) manufacturers use a specific curve (ITIC curve) that defines performance criteria involving voltage sags. Their manufactured equipment must remain functional within a specific voltage-time duration range during voltage sags. ITIC (Information Technology Industry Council) was formerly known as the CBEMA (Computer & Business Equipment Manufacturers Association) [6]. CBEMA generated a curve known as CBEMA curve which shows the susceptibility limits for computer equipment. Then, ITIC developed the CBEMA curve and this is known as ITIC curve now [2]. Shown in Figure 2.3, the ITIC (CBEMA) curve is a set of curves representing the withstanding capability of

computers connected to 120-V, 60-Hz power systems in terms of the magnitude and duration of the voltage disturbance.

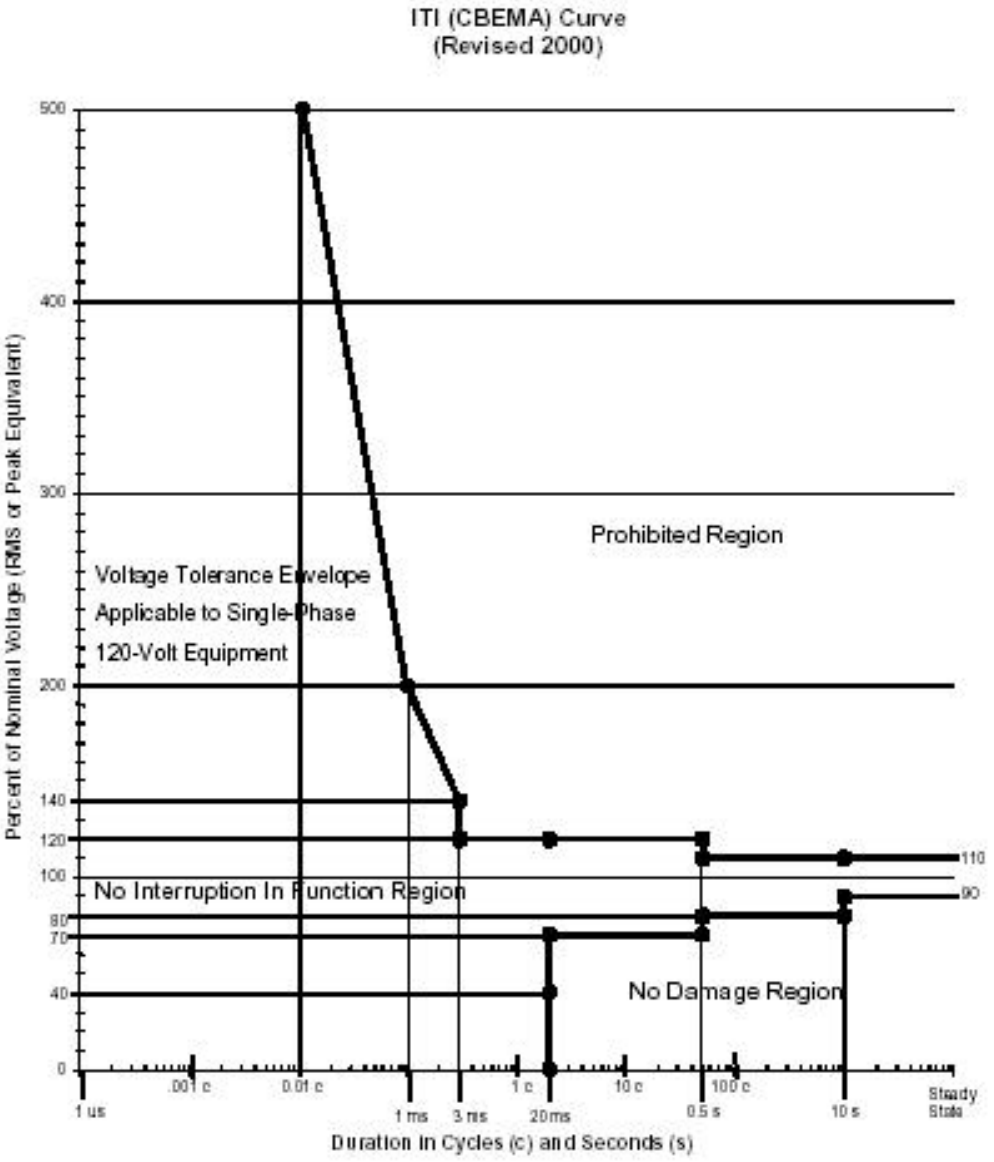


Figure 2.3. ITIC curve [6].

Seven regions are described in this curve but the most important regions relevant to this thesis are the following [6].

1. Voltage Sags: Sags down to 80 % of nominal voltage (20 % sag) are assumed to have a typical duration of up to 10 seconds. Sags to 70 % of nominal voltage (30 % sag) are assumed to have a duration of up to 0.5 seconds.
2. Line Voltage Swell: This is the voltage swell region, having an RMS amplitude of up to 120 % of the RMS nominal voltage, with a duration of up to 0.5 seconds.
3. No Damage Region: In this region, the ITE (Information Technology Equipment) is not expected to operate but it should not be damaged.
4. Prohibited Region: In this region, ITE may be damaged.

2. Analysis of effects and medium

The second basic method for solving voltage sag related power quality problems is the analysis of effects and medium which transmits power quality problems. For example, removing the sensitive equipment from the source of problem could be a cost effective solution. In other cases, by improving weak wiring and grounding, the sensitive equipments could be saved. Removing the medium which transmits the power quality problems could also be another cost effective solution.

3. Power conditioning equipment

If the above approach can not be implemented, then installing a proper power conditioning equipment is a common solution for the power quality problems. Power conditioning equipment includes devices that reduce or eliminate the effects of a power quality disturbance. Power conditioning usually involves voltage conditioning because most power quality problems are voltage quality problems. Most devices are utilized to condition or modify the voltage magnitude or frequency [2]. Power conditioning can be used to condition the source, the transmitter, or the receiver of the power quality problem. The cost of power conditioning solutions is increased from end-user side to utility side. Some common power conditioning equipment that correct voltage sags are given below.

Line-voltage regulators: These regulators are transformers specially designed to regulate the output voltage when the input voltage changes. They make changes to keep the output voltage relatively constant. Types of line regulators are: Tap changers, buck-boost regulators, CVT (Constant-voltage transformer).

M-G Sets (Motor-generator Sets): A motor is connected to the utility supply and runs the generator through a shaft or belt, providing clean power to critical equipment. If power is interrupted, the generator keeps supplying power to critical loads by using diesel or natural gas as the fuel. A rechargeable battery pack or a flywheel can be added to M-G Sets to provide power during ride through [2]. Maintenance and safety are the main concern [2], [4].

Magnetic Synthesizers: These regulators employ resonant circuits which are made of nonlinear inductors and capacitors to store energy, pulsating saturation transformers to modify the voltage waveform, and filters to filter out harmonic distortion. They supply power through a zig-zag transformer, which traps triplen harmonic currents and prevents them from reaching the power source. They can be bulky and noisy [2].

SVC (Static VAR Compensators): These regulators utilize a combination of capacitors and reactors to regulate the voltage quickly. They use solid-state switches that insert the capacitors and reactors at the right magnitude to keep the voltage from fluctuating. However they are quite large and expensive [2].

UPS (Uninterruptible Power Supplies): A UPS conditions the voltage, both during voltage sags and outages. It provides a constant voltage from a static source (battery, ferroresonant transformer, superconducting magnet etc.) or rotary source (diesel motor-generator set) [2]. The basic building blocks of a UPS system include the battery (with a 5 to 60 minute backup capability depending on its size), an inverter, and a rectifier. They are connected in three different configurations:

i. On-line UPS: Battery backup and continuous sag/swell protection is available all the time. It has a shorter battery life.
ii. Off-line UPS: Time delay of 4-10 milliseconds to engage the UPS during an interruption. It has a longer battery life.
iii. Line interactive UPS: A hybrid of the above two types. It has a shorter time to engage UPS and also saves battery life.
iv. A Rotary UPS module (i.e., a motor-generator set) can be added to the above types to produce a waveform independent of utility voltage and provide a longer backup time during outages.

SMES (Superconducting magnetic energy storage): SMES stores electrical energy within a superconducting magnet. It provides a large amount of power (750 kVA to 500 MVA) for a short time (2 seconds) very quickly (within 2 milliseconds) [2].

Static Transfer Switch: A static switch is used to transfer the load from one utility to another during a sag. However the main disadvantage is that it needs dual-feed utility supply.

Fuel Cell Based Inverter System: The main disadvantage is its high cost [4].

DVR (Dynamic Voltage Restorer): Dynamic voltage restorers are utilized to mitigate voltage sags which are seen by the sensitive large loads. A DVR has a mainly series connected injection transformer, energy storage module, boost converter and DC to AC inverter. These devices have high standby losses and equipment costs. If there is a voltage sag, then the DVR injects the missing voltage by the transformer which is connected in series with the source voltage. If there is a nominal voltage at the utility, then the DVR may inject a small voltage for the voltage drop of the transformer or may be in short circuit operation. Examples of the applications are protection for semiconductor production plants, high speed paper mills and sensitive drive circuits in the process of uranium enrichment [7], [8]. Table 2.4 compares the cost of different power conditioning equipments.

Table 2.4. Costs for different power quality improvement technologies [3], [4].

Controls protection (<5 kVA):	
CVTs	$1000/kVA
UPS	$500/kVA
MEVR	$250/kVA
Machine protection (10-300 kVA):	
UPS	$500/kVA
Flywheel	$500/kVA
MEVR	$200/kVA
SMES	$600/kW
Rotary UPS	$700/kW
Fuel Cell Based Inverter System	$1,500/kW
Facility protection (2-10 MVA):	
UPS	$500/kVA
Flywheel	$500/kVA
DVR (50% voltage boost)	$300-500/kVA
Static switch (10 MVA)	$600,000
Fast transfer switch (10MVA)	$150,000

Although, many possible techniques have been previously developed and used to mitigate voltage sags, most of these techniques are not optimized to correct voltage sags with short durations. For example, using a UPS (which includes a battery designed to overcome long voltage interruptions) would be unnecessary to correct a voltage sag lasting only a few cycles. Moreover, these techniques may be costly, occupy large volumes, have large weight, and have a relatively low efficiency.

Utilizing the latest semiconductor technology, a special line voltage regulator is proposed by Divan [1] which is the subject of this thesis. This line voltage regulator is called as **"A two-switch single phase electronic line voltage regulator" and abbreviated as "MEVR" with "M" standing for "minimum" indicating that it is the electronic device with minimum number of semiconductor components**. The MEVR device is an electronic line voltage regulator and is specifically designed to correct voltage sags. The topology of MEVR is simpler compared to the other conventional line voltage regulators because only two controlled switches are utilized in the inverter stage and DC capacitors are employed to store energy instead of a battery or other energy storage equipment. Moreover, the inverter is directly connected in series with the line, without a transformer. There is a static by-pass switch used to supply the load

directly from the line when there is a nominal voltage at the line. All of these features provide a low cost, lightweight, simple and efficient method for voltage sag mitigation [9].

As seen in reference [9], two variations of MEVR basic topology are possible. According to the filter capacitor location, there are two variations of MEVR:

1. MEVR with series filter capacitor
2. MEVR with parallel filter capacitor

Although the filter capacitor location is different in these types, the circuit topology of both types is the same. In the following chapters of this thesis, these two MEVR circuits are studied, analyzed, and their behavior investigated by means of computer simulations.

CHAPTER 3

THEORY AND ANALYSIS OF TWO - SWITCH SINGLE PHASE ELECTRONIC LINE VOLTAGE REGULATOR

In this chapter, the two-switch single phase electronic line voltage regulator will be investigated and it's theoretical analysis will be explained utilizing phasor diagrams and other analytical methods. Sizing of the energy storage capacitors (C_{dc1}, C_{dc2}) is obtained. An analytical equation for the inverter holding time (T_h), which defines the capacity of the regulator under deep voltage sag conditions, is derived for various conditions [10]. Control methods and voltage sag detection methods are studied. Finally, the low pass LC filter of the line voltage regulator is designed and discussed.

3.1 GENERAL DISCUSSION

As discussed in chapter 2, there are various solutions for the correction of voltage sags. However, the MEVR is particularly designed for voltage sag correction. Before attempting in depth analytical investigations of MEVR, a general discussion of various electronic voltage regulators will be conducted.

Many different types of electronic line voltage regulator topologies have been designed and are discussed in various sources [1]-[3], [8], [10]-[17]. These topologies are briefly described as follows:

1. Electronic line voltage regulators with mains frequency transformer: Electronic tap changer is an example to this category. It includes a low frequency transformer with various secondary tappings, which are connected to the output via static switches. This circuit allows bidirectional power flow [11]. However, it is not considered as "fully electronic" due to the large 50 Hz power transformer involved.

2. Static VAR compensator (SVC): SVCs include capacitors and inductors which are inserted into the circuit using solid-state switches to regulate voltage [2], [8].

3. Electronic line voltage regulators with battery back-up: Uninterruptible power supplies (UPS) are the main example of this category. They include a rectifier, inverter and battery to provide output voltage [2], [11].

4. Voltage-dip proofing inverter: This is similar to an off-line UPS, but utilizes a capacitor as the energy storage device, instead of a battery. When a voltage sag occurs, a static switch is turned off, isolating the line from the output. During voltage sag condition, the capacitor supplies the load through an inverter. While a UPS is designed mainly for longer-duration voltage interruptions, voltage-dip proofing inverters are mainly designed to mitigate voltage sags [12].

5. High frequency AC-AC electronic transformer topologies: Such topologies have been described in various sources [10], [13]. The electronic transformer accepts source voltage directly and provides an electronically controlled output voltage. These may include a high-frequency transformer but are not suitable for large scale systems [10]. However, they allow bidirectional energy flow [13].

6. Active series voltage regulator: An active series voltage regulator has an output which is connected in series with the source side. While different topologies are

possible for active series voltage regulators, their main feature is that the converter output is connected in series with the line, either directly (low power systems) or via a transformer (high power systems). These voltage regulators operate by injecting the missing voltage at the source using a PWM inverter while there is a voltage sag at the line. The input of the converter is connected in parallel with the source.

MEVR belongs to the active series voltage regulator group. Also, the Dynamic Voltage Restorer (DVR) belongs to this category but DVR is more costly compared to MEVR since DVR includes a full-bridge inverter with 4 switches [7]-[8] and a series injection transformer. Another topology called as switched-mode AC/AC voltage regulator with series connected compensation has been proposed [15], which is similar to both DVR and MEVR. It consists of a flyback AC/DC converter connected in parallel to the source, followed by a push-pull DC/AC converter whose output is connected in series with the line. Other topologies called two-switch voltage-doubler, 4-switch regulator with improved source current and buck-boost output have been proposed in the references [16].

3.1.1 Evolution of MEVR

MEVR originated from the back-to-back full bridge inverter active series voltage regulator topology. This variation or evolution of the active series voltage sag regulator topologies will be explained by the following figures.

The complete back-to-back full bridge voltage source inverter (VSI) topology involves two inverters with power transistors with one inverter at the input and the other at the output followed by the series injection transformer as can be seen in Figure 3.1. This voltage regulator can provide two-way power flow but it is expensive.

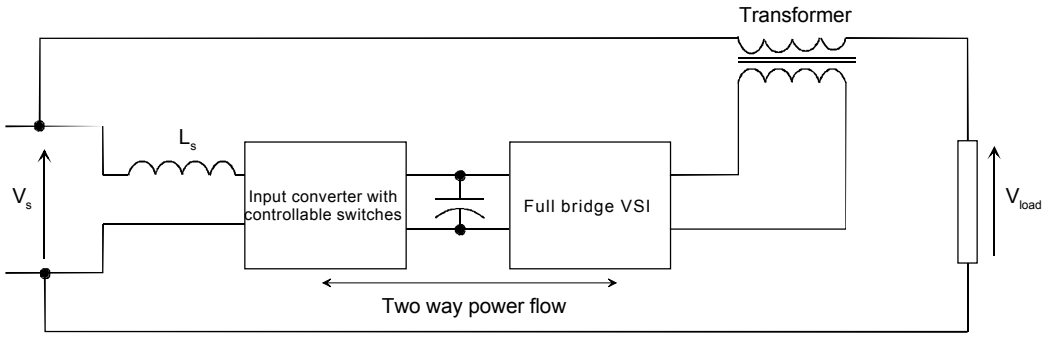


Figure 3.1. Voltage regulator with bidirectional power power flow and complete back-to-back inverter.

In the second type, the input converter is replaced by a diode rectifier as can be seen in Figure 3.2. Therefore, the cost and complexity of this voltage regulator is less than that of previous type. However, as the input converter is made of diode rectifier the circuit is capable of one-way active power flow only.

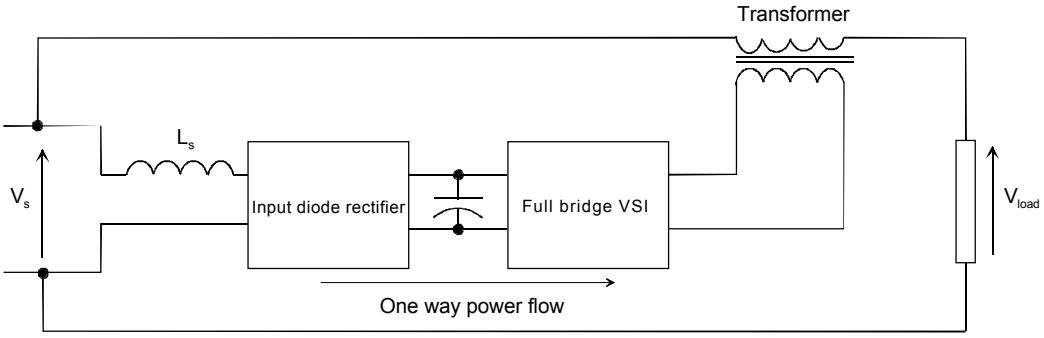


Figure 3.2. Voltage regulator with unidirectional power flow and full bridge VSI.

In the third type, the full bridge inverter is replaced by a half bridge inverter to simplify the circuit as can be seen in Figure 3.3.

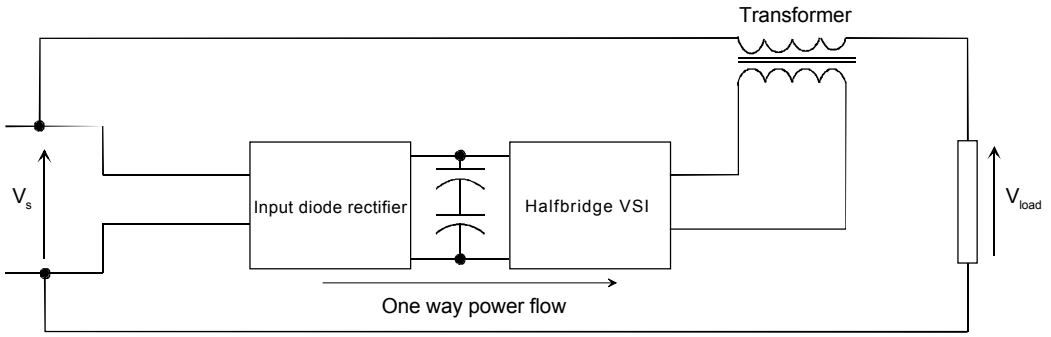


Figure 3.3. Voltage regulator with unidirectional power flow and half-bridge VSI.

The inverters and converters shown in Figures 3.1-3.3 utilize fully controllable switches such as MOSFET (Metal Oxide Semiconductor Field Effect Transistor), IGBT (Insulated Gate Bipolar Transistor), BJT (Bipolar Junction Transistor) etc. In this thesis, all fully controllable switches are indicated with IGBT symbols as seen in circuit diagrams. Moreover, IGBTs have been utilized as controllable switches during MEVR simulation and laboratory implementation.

Two variations of EVR (called MEVR) which are the subject of this thesis form the fourth and fifth types.

The fourth type is MEVR with filter capacitor connected in parallel to the load and inverter output. As seen in Figure 3.4, there is a static bypass switch instead of a transformer to connect the nominal line voltages directly to the load. Also, both converters are simple compared to the converters of previous topologies.

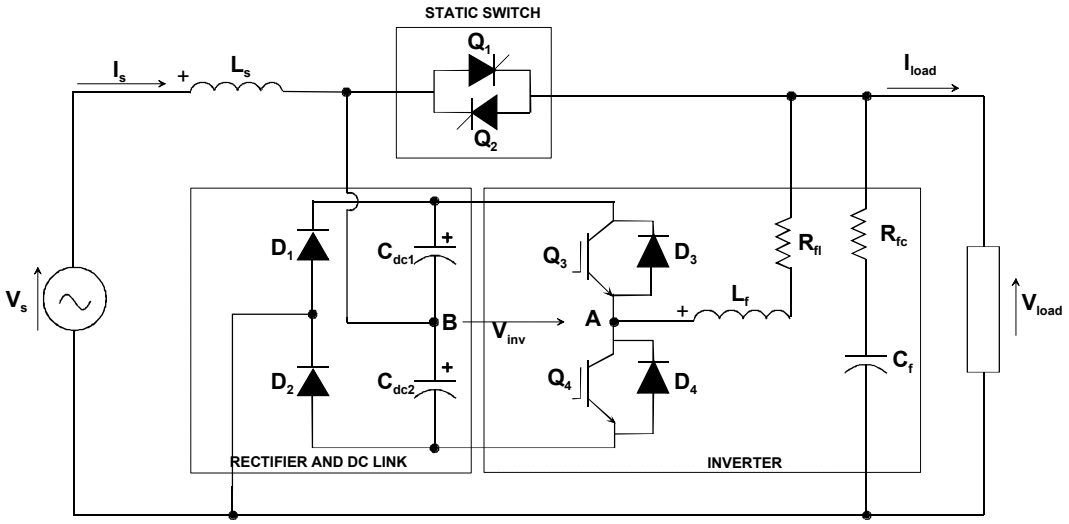


Figure 3.4. MEVR with parallel filter capacitor.

The fifth type is MEVR with filter capacitor connected in series with the inverter output as can be seen in Figure 3.5. The main difference between fourth and fifth types is the location of the filter capacitance, while the remaining parts are the same.

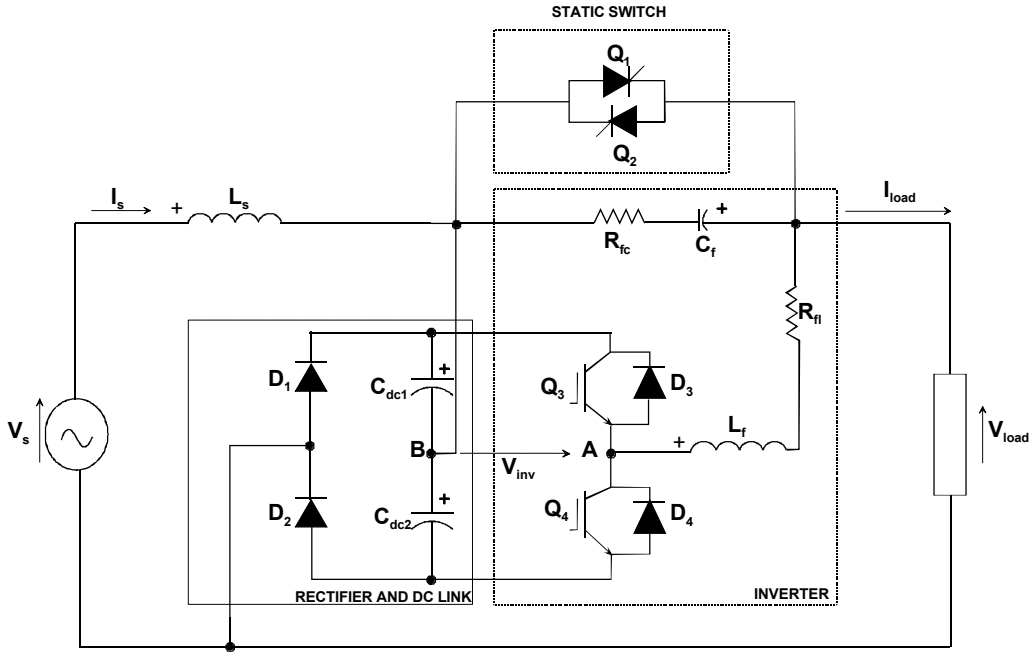


Figure 3.5. MEVR with series filter capacitor.

3.1.2 Operating Principle of MEVR

The MEVR circuit is similar to an off-line UPS because the inverter in the regulator is on only when the source voltage is outside the tolerable limits. Basically, MEVR is formed by three stages as seen from Figure 3.4 and Figure 3.5. These stages are

1. Static bypass switch
2. Inverter with LC filter output
3. Rectifier and DC link

The static bypass switch connects the source to the load during nominal conditions, bypassing the inverter. During nominal source voltage, the inverter is at standby. Under these conditions, the efficiency of MEVR is high because the inverter is off. Moreover, the load voltage is purely sinusoidal while static bypass switch is operating.

There is a sag limit for determining the voltage sag detection. If the source voltage is less than or equal to this sag limit, the main controller detects a voltage sag at the source, the MEVR controller switches the static bypass switch off and starts the inverter (the second part of MEVR) operation. The inverter voltage which is obtained from the energy storage capacitors is added (injected) in series to the source voltage to maintain nominal load voltage. However, the voltage which is added by the inverter is of rectangular pulse nature and has a lot of harmonics due to PWM operation of the power transistors. Therefore, it is necessary to add a low pass filter at the output to filter the inverter voltage and provide smooth load voltage. Typically LC filters are employed and the filter components are filter capacitor (C_f) and filter inductance (L_f). The filter inductance (L_f) is connected in series with the inverter output. The filter capacitor (C_f) may be connected in parallel or series with inverter output. Therefore, there are two MEVR topologies as discussed in section 3.1.1.

During inverter operation, MEVR efficiency will be less compared to nominal mode operation. Moreover, the load voltage may contain some harmonics due to switching operation. By adjusting the sag limit, inverter operation time can be controlled. If the sag limit is set very close to the nominal load voltage, the inverter may operate frequently, decreasing the overall MEVR efficiency.

The third part of MEVR is the rectifier and DC link. The rectifier (half-bridge) includes two diodes. DC link is formed by two capacitors. These capacitors are called the "energy storage capacitors". The diodes in the rectifier stage are used to charge energy storage capacitors from the source side. The energy storage capacitors are used to obtain the required inverter voltage for sag correction.

The three parts of MEVR are described briefly above. The circuit has two main operating modes: Nominal voltage operation and inverter operation.

In nominal voltage operation, the source voltage is nominal, the static bypass switch (Q_1 and Q_2) is switched on and the load is supplied by the nominal voltage. This nominal voltage operation can be seen by the equivalent circuit of MEVR in Figure 3.6.

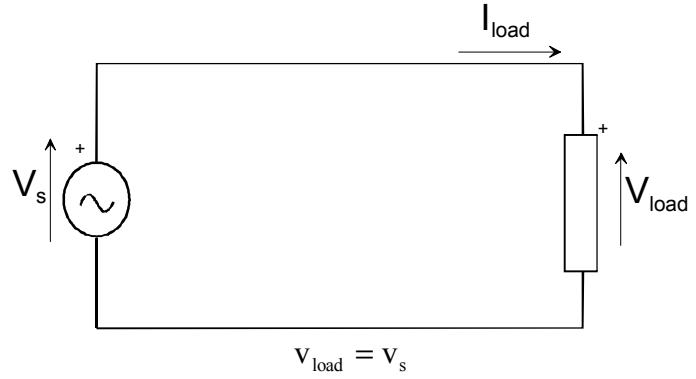


Figure 3.6. Equivalent circuit diagram of MEVR for nominal voltage operation.

When a voltage sag is detected in the source voltage, the static bypass switch is turned off and the inverter stage is enabled. The energy storage capacitor voltages

are added (subtracted) to (from) the low source voltage by PWM operation of the power transistors in the inverter. This operating mode is called as inverter operation and this can be seen in Figure 3.7. Note that, during inverter operation, source voltage, inverter voltage and load voltage are in-phase for the in-phase control method. This subject will be discussed further in the following sections.

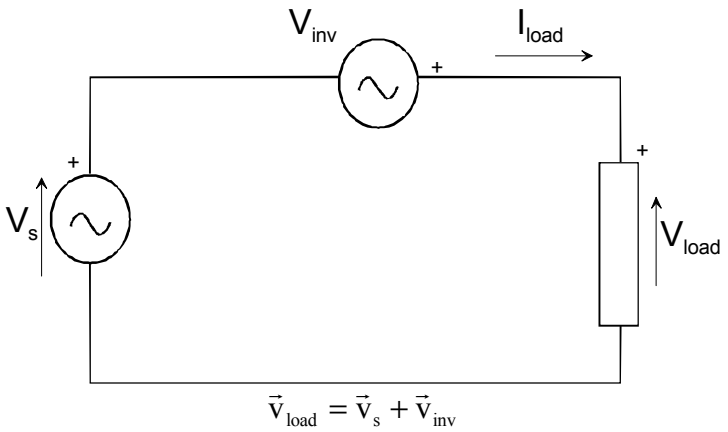


Figure 3.7. Equivalent circuit diagram of MEVR for inverter operation.

MEVR is designed to keep the load voltage at nominal level regardless of source voltage variations. The MEVR circuit injects the required (missing) voltage in series to the source voltage and boosts the low source voltage to nominal value. MEVR can also decrease high source voltages (voltage swells), provided that the appropriate control method is used and an input stage converter with controlled switches is available for bidirectional power flow. However, the main purpose of MEVR is voltage sag correction. The relationship between the source, inverter and load voltages for the sag correction is shown by the sinusoidal waves in Figure 3.8. (Only the fundamental components of inverter voltage and load voltage are shown in Figure 3.8.)

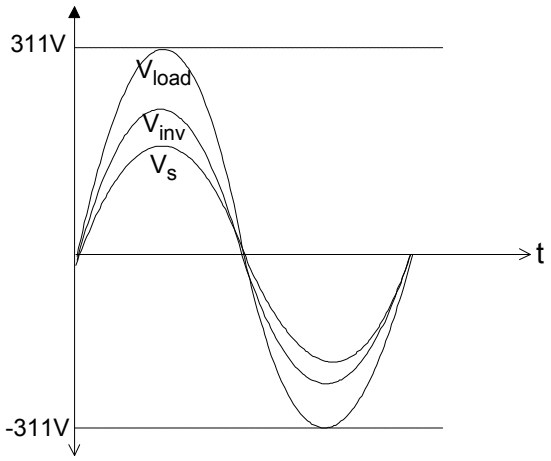


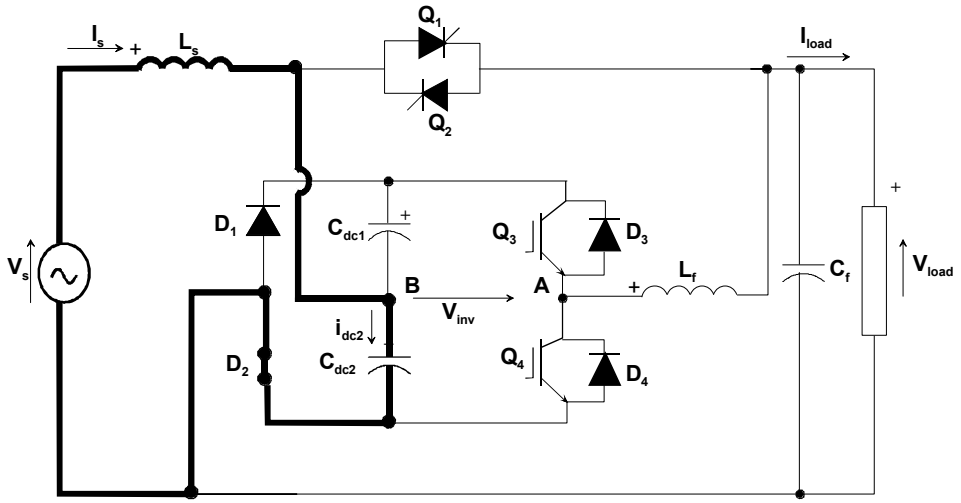
Figure 3.8. Source, inverter and load voltages (fundamental component) during inverter operation.

Figure 3.6 and Figure 3.7 correspond to the two main operation modes of MEVR but in each mode the detailed circuit modes should be studied carefully in order to understand the operation logic clearly.

3.1.3 Circuit Modes of MEVR

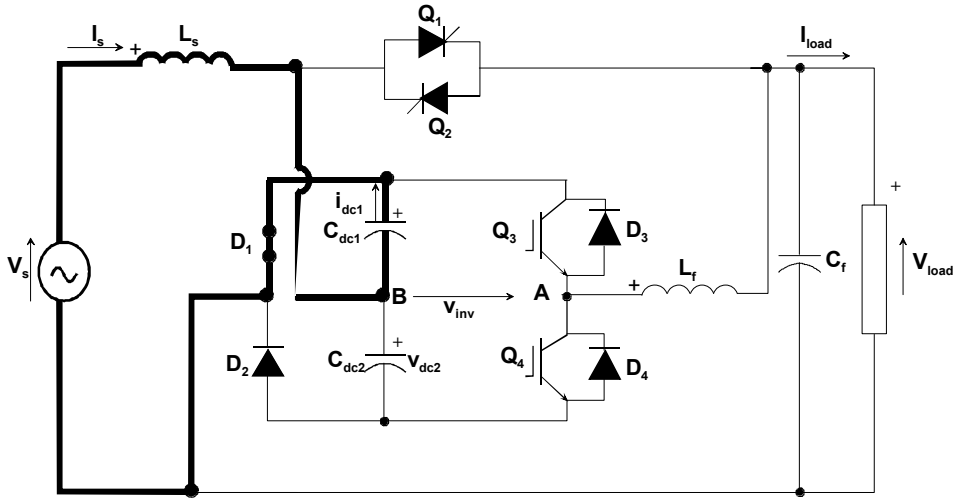
When all possible circuit modes of MEVR circuit are taken into account, the states of switches (SCRs of the static bypass switch, IGBT switches of the inverter, diodes of the rectifier), voltage and current polarities of the circuit elements define the circuit modes. These circuit modes are summarized in Tables 3.1, 3.2 and 3.3.

There are two circuit mode types: Primary modes and secondary modes. The secondary modes of MEVR circuit are seen in the Figure 3.9 and Figure 3.10 and relate to the charging of the energy storage capacitors via the half bridge diode rectifier. Since they are easier to understand and less significant in the operating performance of MEVR circuit, these modes are termed as secondary modes. The primary modes are seen in Figure 3.11 - Figure 3.16.



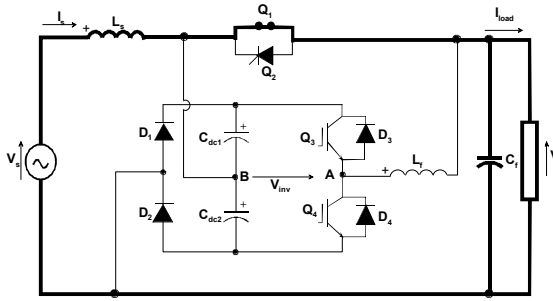
$$v_s = v_{Ls} + v_{dc2} > 0,\ i_s = i_{dc2} > 0$$

Figure 3.9. Secondary mode a.



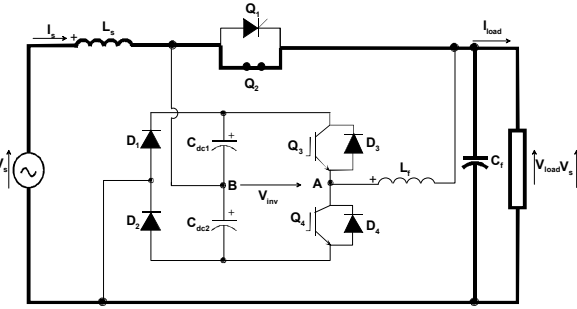
$$v_s = v_{Ls} - v_{dcl} < 0,\ i_s = i_{dc1} < 0$$

Figure 3.10. Secondary mode b.



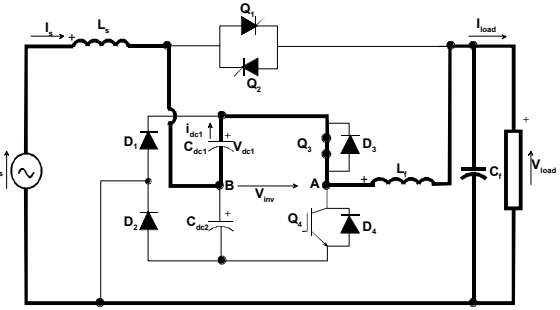
$v_s = v_{Ls} + v_{load}, \quad i_s = i_{load} > 0$

Figure 3.11. Primary mode 1.



$v_s = v_{Ls} + v_{load}, \quad i_s = i_{load} < 0$

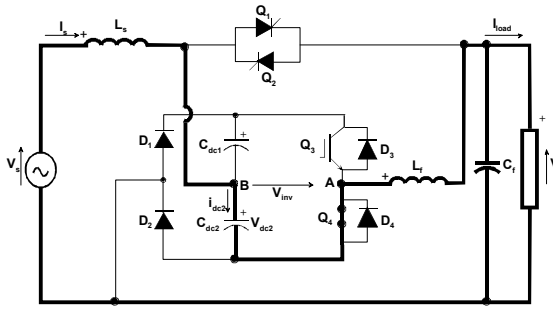
Figure 3.12. Primary mode 2.



$v_s + v_{dc1} = v_{Ls} + v_{Lf} + v_{load}, \quad v_{inv} = v_{dc1} > 0$

$i_s = i_{dc1} = i_{inv} = i_{load} > 0, \quad P_{inv} = v_{inv} \cdot i_{inv} > 0$

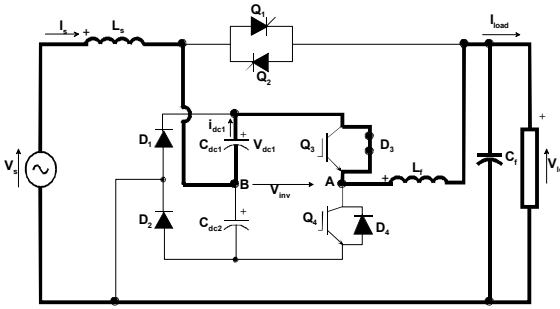
Figure 3.13. Primary mode 3.



$v_s - v_{dc2} = v_{Ls} + v_{Lf} + v_{load}, v_{inv} = -v_{dc2} < 0$

$i_s = i_{dc2} = i_{inv} = i_{load} < 0, P_{inv} = v_{inv} \cdot i_{inv} > 0$

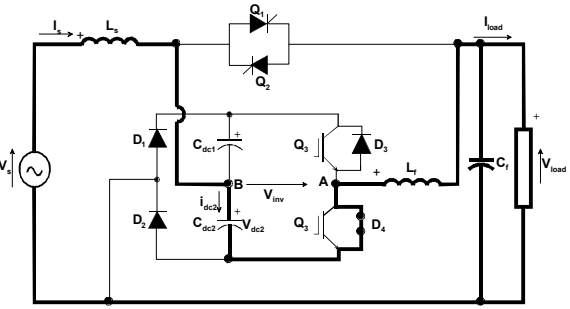
Figure 3.14. Primary mode 4.



$v_s + v_{dc1} = v_{Ls} + v_{Lf} + v_{load}, \quad v_{inv} = v_{dc1} > 0$

$i_s = i_{dc1} = i_{inv} = i_{load} < 0, \quad P_{inv} = v_{inv} \cdot i_{inv} < 0$

Figure 3.15. Primary mode 5.



$v_s - v_{dc2} = v_{Ls} + v_{Lf} + v_{load}, v_{inv} = -v_{dc2} < 0,$

$i_s = i_{dc2} = i_{inv} = i_{load} > 0, \; P_{inv} = v_{inv} \cdot i_{inv} < 0$

Figure 3.16. Primary mode 6.

Table 3.1. Modes for nominal source voltages.

Mode	Mode description	Source voltage	Load current	Q_1	Q_2	Q_3	Q_4	D_3	D_4	C_{dc1}, C_{dc2} D_1, D_2
1	Positive Load Current	Nominal (Positive or Negative)	+	On	Off	Off	Off	Off	Off	See Note
2	Negative Load Current		-	Off	On	Off	Off	Off	Off	

Note: Voltages of C_{dc1} and C_{dc2} are determined by secondary modes (a-c) which are independent of modes (1-7). For modes a-c, see Table 3.3

Table 3.2. Modes for source voltages which are at the outside tolerable limits.

Mode	Mode description	Source voltage	Inverter voltage	Load current	Inverter power	Inverter power flow	Q_1	Q_2	Q_3	Q_4	D_3	D_4	C_{dc1}	C_{dc2}
3	Forward Active	Low or High	+Vdc1	+	+	Power flows from C_{dc1} to load	Off	Off	On	Off	Off	Off	Discharging	See note
4	Reverse Active		-Vdc2	-	+	Power flows from C_{dc2} to load	Off	Off	Off	On	Off	Off	See note	Discharging
5	Reverse Freewheeling		+Vdc1	-	-	Power flows from load to C_{dc1}	Off	Off	Off	Off	On	Off	Charging	See note
6	Forward Freewheeling		-Vdc2	+	-	Power flows from load to C_{dc2}	Off	Off	Off	Off	Off	On	See note	Charging
7	Null state		0	0	0	No change	Off	Off	Off	Off	Off	Off	No change	No change

Note: Voltages of C_{dc1} and C_{dc2} are determined by secondary modes (a-c) which are independent of modes (1-7). For modes a-c, see Table 3.3

Table 3.3. Secondary modes

Mode	Mode description	Source voltage Polarity	V_{dc1}	V_{dc2}	D_1	D_2	C_{dc1}	C_{dc2}
a	C_{dc2} charging by supply	+		$V_{dc2} < V_s$	Off	On		Charging
b	C_{dc1} charging by supply	–	$V_{dc1} < \lvert V_s \rvert$		On	Off	Charging	
c	Neither C_{dc1} nor C_{dc2} charging by supply		$V_{dc1} \geq \lvert V_s \rvert$	$V_{dc2} \geq V_s$	Off	Off		

Note: Primary modes (1-7) and secondary modes (a-c) exist together.
For example, “mode 1-a”, “mode 1-b”, “mode 5-c”, etc

3.2 ANALYSIS AND CONTROL THEORY OF MEVR

In order to understand the behaviour of MEVR under various voltage sag, load power factor and load angle conditions, the general equations for inverter power and inverter voltage are derived in this section. Special cases, such as minimum values of active and apparent power, and optimum conditions for operation are also investigated.

3.2.1 Inverter Power vs. Load Angle Characteristics

The load angle (δ) is defined as the phase angle between the source voltage (V_s) and the load voltage (V_{load}). Inverter active power equation as a function of load angle will be obtained in this section. Generally, the load active power is supplied by both the source and the inverter during inverter operation. Therefore, the inverter active power is given by Eqn.3.1:

$$P_{inv} = P_{load} - P_{s,direct} \tag{3.1}$$

$P_{s,direct}$ is the active power drawn by the load directly from the source. P_{inv} is the active power drawn by the load from the inverter. P_{load} is the total active power (nominal) drawn by the load.

The active source power (P_s) consists of two active powers: $P_{s,direct}$ (defined above) and inverter active input power ($P_{inv,in}$). $P_{inv,in}$ is the power drawn from the source to charge the capacitors.

$$P_s = P_{s,direct} + P_{inv,in} \tag{3.2}$$

The angle between source current and source voltage is ϕ'.

$$P_s = V_s \cdot I_s \cdot \mathrm{Cos}\phi' \tag{3.3}$$

The angle between load current (I_{load}) and source voltage (V_s) is ϕ. These voltage, current phasor diagrams and the angles are shown in the Figure 3.17.

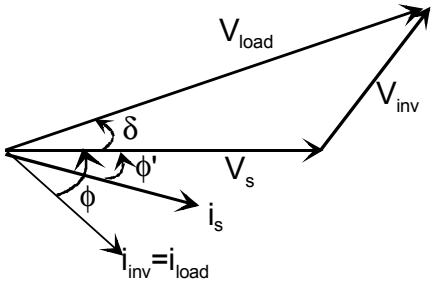


Figure 3.17. Phasor diagram for source power factor angle.

The power flow relation of MEVR is illustrated in Figure 3.18.

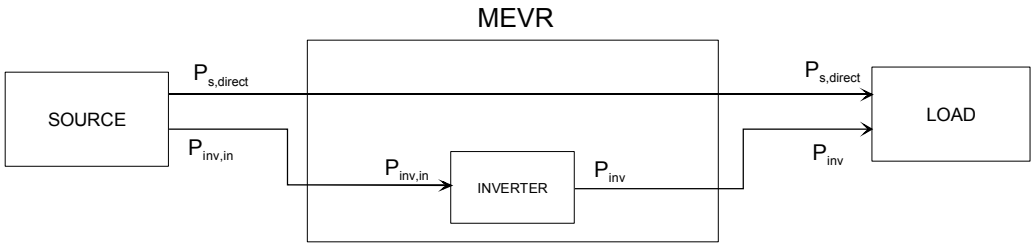


Figure 3.18. Relationship between the load, source, and inverter power.

In Figure 3.18, $P_{inv,in}$ is the power which is drawn from the source in order to charge the energy storage capacitors. The cos(θ) term is the load power factor, and cos(ϕ′) term is the source power factor (Eqn.3.3). In general, the source current is greater than the load current due to capacitor charging currents. In Eqn.3.4 (shown below), the load current is employed instead of the source current because only the load current part of the source current contributes to the power delivered to load as seen in the Figure 3.19. Note that the source current waveform in Figure 3.19 is given for steady state conditions where the energy storage capacitors have discharged down to source voltage value (less than nominal). Therefore, the energy storage capacitors are periodically being charged by the source with current pulses (Modes a or b as given in Figures 3.9- 3.10).

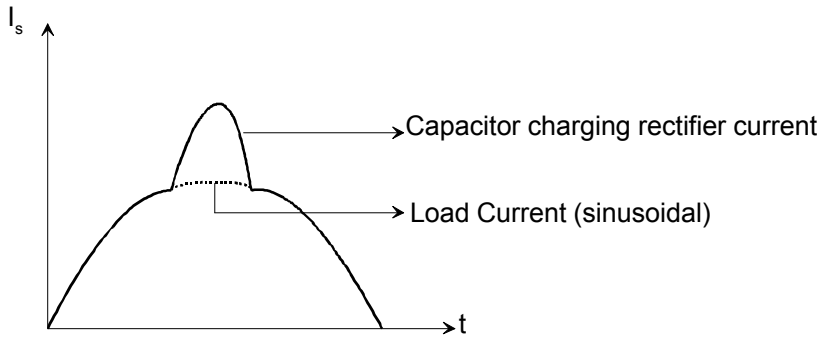


Figure 3.19. Source current.

Defining the load current as I_{load}, the power drawn directly from the source by the load and the load power can be written as in Eqn 3.4 and Eqn 3.5, respectively.

$$P_{s,direct} = V_s \cdot I_{load} \cdot Cos\phi \tag{3.4}$$

$$P_{load} = V_{load} \cdot I_{load} \cdot Cos\theta \tag{3.5}$$

Utilizing Eqn.3.1, Eqn.3.4 and Eqn.3.5, the following inverter power equation is derived.

$$\Rightarrow P_{inv} = V_{load} \cdot I_{load} \cdot Cos\theta - V_s \cdot I_{load} \cdot Cos\phi \tag{3.6}$$

$$\Rightarrow P_{inv} = I_{load} \cdot \left(V_{load} \cdot Cos\theta - V_s \cdot Cos(\theta - \delta)\right) \tag{3.7}$$

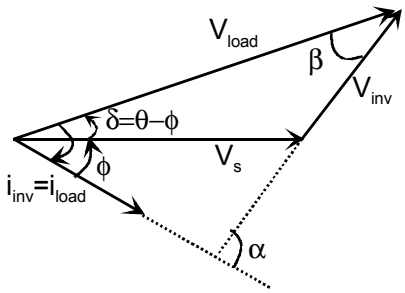


Figure 3.20. Voltage sag phasor diagrams for inductive load.

At this stage, the sag coefficient (S_c) should be defined. The sag coefficient (S_c) will be used to define the voltage sag quantity in the source. The sag coefficient is the normalized (per unit) value of the sag magnitude. If S_c is 1, there is no source voltage and voltage sag magnitude is 100 % of the nominal voltage. If S_c is 0, there is nominal voltage at the source. Negative values of S_c correspond to voltage swell conditions. If S_c is (-1), voltage swell magnitude is 100 % of the nominal voltage. The voltage sag coefficient can be defined by Eqn.3.8, also. This definition can be understood more easily by Table 3.4.

$$S_c = \frac{\Delta V_{sag}}{V_{nom}} = \frac{V_{nom} - V_s}{V_{nom}} \tag{3.8}$$

Table 3.4. Table for voltage sag coefficient.

S_c	**V_s (RMS source voltage)**	**Voltage sag/swell percentage**
1	0	100 % voltage sag
0.5	110 V	50 % voltage sag
0	**220 V**	**Nominal voltage**
-0.5	330 V	50 % voltage swell
-1	440 V	100 % voltage swell
-1.5	550 V	150 % voltage swell

Where, V_{nom} is the nominal voltage. For simplicity, the load voltage and source voltage can be defined in terms of the nominal voltage and sag coefficient as shown below.

$$V_{load} = V_{nom} \tag{3.9}$$

$$V_s = (1 - S_c) \cdot V_{nom} = (1 - S_c) \cdot V_{load} \tag{3.10}$$

From Eqn.3.7, Eqn.3.9 and Eqn.3.10, the inverter power equation is developed as Eqn.3.11.

$$P_{inv} = V_{nom} \cdot I_{load} \cdot \left[\text{Cos}\theta - (1 - S_c) \cdot \text{Cos}(\theta - \delta)\right] \tag{3.11}$$

As seen in Eqn.3.11, the inverter power varies with the cosine of load angle, δ, because all the other parameters in the equation are fixed for specified source voltage (S_c) and load conditions (I_{load}, θ). In other words, in Eqn.3.11, only δ can be controlled independently.

The inverter power is a negative cosine wave which is shifted upwards on the y-axis by $V_{nom}I_{load}\cos(\theta)$, and shifted to the right on the x-axis by θ. As seen in Eqn.3.11, the cosine wave for the inverter power is obtained for a specified load power factor (cos(θ)) and sag coefficient (S_c) if all circuit conditions such as V_{load}, I_{load} remain the same. The inverter power characteristics in Figure 3.21, is drawn for arbitrary values of S_c and cos(θ).

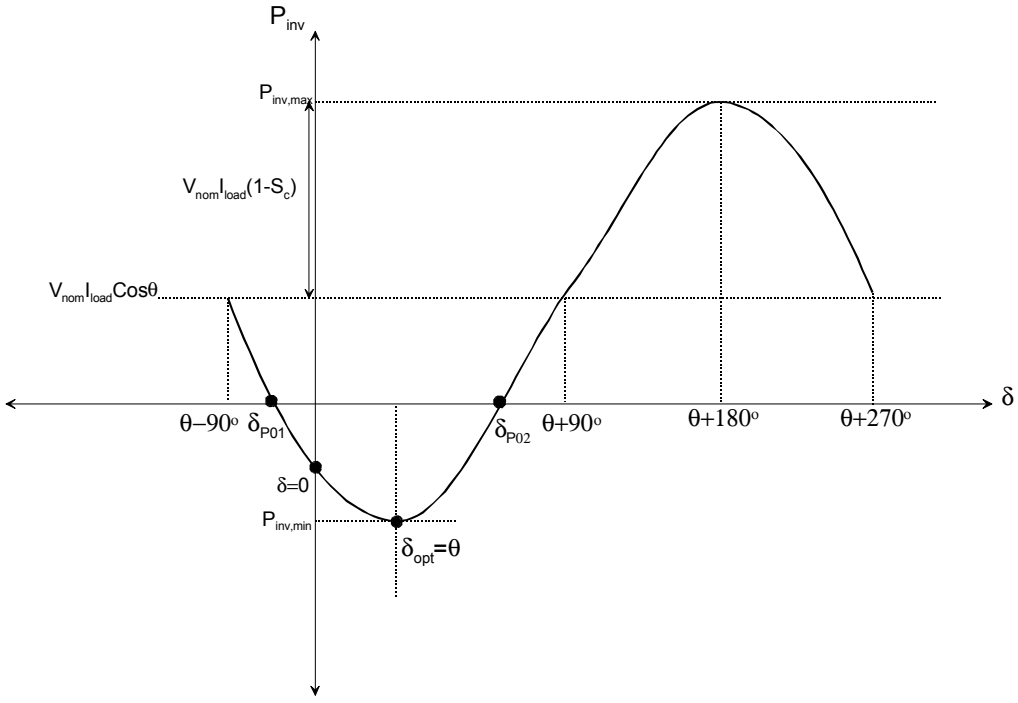


Figure 3.21. The inverter power characteristics for an arbitrary S_c.

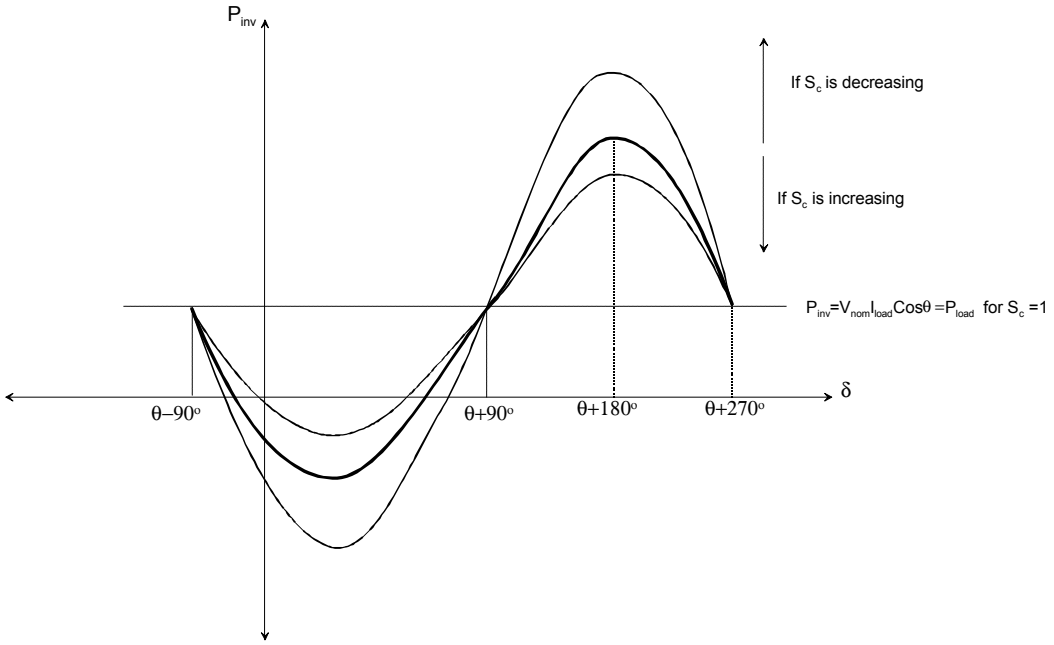


Figure 3.22. The relationship between S_c and $P_{inv.}$

The relationship between sag coefficient (S_c) and cosine wave amplitude (P_{inv}) is given in Figure 3.22. If there is 100 % voltage sag ($S_c = 1$), then the inverter power is equal to load power as seen in this figure.

It is generally desired that the inverter operates with minimum active power in order to discharge the energy storage capacitors as little as possible. However, this is not always possible for all voltage sag conditions as discussed below. Two special cases are analyzed in detail. These are:

1. Minimum injected (inverter) active power,
2. Zero injected (inverter) power

In order to operate MEVR in one of these special conditions, the load angle which is necessary for this operation should be calculated first.

3.2.1.1 Load Angles for Zero Inverter Power Operation (δ_{P01}, δ_{P02})

As seen in Figure 3.21, the inverter power will be equal to zero at two different values of load angle: δ_{P01}, δ_{P02}. These angles are calculated in this section. If Eqn.3.11 is equaled to zero, these two load angles can be obtained.

$$P_{inv} = V_{nom} \cdot I_{load} \cdot \left[\mathrm{Cos}\theta - (1 - S_c) \cdot \mathrm{Cos}(\theta - \delta_{P0})\right] = 0 \tag{3.12}$$

$$\Rightarrow \mathrm{Cos}(\theta - \delta_{P0}) = \frac{\mathrm{Cos}\theta}{(1 - S_c)} \tag{3.13}$$

$$\Rightarrow \pm(\theta - \delta_{P0}) = \mathrm{Cos}^{-1}\left(\frac{\mathrm{Cos}\theta}{1 - S_c}\right) \tag{3.14}$$

As seen in equations above, there are two solutions for δ_{P0}: δ_{P01} and δ_{P02}

$$(\theta - \delta) = \mathrm{Cos}^{-1}\left(\frac{\mathrm{Cos}\theta}{1 - S_c}\right) \qquad \Rightarrow \qquad \delta_{P01} = \theta - \mathrm{Cos}^{-1}\left(\frac{\mathrm{Cos}\theta}{1 - S_c}\right) \tag{3.15}$$

$$-(\theta - \delta) = \mathrm{Cos}^{-1}\left(\frac{\mathrm{Cos}\theta}{1 - S_c}\right) \qquad \Rightarrow \qquad \delta_{P02} = \theta + \mathrm{Cos}^{-1}\left(\frac{\mathrm{Cos}\theta}{1 - S_c}\right) \tag{3.16}$$

For voltage sag conditions where the term $\left|\mathrm{Cos}\theta/(1 - S_c)\right|$ in Eqn.3.15 and Eqn.3.16 is greater than 1, there is no δ solution for zero inverter power. In other words, inverter power cosine wave does not intersect the δ-axis. In this case, only a positive minimum inverter power value is possible, instead of zero inverter power. This can be seen in Figure 3.23.a.

For voltage sag conditions where the term $\left|\mathrm{Cos}\theta/(1 - S_c)\right|$ is equal to or less than 1, there is a solution for zero inverter power. In other words, inverter cosine wave intersects the δ-axis. This can be seen in Figure 3.23.b.

For voltage swell conditions where $S_c<0$, the term $\left|\text{Cos}\theta/(1-S_c)\right|$ is always smaller than 1 and there is always a solution (δ_{P01} and δ_{P02}) for zero inverter power.

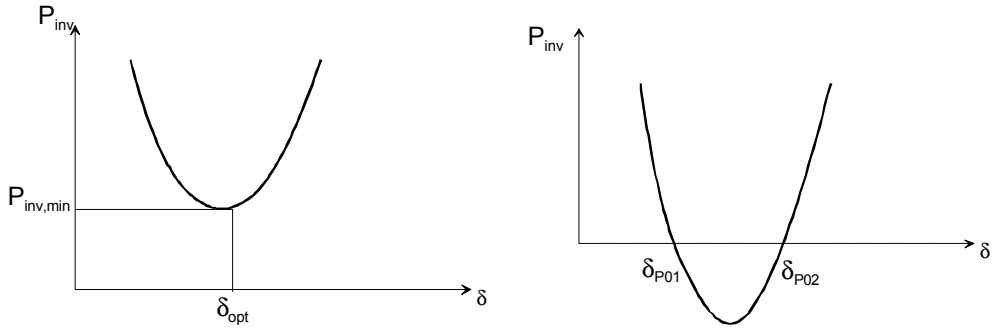


Figure 3.23. Inverter power characteristics for different voltage sag conditions.

If zero inverter power operation is not possible, then the inverter could be operated in minimum inverter power operation as long as the inverter can supply required inverter voltage.

3.2.1.2 Load Angle for Minimum Inverter Power Operation (δ_{opt})

The required load angle for minimum inverter power (δ_{opt}) is calculated in this section. As seen in Figure 3.21, there is a load angle that the inverter power takes its minimum value ($P_{inv,min}$) for a given value of cosθ. To obtain this load angle, the derivative of inverter power (Eqn.3.11) is taken with respect to load angle and equaled to zero.

$$\frac{dP_{inv,out}}{d\delta}=\frac{d\left[I_{load}\cdot\left(V_{load}\cdot\text{Cos}\theta-V_s\cdot\text{Cos}(\theta-\delta)\right)\right]}{d\delta}=0 \tag{3.17}$$

$$\Rightarrow -I_{load}\cdot V_s\cdot\text{Sin}\left(\theta-\delta_{opt}\right)=0 \tag{3.18}$$

$$\Rightarrow \text{Sin}\left(\theta-\delta_{opt}\right)=0 \tag{3.19}$$

$$\Rightarrow \left(\theta-\delta_{opt}\right)=\pi\cdot k \tag{3.20}$$

Due to $-90° < \delta_{opt} < 90°$ and k = 0,1,2,...

$$\delta_{opt} = \theta \tag{3.21}$$

The optimum load angle (δ_{opt}) is obtained as equal to load power factor angle. In other words, if the load angle is equaled to θ, the inverter power will be equaled to its minimum value. This minimum inverter power is obtained at cos(ϕ) = 1 as seen from Eqn.3.22 below.

$$P_{inv,min} = P_{inv}(\delta = \delta_{opt} = \theta) = I_{load} \cdot (V_{load} \cdot Cos\theta - V_s) \tag{3.22}$$

Source power factor cos(ϕ') is improved and inverter sag correction duration (inverter holding time) lasts longer by applying minimum inverter power condition.

3.2.2 Inverter Voltage vs. Load Angle Characteristics

From the phasor diagram in Figure 3.20, it is evident that the required inverter voltage increases as the load angle increases, where the minimum value of inverter voltage is expected to occur at $\delta = 0$. As the inverter voltage is obtained from the energy storage capacitors, there is an upper limit to the voltage which can be produced by the inverter. This means that the inverter can not supply the required inverter voltage for all voltage sag and load angle conditions. Therefore, in this section, the required inverter voltage for a certain condition is obtained.

The required inverter voltage equation will be derived as a function of the load angle, δ, and sag coefficient, S_c. The phasor diagram in Figure 3.24 is employed to obtain inverter voltage equation.

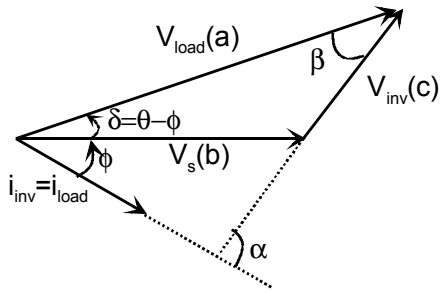


Figure 3.24. Phasor diagram for calculation of the inverter voltage.

$$V_{inv} = \sqrt{V_s^2 + V_{load}^2 - 2 \cdot V_s \cdot V_{load} \cdot \mathrm{Cos}\delta} \tag{3.23}$$

If Eqn.3.9 and Eqn.3.10 are utilized in Eqn.3.23, the inverter voltage equation is obtained with respect to sag coefficient, nominal voltage and load angle as seen in Eqn.3.24 below.

$$\Rightarrow V_{inv} = \sqrt{(1 - S_c)^2 \cdot V_{nom}^2 + V_{nom}^2 - 2 \cdot (1 - S_c) \cdot V_{nom} \cdot V_{nom} \cdot \mathrm{Cos}\delta} \tag{3.24}$$

$$V_{inv} = V_{nom} \cdot \sqrt{S_c^2 - 2 \cdot S_c + 2 \cdot \mathrm{Cos}\delta \cdot S_c + 2 - 2 \cdot \mathrm{Cos}\delta} \tag{3.25}$$

The same voltage phasor diagram can be used to obtain the phase angles of each voltage vector. To obtain α which is the angle between inverter voltage and load current (also, inverter current), β which is the angle between inverter voltage and load voltage can be derived using the triangle abc in Figure 3.25.

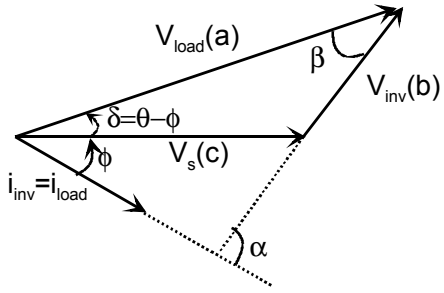


Figure 3.25. Phasor diagram for equation of β.

$$V_s = \sqrt{V_{inv}^2 + V_{load}^2 - 2 \cdot V_{inv} \cdot V_{load} \cdot \text{Cos}\beta} \tag{3.26}$$

Therefore,

$$\beta = \pm \text{Cos}^{-1} \cdot \left[\frac{V_{inv}^2 + V_{load}^2 - V_s^2}{2 \cdot V_{inv} \cdot V_{load}} \right] \tag{3.27}$$

As seen from Eqn.3.27, there are two solutions for β. If the inverter voltage leads load voltage, then both β and δ are positive. If load voltage leads inverter voltage, then both β and δ are negative.

From Figure 3.25,

$$\alpha = \theta + \beta \tag{3.28}$$

If the inverter voltage leads the load current, then α is positive. If the load current leads inverter voltage, then α is negative.

The inverter voltage phase angle (with respect to source voltage) is γ.

$$\gamma = \beta + \delta \tag{3.29}$$

The inverter power as a function of the inverter voltage, load current and α is obtained as Eqn.3.30. This is an alternative method for calculating P_{inv}, if V_{inv} and α are known. In Eqn.3.30, the inverter current is taken as load current because the filter capacitance current is small and the inverter current is equal to load current approximately. This can be seen from the system simulation results in chapter 4.

$$P_{inv} = V_{inv} \cdot I_{load} \cdot \text{Cos}\alpha \tag{3.30}$$

At this stage, the required inverter voltage equation for minimum and zero inverter power conditions will be obtained.

3.2.2.1 The Required Inverter Voltage For Zero Inverter Power Operation

The required inverter (injected) voltage equation for zero inverter power operation is obtained in this section. For this purpose, Eqn.3.15 (δ_{P01}) is combined with Eqn.3.25.

$$V_{inv,required} = V_{nom} \cdot \sqrt{S_c^2 - 2 \cdot S_c + 2 \cdot \mathrm{Cos}\left(\theta - \mathrm{Cos}^{-1}\left(\frac{\mathrm{Cos}\theta}{1 - S_c}\right)\right) \cdot S_c + 2 - 2 \cdot \mathrm{Cos}\left(\theta - \mathrm{Cos}^{-1}\left(\frac{\mathrm{Cos}\theta}{1 - S_c}\right)\right)} \quad (3.31)$$

$$V_{inv,required} = V_{nom} \cdot \sqrt{S_c^2 - 2 \cdot S_c + 2 - 2 \cdot \mathrm{Cos}^2 ? - 2 \cdot \mathrm{Sin}\theta \cdot \sqrt{(1 - S_c)^2 - \mathrm{Cos}^2\theta}} \quad (3.32)$$

3.2.2.2 The Required Inverter Voltage For Minimum Inverter Power Operation

To obtain required inverter voltage for the minimum inverter power operation, optimum delta ($\delta = \delta_{opt} = \theta$) from Eqn.3.21 is utilized in Eqn.3.25.

$$V_{inv,required} = V_{nom} \cdot \sqrt{S_c^2 - 2 \cdot S_c + 2 \cdot \mathrm{Cos}\theta \cdot S_c + 2 - 2 \cdot \mathrm{Cos}\theta} \quad (3.33)$$

3.2.2.3 Inverter Voltage vs. Load Angle Plots

To plot the inverter voltage as a function of load angle, δ, Eqn.3.25 can be rewritten as Eqn.3.34.

$$V_{inv} = V_{nom} \cdot \sqrt{(S_c^2 - 2 \cdot S_c + 2) + (2 \cdot S_c - 2) \cdot \mathrm{Cos}\delta} = V_{nom} \cdot \sqrt{A + B \cdot \mathrm{Cos}\delta} \quad (3.34)$$

Where,

$$A = S_c^2 - 2 \cdot S_c + 2 \quad (3.35)$$

$$B = 2 \cdot S_c - 2 \quad (3.36)$$

For $\delta = 0$,

$$V_{inv} = V_{nom} \cdot |S_c| \tag{3.37}$$

For $\delta = \pm 90°$, $\cos\delta = 0$ so,

$$V_{inv} = V_{nom} \cdot \sqrt{A} = V_{nom} \cdot \sqrt{S_c^2 - 2 \cdot S_c + 2} \tag{3.38}$$

The characteristics of inverter voltage as a function of load angle is given in Figure 3.26.

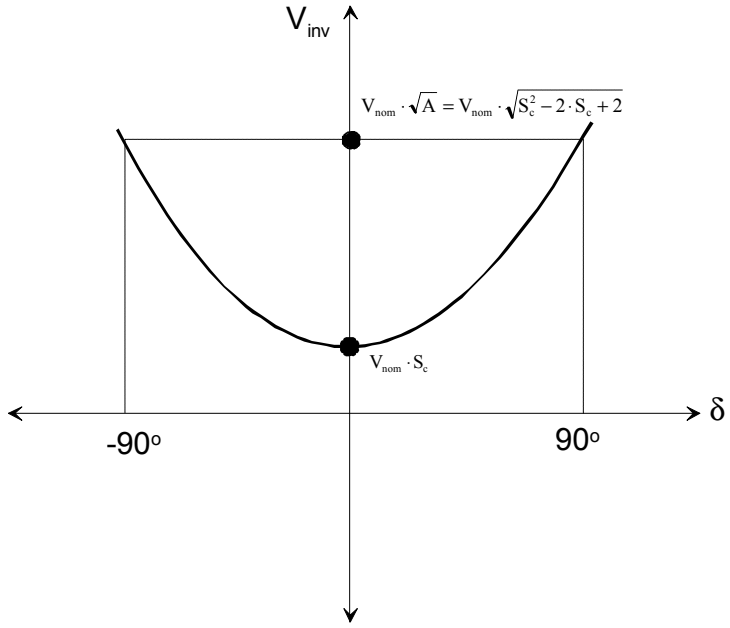


Figure 3.26. V_{inv} vs. δ for a specific S_c.

If Figure 3.26 is extended for different sag coefficients, then a family of curves shown in Figure 3.27 is obtained. If S_c is equal to 1, load voltage is supplied by the inverter only and $V_{inv} = V_{nom}$ for all values of load angle, while if S_c is equal to 0, the required inverter voltage is zero for zero load angle, as seen in Figure 3.27.

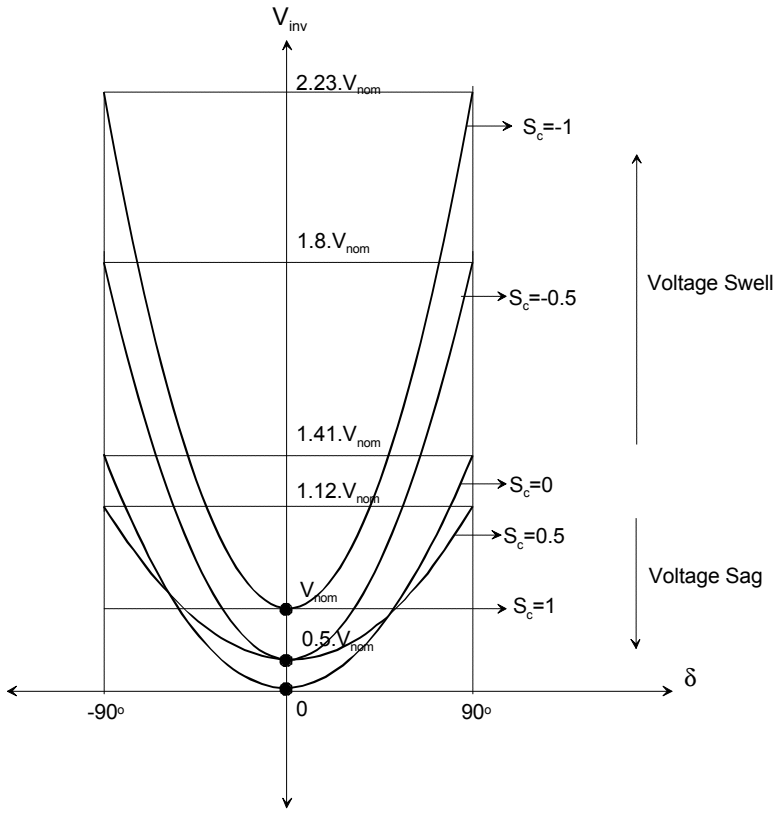


Figure 3.27. V_{inv} vs. δ characteristics for various S_c.

3.2.3 Various Operating Conditions Depending on Load Angle, d

MEVR could be operated at various values of load angle, δ, if the required inverter voltage is available (This subject will be discussed in the next sections). Therefore, the phasor diagram in Figure 3.24 changes according to these operating conditions. In this section, these operating conditions are shown using phasor diagrams.

Case 1: If $\delta = \delta_{opt} = \theta > 0$:

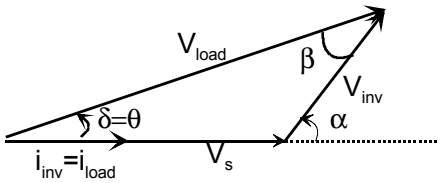


Figure 3.28. Phasor diagram for $\delta = \delta_{opt} = \theta$.

Case 2: If $0 < \delta < \theta$:

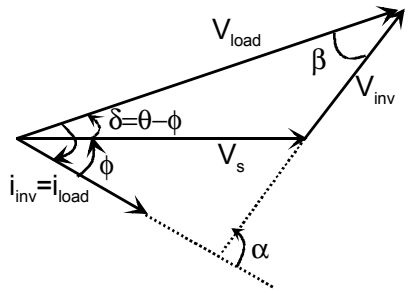


Figure 3.29. Phasor diagram for $0 < \delta < \theta$.

Case 3: If $\delta > \theta$:

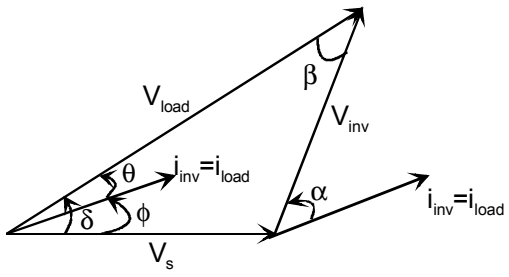


Figure 3.30. Phasor diagram for $\delta > \theta$.

Case 4: If $\delta = 0$ (In-phase Condition):

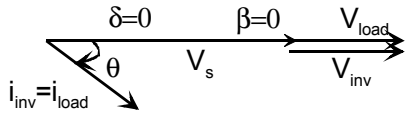


Figure 3.31. Phasor diagram for $\delta = 0$.

All voltages (V_s, V_{load},V_{inv}) are in-phase for zero load angle condition. If this load angle condition is utilized in Eqn.3.25, then Eqn.3.39 is derived.

$$V_{inv} = V_{nom} \cdot |S_c| \tag{3.39}$$

Under in-phase condition, $\beta = 0$ as seen in Figure 3.31.

Case 5: If $\delta < 0$:

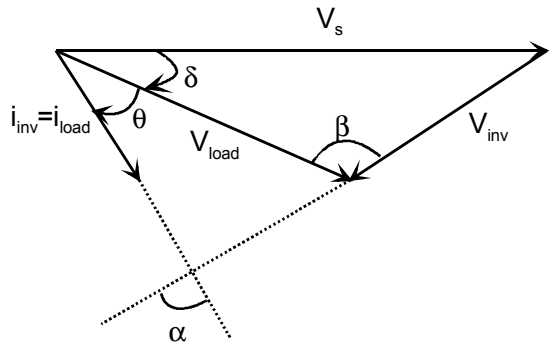


Figure 3.32. Phasor diagram for $\delta < 0$.

In this case,

$$\phi = \theta + |\delta| \tag{3.40}$$

For negative load angles, all previous equations are valid.

3.2.4 Possible Load Angle Range for Inverter Power Minimization

It was previously discussed that it is not possible to inject the required inverter voltage for some conditions since this voltage may not be available from the energy storage capacitors. In this section, the maximum voltage available from the inverter for a given condition will be calculated. This maximum available voltage will also change, depending on the following cases:

- If circuit is at steady state (capacitors have discharged down to the source voltage value), or
- If the circuit is at transient conditions (capacitor voltage is still greater than the source voltage)

This maximum available voltage will also depend on whether overmodulation is allowed for the inverter, or not.

3.2.4.1 Steady State Condition Without Overmodulation

For steady state condition, the peak of the source voltage is equal to capacitor voltages. Therefore, maximum inverter voltage is equal to source voltage and capacitor voltage. The maximum rms voltage that the inverter can supply at steady state is given by Eqn.3.41.

$$V_{inv,max} = V_s = V_{nom} \cdot (1 - S_c) \tag{3.41}$$

It is clear that the maximum inverter voltage is independent of load angle. In order to calculate the range of load angles where the maximum inverter voltage is equal to or greater than required inverter voltage, Eqn.3.41 is solved with Eqn.3.34.

$$\Rightarrow V_{inv,max} = V_{inv,required} \tag{3.42}$$

$$\Rightarrow (1 - S_c) \cdot V_{nom} = V_{nom} \cdot \sqrt{A + B \cdot Cos\delta_{vpossible}} \tag{3.43}$$

$$\delta_{vpossible} = \pm Cos^{-1}\left(\frac{-1}{2 \cdot S_c - 2}\right) \tag{3.44}$$

3.2.4.2 Steady State Condition With Overmodulation

If overmodulation is allowed at the PWM operation of IGBTs and $V_{dc1}=V_{dc2}=V_{dc}$, then the maximum inverter voltage is obtained by Eqn.3.45.

$$V'_{inv,max} = \frac{4}{\pi} \cdot V_{dc} = \frac{4}{\pi} \cdot (1 - S_c) \cdot V_{nom} \tag{3.45}$$

In order to calculate the range of load angles where the maximum inverter voltage is equal to or greater than required inverter voltage, Eqn.3.45 is solved with Eqn.3.34.

$$\Rightarrow V'_{inv,max} = V_{inv,required} \tag{3.46}$$

$$\Rightarrow \left(\frac{4}{\pi}\right)^2 \cdot \left(1 - 2 \cdot S_c + S_c^2\right) = \left(S_c^2 - 2 \cdot S_c + 2\right) + \left(2 \cdot S_c - 2\right) \cdot \mathrm{Cos}\delta'_{\mathrm{vpossible}} \tag{3.47}$$

$$\delta'_{\mathrm{vpossible}} = \pm \mathrm{Cos}^{-1} \frac{\frac{16}{\pi^2} \cdot S_c^2 - S_c^2 + 2 \cdot S_c - \frac{32}{\pi^2} \cdot S_c + \frac{16}{\pi^2} - 2}{2 \cdot S_c - 2} \tag{3.48}$$

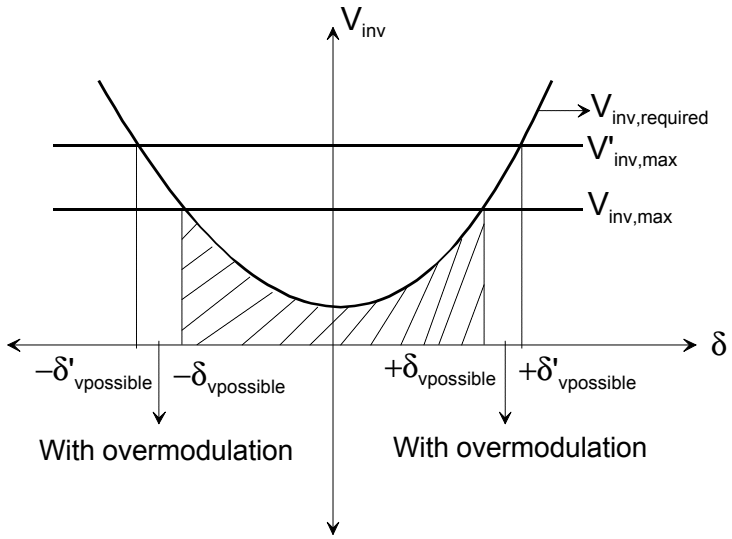


Figure 3.33. Comparison of possible load angles ($\delta_{\mathrm{vpossible}}$ and $\delta'_{\mathrm{vpossible}}$).

The variation of possible load angle range expands while S_c decreases. In Figure 3.34, the relationship between positive possible load angle and sag coefficent is given. For S_c >= 0.5 and no overmodulation, δ is not defined as can be seen in Figure 3.34. As seen from Figure 3.34, utilizing overmodulation leads to wider operation range for voltage sags.

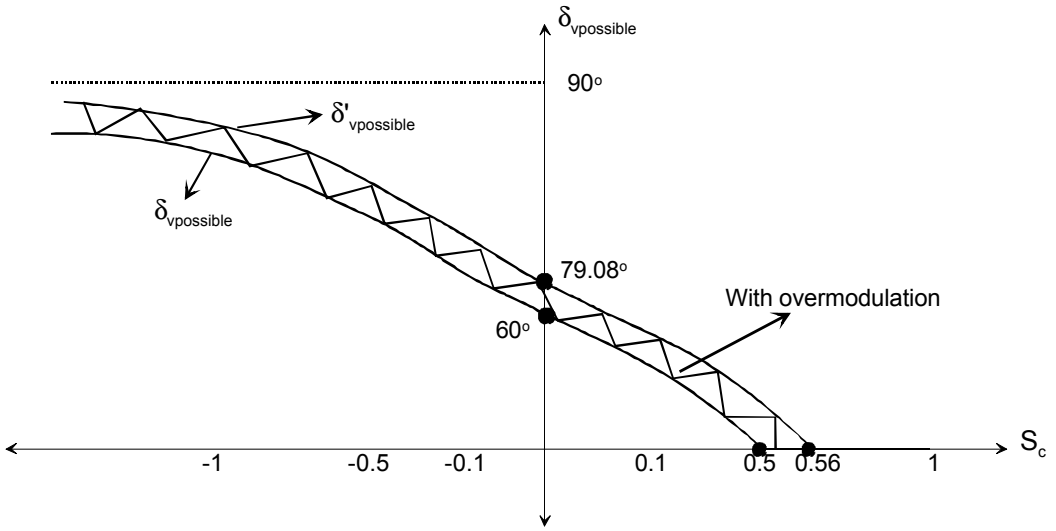


Figure 3.34. Relationship between $\delta_{vpossible}$ vs. S_c and $\delta'_{vpossible}$ vs. S_c.

3.2.4.3 Transient Condition Without Overmodulation

For the transient conditions, the maximum available inverter voltage can not be related to the source voltage because the capacitors are not discharged completely. Therefore, the more general expression which relates capacitor voltages to maximum available inverter voltages is utilized instead. For $V_{dc1}=V_{dc2}=V_{dc}$,

$$V_{inv,max} = \frac{V_{dc}}{\sqrt{2}} \tag{3.49}$$

To obtain possible load angle range, Eqn.3.49 is solved with Eqn.3.34.

$$\delta_{vpossible} = \pm \mathrm{Cos}^{-1}\left(\frac{V_{dc}^2}{2\cdot(2S_c-2)\cdot V_{nom}^2} - \frac{S_c^2-2\cdot S_c+2}{2\cdot S_c-2} \right) \tag{3.50}$$

3.2.4.4 Transient Condition With Overmodulation

If overmodulation is allowed, the maximum inverter voltage is greater than Eqn.3.49. For $V_{dc1}=V_{dc2}=V_{dc}$,

$$V'_{inv,max} = \frac{4}{\pi} \cdot \frac{V_{dc}}{\sqrt{2}} \tag{3.51}$$

To obtain possible load angle range, Eqn.3.51 is solved with Eqn.3.34.

$$\delta'_{vpossible} = \pm \mathrm{Cos}^{-1}\left(\frac{16 \cdot V_{dc}^2}{2 \cdot \pi^2 \cdot (2S_c - 2) \cdot V_{nom}^2} - \frac{S_c^2 - 2 \cdot S_c + 2}{2 \cdot S_c - 2} \right) \tag{3.52}$$

3.2.5 Control Methods for MEVR

In this section, three different control methods possible for MEVR are given and discussed. These are,

1. In-Phase Injected Voltage Method: This is the simplest control method for voltage sag correction.
2. Injected Power Minimization Method: This is a more complex method which involves phase shifting the injected voltage in order to minimize the injected power, therefore extending the discharge duration of the capacitors.
3. Closed Loop Control Method: This is a method proposed by Tsai [10] which directly utilizes a feedback from the load voltage to determine the inverter voltage.

3.2.5.1 In-Phase Injected Voltage Method

In this section, the two-switch single phase MEVR is analyzed using phasor analysis for the in-phase injected voltage method, which is the simplest method for MEVR sag correction.

The source voltage is measured and compared with the reference voltage. The missing voltage for voltage sag is injected by the inverter which is in-phase with the source voltage. No feedback from the actual load voltage is taken. Figure 3.35 shows the block diagram of this control logic.

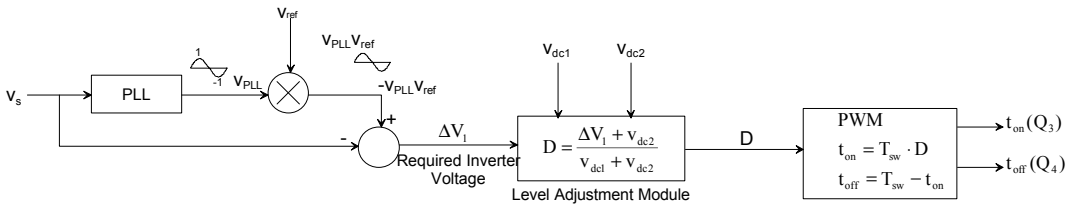


Figure 3.35. The block diagram of the in-phase injected voltage method.

The source voltage is measured and a PLL (Phase Locked Loop) block is used to generate a unit sine wave which is in-phase with the source voltage. This sine wave is multiplied by the reference voltage (V_{ref}) which is a constant value. The product of this multiplication is equal to the sine wave which is desired at the output of the regulator. Thus, this voltage has the same phase and zero-crossing points with the source voltage. Then the control software calculates the difference between the desired voltage and the actual source voltage (V_s). This difference between the desired and actual source voltages is called ? V_1.

$$\Delta V_1 = V_{ref} \cdot V_{PLL} - V_s \tag{3.53}$$

If there is a voltage sag, ? V_1 is not equal to zero. This is the missing voltage, which should be injected by the inverter. Therefore, the reference voltage of the inverter is ? V_1.

This signal (? V_1) is sent to the "Level Adjustment Module" and then to the PWM Generation Module. Both of these modules are common to all three control methods. Thus, these two modules will be described in only this control method.

The Level Adjustment Module is a requirement of this circuit topology because the injected voltage is limited by the voltages available at that instant on capacitors C_{dc1} and C_{dc2}. Therefore, in addition to the signal ? V_1, this module measures V_{dc1} and V_{dc2} to determine the duty cycle (D) of the PWM signal. This module is called "Level Adjustment Module" because the level of capacitor voltages affect the duty cycle. D is duty cycle of top IGBT (Q_3). Thus, (1-D) is duty cycle of bottom IGBT (Q_4). The level adjustment module utilizes ? V_1, the energy storage capacitor voltages and calculates the duty cycle, D, for PWM operation.

$$D = \frac{\Delta V_1 + V_{dc2}}{V_{dc1} + V_{dc2}} \tag{3.54}$$

Note that, if D is greater than 1, it is limited to 1 and if D is less than zero, it is limited to 0. This means the resultant value of D will always be between 0 and 1. The logic behind Eqn. 3.54 can be explained as follows:

There are two energy storage capacitors on the regulator: C_{dc1} and C_{dc2}. Assuming that these capacitors are initially fully discharged, during first positive half cycle of source voltage, C_{dc2} is charged to peak value of the source voltage (311 V for 220 V_{rms} nominal voltage) through diode D_2. This is Mode a (see sec.3.1.3). During first negative half cycle of the source voltage, C_{dc1} is charged to peak value of the source voltage through diode D_1. This is Mode b. During voltage sags, energy storage capacitors are continuously charged and discharged. Since the peak value of the source voltage is less than nominal value during voltage sags, the energy storage capacitors will usually be charged to a lower value.

Assuming C_{dc1} and C_{dc2} are charged, if the top IGBT is switched on, then V_{dc1} is added to the source voltage (Mode 3). If the bottom IGBT is switched on, then V_{dc2} is subtracted from the source voltage (Mode 4). Thus, by switching between Mode 3 and Mode 4 successively, the controller can increase or decrease the instantaneous voltage at the output of the inverter. The instantaneous value of ΔV_1 (missing voltage) should determine the amount of voltage to be added or subtracted during a particular switching cycle.

Thus, the inverter will be producing PWM pulses at the inverter output. These will be superimposed on the sinusoidal source voltage as illustrated in Figure 3.36.

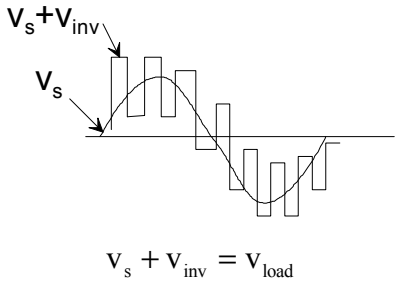


Figure 3.36. Unfiltered load voltage.

The duty cycle of each PWM pulse is calculated as follows:

To calculate the mean voltage of the inverter output for one switching period (T_{sw}), the volts-seconds balance principle is employed (Figure 3.37).

For one inverter switching cycle:

$$V_{inv,mean} \cdot T_{sw} = t_{on} \cdot V_{dc1} - t_{off} \cdot V_{dc2} \tag{3.55}$$

$$V_{inv,mean} = \frac{t_{on} \cdot V_{dc1} - t_{off} \cdot V_{dc2}}{T_{sw}} = \frac{t_{on} \cdot V_{dc1} - (T_{sw} - t_{on}) \cdot V_{dc2}}{T_{sw}} \tag{3.56}$$

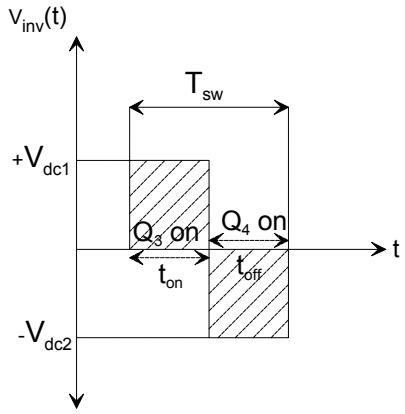


Figure 3.37. Inverter output voltage.

Note that $V_{inv,mean}$ should be equal to the missing voltage (ΔV_1) during that switching cycle. Using Eqn. 3.56, duty cycle, D, of top IGBT (Q_3) is obtained as:

$$D = \frac{t_{on}}{T_{sw}} = \frac{V_{inv,mean} + V_{dc2}}{V_{dc1} + V_{dc2}} = \frac{\Delta V_1 + V_{dc2}}{V_{dc1} + V_{dc2}} \tag{3.57}$$

In Eqn.3.57, all parameters (ΔV_1, V_{dc1}, V_{dc2} and T_{sw}) are known, so the duty cycle, D, and t_{on} for the top IGBT can be calculated. Then, the control software generates the PWM1 and PWM2 signals according to this duty cycle.

This is the simplest control method for MEVR since all voltage phasors (source voltage, injected voltage and load voltage) are in-phase. Therefore, they can be added as scalar quantities. Figure 3.38-(a) shows phasor diagram for the inductive load while Figure 3.38-(b) shows phasor diagram for the capacitive load for voltage sag condition.

Figure 3.38. Phasor diagrams for voltage sags:
(a) Inductive load, (b) Capacitive load.

However, this control method can not be utilized for voltage swell correction unless the diode rectifier is replaced by an input stage converter with controlled switches which allows bidirectional power flow, as well as the addition of Transient Voltage Surge Supressors (TVSS) for protection against sudden voltage surges.

During voltage swells, there is an overvoltage at the input of the circuit. Voltage swell causes overcharging of the DC bus capacitors. When the voltage swell occurs at the source side, it is required that a negative voltage (180° phase shift with respect to source) is injected by the inverter. This negative voltage will be added to the source voltage to reduce it. However, for voltage swell condition, the inverter power becomes negative ($P_{inv} < 0$).

Figure 3.39. Phasor diagrams for voltage swells:
(a) Inductive load, (b) Capacitive load.

As shown in Figure 3.39, for voltage swell, the angle between the inverter voltage vector and load current (inverter current) vector is always greater than 90º, causing inverter power to be negative as discussed in previous paragraph. As a result, the energy storage capacitors may become overcharged and the excessive voltage may become higher than the IGBT collector-emitter voltage blocking ratings. Consequently, the IGBTs and DC bus capacitors may be damaged due to overvoltage.

3.2.5.2 Injected Power Minimization Method

The purpose of minimizing the injected power is to obtain rated load power while utilizing the source more effectively. In other words, it is aimed that source power

is employed as much as possible compared to inverter power for supplying the load. Thus, the power drawn from the inverter is decreased as much as possible, decreasing the discharge rate of the capacitors and extending the holding time of MEVR. Applying this approach, the source power factor is improved but the inverter (injecting) voltage is increased. However, the voltage supplying capacity of the inverter is limited by the energy storage capacitor voltages. Thus, the minimum injection power approach can not be employed for all conditions as discussed in section 3.2.4.

As discussed in section 3.2.1, minimum value of inverter power can be positive, zero or negative. However, negative values of inverter power should be avoided to prevent overcharging of capacitors. Therefore, if the minimum inverter power is negative, zero inverter power should be utilized instead of minimum inverter power. Minimum inverter power or zero inverter power conditions can be achieved by adjusting the load angle, δ, as described in section 3.2.1. This means that the injected voltage and the load voltage will not be in-phase with the source voltage.

The block diagram of this control method is shown in Figure 3.40. This block diagram also includes an algorithm for determining the best value of load angle for the given operating conditions. This algorithm is given in Figure 3.41.

The injected power minimization method is more complicated compared to the in-phase injected voltage method. It can be implemented on a fast microcontroller (such as a DSP). Its advantage is that it draws the minimum power possible from the inverter during a voltage sag, and extends the holding time of the DC bus capacitors.

This method is also applicable for voltage swell conditions. During a voltage swell, the algorithm will automatically select a load angle which produces zero inverter power and avoid overcharging of the capacitors. No power will flow back to the input side, so a bidirectional input converter is not required.

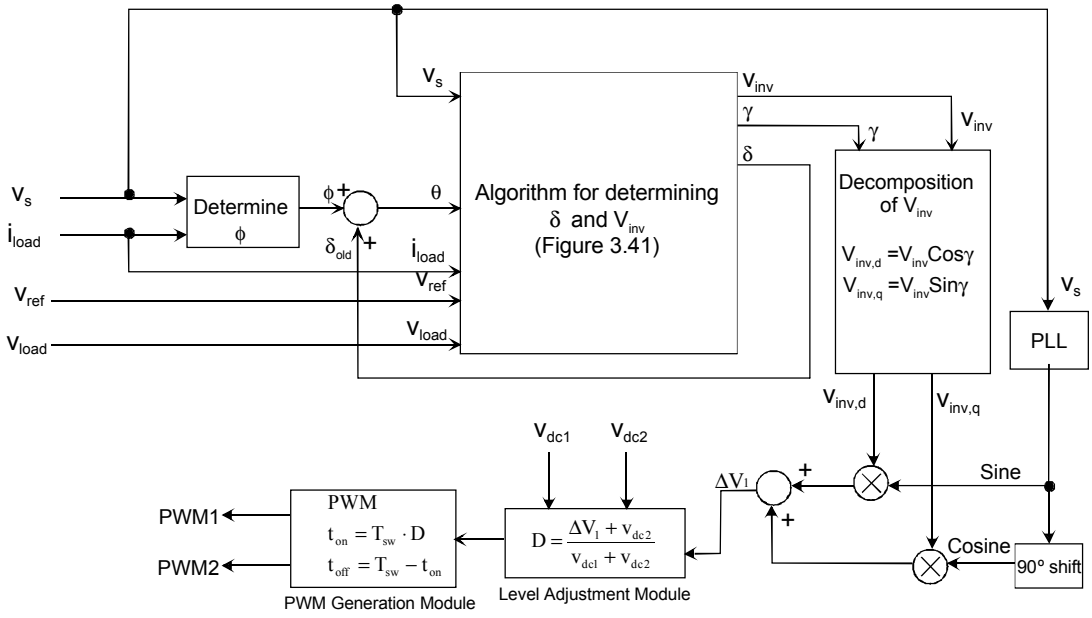


Figure 3.40. The block diagram of the injected power minimization method.

3.2.5.3 Closed Loop Control Method

This control method has been proposed by Tsai [10] for MEVR. In this method, the following feedbacks are used: V_{dc1}, V_{dc2}, V_{load}, V_s. A simplified form of Tsai's control block diagram is given in Figure 3.42. This control method can be utilized for both voltage sag and swell correction. However, the operation of the controller is different for voltage sags and swells.

For sag correction: The controller measures the load voltage (V_{load}) and calculates the rectified mean value of this voltage. The resulting DC signal is proportional with the load voltage's magnitude. This is compared with a reference value (V_{ref}). The difference between the two signals is the error signal (V_{err}), which is also the input of a PI-controller (this is called "DC Voltage Regulator" by Tsai).

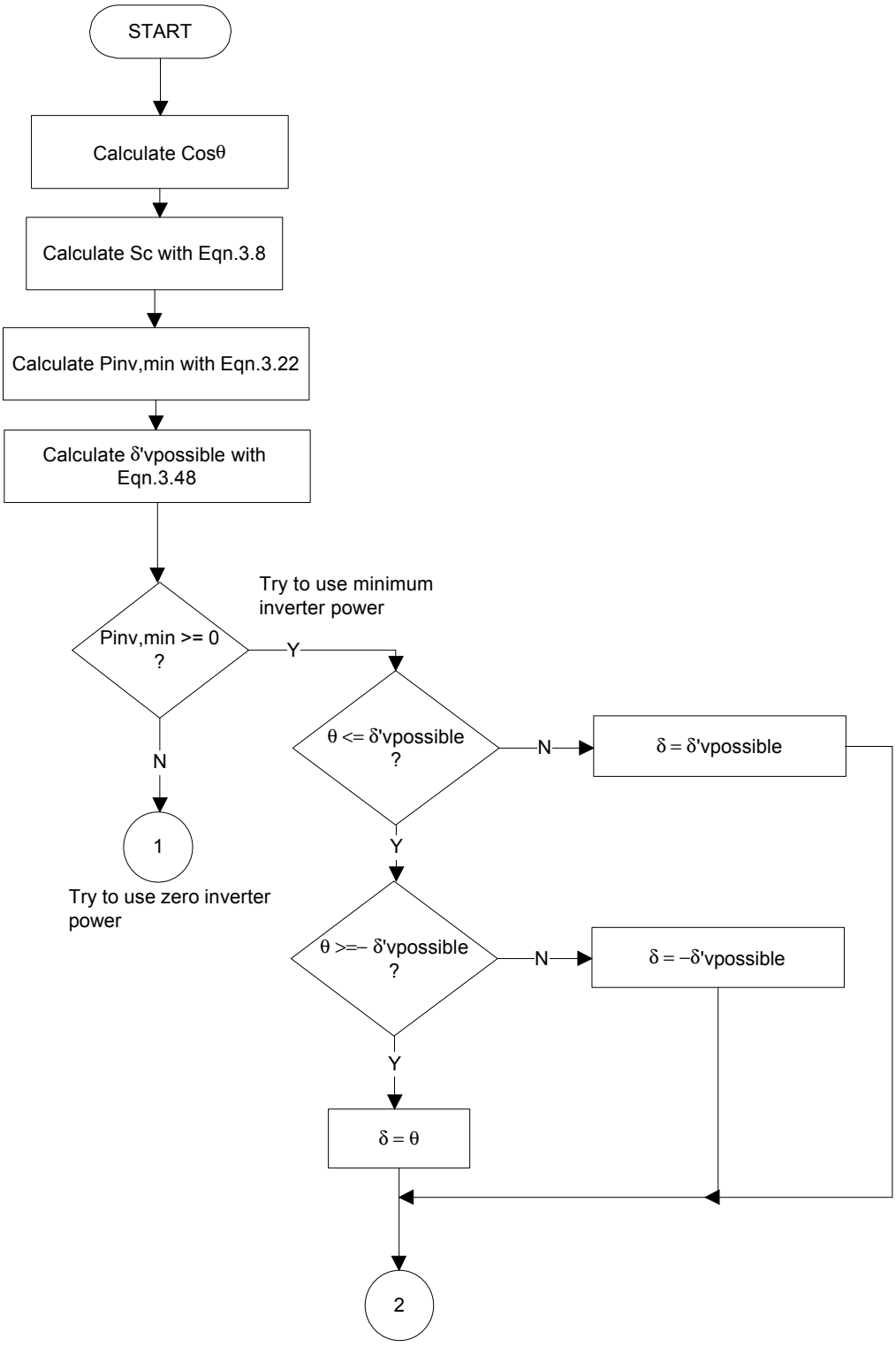


Figure 3.41. Flowchart of load angle determination algorithm.

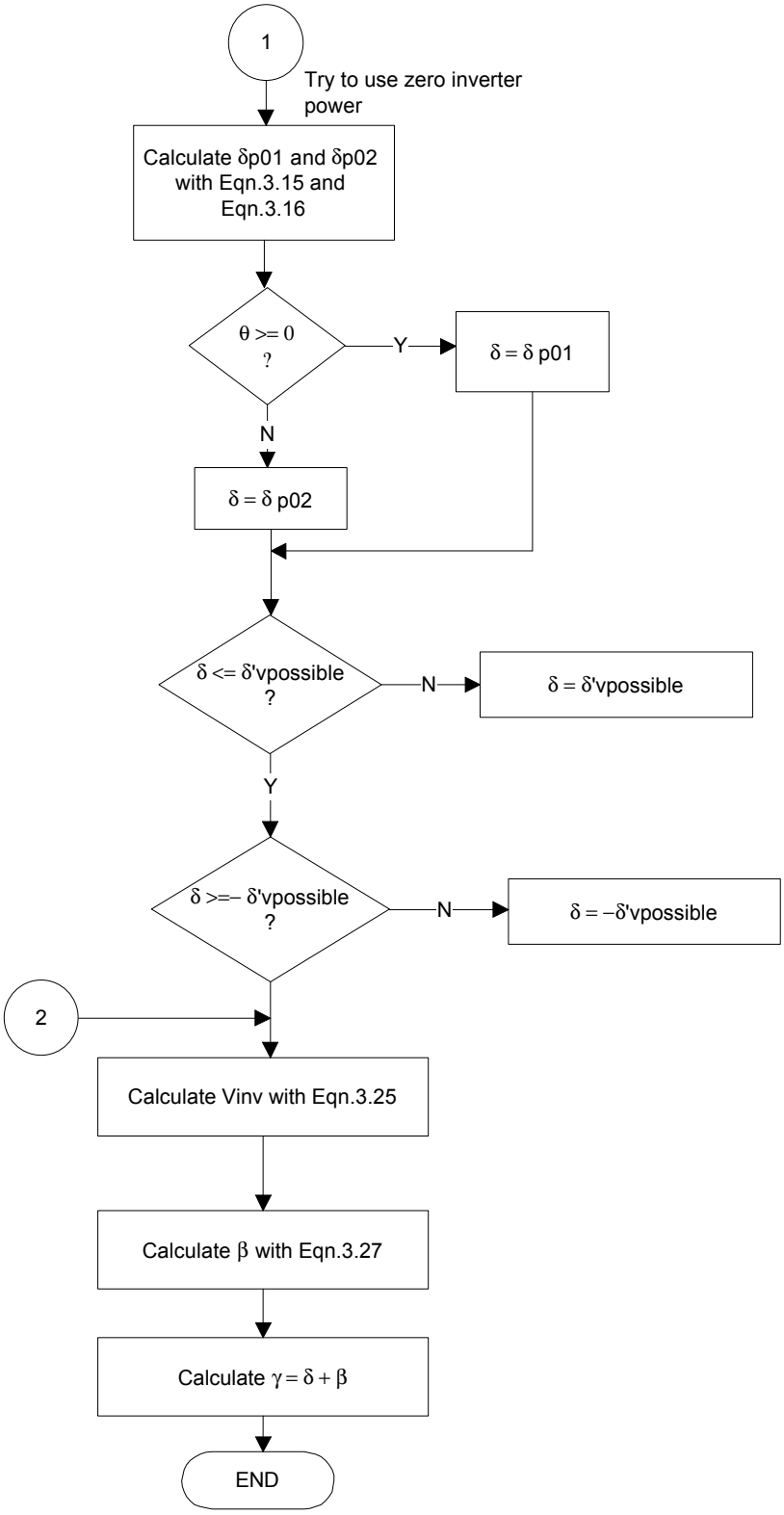


Figure 3.41. (cont'd).

The output of the PI-controller is multiplied by a unit sine wave (v_{ac}) which is produced by the phase locked loop (PLL) module. v_{ac1} is the sine wave which is in-phase with source voltage and supplied for only voltage sag conditions. v_{ac2} is the cosine wave which is quadrature with source voltage and it is different from zero when there is a voltage swell. Note that for voltage sag conditions, there will be no cosine component ($v_{ac2} = 0$) because the energy storage capacitor voltages will be less than the set value (V_{dcset}).

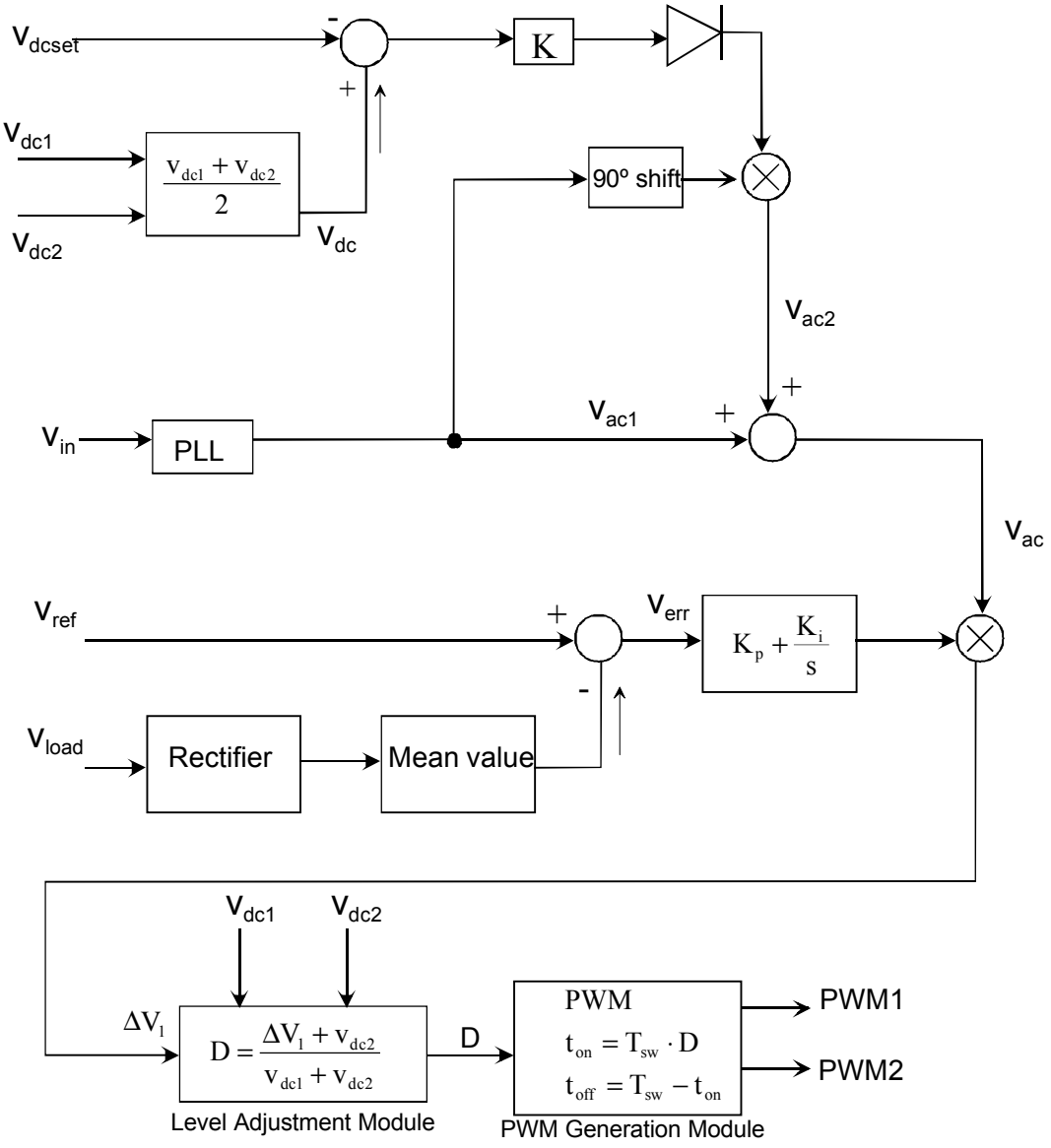


Figure 3.42. The block diagram of closed loop control method [10].

Thus, the output of the gain "K" will be negative and the following block will produce a zero voltage signal. This block behaves similar to a diode. If K is positive, then the output of block is different from zero. If K is negative, then the output of this block is equal to zero.

v_{ac} is the summation of v_{ac1} and v_{ac2}. v_{ac} determines the phase of the injected inverter voltage. The output of the PI controller determines amplitude of the inverter voltage. The required inverter voltage, ΔV_1, is formed by multiplication of output of the PI controller and v_{ac}.

The remaining part of the controller (Level Adjustment and PWM Generation) are the same as in the other control methods. (Tsai has implemented these parts in a more complicated manner, with additional feedbacks from the load voltage, source voltage and load current. However, the end result will be similar in function to the Level Adjustment and PWM Generation modules used in this thesis.)

For Swell Correction: The controller generates a phase shift in the inverter voltage. (For voltage sags, the inverter voltage is in phase with the source voltage). Phase shifting is applied to the inverter voltage to avoid overcharging the capacitors during voltage swells.

For voltage sags, the inverter voltage has only one component: In-phase component with source voltage. However for voltage swells, the inverter voltage needs to have two components in order to provide phase shifting: In-phase component and quadrature component.

The controller shown in Figure 3.42 operates similarly voltage sag operation during voltage swells. The main differences compared to voltage sag operation can be listed as follows:

i. As the load voltage (V_{load}) is greater than the reference voltage (V_{ref}), the error signal (V_{err}) and the output of PI-controller will be negative.

ii. At the beginning of a voltage swell, the inverter voltage will be in-phase with the source voltage because the quadrature component for the inverter voltage has not been obtained yet. This will cause a negative inverter voltage to be injected (i.e. the phase difference between V_{inv} and V_s is 180º). This, in turn, will cause the inverter power to have a negative value, overcharging the energy storage capacitors. The controller will respond to this by obtaining a positive quadrature term: The mean capacitor voltage (V_{dc}) will be greater than the set value (V_{dcset}), resulting in a positive value at the output of the gain block "K". Hence, the 90º phase-shifted unit cosine wave will be multiplied by this factor. This means that if the capacitor voltages increase, the amplitude of the quadrature term will be increased by the same amount, causing a phase shift of the inverter voltage as well as an increase in its overall magnitude.

The overall result is that the quadrature component of the inverter voltage determines phase shifting of inverter voltage. The amplitude of quadrature component is proportional to the difference between mean capacitor voltages (V_{dc}) and the reference capacitor voltage (V_{dcset}).

This controller uses three important coefficients which should be determined. These are: The integrator gain (K_i), proportional gain (K_p) and the gain of the DC bus control section (K). K_i accumulates error and does not respond quickly. When the error becomes zero, the integrator output takes a constant value. This means that V_{load} is equal to the desired reference value. However, K_p responds quickly with respect to K_i. This gain value produces an output which is proportional to input error. The value of K is important in determining the amplitude of the quadrature component of the inverter voltage.

3.2.5.4 Comparison of In-Phase And Energy Minimization Methods

In this section, the performance of two control methods, in-phase injected voltage method and injected power minimization method are compared. The comparison is made for three different sag conditions: S_c = 0.3, 0.5 and 0.7. The load conditions for this analysis are Cos(θ) = 0.8 (inductive), P_{load} = 1 kW. The nominal voltage is V_{nom} = 220 V and the load current is I_{load} = 5.68 A. For injected power minimization method, the block diagram in Figure 3.40 and flowchart in Figure 3.41 have been utilized. The required d and q components of the inverter voltage have been calculated using this method and MEVR has been simulated as described in chapter 4.

The method of calculation for S_c = 0.3 is given below as an example.

a) In-phase injected voltage control method for S_c = 0.3

V_s = 154 V from Eqn.3.10.
$V_{inv} = V_{load} - V_s$ = 66 V
δ = 0 (because in-phase injected voltage control method is used)
θ = ϕ = 36.87°
P_{inv} = 299 W from Eqn.3.11.

The phasor diagram for this condition is given in Figure 3.43.

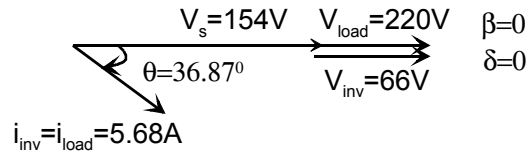


Figure 3.43. Phasor diagram for S_c = 0.3 and in-phase injected voltage control method.

b) Injected power minimization method for $S_c = 0.3$

$P_{inv,min} = 124.96$ W from Eqn.3.22.

Since $P_{inv,min} > 0$, the inverter energy can be minimized. Utilizing the flow chart in Figure 3.41, $\delta'_{vpossible} = \pm 60.20°$ as calculated by Eqn.3.48. Since, for minimum inverter power, the load angle, $\delta = \theta = 36.87°$ and this value is within the limits of $\delta'_{vpossible}$, $P_{inv,min} = 124.96$ W

$V_{inv} = 133.82$ V from Eqn.3.25,
$\beta = 43.66°$ from Eqn.3.27,
$\gamma = 80.53°$ from Eqn.3.29,

The phasor diagram for this condition is given in Figure 3.44.

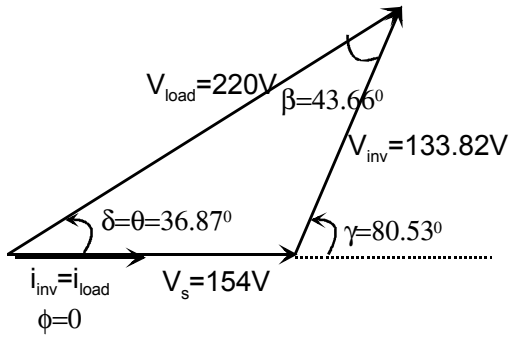


Figure 3.44. Phasor diagram for S_c=0.3 and injected power minimization control method.

The results for all three sag conditions are listed in Table 3.5. The results given in this table are theoretical calculations, but they have also been verified using simulation results. The source current THD values have been obtained from simulations.

The results indicate that,

- the active inverter power is decreased by an important amount if injected power minimization is used,
- however, higher values of inverter voltage need to be injected during injected power minimization, which causes higher values of apparent inverter power, S_{inv},
- injected power minimization method also decreases the THD of the source current,
- the load current and inverter current are not affected by these methods.

Table 3.5. Results of in-phase and injected power minimization calculations.

	S_c = 0.3		S_c = 0.5		S_c = 0.7	
	Inphase	**Min energy**	**Inphase**	**Min energy**	**Inphase**	**Min energy**
V_{inv}	66.00 V	133.82 V	110.00 V	140.00 V	The inverter could not inject required voltage.	
I_{inv}	5.68 A	5.68 A	5.68 A	5.68 A		
P_{inv}	300.00 W	124.96 W	500.00 W	374.82 W		
S_{inv}	374.88VA	760.09VA	624.80VA	795.20VA		
$I_{s,THD}$	14.0 %	12.5 %	12.4 %	11.4 %		

3.3 INVERTER HOLDING TIME AND ENERGY STORAGE CAPACITOR SIZING

In this section, an approach for sizing the energy storage capacitors will be established. The energy storage capacitors are C_{dc1} and C_{dc2} in Figure 3.4. The energy storage capacitor ratings should be determined and sized appropriately because the voltage injection capability of MEVR depends on the energy storage capacitor values. In addition to the capacitance value of the energy storage capacitors, a parameter that relates the capacitances to the voltage sag depth and duration of the sag compensation must be defined.

At the initial power-up stage the voltage regulator, the energy storage capacitors are assumed to be completely discharged. During the first cycle during which the source voltage is applied to MEVR, these capacitors will be charged through the diodes (D_1, D_2). This corresponds to Mode a and Mode b as explained in section 3.1.3.

In this work, the inverter holding time, T_h, will be defined as the duration of the inverter load voltage regulation capability while the voltage sag is present at the source side. It is obvious that, if there is less than the required voltage on the energy storage capacitors, then the line voltage regulator can not correct the voltage sag for a long duration. The inverter holding time depends on the voltage sag magnitude, load power, initial storage capacitor voltage, final storage capacitor voltage, and voltage tolerance.

3.3.1 Sizing of Energy Storage Capacitor

The objective of energy storage capacitor sizing study is to derive a mathematical relationship between the inverter holding time and the capacitor capacitance. This relationship will be verified by utilizing a circuit simulation tool. The following assumptions will be made for the storage capacitor sizing study.

1. There is a 100 % voltage sag at the source voltage (worst sag case),
2. There is a load which has constant power during a voltage sag, even if there is a decrease in the load voltage (i.e., a switched mode power supply type of load),
3. P_{load} is the average power drawn by the load, even if the number of sag cycles is not an integer. In other words, the instantaneous power variations within 1 cycle are ignored and average power remains the same.
4. Initially there is a nominal source voltage between the input terminals of the line regulator. The energy storage capacitors are initially charged to the peak source voltage (pre-sag voltage condition).

The given values for the analysis are the following:

1. $V_{dc,init}$: Initial capacitor voltage (at the beginning of the sag).
2. $V_{dc,fin}$: Final capacitor voltage (at the end of the operation).
3. T_h: Required inverter holding time with 100 % sag (interruption) while the inverter is capable of regulating the load voltage.
4. P_{load}: Load Power.
5. T_v: Voltage tolerance. This is the minimum allowable load voltage accepted as nominal in per unit (normalized to the rated voltage). For load voltage accepted as nominal, $V_{load} \geq T_v \cdot V_{nom}$
6. η: The energy efficiency of MEVR.

If we choose T_v as 0.9 and $V_{load,rms}$ is given as 220 V, then the minimum load voltage which is accepted as nominal is obtained as 198 V ($V_{load,rms} = 0.9 \cdot 220 = 198V$).

The storage capacitor voltage variations during T_h in this analysis are given in Figure 3.45. As seen in this figure, the voltage sag condition begins at time t_1. The DC bus voltage (V_{dc}) is defined as the mean of the two storage capacitor voltages as given by Eqn.3.58. If it is assumed that there is a nominal voltage (V_{nom}) at the source at t_1, the initial DC bus voltage is equal to the peak of the nominal voltage ($V_{dc,init} = V_{dc}(t_1) = \sqrt{2} \cdot V_{nom} = 311V$).

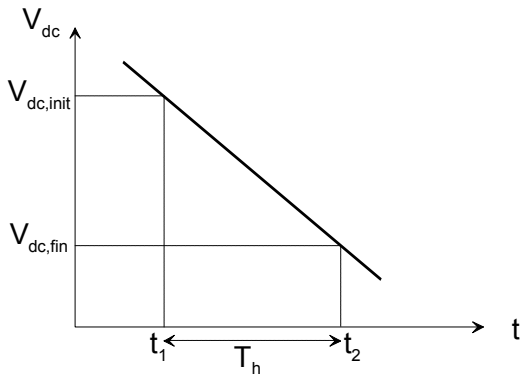


Figure 3.45. Storage capacitor voltage variation vs. time during deep sag compensation.

$$V_{dc} = \frac{V_{dc1} + V_{dc2}}{2} \tag{3.58}$$

The inverter supplies the load with the nominal voltage during T_h. $V_{dc,fin}$ is the average final storage capacitor voltage at time t_2 and it is given by Eqn.3.59. $V_{dc,fin}$ is the allowable minimum DC bus voltage in order to obtain a load voltage which is within the nominal range. This final voltage will be obtained as a function of the initial storage capacitor voltage in the following analysis.

$$V_{dc,fin} = \frac{V_{dc1,fin} + V_{dc2,fin}}{2} \tag{3.59}$$

The energy output from the inverter is equal to the difference between the total storage capacitor energy at the beginning of voltage sag correction and total storage capacitor energy at the end of the voltage sag correction. However, not all of the inverter energy is transferred to the load, but some of it is dissipated in the filter and the inverter switches. The inverter energy which is output to the load is transferred during T_h by the inverter efficiency, η, as written in Eqn.3.61. The storage capacitor value in Eqn.3.61 is given as C_{dc}. The storage capacitor values are taken as equal to each other.

$$C_{dc} = C_{dc1} = C_{dc2} \tag{3.60}$$

$$W_{inv} = 2 \cdot \frac{1}{2} \cdot C_{dc} \cdot \left(V_{dc,init}^2 - V_{dc,fin}^2 \right) \cdot \eta \tag{3.61}$$

The inverter energy can also be written in terms of the inverter power, P_{inv}, and the holding time as in Eqn.3.62.

$$W_{inv} = P_{inv} \cdot T_h \tag{3.62}$$

If Eqn.3.61 and Eqn.3.62 are solved together, then the energy storage capacitor equation as a function of efficiency, inverter power and holding time is derived as Eqn.3.64.

$$2 \cdot \frac{1}{2} \cdot C_{dc} \cdot \left(V_{dc,init}^2 - V_{dc,fin}^2 \right) \cdot \eta = P_{inv} \cdot T_h \tag{3.63}$$

$$C_{dc} = \frac{P_{inv} \cdot T_h}{\left(V_{dc,init}^2 - V_{dc,fin}^2 \right) \cdot \eta} \tag{3.64}$$

3.3.2 Determination Of The Holding Time

Eqn.3.64 will be extended to determine the holding time, T_h, for a given voltage sag condition. $V_{dc,fin}$ is the allowed voltage of the storage capacitor at the end of the voltage sag correction of the inverter. This final storage capacitor voltage determines inverter holding time (T_h). If this voltage is allowed to be lower, then T_h lasts longer.

In this section, it is assumed that the in-phase voltage injection method is applied to correct the voltage sag as this method requires the largest energy supply to the load (compared to injected power minimization method) and implies the worst case in terms of capacitor sizing requirements. This approach also results in simplified calculations. In this case, the load voltage is obtained by Eqn.3.65.

$$V_{load} = V_s + V_{inv} \tag{3.65}$$

If T_v is utilized in Eqn.3.65, then final (critical) value of capacitor voltage is obtained by Eqn.3.67. V_{nom} is the nominal load voltage in rms (220 V) in this equation.

$$V_{dc,init} = \sqrt{2} V_{nom} \tag{3.66}$$

$$V_{dc,fin} = \sqrt{2} V_{nom} T_v - \sqrt{2} V_{nom} \left(1 - S_c \right) \tag{3.67}$$

$$P_{inv} = S_c \cdot P_{load} \tag{3.68}$$

From Eqn.3.64,

$$T_h = \frac{C_{dc} \cdot \left(V_{dc,init}^2 - V_{dc,fin}^2\right) \cdot \eta \cdot}{P_{inv}} \tag{3.69}$$

$$\Rightarrow T_h = \frac{2 \cdot C_{dc} \cdot V_{nom}^2 \cdot \eta \cdot \left[1 - \left(T_v + S_c - 1\right)^2\right]}{S_c \cdot P_{load}} \tag{3.70}$$

Eqn.3.70 is valid for a certain range of voltage sags because for values of S_c which are less than a certain threshold, T_h will be infinity. Since MEVR is also a voltage doubler, this device is capable of supplying up to twice the source voltage to the load continuously. Therefore, there is a certain source voltage limit above which MEVR supplies desired load voltage continuously and the holding time is infinite.

The storage capacitor voltage is sufficient to inject the required inverter voltage for this condition, the load is supplied by nominal voltage within the tolerance limits continuously. Theoretically infinite inverter holding time means that the peak of the source voltage is greater than final storage capacitor voltage ($V_{dc,fin}$) value for this voltage sag condition. At this stage, this sag coefficient limit for infinite inverter holding time equation as a function of voltage tolerance (T_v) will be derived. During this limiting case, the voltage injected by the inverter is equal to the source voltage if the inverter is operated in the linear modulation region and does not enter the overmodulation region.

$$V_s = V_{inv} \tag{3.71}$$

$$V_s + V_{inv} = V_{load} = V_{nom} \cdot T_v \tag{3.72}$$

$$\Rightarrow 2 \cdot V_s = V_{nom} \cdot T_v \tag{3.73}$$

Solving Eqn.3.73 together with Eqn.3.10,

$$2 \cdot \left(1 - S_{c,limit}\right) \cdot V_{nom} = V_{nom} \cdot T_v \tag{3.74}$$

$$S_{c,limit} = 1 - \frac{T_v}{2} \tag{3.75}$$

As a result, the general expression for inverter holding time (T_h) is,

$$T_h = \begin{cases} \dfrac{2 \cdot C_{dc} \cdot V_{nom}^2 \cdot \eta \cdot \left[1 - \left(T_v + S_c - 1\right)^2\right]}{S_c \cdot P_{load}}, & S_c > 1 - \dfrac{T_v}{2} \\ \infty, & S_c \le 1 - \dfrac{T_v}{2} \end{cases} \tag{3.76}$$

Note that for in-phase voltage injection control, because common current flows in the circuit, the proportion of the source voltage to the inverter voltage is equal to the proportion of source power to the inverter power. This is also true for energy since all the power will flow for the same time duration as seen from Eqn.3.77.

$$\frac{V_s}{V_{inv,fund}} = \frac{1 - S_c}{S_c} = \frac{P_s}{P_{inv}} = \frac{W_s}{W_{inv}} \tag{3.77}$$

3.3.3 Calculations and Results for Capacitor Sizing and Holding Time

3.3.3.1 The Effect of MEVR Application on Capacitor Sizing

Capacitor sizing is determined by power quality (or voltage regulation capability) requirements of the application. For equipment conforming to ITIC specifications, for example, the equipment will operate in region A of Figure 3.46 without problems but will not be protected in region B of Figure 3.46 where sag problems are most frequent (see chapter 2). Therefore, MEVR which is to be designed to protect IT equipment should be designed such that region B is included in the protected region as well. Capacitor sizing should be made according to the limiting values of this region.

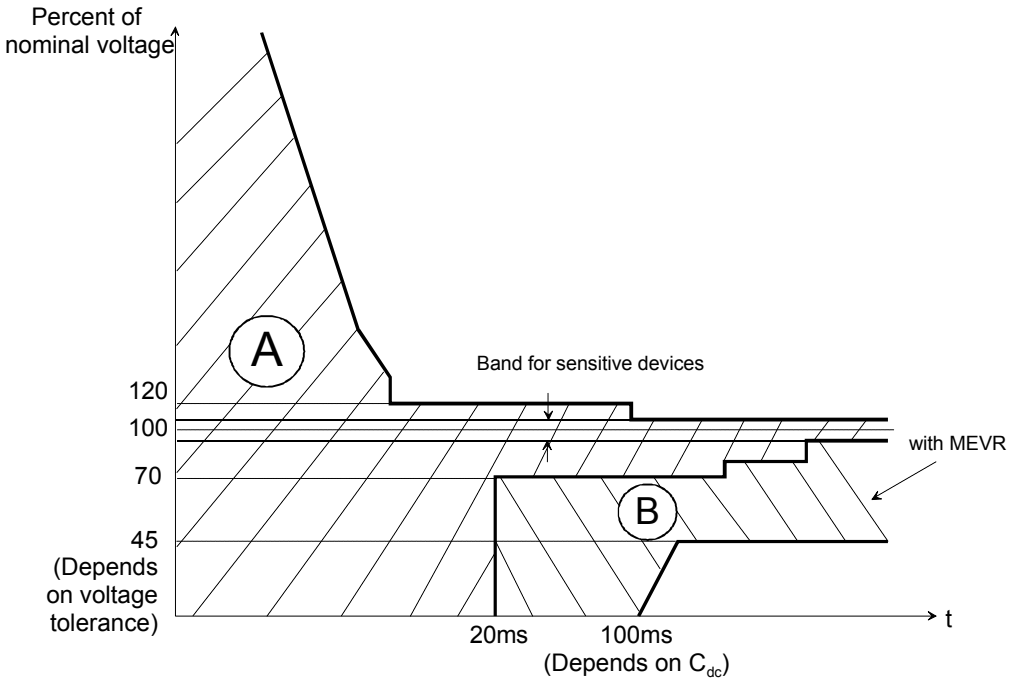


Figure 3.46. ITIC curve with MEVR.

ITIC curve for IT equipment was given in chapter 2. A simplified version of this curve is shown in Figure 3.46. As seen here, the IT equipment must operate without any problems in region A. However, these sensitive devices can not operate in region B with full performance or without problems. If a power conditioning equipment such as MEVR is installed between source and load, the region where the IT equipment operates without any interruption in its function will be extended to include region B as well as region A as shown in Figure 3.46.

The maximum duration for 100 % voltage sag depends on the size of the storage capacitors in MEVR. A typical value of 100 ms is indicated in Figure 3.46.

The upper limit for steady state operation of MEVR depends on T_v (voltage tolerance) as shown in Figure 3.46. This upper limit is investigated in detail in section 3.3.2.

There is a band on Figure 3.46 representing device sensitivity. This bandwidth changes with respect to device sensitivity. If the device is more sensitive to voltage variations, then this band is narrower. With decreasing device sensitivity, this bandwidth increases. In order to operate MEVR with more sensitive devices, the voltage sag limit (see section 3.1.2) should be selected closer to the nominal voltage. In this case, MEVR will have less tolerance on voltage sags and the inverter will start operating as soon as the line voltage drops below this threshold. Thus, MEVR can be used as a high quality voltage regulator with low error. However, the drawback of selecting a voltage sag limit close to nominal will be more frequent operation of the inverter, decreasing MEVR efficiency.

3.3.3.2 Determination of Energy Storage Capacitance

At this stage, the analytical formulas will be applied to calculate the storage capacitor value for a MEVR with 220 V and 1 kW ratings. In the design, the critical holding time will be selected as 3 cycles for 100 % voltage sag (worst case voltage sag) condition. This choice is based on the product datasheets of several commercial EVRs with similar attributes to MEVR. These equipment are designed for applications such as IT equipment and their purpose is to correct for the frequent voltage sags occuring in region B of Figure 3.46. After calculating the capacitance, the holding time of MEVR will be calculated for different voltage sag conditions.

In this analysis, the inverter efficiency should be known. The inverter efficiency will be obtained utilizing circuit simulation. To obtain inverter efficiency, the two-switch line voltage regulator is simulated for the 100 % voltage sag and the inverter losses are obtained utilizing calculation of conduction losses. In the circuit simulation, the load is an RL load with 1kW power rating at 220 Vrms. The switching frequency is 20 kHz. The energy storage capacitors are 1000 μF during efficiency calculations. The conduction losses are calculated for 1 cycle by simulator. The switching losses can not be calculated accurately by the simulator.

Therefore, the switching losses are assumed to be equal to conduction losses. Also, all the other losses including passive component losses in the inverter are taken as 1% of the inverter power (P_{inv}). P_{inv} is calculated as 1.037 kW and P_{others} is calculated as 10.367 W. The total inverter losses is calculated as 32.033 W and the inverter efficiency is calculated as 97 %. The calculation results are given in Table 3.6.

Table 3.6. Inverter conduction and switching losses.

	Conduction Losses (W) (Off-state +On-state)	**Switching Losses (W)**
Q_3	3.3661	3.3661
Q_4	3.4960	3.4960
D_3	2.1451	2.1451
D_4	1.8266	1.8266

$$P_{inv,losses} = P_{cond+switch} + P_{others} = 21.6676 + \frac{1}{100} \cdot P_{inv} = 21.6676 + 10.366 = 32.0336\text{W}$$

$$\eta = \frac{P_{inv}}{P_{inv} + P_{losses}} = \frac{1036.6}{1036.6 + 32.0276} = 97\%$$

For 100 % voltage sag condition, only the inverter supplies the load and the inverter power is equal to the load power (1000 W). Since the pre-voltage sag condition is the nominal source voltage, the initial storage capacitor voltage ($V_{c,init}$) is 311 V, the voltage tolerance (T_v) is taken as 0.9. The final storage capacitor voltage is equal to 280V (90 % of initial value). For a holding time of 3 cycles (60 ms), from Eqn.3.64, C_{dc} is calculated as **3.37 mF**.

At this stage, the inverter holding time for this storage capacitor value should be verified by the circuit simulation. Employing 3.37 mF for storage capacitor, the MEVR circuit is simulated to determine whether the designed MEVR is able to supply the load with nominal voltage for 3 cycles at 100 % voltage sag condition. This circuit simulation is run for the parameters in Table 3.7.

Table 3.7. Simulation parameters for verifying the energy storage capacitor size calculation.

Load	RL load, PF=0.8 lagging
C_{dc1},C_{dc2}	3.37 mF
L_f	3 mH + 0.2 Ω
C_f (Paralleled to load)	15 μF + 100 mΩ
Source voltage	0 (100 % voltage sag)

The load fundamental voltage amplitude is measured as 281 V at the end of three cycles. This amplitude is in the tolerance range of the load voltage because T_v is 0.9. It is observed that simulation results are in agreement with theoretical calculations.

3.3.3.3 Determination of Holding Time Value for Different Voltage Sags

The voltage sags are classified according to their durations (instantaneous, momentary, and temporary) as discussed in chapter 2. Utilizing Eqn.3.76, various inverter holding time values are obtained with respect to different voltage sag conditions, theoretically. These values are given in Table 3.8.

Table 3.8. $T_{h,theoretical}$ for various sag coefficients.

S_c	**$T_{h,theoretical}$**
1.0	60.00 ms (3 cycles)
0.8	201.72 ms (10 cycles)
0.6	395.53 ms (20 cycles)
<=0.5	∞

As seen from the results in Table 3.8, if the sag coefficient is greater than 0.5, then the inverter could correct voltage sags for a maximum of about 20 cycles (400 ms). These voltage sag durations are in the instantaneous voltage sag class. The required storage capacitor value for momentary and temporary voltage sags can be obtained utilizing Eqn.3.64. The required energy storage capacitor value for momentary voltage sags (3 seconds) is calculated as **168.80 mF**. The required energy storage capacitor value for temporary voltage sag (1 minute) is calculated as **3.38 F**. As the

capacitor size becomes large, it appears that MEVRs are effective for instantaneous and momentary voltage sags, but not temporary and deep voltage sags. It is apparent that for temporary deep sags, the cure is to utilize more effective energy storage elements such as batteries, flywheel systems, or continuous energy sources such as diesel generators and fuel cells.

3.3.3.4 Comparison of Holding Times: Theory vs. Simulation Results

As discussed above, the inverter holding time is obtained from two approaches:

1. Theoretically
2. Utilizing circuit simulation

The theoretical inverter holding time ($T_{h,theoretical}$) is calculated by Eqn.3.76.

The inverter holding time by simulation ($T_{h,simulation}$) is obtained by running MEVR circuit simulation. In these simulations, the MEVR full circuit model is run for the various voltage sags. The intersection point of V_{dc1} and the critical DC bus voltage value ($V_{ccritical}$) is taken as $T_{h,simulation}$ for that voltage sag condition. This subject will be discussed in chapter 4.

MEVR full model is simulated by the parameters which are given in Table 3.9. The applied sag coefficient range is from 0.5 to 1.

Table 3.9. Simulation parameters for calculation of $T_{h,simulation}$.

SIMULATION PARAMETERS	
Load types	RL with power factor 0.8
Load power at nominal voltage	1 kW
Storage capacitors (C_{dc1}, C_{dc2})	3.37 mF
Source resitance (R_s)	45 mΩ
Filter inductance (L_f)	3 mH
Filter capacitance (C_f)	15 μF
Initial capacitor voltage ($V_{dc,init}$)	311 V
Maximum time step	0.5 μs
Minimum time step	0.1 μs

$T_{h,theoretical}$ and $T_{h,simulation}$ are compared in Table 3.10. The comparison is also shown by Figure 3.47.

Table 3.10: T_h vs. S_c for RL load.

RL LOAD		
S_c	$T_{h,theoretical}$ (ms)	$T_{h,simulation}$ (ms)
1	60.00	58.00
0.9	126.57	126.00
0.7	289.30	289.00
0.6	395.53	405.70
0.55	458.82	467.50
0.5	∞	∞

From Figure 3.47 for T_h vs. S_c above, the following comments can be made:

1. Minimum T_h is observed for $S_c = 1$. T_h increases as S_c decreases.
2. T_h values and S_c match perfectly until 60 % voltage sag.

3.4 VOLTAGE SAG DETECTION METHODS AND DURATIONS

3.4.1 Voltage Sag Detection Methods

Voltage sag detection is one of the key points of MEVR control logic. The controller monitors the source voltage and compares it with a reference value continuously so that all the voltage variations can be detected. There are various sag detection methods but the following two criteria should be taken into account to select the best voltage sag detection method:

1. The selected method must detect voltage sags correctly without false alarms,
2. The selected method should detect voltage sags as soon as possible for quick correction.

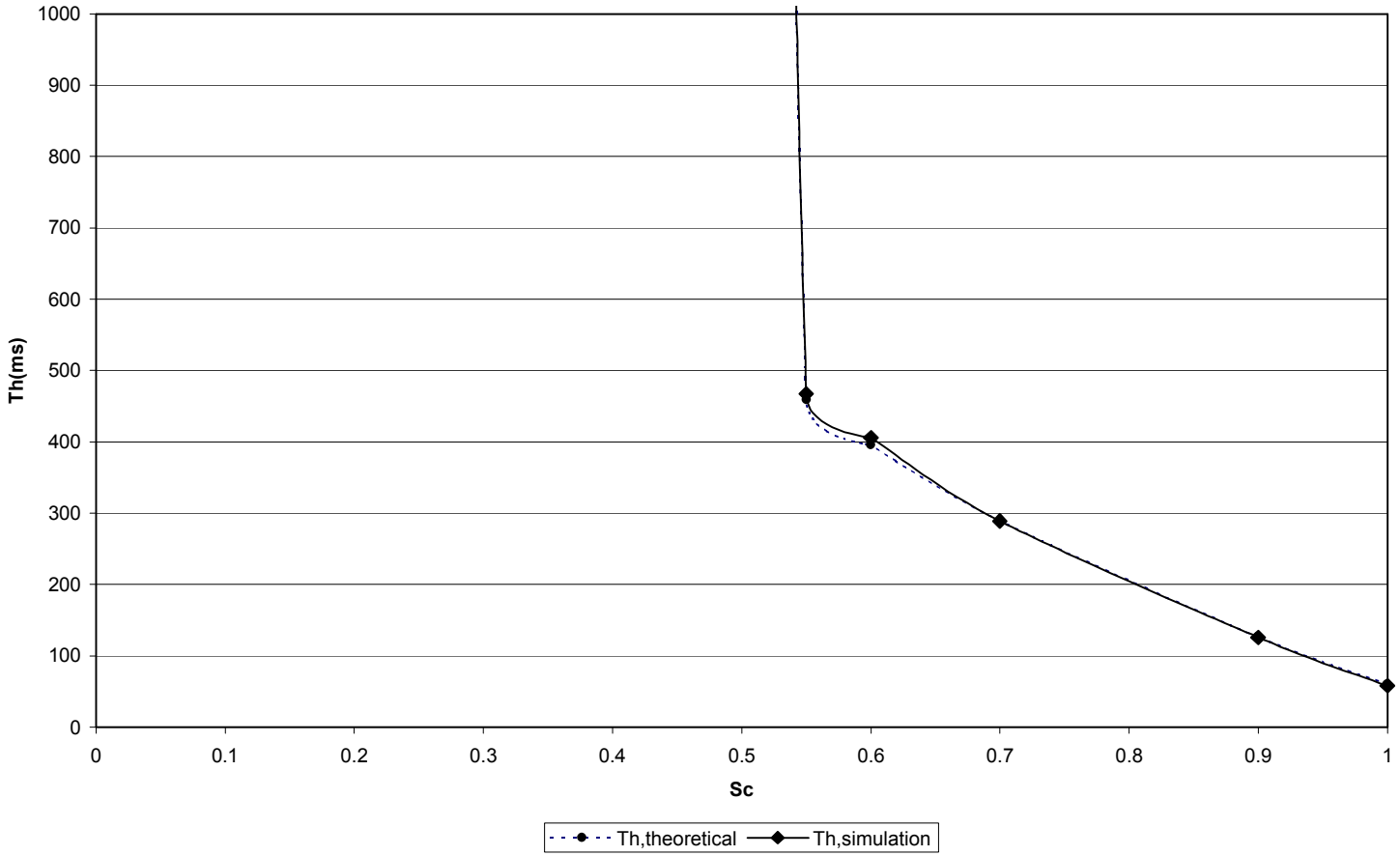


Figure 3.47. T_h vs. S_c comparison for RL load.

Five different voltage sag detection methods are discussed in the following sections.

3.4.1.1 Method 1: Comparing $|\Delta V_1|$ and V_{tol}

Method 1 compares ΔV_1 and a given tolerance value, V_{tol}. If $\Delta V_1 > V_{tol}$, then there is a voltage sag in the line. Otherwise, there is no voltage sag. ΔV_1 is the difference between the actual source voltage and the reference voltage. These two waves and ΔV_1 are sinusoidal waves.

$$\Delta V_1 = \left| V_{ref} \cdot V_{pll} - V_s \right| \tag{3.78}$$

V_s is the source voltage, V_{ref} is the given reference value, V_{pll} is the unit sinusoidal wave which has the same phase and zero-crossing points with the source voltage and V_{tol} is the defined tolerance value.

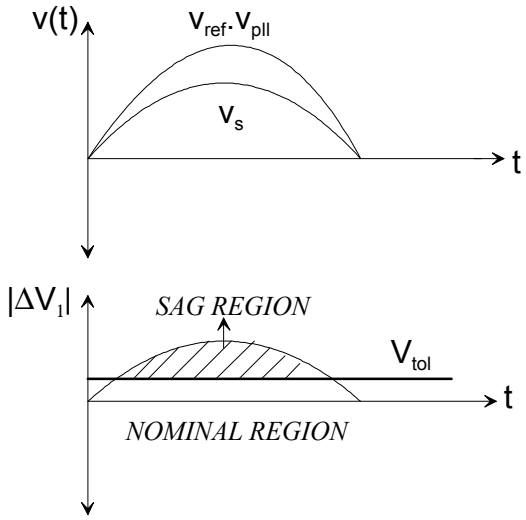


Figure 3.48. Comparing ΔV_1 and V_{tol} for voltage sag detection.

The advantage of this method is its simplicity. The disadvantage is that this method does not give accurate results for all points in a cycle. Around the zero-crossing

points, the difference is always smaller than V_{tol}, even if there is a voltage sag in the line.

3.4.1.2 Method 2: Calculating Per-unit Voltage Sag

In this second method, voltage difference per unit is calculated using the instantaneous values given in Eqn.3.79. This value is compared with a given reference. Eqn. 3.79 defines voltage sag percentage of instantaneous the source voltage:

$$\Delta V_{pu} = \frac{|\Delta V_1|}{|V_{ref} \cdot V_{pll}|} = \frac{|V_{ref} \cdot V_{pll} - V_s|}{|V_{ref} \cdot V_{pll}|} \tag{3.79}$$

If ΔV_{pu} is greater than $V_{pu,ref}$, then there is a voltage sag in the line.

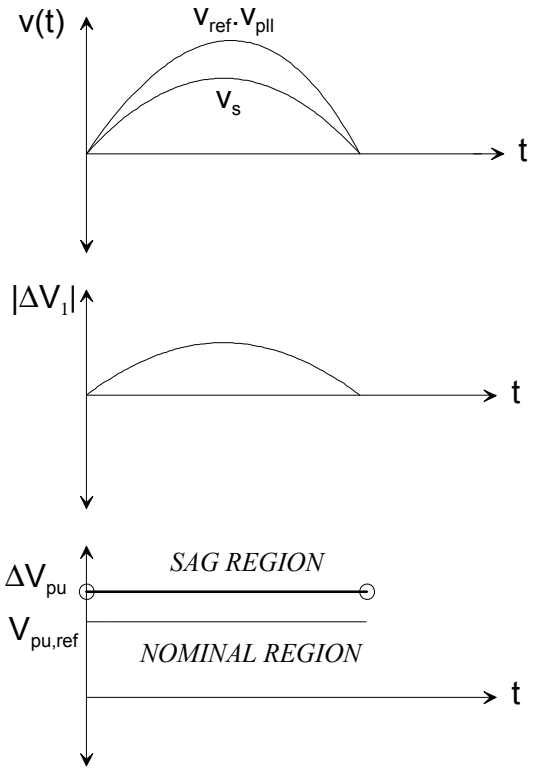


Figure 3.49. Calculating per unit voltage sag value for method 2.

The main advantage of this method is, there are no false alarms like first method. The disadvantages are:

i. Assuming the control circuit is implemented using a microprocessor, division is a time consuming process for microprocessors.
ii. When the denominator is zero, the microprocessor gives errors and program stops. It is not possible to implement this formula in practice unless the zero-crossings are ignored.

3.4.1.3 Method 3: Calculating True RMS of Source Voltage

The true RMS of the source voltage (sinusoidal or non-sinusoidal) is calculated using the instantaneous voltage values. Then, this value is compared with the reference. If this value is lower than reference, there is a voltage sag in the line:

$$V_s < V_{ref} \tag{3.80}$$

The advantages of this method are:

i. Method 1 does not operate accurately about zero-crossing but this method does.
ii. Method 1 assumes source voltage is purely sinusoidal. However, source voltage is not always sinusoidal. There are transients, for example. In this method, the RMS value is calculated. Therefore, it is not dependent on wave shape of source voltage.

The disadvantages of this method are:

i. This method must wait at least one half cycle to detect voltage variation.
ii. Assuming control circuit is implemented using a microprocessor, the rms calculation is difficult and it takes microprocessor time.

3.4.1.4 Method 4: Acceptable Band Method

If the source voltage is within the specified band, the voltage is assumed as nominal in this method.

Nominal Condition: $\left|V_{ref} \cdot V_{pll} \cdot K_{sag}\right| \le \left|V_s\right| \le \left|V_{ref} \cdot V_{pll} \cdot K_{swell}\right|$ (3.81)

Voltage Sag Detection Condition: $\left|V_s\right| < \left|V_{ref} \cdot V_{pll} \cdot K_{sag}\right|$ (3.82)

Voltage Swell Detection Condition: $\left|V_s\right| > \left|V_{ref} \cdot V_{pll} \cdot K_{swell}\right|$ (3.83)

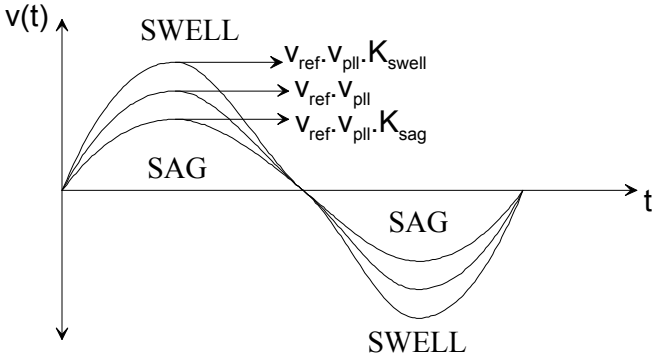


Figure 3.50. Acceptable band method for voltage sag detection.

The advantages of this method are:

i. Because the calculations in this method do not burden the microprocessor, this is a relatively easy method.
ii. The tolerable bandwidth is easily changed according to user's requirements. Therefore, the user's acceptable voltage limit is adjusted easily using K_{sag} and K_{swell}.
iii. It is not necessary to wait for at least one half cycle or more to detect voltage variation; voltage sag/swell can immediately be detected.
iv. There is no problem at the zero-crossing points because similar to the actual voltage, the reference voltage is also zero at these points.

The disadvantages of this method are:

i. In practice, due to noise, the voltage may not be measured accurately at the zero-crossing points. Therefore, these measurements should be ignored. Thus, except for these points, this detection method can be used.
ii. The limits utilized in this method are not a specified band which is necessary for accurate decision. Due to missing source voltage measurements, at the voltage near these limits, the control may not be able to decide if there is a nominal voltage or a voltage sag. Therefore, if this method is applied as a control method, mode transitions occur immediately and the switches are burdened with frequent commutations.

3.4.1.5 Method 5: Acceptable Band Method With Hysteresis & Time Delay

In this thesis, method 5 is applied on the experimental prototype as the voltage sag detection method. This method is obtained from the fourth method by some modifications. These modifications are applied to obtain more practical and realistic results.

Modification 1: Even if voltage sag/swell is detected, it is necessary to wait for a definite time to be sure. If voltage sag/swell continues during this time, then it is decided as a voltage sag/swell. This time is added to fourth method.

Modification 2: In the fourth method, there are only two limits which are K_{sag} and K_{swell}. However, in the fifth method, there are four limits: This is because a hysteresis band is added to both limits. In other words, when the voltage is decreasing, the lower limit (SAG_NOM_MIN) is used to detect a voltage sag (Figure 3.51). However, when the voltage is increasing, the upper limit (SAG_NOM_MAX) is used to detect the end of a voltage sag (Figure 3.52). A similar situation exists for voltage swell limits (Figures 3.53 - 3.54).

If the measured voltage is too close to the limit values, then method 5 remains in the active (present) mode. The utilized limits are also chosen according to active mode. This can be more clearly understood by the following illustrations:

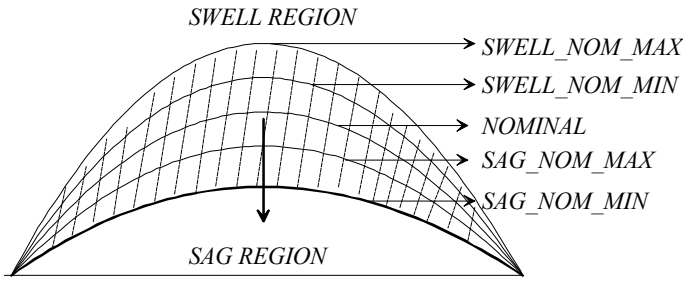


Figure 3.51. Nominal to voltage sag transition: SAG_NOM_MIN limit is used.

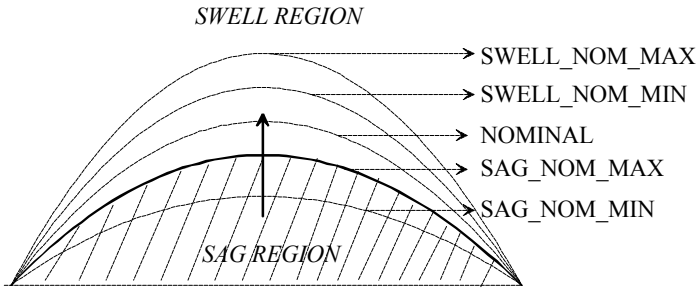


Figure 3.52. Voltage sag to nominal transition: SAG_NOM_MAX limit is used.

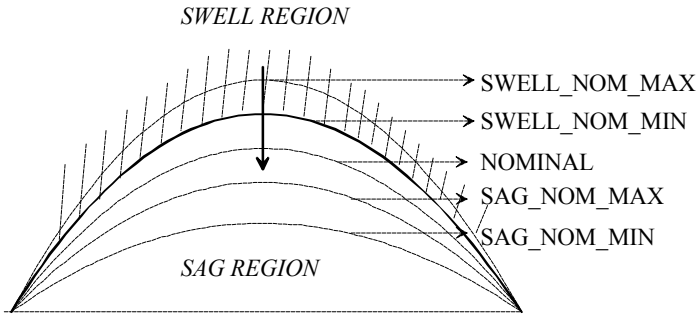


Figure 3.53. Voltage swell to nominal transition: SWELL_NOM_MIN limit is used.

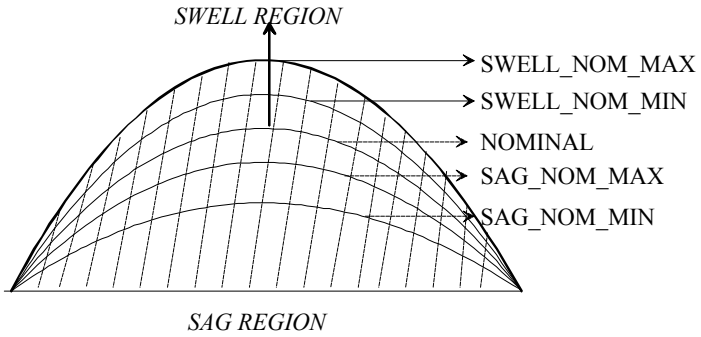


Figure 3.54. Nominal to voltage swell transition: SWELL_NOM_MAX limit is used.

3.4.2 Minimum Transition Times Required to Switch Between Bypass Operation and Inverter Operation

If there is a nominal voltage in the line, the static bypass switch is on and inverter is off. This condition of the electronic line voltage regulator is called as Bypass Operation. If a voltage sag condition is detected, then the controller switches static bypass switch off and IGBT's of inverter on. This condition of the electronic line voltage regulator is called as Inverter Operation. However, the interval of time between the two transitions is important. The thyristors of the static bypass switch do not turn off instantly. A definite time is required for thyristor commutation, as well as the "reverse recovery time".

The simulations show that in the worst case, the device must wait at least a half cycle for 50 Hz which is equal to 10 ms for natural commutation of thyristors. Then, the IGBT's could be switched on. Otherwise, the thyristors would not be off when IGBTs were turned on. Then a short circuit would occur and excessive currents between thyristors and IGBT's would flow (i.e. "shoot-through" fault). Thus, in the computer simulations and the implementation at the laboratory, this transition time is taken as 11 ms. The remaining 1 ms interval takes into account thyristor turn-off and reverse recovery times.

3.4.3 Total Response Time of The Voltage Regulator

The total response time of the line regulator is defined as the time interval beginning with voltage sag detection, and ending with the activation of inverter (IGBTs). In other words:

$$\Delta t_{response} = \Delta t_{sag\ detection} + \Delta t_{transition} \tag{3.84}$$

For the fifth sag detection method, a time delay is employed to make sure that a voltage sag has started. This delay is taken as 5 ms in the implementation. The transition time is 11 ms, as explained in section 3.4.2. Therefore,

$$\Delta t_{response} = 5ms + 11ms = 16ms \tag{3.85}$$

3.5 OUTPUT FILTER DESIGN

A second order low pass LC filter is utilized to filter out the harmonics at the MEVR output. As discussed in section 3.1.1, two different LC filter variations are employed for filtering inverter harmonics. The difference between them is the location of the filter capacitance. The filter capacitance (C_f) can be paralleled to inverter output or it can be connected in series with inverter output. The filter inductance (L_f) location is the same for both types of LC filter topologies and it is connected in series with the inverter output. The sizing of the filter capacitance and the inductance will be determined in this section. The design will start by the 50 Hz analysis for capacitance and inductance to determine maximum values of them, and also obtain the minimum resonance frequency of the filter.

1. Filter Inductance (L_f) Design: The allowed voltage drop determines the maximum value of the filter inductance. Allowed voltage drop of the filter inductance is taken approximately as 5 % of the nominal voltage at 50 Hz. Therefore, maximum voltage drop of the filter inductance should be 11 V for 220 V nominal voltage.

The filter inductance current is approximately the load current but its current has more harmonics than the load current. Therefore, maximum inductance current can be equal to load current.

$$I_{L_f} = I_{load} = 5.68A \tag{3.86}$$

Utilizing these current and voltage ratings for the filter inductance, 6.16 mH is obtained for the maximum inductance as seen in the calculation below:

$$L_f = \frac{V_L}{\omega \cdot I_{load}} = \frac{11}{2 \cdot \pi \cdot 50 \cdot 5.68} = 6.16mH \tag{3.87}$$

2. Filter capacitance (C_f) design: The allowed capacitor current determines the maximum value of the filter capacitance. Maximum allowed capacitor current is taken as equal or less than 1/3 of the load current. Therefore, maximum filter capacitance current should be equal to 1.893 A as seen in the calculation below.

$$I_{C_f} = \frac{1}{3} \cdot I_{load} = 1.893A \tag{3.88}$$

If the filter capacitance is paralleled to the load (MEVR with parallel filter capacitance), the maximum voltage is equal to load voltage. If the filter capacitance is connected in series with inverter output (MEVR with series filter capacitance), then the filter capacitance voltage is equal to maximum inverter voltage. The maximum inverter voltage is obtained for the 100 % voltage sag condition because only the inverter supplies nominal voltage to the load when there is 100 % voltage sag. Therefore, the filter capacitance voltage rating is taken as nominal voltage (220 V) for both variations of MEVR.

Utilizing these filter capacitance current and voltage ratings, the maximum capacitance value is obtained as 27.38 μF as seen in the calculation below.

$$C_f = \frac{I_{Cf}}{2 \cdot \pi \cdot f \cdot V_{C_f}} = \frac{I_{load} \cdot \frac{1}{3}}{2 \cdot \pi \cdot 50 \cdot V_{load}} = 27.38\mu F \tag{3.89}$$

As a result, the **maximum** values of LC filter components are:

$L_f = 6.16$ mH, $C_f = 27.38$ μF

3. <u>The Minimum Filter Resonance Frequency:</u> The gain equation of a low pass LC filter is given by:

$$\left|H(j\omega)\right| = \left|\frac{V_{out}}{V_{in}}\right| = \frac{1}{\left|1 - \omega^2 \cdot L \cdot C\right|} \tag{3.90}$$

The relationship between frequency and the gain is given in Figure 3.55.

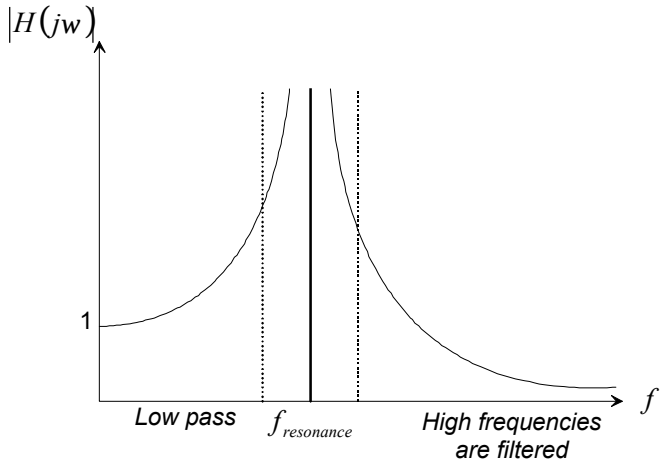


Figure 3.55. H (jω) vs. f for a second order LC filter.

Therefore, the resonance frequency equation of a low pass LC filter is obtained by Eqn.3.91.

$$f_{resonance} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \tag{3.91}$$

The desired (low pass) frequencies must be much smaller than $f_{resonance}$. This frequency is 50 Hz for our circuit. Thus, fundamental component is passed to the load directly. The undesired frequencies must be much greater than $f_{resonance}$. This frequency is 20 kHz (switching frequency of the IGBTs) for our circuit. Thus, the harmonics with high frequencies will be filtered out.

Utilizing maximum possible filter capacitance and inductance values calculated above and Eqn. 3.92, the minimum resonance frequency of LC filter of MEVR is calculated as 387.53 Hz .

The LC filter gain is infinite for this resonance frequency, it passes 50 Hz and does not pass 20 kHz and their harmonics. However, smaller filter sizes are more suitable to reduce inverter volume and weight. With smaller capacitance and inductance values, the filter resonance frequency will have higher values. This can be seen from the Eqn.3.91.

Utilizing circuit simulations, and trial and error method, after several trials, the following LC filter inductance and capacitance values have been determined. With the filter values given below, the output voltage has very low harmonic content:

$L_f = 3$ mH, $C_f = 15\mu$F, $f_{resonance} = 750$ Hz

Also, the following internal resistances are included (representing the ESR of the components) in series with the filter inductance and filter capacitance, respectively, for increasing the damping effect of LC filter:

$R_{Lf} = 200$ mΩ, $R_{Cf} = 100$ mΩ

Initial simulation results indicated that this filter produced an almost sinusoidal output voltage, filtering out almost all of the harmonics produced by the inverter. However, due to the resonance frequency at 750 Hz, the filter amplified harmonics around the resonance frequency (700 – 800 Hz range).

To correct this behaviour, a load voltage feedback control is added to the in phase injection method controller. The load voltage is compared with the reference voltage and the error term is passed through a P-controller (a gain), as shown in Figure 3.56. This controller reduces the small fluctuations in the load voltage. The resulting load voltage waveform has very low harmonic content, almost a pure sinusoidal waveform.

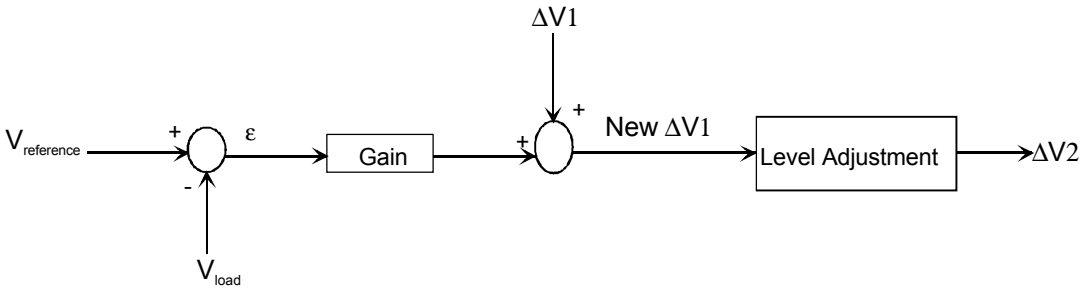


Figure 3.56. Load voltage feedback control block diagram.

The error term (ε) can be positive or negative. It is added to the required inverter voltage, ΔV1, to regulate load voltage instantaneously. Thus, the corrected required inverter voltage is utilized for level adjustment to produce carrier wave, ΔV2.

Simulations are performed utilizing this filter topology, as discussed in chapter 4.

CHAPTER 4

MEVR MODELLING AND SIMULATIONS

4.1 INTRODUCTION

This chapter describes the modelling and simulation of a single phase MEVR. Circuit simulation results are also given. The power section of MEVR is modeled the same manner as MEVR with parallel capacitor filter shown in chapter 3. In these circuit simulations, in-phase injected voltage method with load voltage feedback control and injected power minimization open loop control methods are applied. The circuit simulation parameters are given in Table 4.1. A computer simulation package program Ansoft-Simplorer (Student version, 6^{th} version) [30] that is a graphic window based (pick-and-place) power electronic circuit simulator is utilized. The software provides fast and accurate results with no numerical convergence problems.

Basically, two simulation models are utilized for investigating MEVR performance. These are the following.

1. MEVR Full Model: Switching operation of IGBTs is modeled and switches operate at 20 kHz switching frequency.

2. MEVR Average Model (switching ripple is neglected): The inverter stage is modeled with controlled voltage sources and controlled current sources for simplicity.

Since circuit simulations with long durations (in orders of seconds) can not be efficiently performed by simulating each switching operation within a reasonable time, the averaging method is utilized in such simulations. In both the average model simulation and full model simulation, the control algorithms and other elements remain the same. In the following sections, the conrol algorithm is discussed in detail. The control logic utilized in MEVR simulations is given with flow chart in Figure 4.2 and will be discussed in detail in the following sections.

Table 4.1. MEVR simulation parameters.

Source line resistance	R_s	45 mΩ
Load resistance	R_{load}	30.98 Ω
Load inductance	L_{load}	73.98 mH
Load power factor	Cos(θ)	0.8
Load power	P_{load}	1 kW at 220 V_{rms}
Load rms current	I_{load}	5.68 A at 220 V_{rms}
Energy storage capacitors	C_{dc1}, C_{dc2}	3.27 mF
Filter inductance	L_f	3 mH
Internal resistance of filter inductance	R_{Lf}	0.2 Ω
Filter capacitance	C_f	15 μH
Internal resistance of filter capacitance	R_{Cf}	100 mΩ
Switching frequency of IGBTs	f_{sw}	20 kHz
Simulation program name	Simplorer P.E. Simulation Software Package Program	
The minimum time step	0.1 μs	
The maximum time step	0.5 μs	

4.2 MEVR SIMULATIONS WITH FULL MODEL

In this section, MEVR simulation circuit and the simulation methods will be explained. The simulation circuit is given in Figure 4.1. As seen in the figure, MEVR simulation circuit consists of three main stages. These are

1. MEVR power stage
2. MEVR supervisory state machine
3. MEVR control blocks

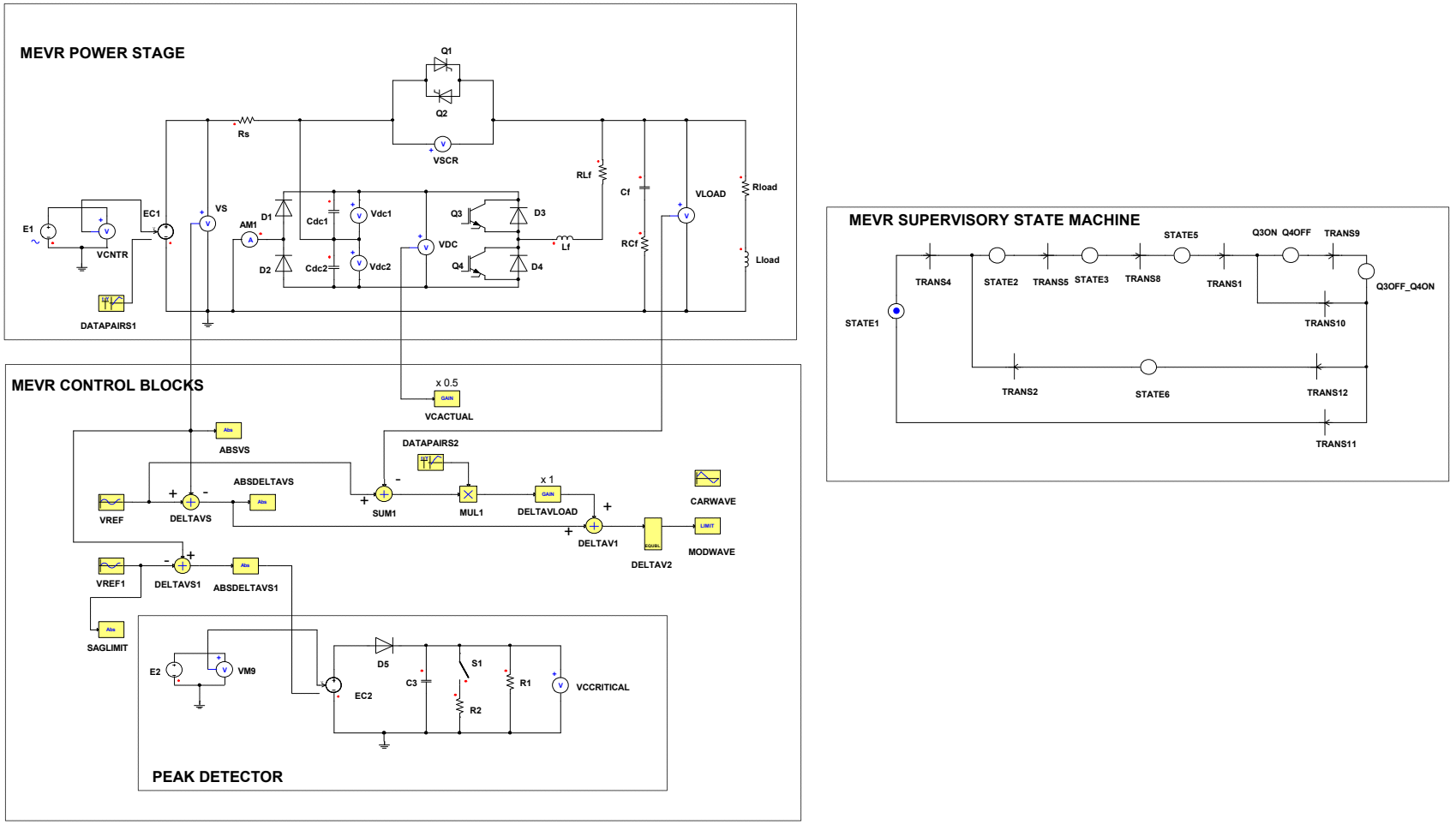


Figure 4.1. MEVR simulation circuit full model with switches.

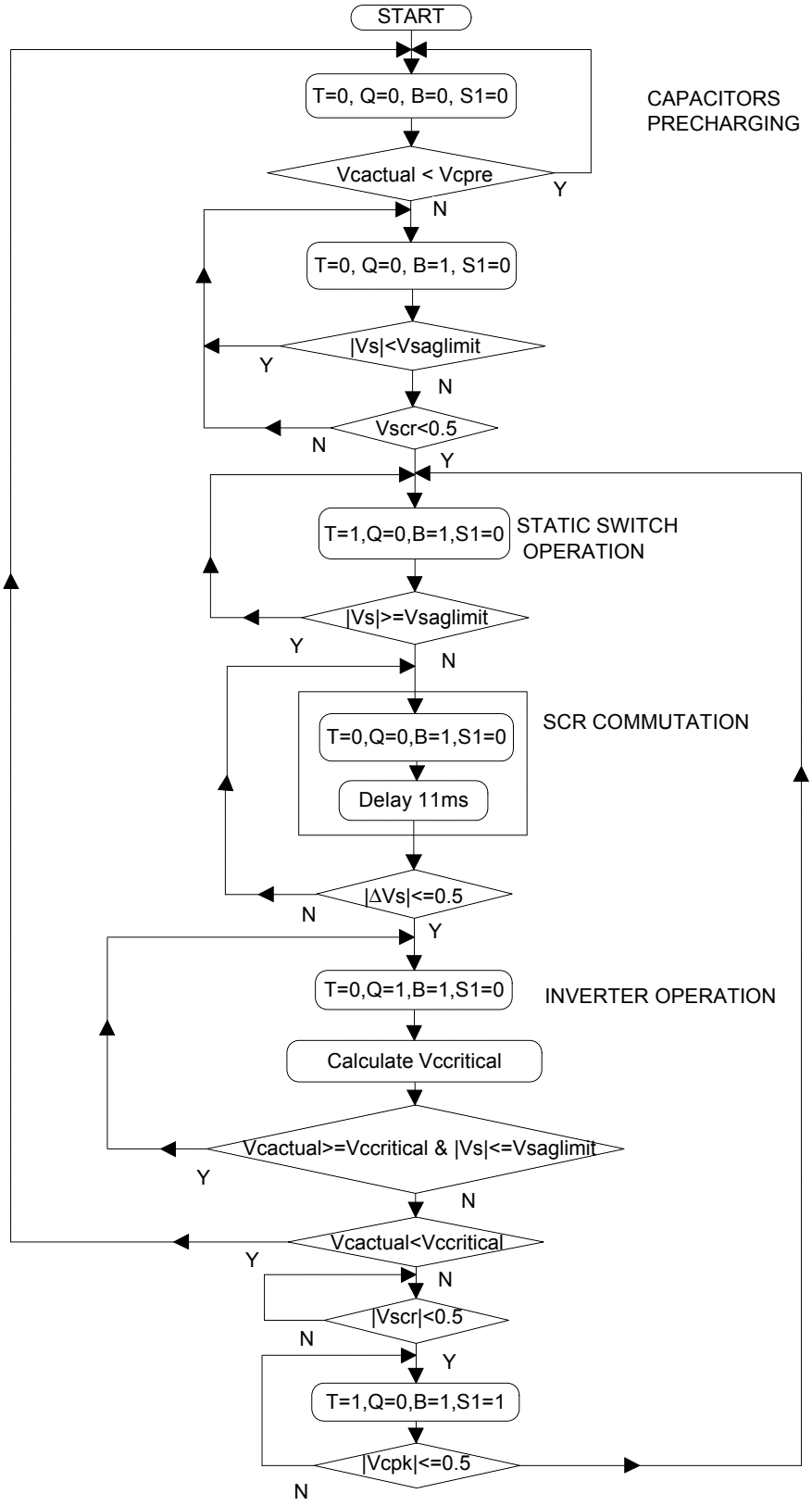


Figure 4.2. MEVR system control flowchart.

Since MEVR power stage was investigated in chapter 3, it will not be described here.

MEVR system control flowchart is given in Figure 4.2. This flowchart has been implemented utilized MEVR supervisory state machine shown in Figure 4.1. For the control flowchart given in Figure 4.2, the following variables are utilized:

1. T: Enable signal for static bypass switch (0 = Static bypass switch is OFF, 1 = Static bypass switch is ON)
2. Q: Enable signal for the inverter (0 = Inverter is OFF, 1 = Inverter is ON)
3. B: Enable signal for bypass switch in precharging circuit, not used in this simulation (0 = Bypass switch is OFF, 1 = Bypass switch is ON)
4. S: Enable signal for peak detector discharging switch (0 = Switch is OFF, 1 = Switch is ON)

For the same flowchart, the following constants should be defined:

1. Vcpre: The threshold for average energy storage capacitor voltage in order for precharging condition to end.
2. Vcpk: The threshold for peak detector capacitor (C_3) to be accepted as completely discharged.

The remaining variables and constants are shown in Figure 4.1 or defined below in the description of MEVR supervisory state machine.

MEVR supervisory state machine is the stage with the main control logic. MEVR control blocks perform calculations which are required for the circuit control and monitoring. The control circuit generates three control signals as outputs.

1. THGATE for static switch (Q_1, Q_2)
2. Q3GATE for top IGBT (Q_3)
3. Q4GATE for bottom IGBT (Q4)

The circuit simulation starts with STATE1 in state machine. All control swithes are off during the initial power up of MEVR.

STATE1:
THGATE:=0
Q3GATE:=0
Q4GATE:=0

If all conditions in TRANS4 are satisfied, the static bypass switch can be switched on (STATE2). These conditions are

1. If the source voltage is greater than a tolerance value (nominal source voltage)
2. The voltage difference on the static switch is smaller than 0.5 V
3. The energy storage capacitor voltages are charged up to a definite value (at least 250 V).

TRANS4:
(ABSVS.VAL>SAGLIMIT.VAL) AND (VSCR.V<0.5)AND(VCACTUAL.VAL>=250)

As seen in STATE2, the static switch is on and the discharging switch in the peak detector (S1) is off.

STATE2:
THGATE:=1
Q3GATE:=0
Q4GATE:=0
S1CONTROL:=0

The peak detector is utilized to determine the required inverter voltage to obtain $T_v.V_{ref}$. For this purpose, the difference between VREF1 and VS is calculated (DELTAVS1). VREF1 is a sinusoidal wave with 280 V peak voltage.

DELTAVS1:

VREF1-VS

Then, the absolute value of DELTAVS1 is calculated (ABSDELTAVS1). If ABSDELTAVS1 is greater than capacitor voltage, C_3, of the peak detector, then C_3 is charged. Otherwise, C_3 is slowly discharged through R_1 (Time constant C_3R_1=1min). During voltage sag condition, S1 switch parallel to C_3 is off (S1CONTROL=0). If the voltage sag condition ends, then S1 is switched on (S1CONTROL=1) and C_3 is quickly discharged through R_2 (Time constant C_3R_2 = 10μs).

Until a voltage sag detection occurs, all switches stay in these conditions (STATE2). The voltage sag detection condition is given in TRANS5.

TRANS5:

ABSVS.VAL<SAGLIMIT.VAL

If a voltage sag is detected, the control logic waits for two conditions to be satisfied below:

1. 11 ms for the SCRs' commutation time and reverse recovery time
2. The absolute value of difference between reference voltage and the source voltage (ABSDELTAVS) is smaller than 0.5 V for inverter switching to soft start.

The states and transitions for these conditions are given below:

STATE3:

THGATE:=0

Q3GATE:=0

Q4GATE:=0

TRANS8##11m

TRANS8

11ms

STATE5:

THGATE:=0

Q3GATE:=0

Q4GATE:=0

TRANS1

ABSDELTAVS.VAL<=0.5

After these conditions are met, the inverter starts to operate. The sine-triangle PWM method is utilized to generate PWM pulses in MEVR simulation. The control blocks generates modulating wave (MODWAVE) and carrier wave (CARWAVE). At this stage, the PWM pulse generation method will be explained.

CARWAVE block generates carrier wave (triangle wave) with 20 kHz frequency and 311 V peak value. MODWAVE block generates modulating wave which depends on energy storage capacitor voltages (V_{dc1}, V_{dc2}) and required inverter voltage (DELTAV1).

DELTAV1 (ΔV_1) is the missing voltage at the source due to voltage sags. It is also the required inverter output voltage to obtain desired load voltage. The DELTAV1 block generates this required inverter voltage. DELTAV1 is generated by adding two separate terms: DELTAVS and DELTAVLOAD.

DELTAVS is the missing voltage or difference between reference voltage and the source voltage. The inverter tries to inject this voltage to obtain nominal laod voltage. DELTAVS is the dominant term in DELTAV1.

DELTAVS:

DELTAVS:=VREF-VS

However, since there are harmonics at the filter resonance frequency on the load voltage (VLOAD), the nominal load voltage can not be obtained with only DELTAVS. The LC low pass filter (L_f, C_f) filters the harmonics at switching frequency but can not filter out the harmonics at its resonance frequency. Therefore, there is a P-controller to compensate for the small errors. Since the gain of the P-controller is taken as 1, the P controller adds the difference between reference voltage and the load voltage to DELTAV1 block. Note that, this P controller is also enabled with IGBT switching.

DELTAVLOAD (P-Controller):

DELTAVLOAD:=VREF-VLOAD

Thus, DELTAVS and DELTAVLOAD form DELTAV1.

DELTAV1:

DELTAV1:=DELTAVS+DELTAVLOAD

Utilizing DELTAV1 and the energy storage capacitor voltages, DELTAV2 block generates the modulating wave. This operation is called “Level Adjustment” (See chapter 3). Since this is not an actual lab prototype, the measured energy storage voltages are not scaled down to low voltage levels (i.e. 5 V). Instead, the actual measured voltages at 311 V levels are used.

DELTAV2:

$$\mathrm{DELTAV2} = 622\mathrm{D} - 311 = 622 \cdot \left(\frac{\mathrm{DELTAV1} + V_{dc2}}{V_{dc1} + V_{dc2} + 0.0001} \right) - 311 \qquad (4.1)$$

In the equation, D is the duty cycle for PWM of the top IGBT (Q_3). This D is dependent on DELTAV1 and the energy storage capacitor voltages. In the denominator of this equation, there is a small constant value (0.0001) to avoid division by zero error. The relationship between DELTAV2 and D can be shown in Figure 4.3.

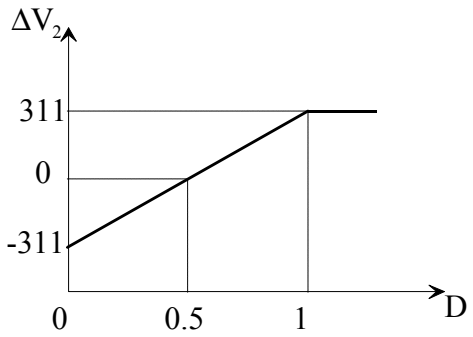


Figure 4.3. Relationship between DELTAV2 and D.

MODWAVE block limits the output of DELTAV2 within –311 V and 311 V range. The output of MODWAVE block is compared with the triangular wave (CARWAVE) to switch the IGBTs in the simulation (i.e., sine-triangle PWM method). The comparison of modulating wave and carrier wave is performed in the state machine. If MODWAVE is smaller than CARWAVE, the bottom IGBT is switched on.

TRANS9

MODWAVE.VAL<=CARWAVE.VAL

Q3OFF_Q4ON

THGATE:=0

Q3GATE:=0

Q4GATE:=1

If MODWAVE is greater than CARWAVE, the top IGBT is switched on.

TRANS10

(MODWAVE.VAL>CARWAVE.VAL)AND(VCACTUAL.VAL>=VCCRITICAL.V) AND ((ABSVS.VAL<SAGLIMIT.VAL) OR (ABS(VSCR.V)>=0.5))

Q3ON_Q4OFF

THGATE:=0

Q3GATE:=1

Q4GATE:=0

To continue inverter operation, the conditions in TRANS10 should be true. This means that, the actual DC bus voltage should be greater than critical DC bus voltage value and the voltage sag conditions should continue or the voltage on static bypass switch should be greater than or equal to 0.5 V.

To end inverter operation, either one of the following two conditions should occur.

1. There is nominal source voltage and the voltage drop on static bypass switch is less than 0.5 V, or
2. The actual DC bus voltage is less than the critical value.

If the first condition is true, then the circuit should return to nominal conditions. Then IGBTs are switched off, the static bypass switch is switched on. Also, S1 is switched on to discharge the capacitor of peak detector.

STATE6

THGATE:=1

Q3GATE:=0

Q4GATE:=0

S1CONTROL:=1

If the capacitor of peak detector is totally discharged (TRANS2), then S1 can be switched off (STATE2).

TRANS2

ABS(C3.V)<=0.5

In TRANS11, the second condition is satisfied. If this condition is true, there is not enough voltage to inject required inverter voltage.

TRANS11

VCACTUAL.VAL<VCCRITICAL.V

In this case, all switches are switched off and the circuit returns to its initial state (STATE1) to wait for nominal conditions.

4.2.1 Simulation Results

MEVR simulation circuit with switching components are performed for three voltage sag conditions:

i. Sc = 0.3
ii. Sc = 0.5
iii. Sc =0.7

For sag coefficients less than 0.5, MEVR can inject nominal voltage for an unlimited amount of time as discussed in chapter 3. In these simulations, the holding time is defined as the duration from the start of inverter operation until the actual DC bus voltage becomes less than the critical DC bus voltage. At this instant, all controlled switches are switched off. In other words, MEVR stops voltage generation completely if it is not able to generate the required nominal voltage (within tolerance limit, T_v).

Results for 30 % voltage sag:

The results for 30 % voltage sag are given in Figures 4.4 - 4.11 and Table 4.2.

Table 4.2. Total harmonic distortions for S_c=0.3
(calculated between 100-120ms).

	THD (%)
Load voltage	1.24
Source current	14.48

It is seen that MEVR corrects the 30 % voltage sag for an unlimited amount of time. The load voltage waveform has a low value of THD. During inverter operation, the difference between the reference and actual load voltage (ΔV) is quite small as seen in Figure 4.4.

Considering the transition of MEVR from nominal (static switch) to voltage sag (inverter) operation which occurs between 40 - 60ms, the circuit waits for 11 ms for thyristor commutation and reverse recovery, then it waits for the first zero crossing of DELTAVS as seen in Figure 4.4. This is necessary for the soft start-up of the inverter. If the inverter is started immediately after the 11 ms waiting time and DELTAVS is not zero at this instant, then the sudden change in the inverter voltage causes large oscillations and harmonics in the load voltage. Therefore, soft start-up of the inverter is the gradual increase of inverter voltage, starting from zero.

During the transition from nominal voltage to voltage sag, there is a short interruption in the load voltage of about one cycle. However, the transition from voltage sag back to nominal voltage is quite smooth and unnoticeable in the load voltage, without any interruption.

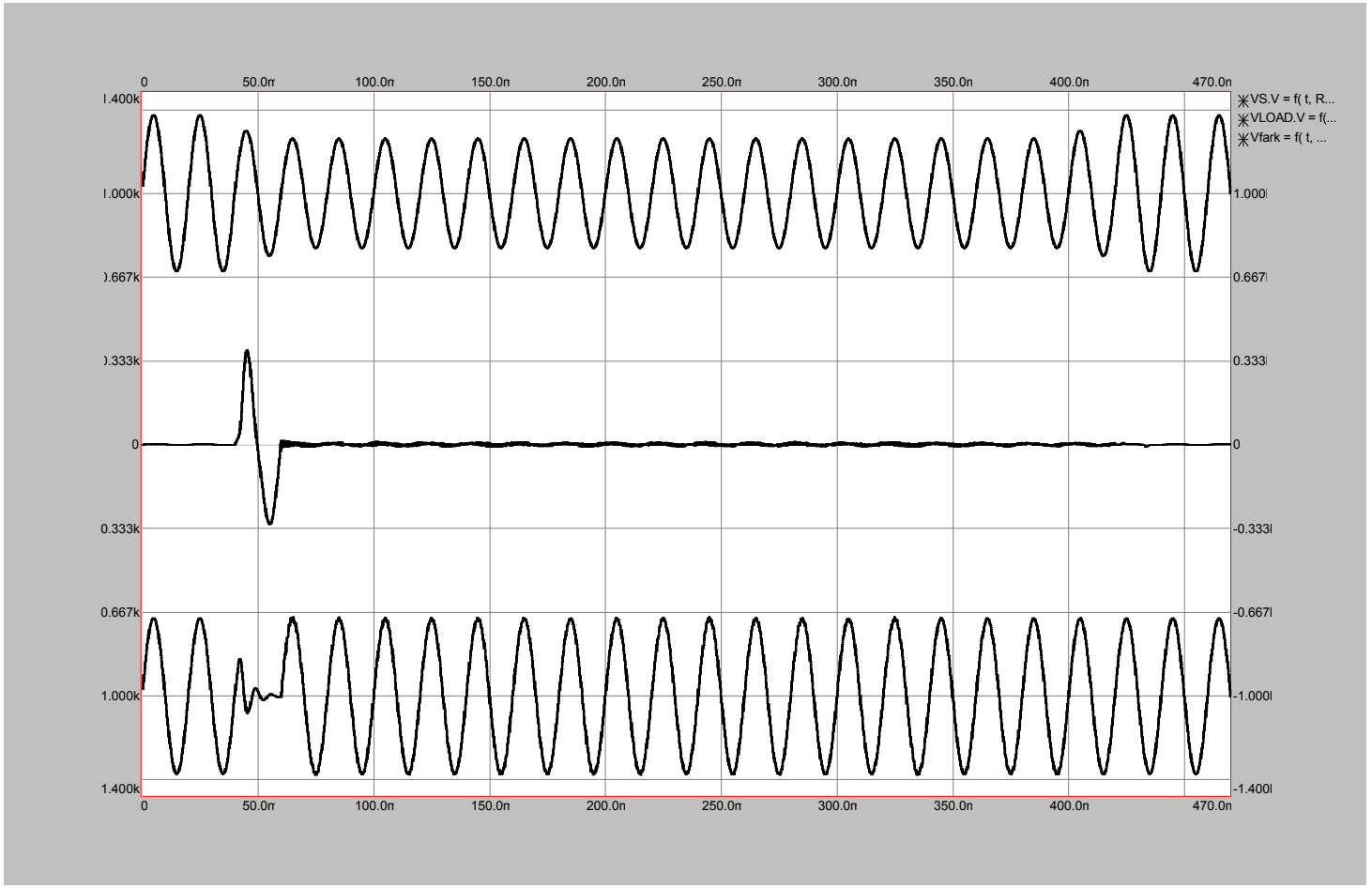


Figure 4.4. V_s, ΔV, V_{load} for S_c 0.3.

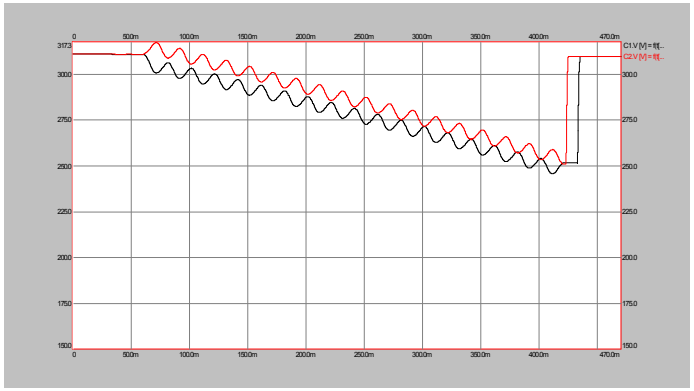


Figure 4.5. V_{dc1}, V_{dc2} for S_c 0.3.

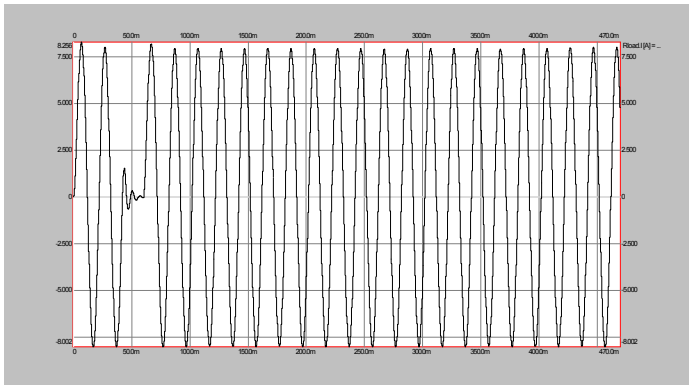


Figure 4.6. I_{load} for S_c 0.3.

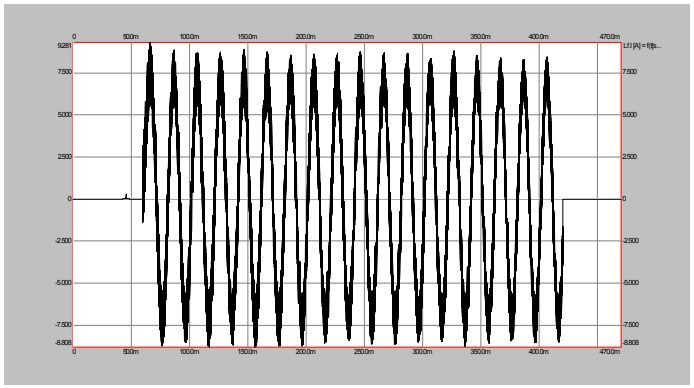


Figure 4.7. I_{Lf} for S_c 0.3.

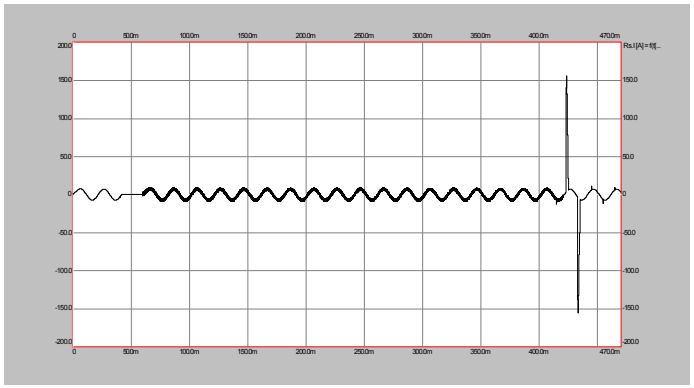


Figure 4.8. I_s for S_c 0.3.

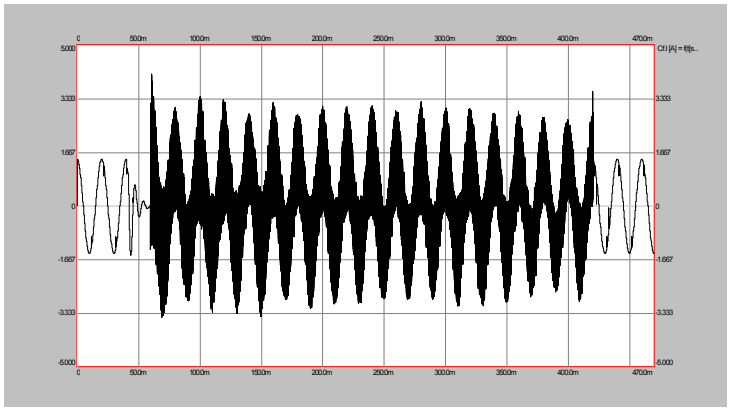


Figure 4.9. I_{Cf} for S_c 0.3.

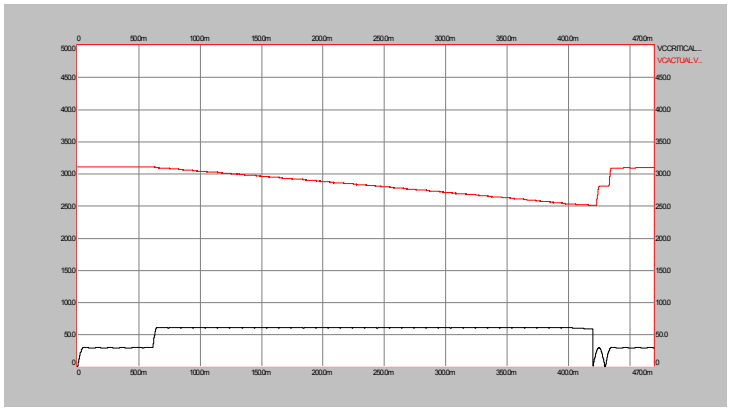


Figure 4.11. $V_{critical}$ and $V_{cactual}$ S_c 0.3.

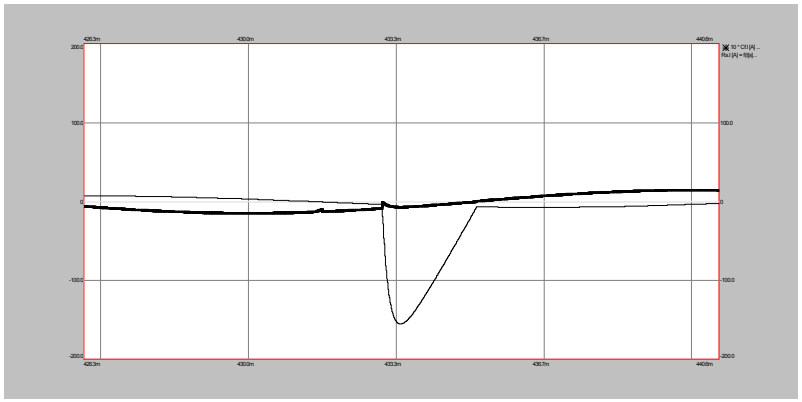


Figure 4.10. I_{Cf} and $I_{s.}$

The discharging of energy storage capacitors are shown in Figure 4.5. During the voltage sag, the peak value of source voltage is 218 V. Throughout the simulation, the capacitor voltages are always above this value. As a result, the capacitors are never charged by the source. They continue to discharge until the source voltage returns to nominal conditions at 420 ms.

The shape of the energy storage capacitor voltage waveforms should be discussed further: During each cycle, the capacitor voltages decrease and increase periodically. However, the amount of decrease is always greater than the amount of increase, resulting in a net reduction in capacitor voltages at the end of each cycle. Such behavior of capacitor voltages can be explained by considering the instantaneous value of inverter power. When the inverter voltage and current have the same polarity, the instantaneous inverter power is positive and one of the IGBTs (Q_3 or Q_4) is conducting. This corresponds to power delivered from the inverter to the load, discharging the capacitors. However, when the inverter voltage and current are of the opposite polarities, the instantaneous inverter power is negative and one of the freewheeling diodes (D_3 or D_4) is conducting. This corresponds to power delivered from the load to the inverter, charging the capacitors. This is possible because while the inverter switching determines the inverter voltage waveform, the current is determined only by the load, which is inductive, causing a phase difference between load voltage and current.

The load current shown in Figure 4.6 is also sinusoidal and it is similar to load voltage waveform. The filter inductance current is shown in Figure 4.7. The peak value of this current is about 9 A (6.36 A_{rms}). This current includes load current, filter capacitor current and harmonics due to inverter operation.

The source current is given in Figure 4.8. During inverter operation, the waveform includes the fundamental value (similar to nominal operation), but it also contains harmonics (THD = 14.48 %). This is because there is no filter to limit these harmonics at the source side. These harmonics which are injected to the source are

undesired as they increase the TDD (Total Demand Distortion) at the point of common coupling (PCC). If a suitable filter is added to the source side, these harmonics can be reduced.

Immediately after MEVR returns to nominal voltage, the energy storage capacitors are charged through D_1 and D_2. This is characterized by the large current pulses (150 A) superimposed on the source current at 424 ms and 434 ms. The capacitor charging current pulses can also be seen in the following cycles, but with much smaller magnitudes because the capacitors are not discharged significantly. The large initial charging current is because in the simulation model the line impedance is not modeled and therefore there is no impedance to limit the charging current. In a practical implementation of MEVR, the current peaks are expected to be significantly less than the simulation results of 150A.

The filter capacitor current is shown in Figure 4.9. During inverter operation, the capacitor filters out the load voltage harmonics but it absorbs all current harmonics, resulting in a current waveform with a very high THD. After the circuit returns to nominal conditions, the capacitor current is almost sinusoidal. However, as seen in Figure 4.10 (the magnified view of filter capacitor current and source current during nominal conditions), there are periodic dips in the filter capacitor current. There are two reasons for these dips: The main reason is due to the large charging current pulse in the source current; there is a sudden voltage drop of about 7 V on the series source impedance. This causes a very large negative dv/dt on the filter capacitor, reducing its current. The second reason is, during zero crossings of the source current, there are instants where both Q_1 and Q_2 are off. At these instants, there are sudden interruptions in the load voltage, causing current dips in the filter capacitor.

Figure 4.11 shows the actual DC bus voltage which is continuously decreasing during the voltage sag. It also shows the critical DC bus voltage limit for this

voltage sag condition. Since the actual voltage is above this limit, MEVR continues inverter operation until nominal voltage conditions return.

Results for 70 % voltage sag:

The results for 70 % voltage sag are given in Figures 4.12 - 4.18 and Table 4.3.

Table 4.3. Total harmonic distortions for $S_c = 0.7$
(calculated between 100-120 ms).

	THD (%)
Load voltage	1.09
Source current	10.95

It is seen that MEVR corrects the 70 % voltage sag for approximately 14.5 cycles (up to 350 ms). After this instant, the voltage available on the energy storage capacitors is not sufficient to produce a nominal load voltage, so MEVR stops operation and waits for nominal conditions to return. During voltage sag correction, the load voltage waveform has a low value of THD.

Similar to the previous simulation for $S_c = 0.3$, the inverter is soft started during nominal to voltage sag transition, without any oscillations in the load voltage.

From Figure 4.12, it is seen that during the transition from voltage sag back to nominal voltage conditions, MEVR enables nominal voltage operation smoothly after the interruption.

The discharging of energy storage capacitors is faster in this simulation (Figure 4.13) since there is a deeper voltage sag, and the inverter has to supply higher power compared to 30 % voltage sag conditions. After the inverter operation is stopped by MEVR control logic, the capacitor voltages remain constant.

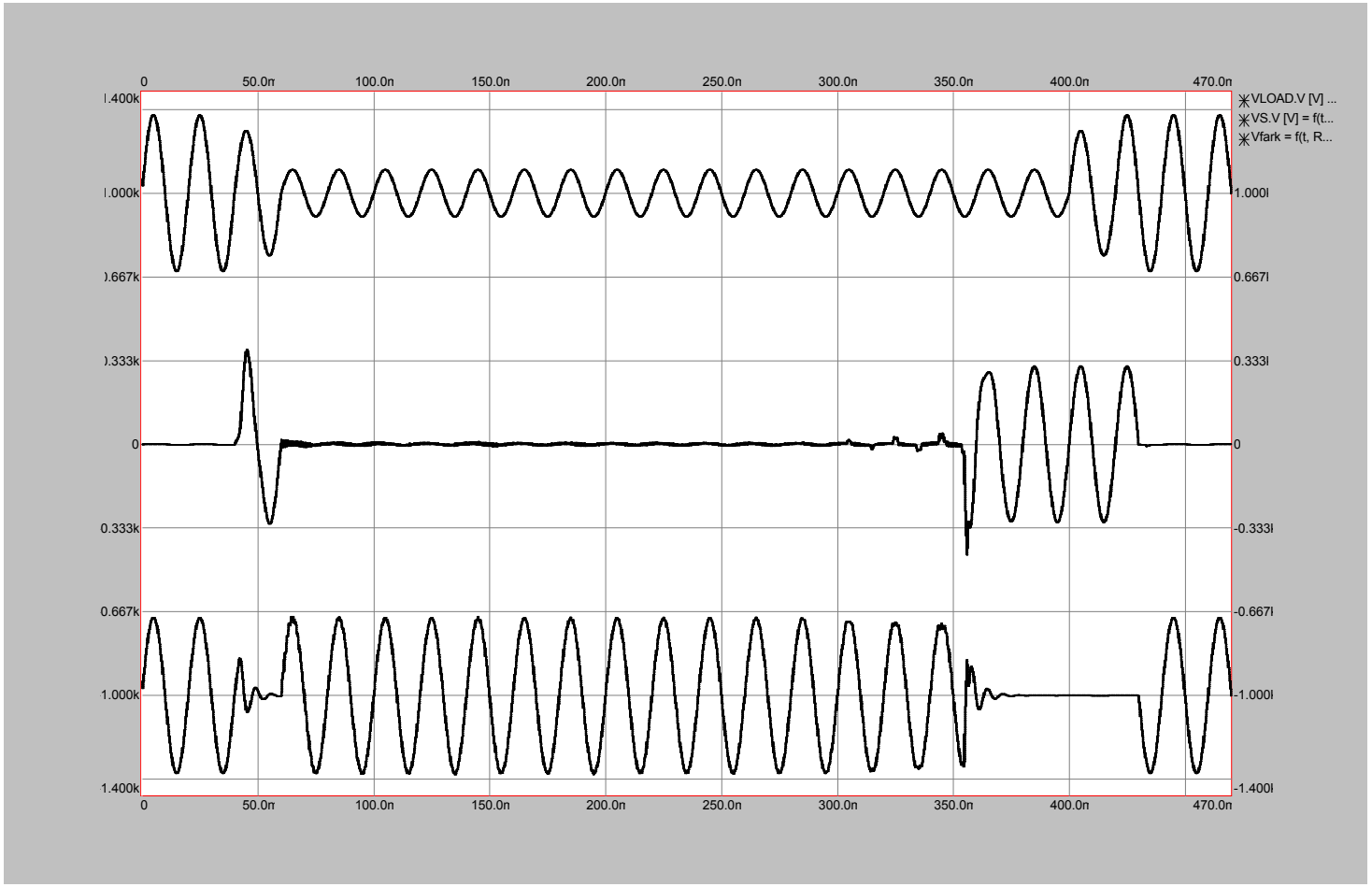


Figure 4.12. V_s, ΔV, V_{load} for S_c 0.7

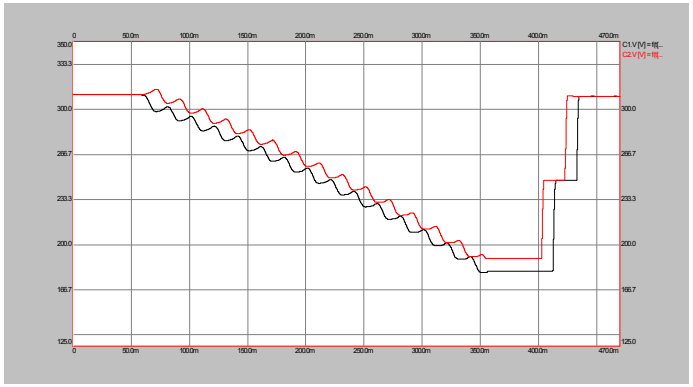


Figure 4.13. V_{dc1}, V_{dc2} for S_c 0.7.

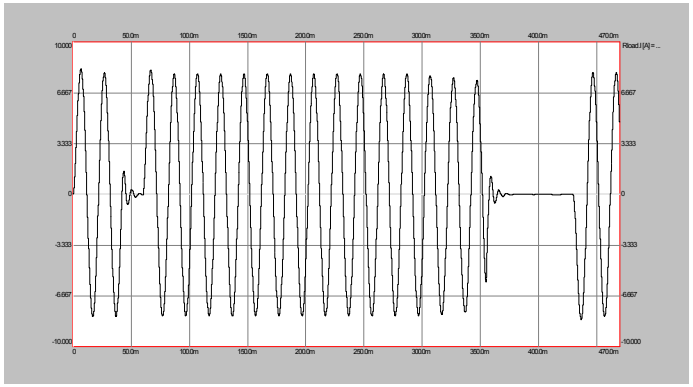


Figure 4.14. I_{load} for S_c 0.7.

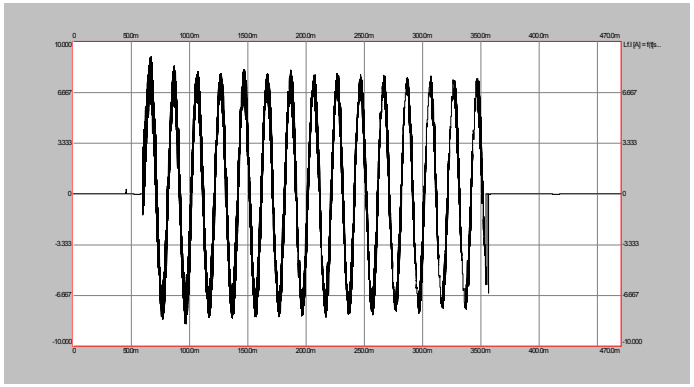


Figure 4.15. I_{Lf} for S_c 0.7.

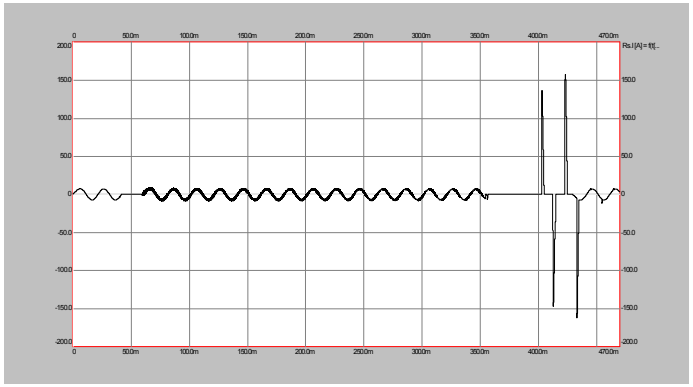


Figure 4.16. I_s for S_c 0.7.

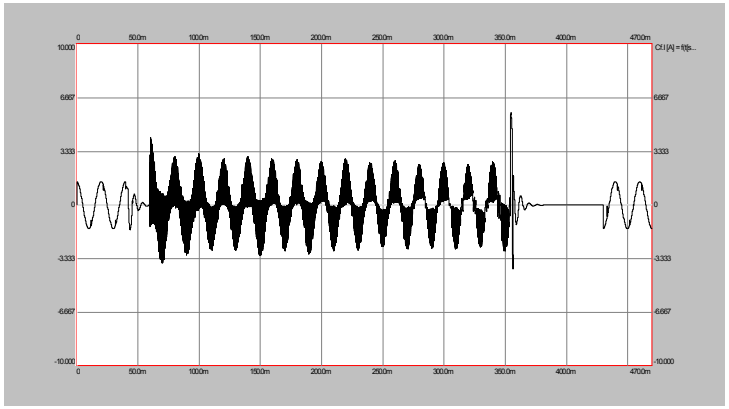


Figure 4.17. I_{Cf} for S_c 0.7.

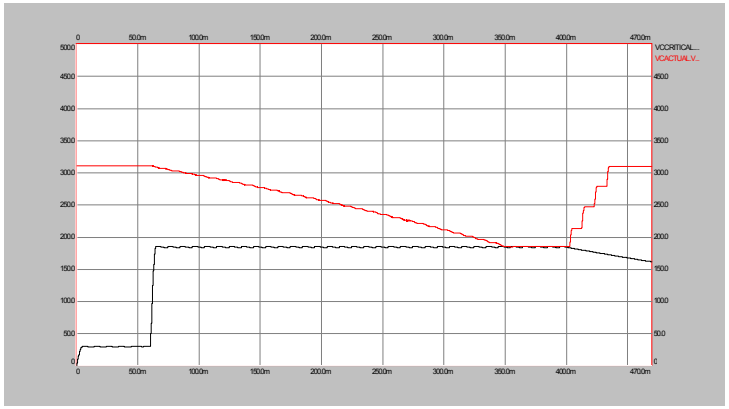


Figure 4.18. $V_{critical}$ and $V_{cactual}$ for S_c 0.7.

When the source voltage returns to its nominal value, it seen that the energy storage capacitors are charged up to 311 V in two cycles as seen from Figure 4.13. This is because of the simulation conditions: The source voltage returns to nominal value gradually, in two cycles.

Figure 4.18 shows the actual DC bus voltage and the critical DC bus voltage limit. MEVR continues its inverter operation up to 350 ms, where the two curves intersect. After this instant, it is unable to supply nominal voltage to the load, so it stops voltage generation altogether, waiting for the nominal conditions to return. Similar comments can be made on the remaining figures.

Comparing the results for 30 % voltage sag and 70 % voltage sag, it is seen that source current THD decreases as sag coefficient increases. This is expected because THD is defined as the total harmonic content to fundamental component ratio for the given waveform (source current). The magnitude of the PWM waveform pulses are similar at both sag values due to similar capacitor voltages, resulting in comparable harmonic content. However, the fundamental value of the source current is proportional to the sag coefficient (source current increases as source voltage decreases because source power is constant). This means the source current will increase more than twice as S_c increases from 0.3 to 0.7, decreasing the THD from 14.48 % to 10.95 %.

Results for 100 % voltage sag:

The results for 100 % voltage sag are given in Figures 4.19 – 4.26 and Table 4.4.

Table 4.4. Total harmonic distortion for S_c=1.0 (calculated between 100-120ms).

	THD (%)
Load voltage	3.85

A 100 % voltage sag corresponds to the worst case condition for MEVR, where all of the load power is supplied by the energy storage capacitors. From Figure 4.21, it is seen that MEVR can supply the load for 3 cycles before cutting off. The capacitor values (3.37 mF) were calculated for T_h = 60 ms (3cycles) in chapter 3. These results verify the theoretical calculations. The fundamental component peak value of the load voltage during the last cycle (100-120 ms) is calculated as 298.9V from Fourier analysis, which is above the tolerance limit of 280 V. The capacitors discharge very quickly (Figure 4.20) due to the highest value of power drawn from them (1 kW).

4.3 MEVR SIMULATION CIRCUIT WITH AVERAGING METHOD

In order to simulate the circuit for longer voltage sag durations (3 seconds, etc), MEVR model described in section 4.2 is too complex as it requires excessive durations (more than 1 day) and hard disk space to complete the simulation. This is because each IGBT switching is modeled in the full simulation. The simulation in section 4.2 is ideal for examining the waveforms in detail for shorter durations, but not suitable to simulate momentary and temporary voltage sags.

In order to simulate momentary and temporary voltage sags, a simplified model of the inverter has been used. This method is called the “Average Method”. Instead of modeling each switching cycle in detail, it is assumed that the inverter generates the required voltage (current) “on an average base” using controlled voltage (current) sources. Thus, voltage and current pulses are replaced with their average value equivalents and with the average model the simulation step size can be increased by orders of magnitude.

Figure 4.27 shows the simulation model of MEVR for this method. The effects of the inverter are inherently modeled by the controlled voltage sources VDEP1 and VDEP2. The output voltages of these sources depend on the capacitor voltages and duty cycle as follows:

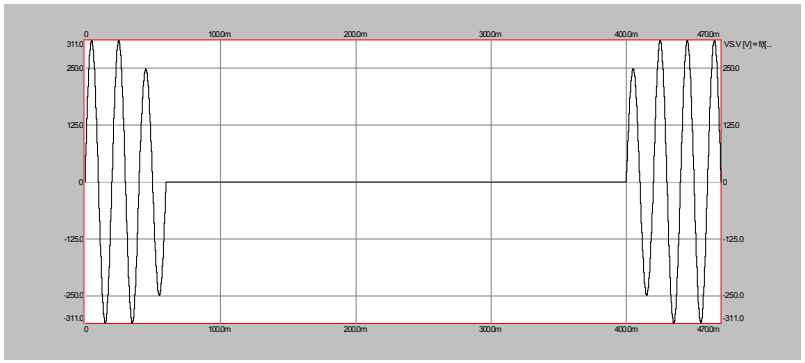


Figure 4.19. V_s for $S_c = 1$.

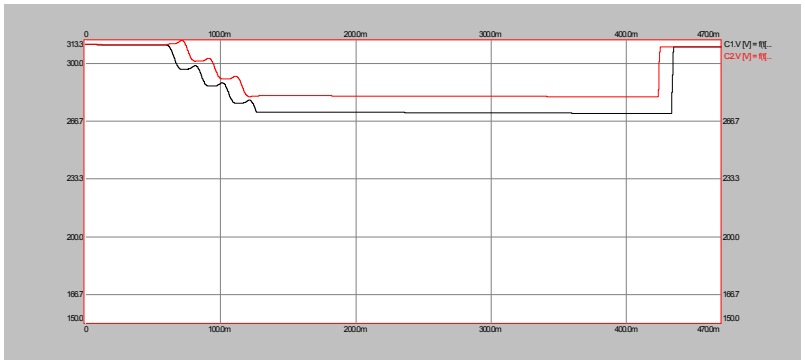


Figure 4.20. V_{dc1}, V_{dc2} for $S_c = 1$.

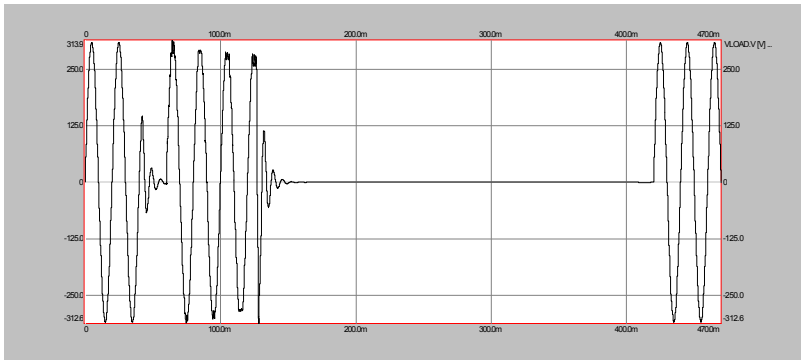


Figure 4.21. V_{load} for $S_c = 1$.

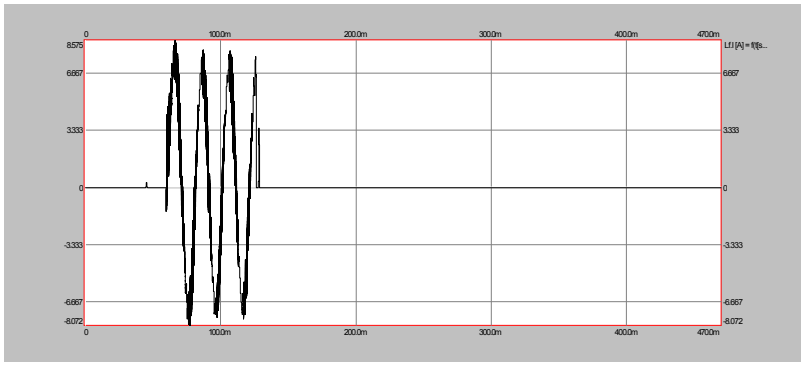


Figure 4.22. I_{Lf} for $S_c = 1$.

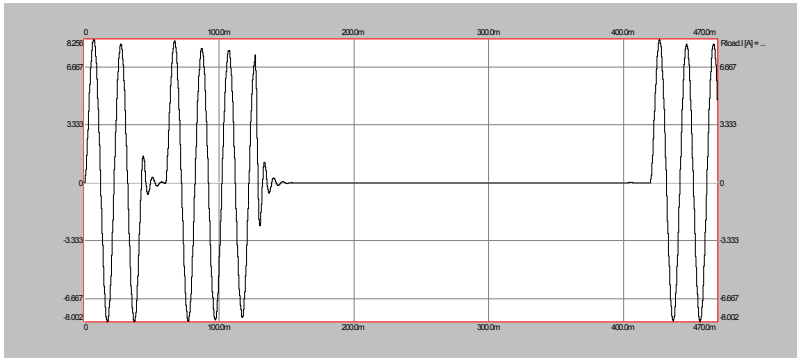


Figure 4.23. I_{load} for $S_c = 1$.

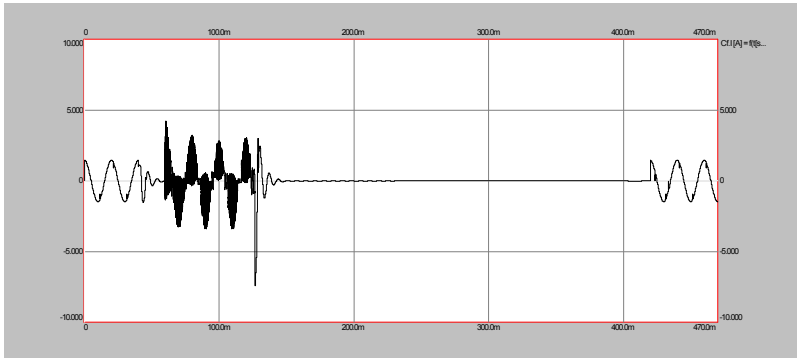


Figure 4.24. I_{Cf} for $S_c = 1$.

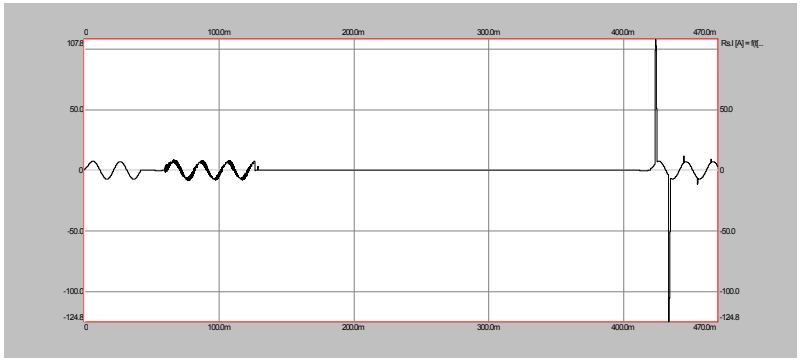


Figure 4.25. I_s for $S_c = 1$.

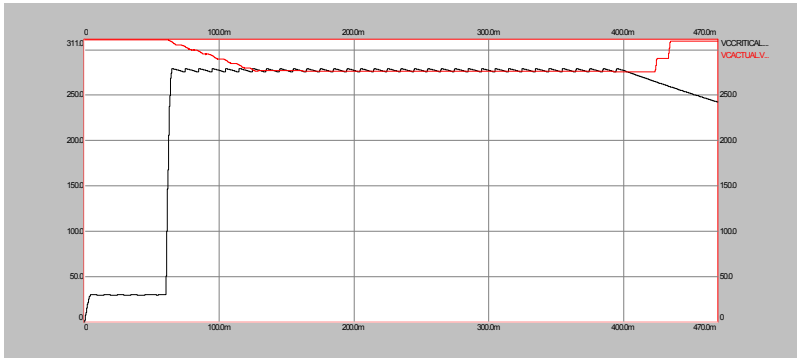


Figure 4.26. $V_{ccritical}$ and $V_{cactual}$ for $S_c = 1$.

$$VDEP1 := V_{dc1} \cdot D$$

$$VDEP2 := -V_{dc2} \cdot (1 - D)$$

Thus, the resultant voltage produced by the inverter is modeled by this method without performing any switching action.

In the actual MEVR, the capacitors will be discharged as the inverter supplies current to the load. In the model, the inverter is not modeled by actual IGBTs and anti-parallel diodes. Therefore, the inverter current to the capacitors will be modeled by two controlled current sources that are used to discharge these capacitors, depending on the duty cycle and load current as follows:

$$IC1 := I_{Lf} \cdot D$$

$$IC2 := I_{Lf} \cdot (1 - D)$$

4.3.1 Long Duration Sag Simulations Employing The Average Method

With the control cycle being 50μs, the integration step size of the average model simulation can be selected fairly large. Minimum time step is 0.5μs and maximum time step is 10μs in these simulations.

Utilizing Eqn.3.64, the energy storage capacitor value for 500 ms holding time is calculated as 28.13 mF. Utilizing this storage capacitor value, the simulation with averaging method is performed and the simulation results are given in Figures 4.28–4.29. As seen from Figure 4.29, the actual DC bus voltage intersects the critical DC bus value at 584 ms. The peak value of the load voltage fundamental is 294.45V for 580m –600ms. The holding time is equal to 584ms – 20ms = 564ms (The voltage sag correction starts at 20ms). This is because the losses in the circuit are small. There are no switching and conduction losses. Therefore, the holding

time duration is longer than the theoretical value, which was calculated for 97 % MEVR efficiency.

The required energy storage capacitor value for momentary voltage sags (3 s) is calculated as 168.8 mF. This energy storage capacitor is enough to inject the required inverter voltage for 100 % voltage sag for a duration of 3 s. A simulation with the averaging method is performed for 3 s duration. The storage capacitor value is 168.8 mF in this circuit simulation. Since this duration is too long to display graphically, only the last 2 cycles are given for the 3s voltage sag simulation (Figure 4.32). Here, it is seen that the top of the waveform is flat, indicating that the inverter is in overmodulation mode. However, the waveform contains ripple at the output filter resonance frequency (750 Hz). This is because overmodulation of PWM waveform adds low frequency harmonics to the inverter output. The harmonics close to the filter resonance frequency are amplified by the filter. It should be noted that load voltage feedback control was not employed in the average model. If this was employed, the effects of this resonance could be decreased.

The actual DC bus voltage intersects critical DC bus voltage at 3365 ms. The holding time is equal to 3365 ms – 20 ms = 3345 ms. The peak value of the fundamental load voltage is 294.77 V at the time range of 3340 ms- 3360 ms. The results of this simulation are given in Figures 4.30 – 4.32.

Temporary voltage sags of 60 seconds duration could not be simulated, even using the averaging method because of the excessive simulation time required and insufficient hard disk capacity.

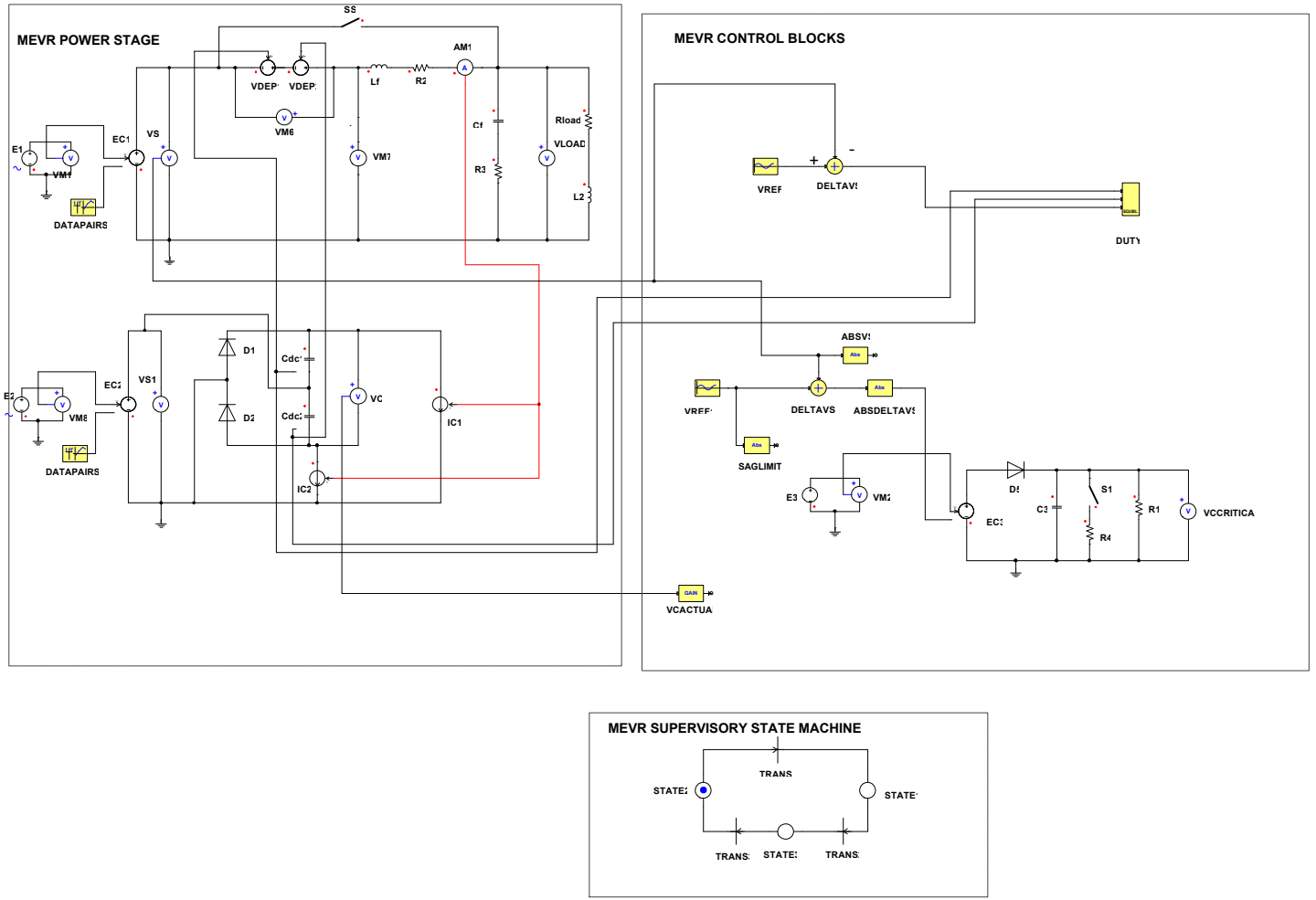


Figure 4.27. MEVR simulation circuit with averaging method.

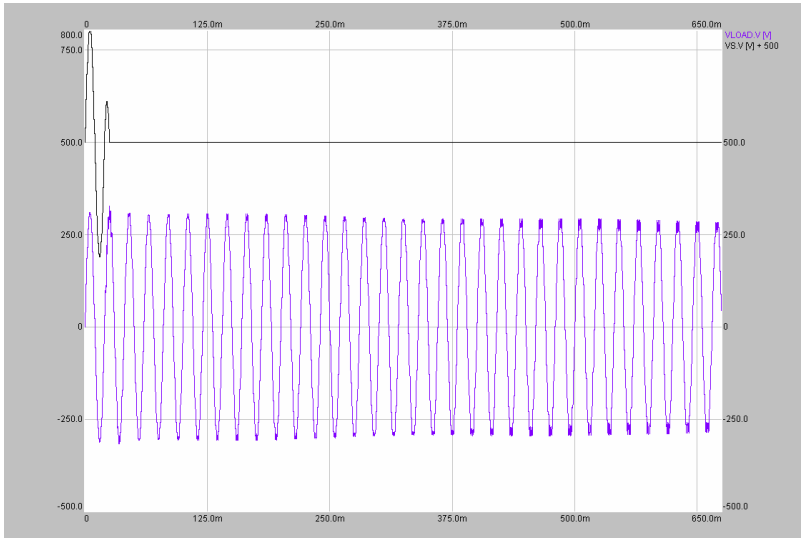


Figure 4.28. V_s and V_{load} for 500ms.

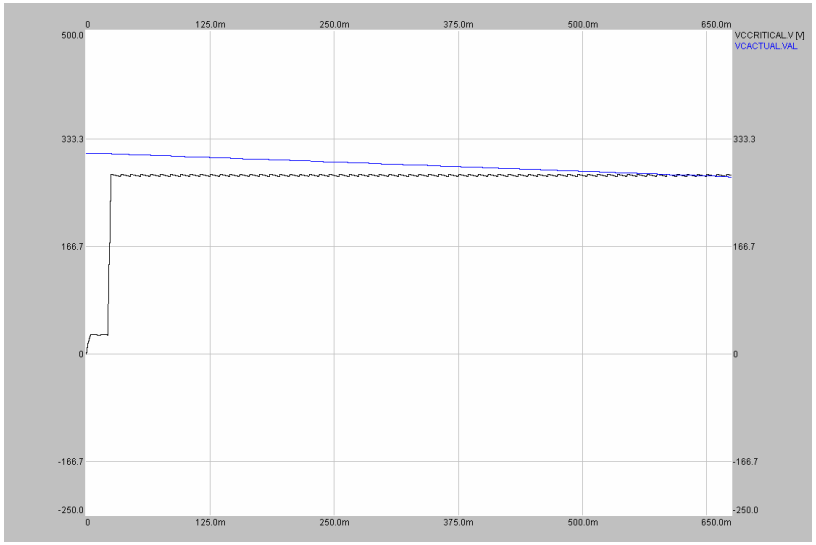


Figure 4.29. $V_{cactual}$ and $V_{ccritical}$ for 500ms.

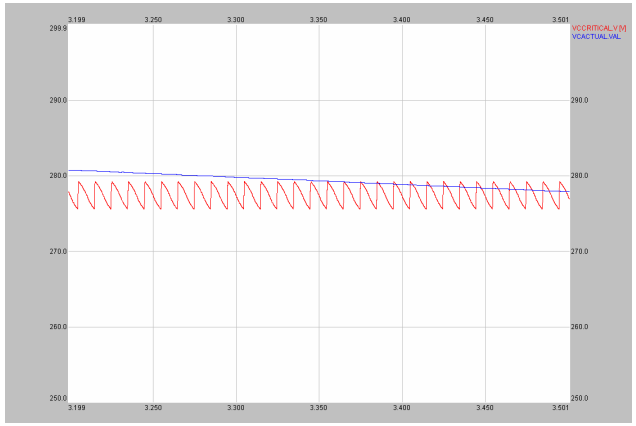


Figure 4.30. $V_{cactual}$ and $V_{ccritical}$ for 3s

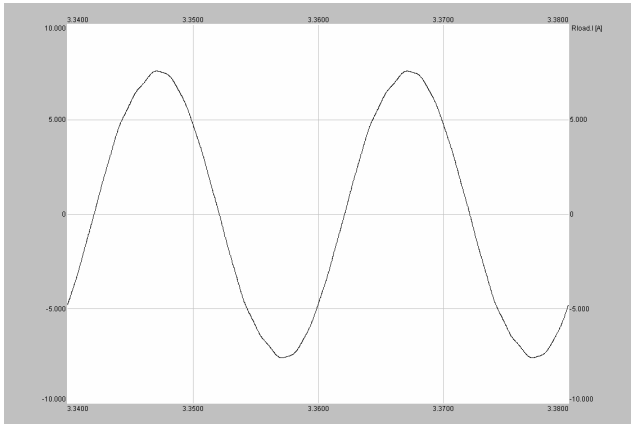


Figure 4.31. I_{load} for 3s

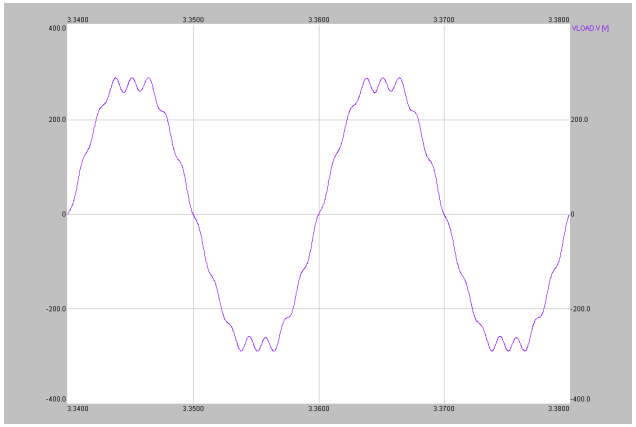


Figure 4.32. V_{load} for 3s

4.4 MEVR SIMULATION CIRCUIT FOR INJECTED POWER MINIMIZATION

To investigate the behavior of the injected power minimization method, the simulation circuit in Figure 4.33 is utilized. In order to simplify the circuit simulation, the calculations employing the block diagram and corresponding flowchart given in Figures 3.40-3.41 is performed manually (off-line) to determine the d-axis and q-axis components of the required inverter voltage for a certain voltage sag condition. Afterwards, the open-loop simulation model described below is used to inject the required inverter voltage.

In this circuit simulation, the inverter in-phase voltage component (INPHASE_COMPONENT) is obtained by multiplying the d-axis component of required inverter voltage with a sine waveform. Similarly, the inverter quadrature voltage component (QUADRATURE_COMPONENT) is obtained by multiplying the q-axis component of the required inverter voltage with a cosine waveform. Afterwards, these two components are added to form $V_{invrequired}$. This summation is the reference voltage for the inverter and it is required for the voltage sag compensation. $V_{invrequired}$ is added with source voltage to obtain reference voltage for the nominal load voltage (VREF). DELTAVLOAD is the difference between VREF and VLOAD. DELTAV1 is the summation of DELTAVLOAD and Vinvrequired. Then, DELTAV2 and duty cycle for the PWM operation are as discussed in the previous sections.

Utilizing this simulation circuit, source current THD is calculated and given in Table 3.5. Also, inverter voltage, inverter current, inverter output power are calculated. These calculations are in accordance with the value in Table 3.5.

4.4.1 Simulation Results for The Injected Power Minimization Method

The simulation results and theoretical results are compared in Table 4.5 for S_c = 0.3. As seen from this table, the results are mainly in accordance with each other.

Table 4.5. The comparison of simulation and theoretical results for injected power minimization method.

Sc = 0.3	**100 ms- 120 ms**	
	Simulation results	**Theoretical results**
V_{inv}	131.18 V_{rms}	133.82 V_{rms}
I_{inv}	5.08 A_{rms}	5.68 A_{rms}
P_{inv}	115.83 W_{mean}	124.96-W
I_s (THD)	12.88 %	-
V_{load} (THD)	1.34 %	-

Note that, if in-phase voltage injection method had been used instead of injected power minimization method, the inverter would supply 30 % of the load power for S_c = 0.3 (utilizing Eqn.3.68), so P_{inv} would be 300 W for a 1 kW load. The simulation results above support theoretical analysis. With injected power minimization method, for Sc = 0.3, the inverter power is reduced by approximately 60 %.

The graphical results for this simulation are given in Figures 4.34 – 4.37.

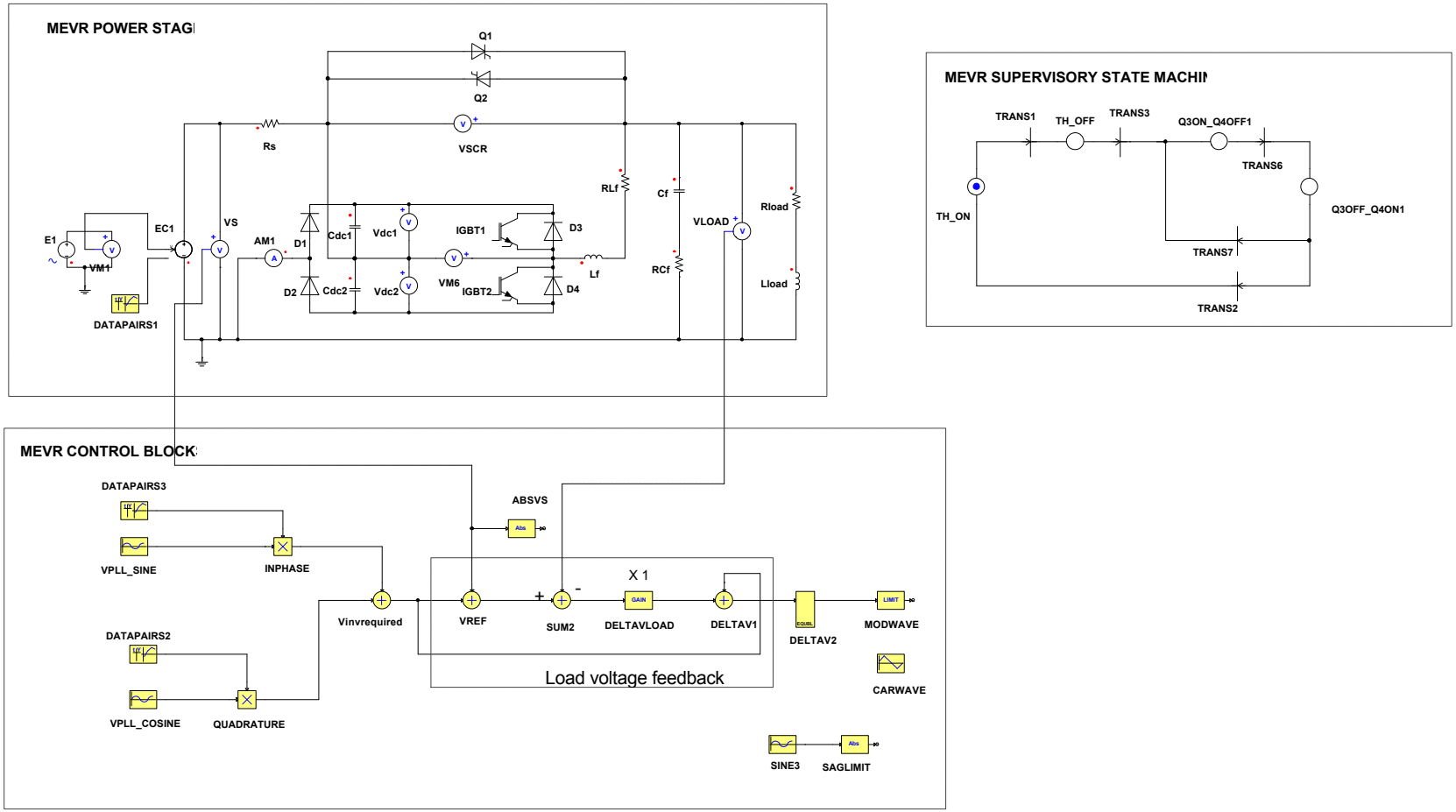


Figure 4.33. Simulation circuit for injected power minimization.

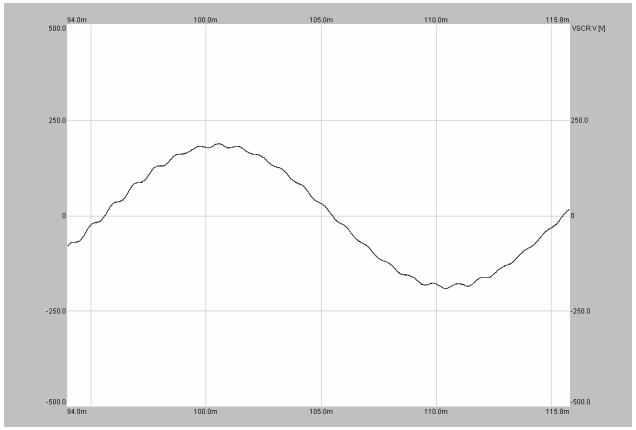


Figure 4.34. V_{inv} for S_c =0.3.

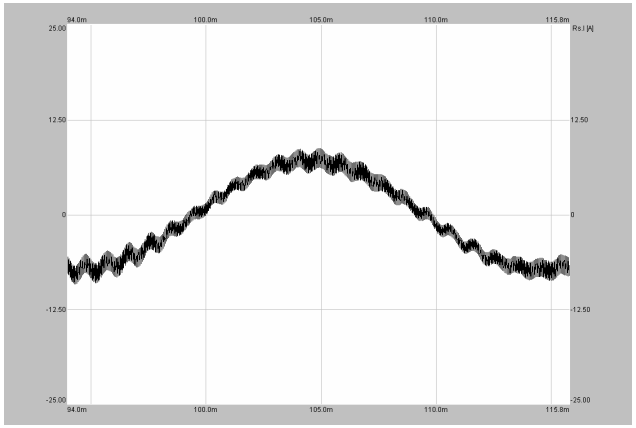


Figure 4.35. I_s for S_c = 0.3.

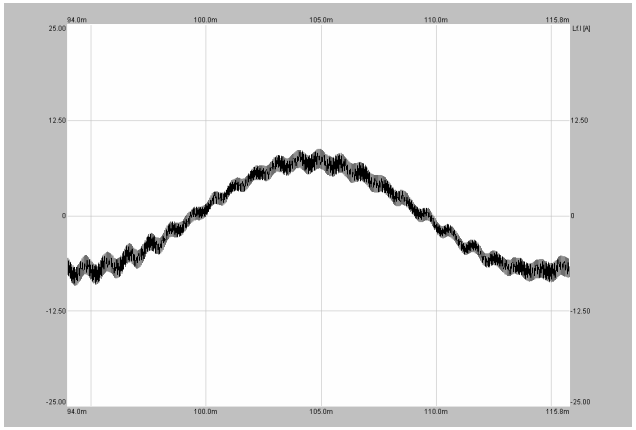


Figure 4.36. I_{inv} for S_c = 0.3.

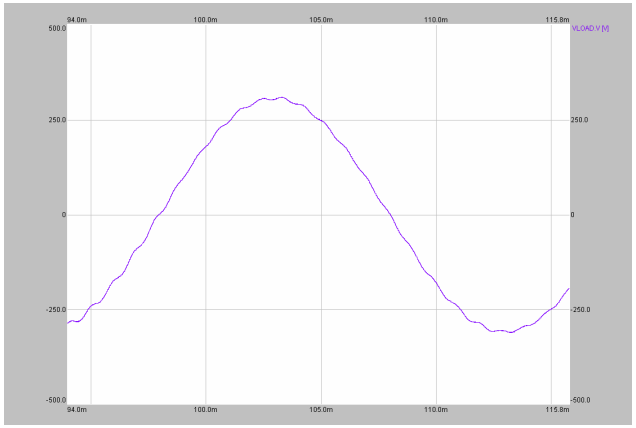


Figure 4.37. V_{load} for S_c = 0.3.

4.5 VALIDATION OF AVERAGE MODEL

In this section, the MEVR average model utilized during simulations is validated by comparing its results with MEVR full model results for the same simulation conditions.

The simulation conditions for this comparison are 70 % voltage sag ($S_c = 0.7$) with $C_{dc1} = C_{dc2} = 3.37$mF. The simulations have been performed up to 200 ms. For comparison, all waveforms are plotted between 100 ms and 200 ms in Figures 4.38-4.41. The load voltage and capacitor voltages can be seen in these figures for both simulation models.

It is observed that the load voltage waveforms are in accordance with each other (Figure 4.38 and Figure 4.39). Although MEVR full model simulates each switching operation, the output filter produces a clean waveform very similar to the one obtained from MEVR average model.

The capacitor voltages are also very similar for both simulation models. The voltage of C_{dc1} drops from 295 V to 257 V within 100 ms for both models (Figures 4.40 and 4.41). For C_{dc2}, the voltage drops from 295 V to 257 V for the average model, while it drops from 298 V to 260 V for the full model. This offset of 3 V in the full model can be explained by the delay time (close to 1 cycle) in the full model. In the MEVR average model, the thyristors and IGBTs are not modeled, so there is no commutation time. The inverter starts operating immediately. Therefore at 100 ms, the inverter in the average model has operated more than the inverter in the full model. As a result, the capacitors in the average model are expected to be at a lower voltage compared to those in the full model.

In general, MEVR average model has been validated as above. For long simulations, the average model can be used instead of the full model with similar results.

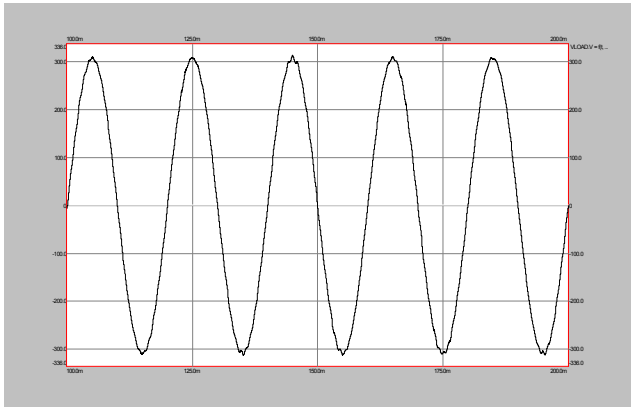


Figure 4.38. V_{load} for full model.

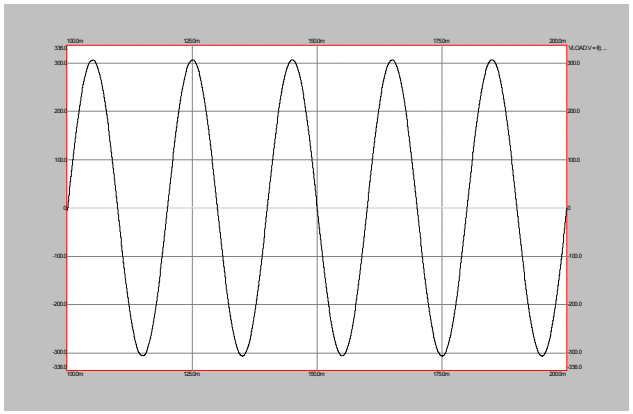


Figure 4.39. V_{load} for average model.

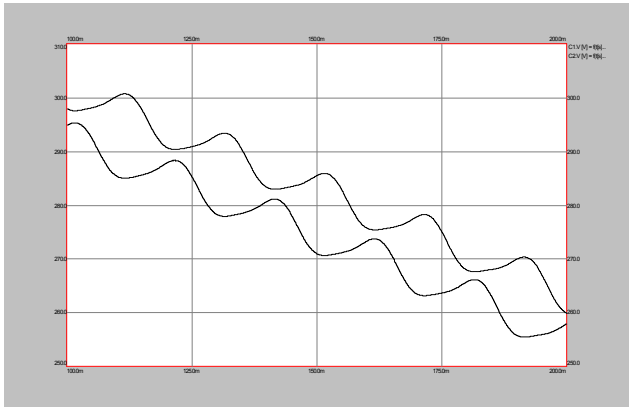


Figure 4.40. V_{dc1}, V_{dc2} for full model.

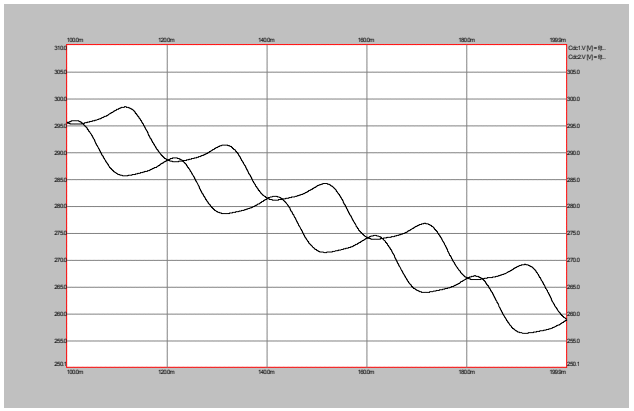


Figure 4.41. V_{dc1}, V_{dc2} for average model.

4.6 MEVR FULL MODEL SIMULATIONS FOR CONSTANT POWER LOAD

Until this section, MEVR simulations were run for RL type load. To investigate MEVR simulation circuit behaviour for constant power load, the full model is utilized. Moreover, these simulations are necessary for investigating characteristics of non-linear or IT equipment which has SMPS at the input terminals. The simulation circuit is shown in Figure 4.42.

The constant power load in Figure 4.42 simulates IT equipment which has SMPS at the input terminals. This load is a bridge rectifier with parallel voltage controlled current source (IC1 = 1000W/VM7). For this load, the load resistance value depends on the voltage. Therefore, this resistance is modeled as a controlled current source (IC1). That current source is dependent on measured voltage (VM7) and requires constant power (P_{load}) at the output of diode rectifier.

Simulations for constant power load have been run for 30 % voltage sag. All other parameters (except the type of load and the load voltage feedback gain, Kp) for these simulations are the same with previous simulation parameters. The gain in load voltage feedback circuit was selected as Kp = 1.2 since this value of gain yields a slightly lower value of load voltage THD.

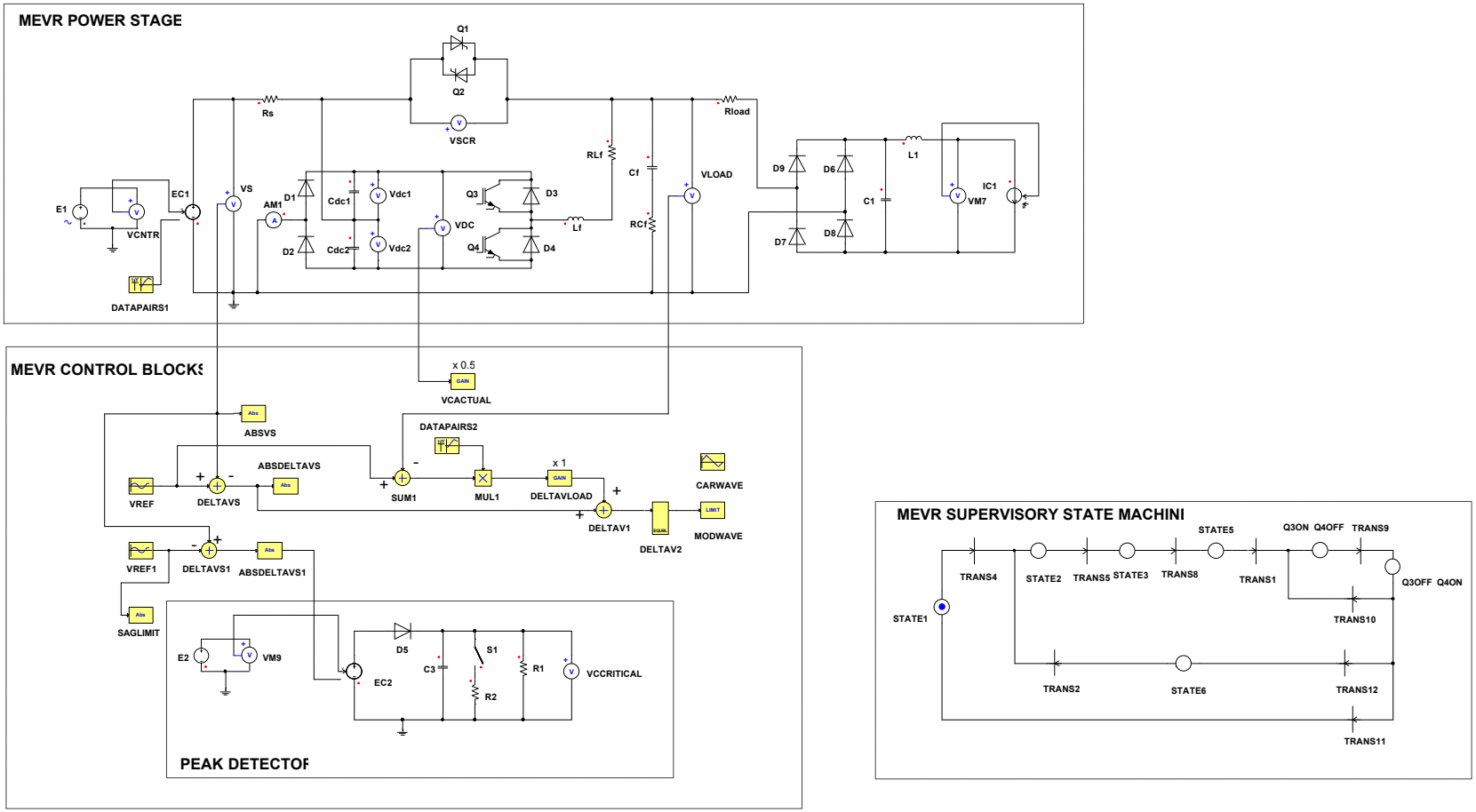


Figure 4.42. MEVR full model for constant power load.

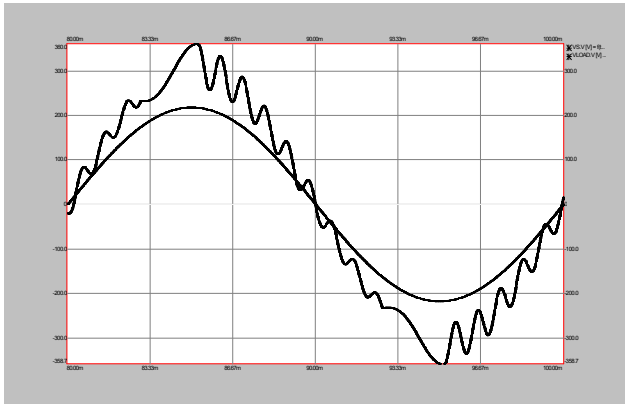


Figure 4.43. V_s, V_{load} for constant power load.

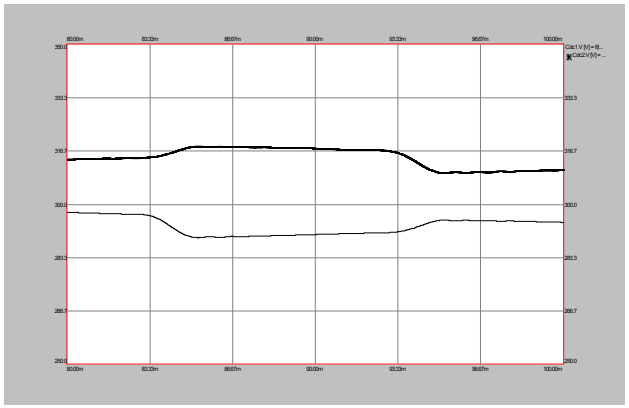


Figure 4.44. C_{dc1}, C_{dc2} for constant power load.

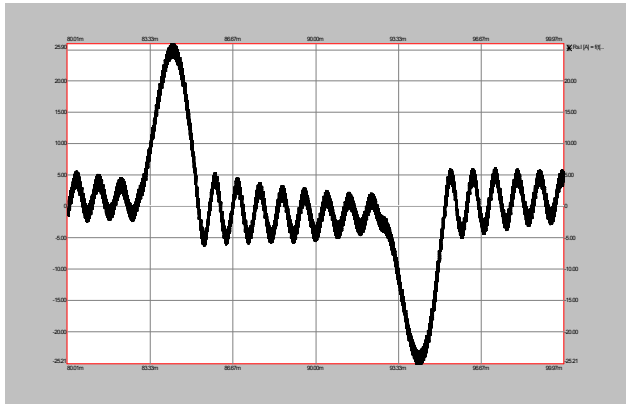


Figure 4.45. I_s for constant power load.

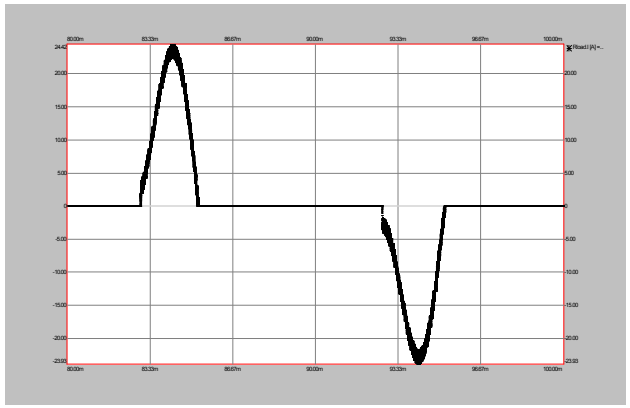


Figure 4.46. I_{load} for constant power load.

As seen from simulation results, the load voltage in Figure 4.43 is not a pure sine wave and has harmonics causing a high THD (between 11 % and 12 %). The harmonics are mainly in the 750 Hz – 1000 Hz range, which corresponds to the LC filter resonance frequency and slightly higher frequencies. However, the fundamental value of the load voltage is 311 Vpeak, indicating that MEVR corrects the voltage sag as predicted.

Figure 4.46 shows the load current. Due to to the non-linear nature of the load, the load current is not continuous but it is in the form of pulses instead. This is because the load draws current only when the capacitor in the load (C1 in Figure 4.42) has discharged below the absolute value of load voltage, VLOAD.

Due to the discontinuous load current waveform, constant power load causes a non-sinusoidal source current (Figure 4.45). It is also seen that the source current is affected from the load voltage since current pulses at the same harmonic frequencies as the load voltage harmonics are present in this waveform.

The energy storage capacitor voltages are shown in Figure 4.44. The main difference between this simulation and the previous simulations for RL loads is in the shape of this waveform. As the load draws discontinuous current from MEVR, the charging and discharging of these capacitors occurs only during certain intervals of each cycle. During the remaining part of the cycle, the energy storage capacitor voltages remain almost constant.

CHAPTER 5

LABORATORY IMPLEMENTATION OF MEVR

5.1 INTRODUCTION

The single phase MEVR has been implemented for testing at the laboratory with a rating of 1 kW. The power stage of MEVR is given in reference [1] (However, the control strategy of the device is not given in this reference). Therefore, "In-phase Injected Voltage Method" is used in this implementation as explained in section 3.2.5.1. In this implementation, MEVR is utilized for voltage sag correction only. For voltage swells, no correction is made and the source voltage is directly transferred to the load via the static switch. MEVR circuit has been tested in laboratory using RL load with voltage sag tests.

MEVR hardware is formed by two main stages: Power stage and Control stage. The overall photograph of the device is shown in Figure 5.1 below.

The control stage of MEVR is formed of the following:

i. DSP board, using TMS320F240 DSP Controller
ii. Embedded control software, running on TMS320F240 DSP controller
iii. Converter Interface Board (CIB)
iv. Power Supply Board (PSB)
v. Gate Drive Circuit Board (GDC)

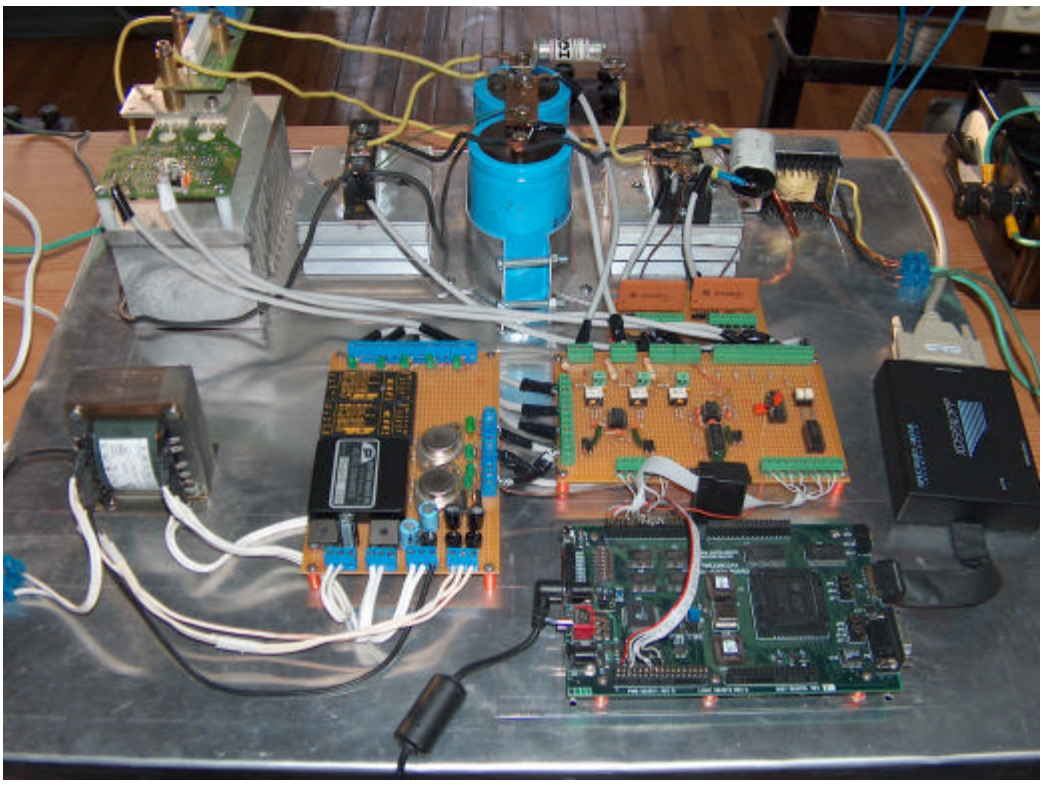


Figure 5.1. Overall picture of MEVR test circuit.

5.2 POWER STAGE

Voltage sag regulation is performed at the power stage of MEVR. These components are the following (see Figure 3.4 for the location of these components on MEVR schematic):

Q_1, Q_2 : Thyristors (Static bypass switch)

Q_3, Q_4 : IGBTs

C_{dc1}, C_{dc2} : Energy storage capacitors

D_1, D_2 : Charging diodes

D_3, D_4 : Freewheeling diodes

L_f : Filter inductance

MEVR power stage can be divided into three main groups: Static bypass switch, inverter, rectifier and DC Link (see Figure 5.2 for photograph).

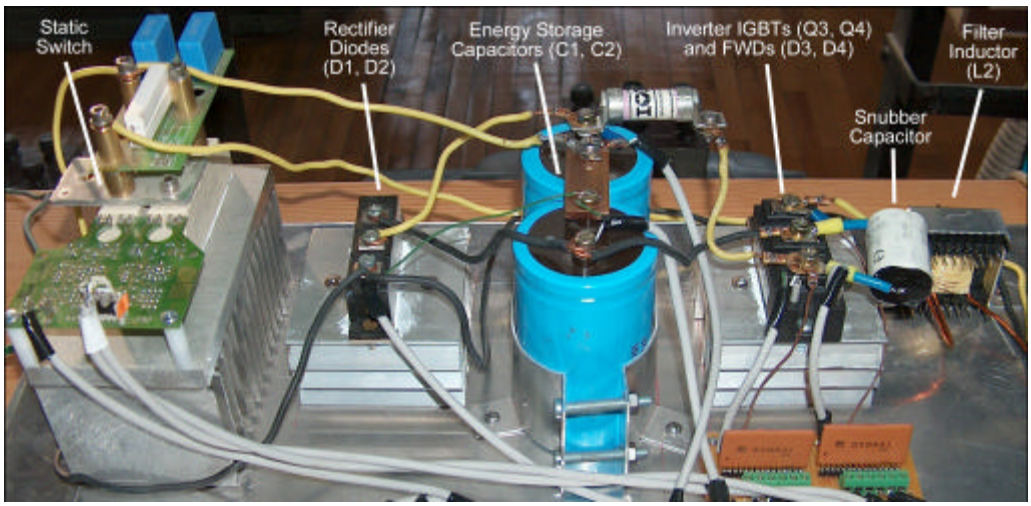


Figure 5.2. Picture of power stage components.

Note that for an actual MEVR implementation, an "energy storage capacitor precharging circuit" should also be included in the power stage in order to prevent excessive inrush currents during initial capacitor charging. When MEVR is switched on for the first time, the energy storage capacitors will initially be fully discharged. Unless there is a current limiting circuit, the storage capacitors will draw large charging current pulses from source. A precharging circuit can be added by including a series current limiting resistance between source inductance and the midpoint of energy storage capacitors. However, after the storage capacitors have been charged (i.e., after one cycle), this resistance should be bypassed using a relay or static switch to avoid additional voltage drops and power losses. The current rating of this relay or static switch should be at least equal to the maximum source current. Such a precharging circuit is shown in reference [9]. The laboratory prototype does not include a precharging circuit in order to reduce circuit complexity. Because the initial voltage is increased employing a variac, the inrush currents are avoided. The filter capacitor has also not been utilized at the output of test circuit.

5.2.1 Selection of Power Stage Components

5.2.1.1 IGBTs (Q_3, Q_4) and Freewheeling Diodes (D_3,D_4)

The IGBT voltage ratings have been selected twice as much as the maximum voltage observed across the terminals of the IGBTs. Since the IGBTs would observe 622V (the summation of two capacitor voltages),

$$V_{ce,max} = V_{dc1} + V_{dc2} \tag{5.1}$$

Therefore, the voltage rating of IGBTs are selected as 1200 V. A 100 % safety margin for voltage is used because during switching of IGBTs, the stray inductances and capacitances in the circuit may cause resonances. These resonances can cause up to 100 % voltage overshoots during worst case conditions.

As MEVR test circuit is designed for 1 kW rating with 0.8 lagging power factor, rated current will be 5.68 A_{rms}. The maximum current value that IGBTs will carry is 8 A (peak). However, the current rating is selected as 16 A because of 100 % safety margin. This safety margin has been selected in order to obtain a sufficient thermal safety margin (to keep switching and conduction losses at an acceptable level).

Fuji Electric 2MBI50N-120 is used as the IGBT module. This module includes two IGBTs (Q_3, Q_4) and two freewheeling diodes (D_3, D_4). The voltage rating of IGBTs are 1200 V, current rating is 50 A. This module is installed on a heatsink with natural cooling.

5.2.1.2 Diode module (D_1, D_2)

These diodes are used for charging the energy storage capacitors. Powerex CD411299 8846 is used as the diode module. This module includes two diodes connected in series. Diode module is installed on a heatsink with natural cooling.

5.2.1.3 Energy Storage Capacitors (C_{dc1}, C_{dc2})

Two identical capacitors are used as energy storage capacitors. Each of them has 1000 μF capacitance and 450 V voltage ratings. These components' value determines the device capacity (inverter holding time) and ability to correct voltage sags. Therefore, the calculation of storage capacitor values are the most important issue in the design of this circuit. This subject was discussed in chapter 3.

5.2.1.4 Static bypass switch (Q_1, Q_2)

Static bypass switch is used to transfer the nominal source voltage to the load side. SKKT 42B 12E of SEMIKRON is used as the static bypass switch. This is a semi-assembled module, mounted on its heatsink together with its gate drive PCB and busbar. The heatsink is naturally cooled.

5.2.1.5 Filter Inductor (L_f)

It is desired to obtain a sinusoidal load voltage which contains less harmonics. Therefore, filter inductor (L_f) is used at the inverter output. This inductance reduces the load voltage harmonics but also reduces the fundamental component of the load voltage. Increasing the inductance provides a better filter but also a higher voltage drop at the load side. L_f has been selected as 100 μH, so the voltage drop on the inductance is less than 1 V at 50 Hz.

5.2.1.6 Snubber capacitor (C_{sn})

The snubber capacitor is mounted directly on the IGBT module terminals to reduce stray inductances. The snubber is used to protect the IGBTs against voltage overshoots. E.C. MP2-11395J is used as the snubber capacitor, which is parallel to the IGBTs. The capacitor has a value of 470 nF±5 % with a rating of 1400 VDC.

5.3 CONTROL STAGE

5.3.1 The General Controller Design Logic

The main purpose of the control stage is to produce the gate signals (PWM) which are required for controlled switches (thyristors and IGBTs) in the power stage. The control stage monitors source voltage and energy storage capacitor voltages continuously. The error signals are fed to the controller as well. The general inputs and outputs of the controller can be seen in Figure 5.3:

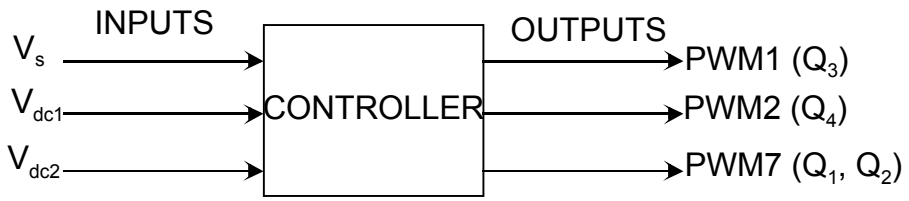


Figure 5.3. Inputs and outputs of the controller.

The main part of controller is the software which is embedded into the DSP microcontroller. This software monitors source voltage of regulator. Thus, the software decides if there is a nominal voltage or a voltage sag. If there is a nominal voltage at the source, the software produces PWM7 for the thyristors and turns static bypass switch on. The pulse train applied to both thyristors is at 10 kHz frequency. At the same time, PWM1 and PWM2 signals for the IGBTs are held at "active low" state to keep them off (-5 V).

If the control program detects a voltage sag at the source, it switches PWM7 signal to "active low" state so that thyristors (static bypass switch) are off. Detection of voltage sag is made according to "Acceptable Band Method With Hysteresis & Time Delay" (discussed in chapter 3). Then, program produces PWM1 and PWM2 signals to switch IGBTs on to operate the inverter. The switching frequency of these semiconductors are 20 kHz (switching period is 50 μs). The inverter produces voltage pulses using the available DC link voltages (energy storage capacitor

voltage). Since the inverter voltage is in series with the source voltage, the PWM voltage waveform is imposed onto the low source voltage as discussed in chapter 3. The "in-phase injected voltage method" is utilized for voltage sag correction.

5.3.2 Control Hardware

5.3.2.1 General Control Hardware Layout and Signal Flow

In this section, the control boards are briefly described. There are four main boards in the control hardware:

i. DSP Board
ii. Converter Interface Board (CIB)
iii. Power Supply Board (PSB)
iv. Gate Drive Circuit Board (GDC)

The control stage communicates with the power stage by signals flowing between them (see Figure 5.4). These are:

Input signals: Analog feedback signals (source voltage and capacitor voltages) and digital status signals (errors) from the power stage

Output signals: Digital control signals for controlling the power semiconductors (PWM1, PWM2, PWM7)

Power Inputs: Power inputs from utility source (220 VAC)

5.3.2.2 Converter Interface Board (CIB)

The converter interface board is the board where signals are transformed between power stage and the control stage (DSP board). The main functions of this board are,

i. Transmits PWM signals from DSP to gate drive circuits of all power semiconductors,
ii. Changes the level of PWM1 and PWM2 signal from 5 V to 15 V,
iii. Transmits error signals from power stages to DSP board,

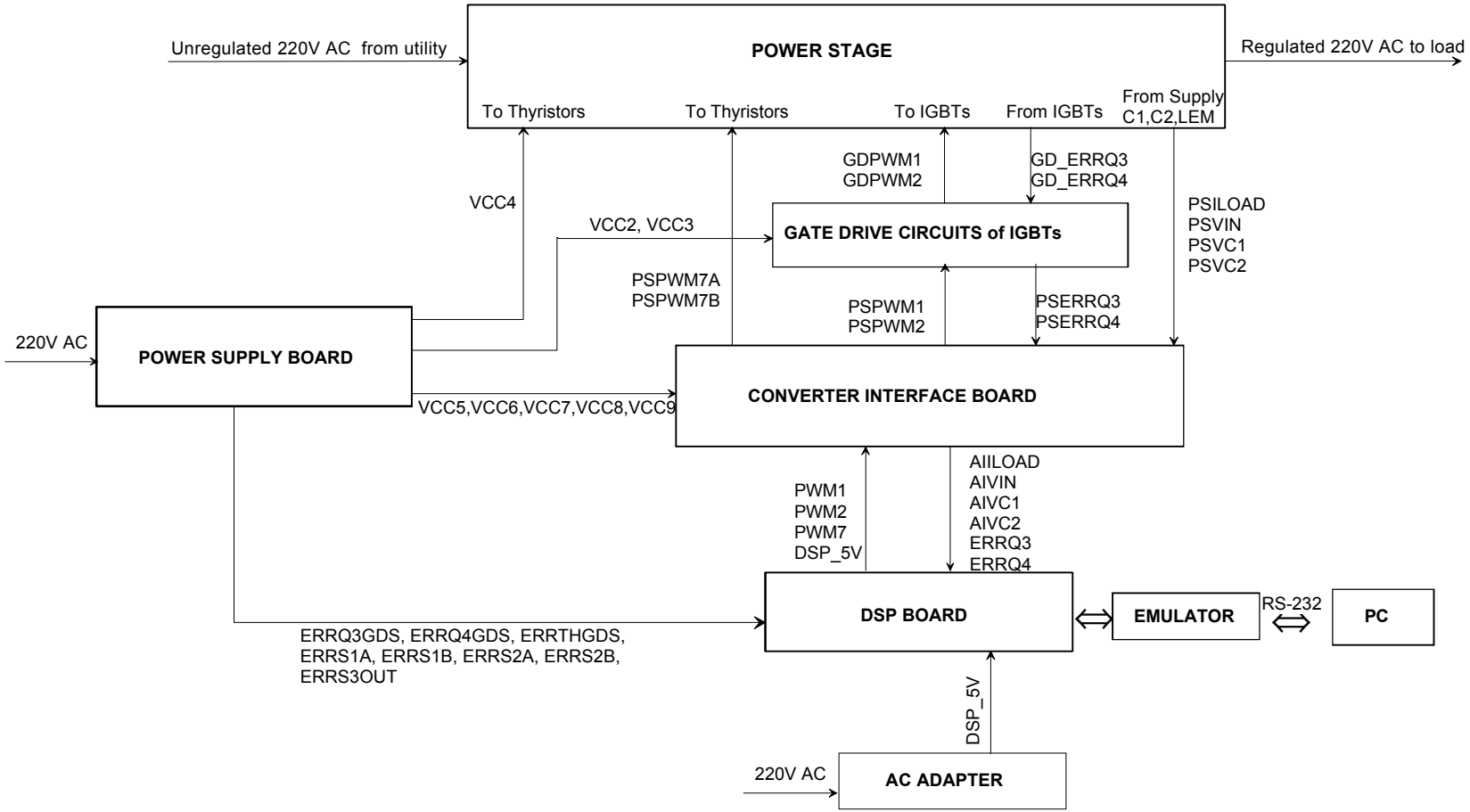


Figure 5.4. Main signal flow diagram.

iv. Changes the level of analog signals from high voltage level to DSP level,

v. Isolates control stage from power stage using analog and digital optocouplers. (7 different reference levels, labeled “GND, GND2,…” etc are used in this converter.) In Figure 5.5, these references are shown.

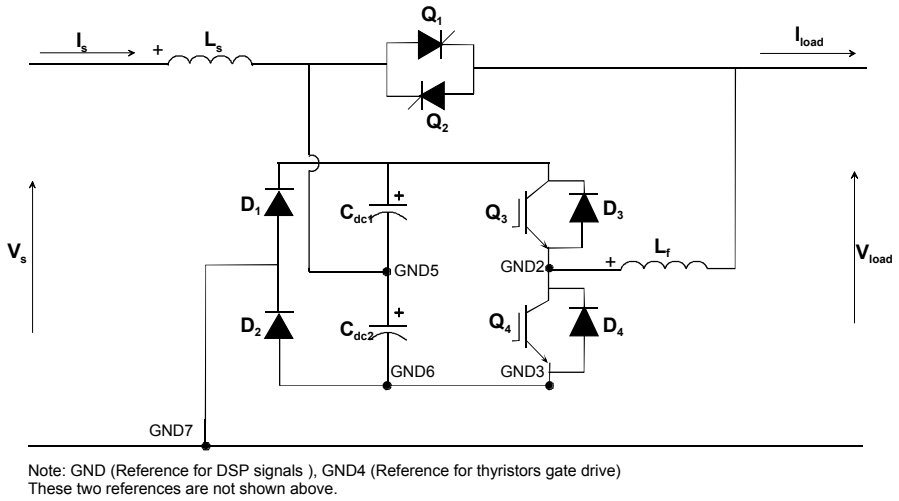


Figure 5.5. Power stage and GND references.

5.3.2.3 Power Supply Board

The power supply board (with its transformer) supplies energy to the components on the control stage boards except DSP board. DSP board is supplied by its own AC adapter (DSP_5 V and GND). The outputs of the transformer are inputs of the power supply board. Transformer supplies different AC voltage and power levels required to power supply board from different secondary windings. Power supply board converts AC voltage to DC voltage and supplies DC voltage to the electronic components on the converter interface board and gate drive circuits.

The 220 V voltage is the input of the transformer. Outputs of the transformer are: $30V_{rms}$/3VA (two identical windings), $24V_{rms}$/24VA, $21V_{rms}$/3VA (two identical windings)

5.3.2.4 Gate Drive Circuits Board

IGBTs on the power stage are controlled by their gates. IGBTs are switched off by applying (–5 V) between their Gate-Emitter terminals and switched on by applying (+15 V) between their Gate-Emitter terminals.

Converter interface board converts DSP board inputs which are at 5 V level (PWM1 and PWM2) to current signals. These current signals are sent to Gate Drive circuits for driving the optocouplers embedded inside. EXB841 is the gate drive component used for IGBT gate drives. EXB841 is a hybrid integrated circuit capable of driving up to 400 A for 600 V IGBTs and up to 300 A for a 1200 V IGBTs. It is suitable for switching at up to about 40 kHz [19]. Since the ratings of our IGBTs are 1200 V, 50 A and the IGBTs are switched at 20 kHz, this drive is suitable for our implementation.

5.3.3 Control Software

5.3.3.1 General Discussion and Objectives of Software

The full control logic of MEVR test circuit with in-phase injected voltage method has been implemented as an embedded software running on the DSP controller (TMS320F240). The software has been written in assembly language of TMS320F240. The software has been written in modular form; each module performing a specific function. In Figure 5.6, these modules and the main (overall) program flowchart is given. The program flow is controlled by the global variable MODE. The state of the main control logic is defined by this variable. Table 5.1 lists possible values of MODE.

From the main program flowchart, it can be seen that the program consists of two main parts:

1. Initilization part, which is executed only once during initial run. This part is used for initilizating variables, registers, timers, interrupts, etc. It is also used

for precharging capacitors (C_{dc1} and C_{dc2}) which are assumed to be discharged during initial power-up.

2. Main-loop part, which is an endless loop running in real time at exactly 20,000 times per second. The main loop is controlled by a Real Time Operating System (RTOS).

The execution rate of these modules are synchronized with the IGBT switching frequency (20 kHz). In case the circuit is correcting a voltage sag and the inverter is operating, the pulse widths of the IGBT pulses will be calculated and updated 20,000 times every second (i.e. at each switching period.)

Table 5.1. MODES of the control program.

MODE	DESCRIPTION OF MODE
0	Initialization mode (Default)
1	Precharging mode
2	Error mode
10	Line voltage is nominal.
11	Line voltage is nominal but there could be a voltage sag. Voltage sag duration is being checked.
12	Line voltage is nominal but there could be a voltage swell. Voltage swell duration is being checked.
20	There is a voltage sag in the line voltage and it's continuing.
21	There is a voltage sag in the line voltage but the line voltage could be nominal. Nominal duration is being checked.
22	There is a voltage sag in the line voltage but there could be a voltage swell in the line voltage. Voltage swell duration is being checked.
30	There is a voltage swell in the line voltage and it's continuing.
31	There is a voltage swell in the line voltage but the line voltage could be nominal. Nominal duration is being checked.
32	There is a voltage swell in the line voltage but there could be a voltage sag in the line voltage. Voltage sag duration is being checked.
40	Nominal (SCR) to voltage sag (IGBT) commutation
41	Nominal (SCR) to voltage swell (IGBT) commutation.
50	Voltage sag (IGBT) to nominal (SCR) commutation.
51	Voltage swell (IGBT) to nominal (SCR) commutation.

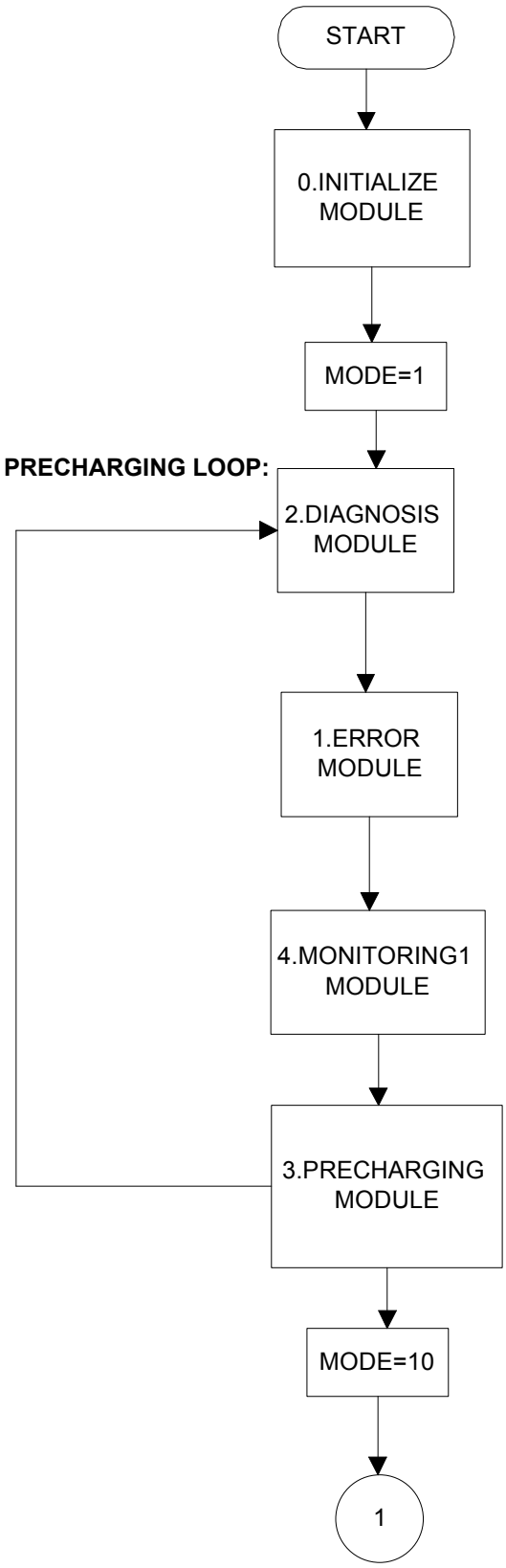


Figure 5.6. Main program flow chart.

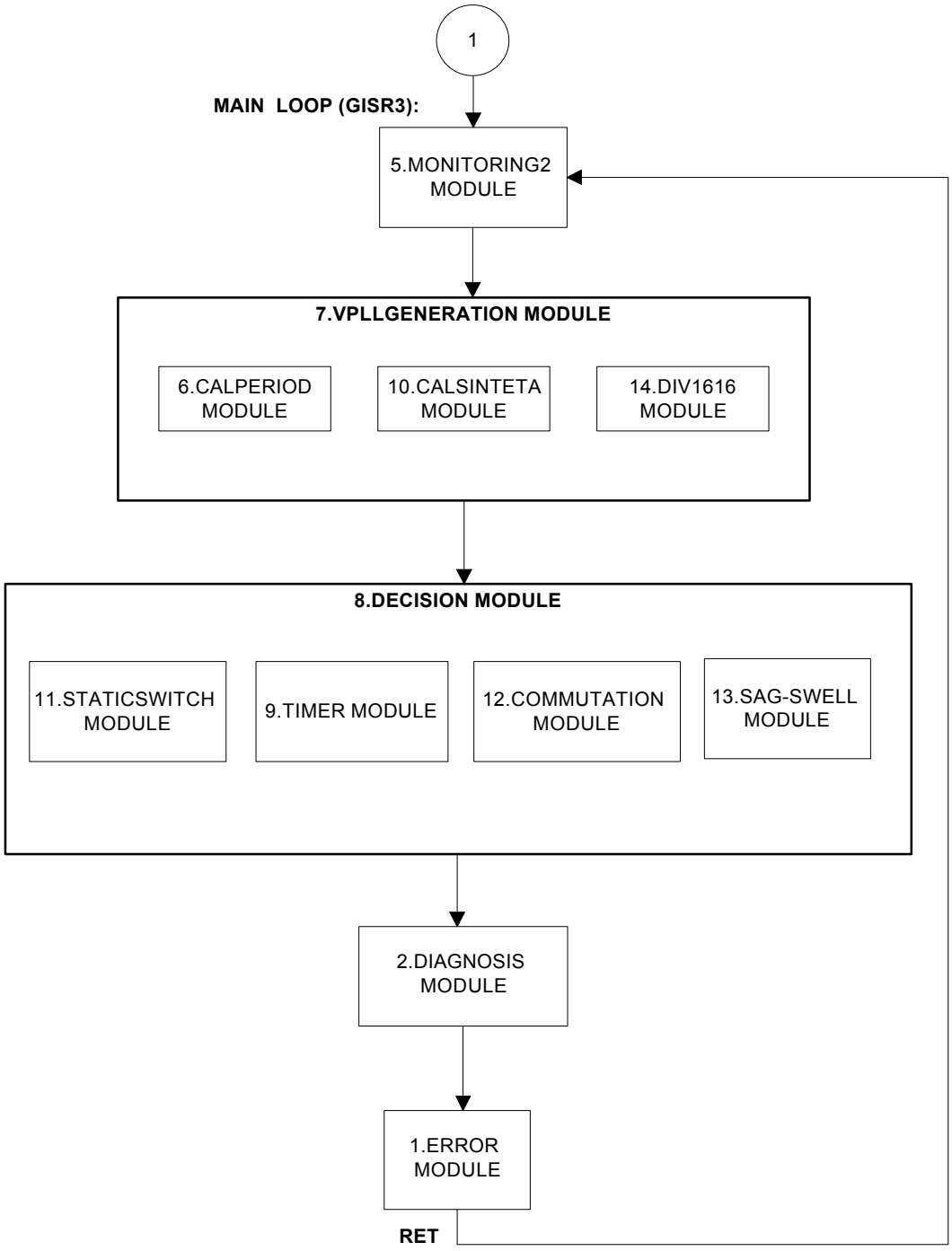


Figure 5.6. Main program flow chart (Continued).

5.4 COMMENTS

A laboratory prototype of MEVR has been implemented. However, this prototype can not be operated at rated voltage and power because MEVR test circuit has problems of operating at voltages above 60 V. The reason the circuit produces problems at higher voltages and currents is EMI (Electromagnetic Interference). Although various measures have been taken to avoid electromagnetic interference, there are still problems due to noise emitted from the power stage that interferes with the control signals.

At voltages higher than 100 V, high values of dv/dt due to IGBT switching cause common mode currents to flow in the control hardware, which are coupled through stray capacitances in the circuit. These cause faulty IGBT operation, even shoot-through faults.

At currents higher than 1 A_{rms}, high values of di/dt cause interferences in the serial communication between PC and Emulator, causing the DSP to halt software execution. These problems arise from the limitations in components, PCB manufacturing, power stage mechanical design and lab equipment. The test setup can be seen in Figure 5.7.

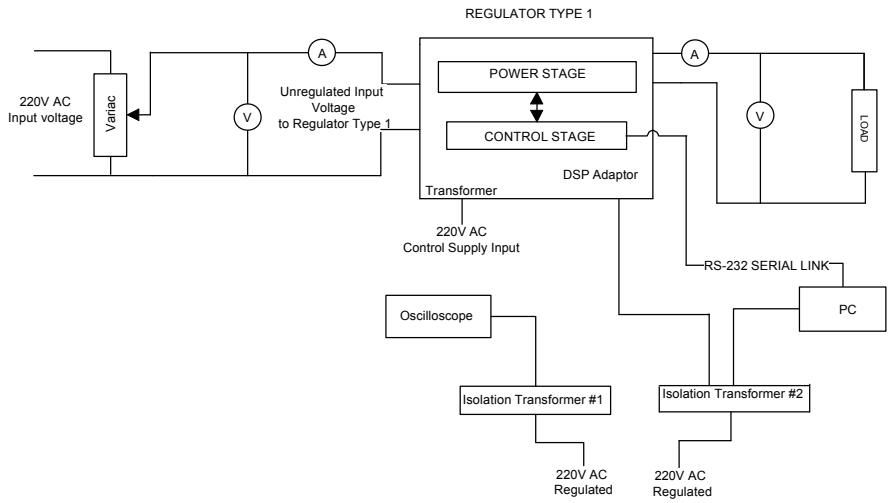


Figure 5.7. Test setup diagram.

CHAPTER 6

CONCLUSION

The following work has been completed within the scope of this thesis: Power quality problems and power conditioning equipment have been investigated. Specifically, voltage sag problems and electronic voltage regulators are taken into consideration. The basic MEVR topology has been the focus of this thesis and the circuit operation has been analyzed in detail. Analytical equations for the inverter power and voltage as a function of the operating conditions (load angle, sag coefficient, load power factor, etc.) have been derived. Limiting conditions for MEVR operation have been investigated in detail. As a result of this analysis, two control methods have been formulated.

The in-phase injected voltage control method has been utilized in most of the circuit simulations as well as for the laboratory prototype control implementation. The main advantage of this method is its simplicity. It can easily be implemented on a low cost microcontroller. Another advantage is the injected voltage is minimized by this method. However, analysis shows that this is not the best control method for minimizing the power drawn from the storage capacitors.

The second control method is the injected power minimization method. This method has the advantage of improving the source power factor, increasing the active power drawn from the source and reducing the active power on the inverter side. This is possible by adjusting the load angle so that MEVR operates at the optimum point on the power vs load angle characteristics. On the other hand, the apparent inverter power is increased because the inverter has to inject higher

voltages. Another disadvantage is due to more complicated control algorithm, more advanced microcontrollers are required for implementation.

A third method for MEVR control, namely the closed loop control method has also been briefly studied. Since this method requires load voltage feedback, it is expected that its response time will be longer during voltage sag correction compared to the other two methods.

Equations for energy storage capacitor sizing and holding time have been derived. The accuracy of the formulas has been verified utilizing circuit simulations for different voltage sag and load conditions. The equation for holding time predicts the actual holding time (determined from circuit simulations) accurately with errors less than 5-10 %.

From the study involving the deep sag compensation capacity of MEVR, it is determined that the inverter holding time depends on storage capacitor capacitance and sag coefficient. The holding time is directly proportional to storage capacitor capacitance. It is inversely proportional with the sag coefficient. If the storage capacitor is selected large, MEVR can correct deep voltage sags or correct voltage sags with longer durations for the same sag coefficient. For low power applications (such as 1-2 kW) and instantaneous voltage sags (0.5 to 30 cycles), storage capacitors in the millifarad range will be sufficient. For longer duration voltage sags (momentary and temporary) and/or higher power applications, storage capacitors must be at least hundreds of millifarads or even in the farads range. With large capacitor sizes being cost prohibitive, it becomes apparent that MEVR is mainly practical for instantaneous voltage sag compensation. Thus, MEVR is optimized for correcting voltage sags and short interruptions. For longer interruptions, deeper sags or high power applications, other solutions such as UPS or flywheel backup systems may be more suitable as discussed in chapter 2. The simple topology of MEVR reduces its cost. Moreover, there is no battery and there is no need for maintenance.

Voltage sag detection methods have been investigated. The “acceptable band method with hysteresis and time delay” has been utilized for voltage sag detection in laboratory prototype. It is observed that this method detects voltage sags quickly and without false alarms.

A second order LC filter has been designed to obtain a sinusoidal load voltage. Load voltage feedback has also been added to the controller to further improve load voltage. MEVR circuit has been simulated extensively to determine its performance under various operating conditions. Simulation results show that a high quality voltage can be maintained at the load side during voltage sags (within the time limit of T_h). The total harmonic distortion of the load voltage is about 1 %, which is within all acceptable limits set by the power quality standards.

A problem observed during simulations occurs due to the LC filter itself. Towards the end of holding time the inverter starts operating in the overmodulation region, causing low frequency harmonics in the load voltage. Harmonics around the filter resonance frequency (750 Hz for this thesis) are amplified further by the LC resonant circuit. These harmonics are visible in the simulation results.

MEVR laboratory prototype has been implemented with a DSP controller and its embedded software for control. However, this MEVR prototype could not be operated at the rated power as discussed in chapter 5.

The main advantage of MEVR is the simplicity in its power stage topology: Only two switches are required for the inverter, and the inverter stage is directly connected to the line, without the need for a transformer. The closest relative of MEVR is DVR (Dynamic voltage restorer), which includes a full-bridge inverter with 4 switches, plus an injection transformer. For short duration voltage sags, MEVR is suitable and preferable in terms of cost and efficiency. However, DVR can compensate for voltage swells as well as voltage sags and it can operate in all the four quadrants of the active-reactive power plane. Therefore, MEVR can be

considered as lower cost and more constrained form of DVR and is suitable for applications that do not require the full capability of DVR. Other types of voltage sag correction equipment involve more complicated topologies, systems and possibly mechanical components (such as motor-generator sets, UPS, etc.).

Another advantage of MEVR is its high efficiency. During nominal voltages (approximately 99.9 % of operation), the static by-pass switch is on and inverter is off. Normally SCRs operate at 50 Hz while during sags the IGBTs operate at 20 kHz. Therefore, during normal operation the semiconductor device losses are quite low, yielding high efficiency. In this respect, MEVR is similar to an off-line UPS.

MEVR also provides the best load voltage quality during nominal voltages. The static by-pass switch connects source to the load directly. Therefore, load voltage is the same as the utility line voltage which is normally a clean supply with low voltage distortion. While it is possible to keep MEVR active all the time by selecting a small tolerance band for the voltage sag, to obtain high quality output voltage MEVR voltage control algorithm must be designed with high quality and fast voltage feedback plus rapid and accurate control methods. However, this approach conflicts with the low cost and high efficiency criteria.

MEVR requires a response time of at least one half cycle (10 ms). The worst case response time can be up to 20 ms (1 cycle) if inverter soft start-up is implemented to reduce the transient oscillations on the load voltage. This means that the load voltage will be interrupted for up to 20 ms during nominal to voltage sag transition.

This interruption is caused by sag detection, commutation time, reverse recovery time and the delay for inverter soft start-up. This interruption time may be decreased by taking the following precautions:

i. The commutation time is one half cycle (10 ms) and necessary for guaranteeing the zero-crossing of the load current to switch thyristor off, if the current is not

monitored. If the thyristor current is monitored by a current transducer (such as LEM) or a resistor in series with the static switch, then the control logic may not have to wait for 10 ms. However, this increases the cost of the controller.

ii. Another method may be to reduce the commutation time by forcing the load current to decrease immediately. This can be possible by switching on one of the IGBTs and providing a more attractive path to the load current. In this case, if the storage capacitor which will support the load current in its present direction is connected in series with the load (by switching on the appropriate IGBT), the current on the thyristor will decrease down to zero quickly [9]. After the load current is zero, this IGBT must be switched off again because the inverter operation will not start yet. Thus, the commutation time of the thyristors may be decreased to less than 10 ms. This method also requires thyristor current monitoring.

iii. If the inverter soft starting is not important for a certain application, then the control logic does not have to wait for the inverter required voltage command (DELTAVS) to be zero. The inverter operation can start immediately after commutation and reverse recovery times.

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