MMIC VECTOR MODULATOR DESIGN

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ABSTRACT

MMIC VECTOR MODULATOR DESIGN

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In this thesis the design of a MMIC vector modulator operating in 9GHz-10GHz band is investigated and performed. Sub-sections of the vector modulator are 4-port (4.8dB) 120^0 phase shift relative to the dedicated port power splitter, digitally controlled variable gain amplifier and the in phase power combiner.

Alternative methods are searched in order to implement the structure properly in the given frequency band. The final design is appropriate for MMIC structure.

4-port (4.8dB) 120^0 phase shift relative to the dedicated port power splitter is studied. The performance is simulated and optimized first on Microwave Office, then on Advanced Design System (ADS) tools.

Various methods to design a digitally controlled variable gain amplifier are studied. The final topology is simulated and optimized on ADS tool.

An in phase power combiner is designed. The performance of the combiner is simulated and optimized on ADS tool.

Lumped element models are replaced with CASWELL H-40 models to achieve a MMIC structure and a layout is drawn. The finalized vector modulator is simulated and optimized on ADS tool.

Key words: MMIC, Vector Modulator, Digitally Controlled Variable Gain Amplifier, Layout

ÖZ

MMIC VEKTÖR MODÜLATÖR TASARIMI

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Bu tezde 9GHz-10GHz bandında çalışacak bir vektör modülatör tasarımı üzerinde araştırma yapılmış ve tasarım gerçekleştirilmiştir. Vektör modülatör; 4 kapılı (4.8 dB) 120^0 faz farklı güç bölücüsü, sayısal olarak kontrol edilen değişken kazançlı yükselteç, ve aynı fazlı güç birleştiricisinden oluşmaktadır.

Verilen frekans bandında bu yapının düzgün çalıştırılabilmesi için gerekli değişik yöntemler üzerinde araştırmalar yapılmıştır. Son tasarım MMIC yapıya uygundur.

4 çıkışlı (4.8 dB) 120^0 faz farklı güç bölücüsü üzerinde çalışılmıştır. Yapının benzetimleri ilk olarak Microwave Office'de daha sonra da Advanced Design System (ADS) programlarında gerçekleştirilmiştir.

Sayısal olarak kontrol edilebilen değişken kazançlı yükselteç için çeşitli yöntemler değerlendirilmiştir. Son yapının ADS programında benzetimi ve optimizasyonu yapılmıştır.

Aynı fazlı bir güç birleştiricisi tasarlanmıştır. Birleştiricinin çalışma benzetimi ve optimizasyonu ADS programında yapılmıştır.

Toplu eleman modelleri MMIC yapıyı sağlayabilmek için CASWELL H-40 modellerle değiştirilmiş ve serim çizilmiştir.

Anahtar Kelimeler: MMIC, Vektör Modülatör, Sayısal Olarak Kontrol Edilen Değişken Kazançlı Yükselteç, Serim

To my family

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CHAPTER 1

INTRODUCTION

1.1 Scope and Objective:

In recent years there has been a considerable interest in the use of direct carrier modulation in order to reduce the complexity and cost of microwave circuits. Any signal applied to the vector modulator can be shifted in phase by an amount Ø and adjusted to the attenuation level A (dB).

Amplitude and phase modulation of microwave signals is needed for phased arrays, electronic warfare systems, digital communications and measurement systems. The performance, size and cost of this vector modulator enable improved systems solutions.

Vector modulators can be used effectively as control elements such as phase shifters and attenuators. If the amplitude level is set to a constant level, the modulator can operate as a constant amplitude phase shifter; or conversely if the phase is set to a constant value, it can behave as an attenuator.

Advanced phased array radars with a limited number of elements and very low side lobes require phase shifters of high resolutions. This high phase resolution is very difficult to obtain with digital phase shifters in hybrid technology or on GaAs substrates because of the accumulating phase errors. GaAs MMIC (monolithic microwave integrated circuit) vector modulators are able to provide these phase

shifts at microwave frequencies since they have excellent amplitude and phase balance over a wide band.

The finalized circuit must be optimized to obtain high phase and amplitude resolution over the band, low VSWR, small insertion loss, high return loss and small incidental phase and amplitude change with desired amplitude and phase setting over the band. In addition, high transition speed, small physical size, low power consumption, minimal need for component matching, low cost and minimal control complexity are important systems considerations and are well served by the all MMIC approach.

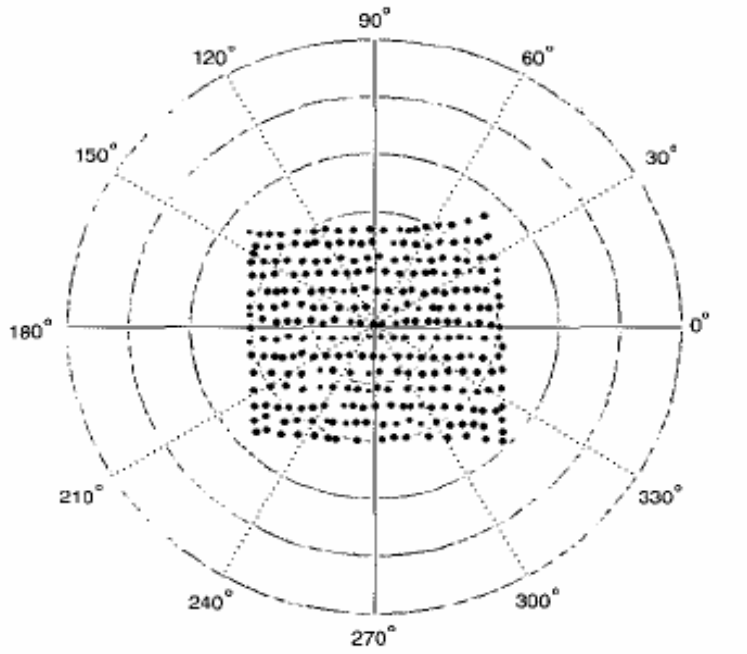

Figure 1 Any (Ø, A) pair can be obtained by the help of vector modulator (constant Ø, variable amplitude) for a fixed frequency [1]

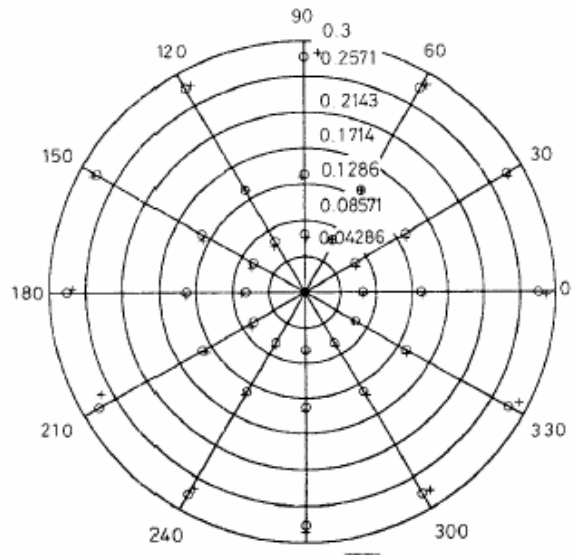

Figure 2 Any (Ø, A) pair can be obtained by the help of vector modulator (constant amplitude, variable Ø) for a fixed frequency [2]

In figure 1; the vector modulator is designed as follows: for a constant phase difference the amplitude level is changed; therefore in a polar coordinate the response is seemed to be a rectangular. In this solution we can not get all (A, Ø) pairs. For example we can not get (10dB, 90^0) pair (assume each circle corresponds to 10 dB); on the other hand (8dB, 90^0) pair can be obtained.

In figure 2; for a constant amplitude difference the phase level is changed; therefore in a polar coordinate the response is seemed to be combination of circles. The radius of the circle is the amplitude level (A dB). All (A, Ø) pair can be obtained in this solution ideally. However; phase resolution and amplitude resolution of the vector modulator determines the how many (A, Ø) pair we can obtain. Because of its quality, the second solution is seemed to be better than the first one for the quality of the output of the vector modulator.

An alternative to vector modulator is phase shifters. Reflective type phase shifters and switched highpass / lowpass phase shifters are among the most important techniques for phase shifting. However, vector modulators are able to adjust both amplitude and phase in one circuit (phase shifters can not cover the full 360^0

range, they have discrete ranges and they do not have amplitude variations) and are well suited MMIC and have low insertion losses and high return losses. In addition, the quality factor of the phase shifters are relatively bad, resulting in high losses and limited phase control ranges. Furthermore, phase shifters are generally digital resulting in low resolution range.

1.2 Organization of the Thesis

The 2nd chapter describes the MMIC applications and the alternative models of the vector modulator.

The 3rd chapter describes the basic theory of the low pass and high pass filter structures used to obtain relative phase shifts. The 4-port 4.8dB 120^0 phase shift relative to the dedicated port power splitter divides the input power equally into three arms with a phase difference of 120° between each port. Advanced Design System simulation and optimization tools were used to simulate and optimize the basic structures. The simulation results were presented at the end of this chapter.

The 4th chapter presents the theory of the variable gain amplifiers and attenuators. Firstly, the theory of variable gain amplifiers and variable gain attenuators were presented, after that the Advanced Design System simulation and optimization results were presented. The simulation results were presented at the end of this chapter.

At the last stage of the vector modulator, an in phase power combiner was used. The work on this part is given in the 5th chapter. After describing the theory of the power combining mechanism, power combiner was presented. Furthermore, we present the total circuit and optimized values with lumped elements. Advanced Design System simulation results were given at the end of this chapter.

In the 6th chapter, lumped elements were changed with the realizable Caswell H-40 linear components. Afterwards, we present the total circuit with layout and due to

lay out mismatches, total circuit was optimized. Optimized values and the simulation results were given at the end of this chapter.

Chapter 7 summarizes the conclusions we arrived at the end of all the work done in this thesis. It discusses the benefits of vector modulators and the recommendations for the possible new realizations and topologies of the vector modulator.

CHAPTER 2

MMIC APPLICATONS and ALTERNATIVE MODELS of VECTOR MODULATORS

2.1 MMIC Applications

The monolithic microwave integrated circuit (MMIC) uses an insulating crystalline material as both the dielectric and the active layer material. Integrated circuits for microwave and millimeter wave frequencies are based on GaAs material. For many new applications, GaAs has become the material of choice because of its ability to perform at high frequencies. It also has a high-resistivity semi-insulating property that reduces cross talk between devices. This permits the integration of active (radio frequency) devices, control (logic) devices, transmission lines, and passive elements on a single substrate. [3]

GaAs's dielectric losses are small compared to Si. CMOS technology can also be used for microwave frequencies; however, constraints in the circuit and layout may be some what different than MMIC technology

Perhaps the primary benefit of GaAs comes from its electron-dynamic properties. In equivalently doped n-type GaAs and silicon, the effective mass of the electric charge carriers in GaAs is far less than that in silicon. This means that the electrons in GaAs are accelerated to higher velocities and therefore transverse the transistor channel in less time. This improvement in electron mobility is the fundamental

property that enables higher frequencies of operation and faster switching speeds [3].

Producing a microwave circuit on a PCB or in MMIC technology has certain advantages and disadvantages. The basic disadvantage of MMIC is the very low flexibility in post-production tuning. Once the MMIC is produced, you can not change or modify a component. Only limited tuning is possible, which brings the ultimate importance of the detailed design. Every and each line segment, corners, connection points, pads, ground vias and cross-talk or coupling between the components must be considered and modeled or simulated. When the design is completed with its layout, EM simulations of suspicious, critical parts are essential. Additional difference in MMIC production is that, different types of the same component are usually limited or not available.

On the other hand, MMIC technology offers many advantages [3]:

(1) Size and weight reduction.
(2) Cost reduction for medium- to large-scale production volumes.
(3) Enhanced system performance from the inclusion of several functions (e.g., RF and logic) on a single circuit.
(4) Enhanced reproducibility from uniform processing and integration of all parts of the circuit.
(5) Enhanced reliability from integration and process-control improvements.
(6) Wider frequency-bandwidth performance from the reduction of parasites in discrete device packaging.
(7) Design performance realized without several iterations—the result of processing and material repeatability, and computer-aided design enhancement.

In addition, it gives the opportunity of symmetric design which is critical for phase and amplitude balance and of low spreads of the different components on the same

chip. Because of these properties, many MMIC digital modulators employing direct vector modulation have been reported during recent years.

2.2 Alternative Models of Vector Modulators

2.2.1 Digital Vector Modulator

The vector modulator is implemented by a direct cascade of three MMIC chips. Digital monolithic vector modulator consists of two and three bit phase shifters followed by a variable gain amplifier. Unlike narrow band approaches separate phase and amplitude functions are typically required for broadband performance with independent control of amplitude and phase [4].

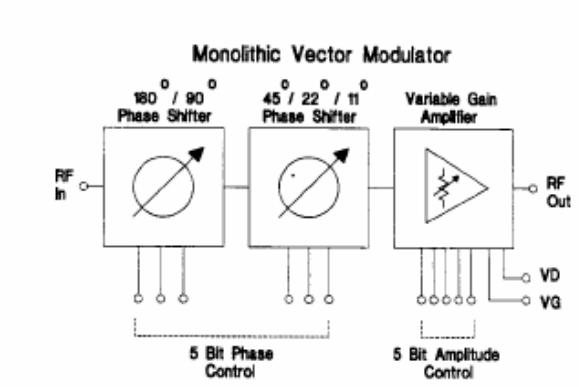

Figure 2.1 Block diagram of the digital vector modulator [4]

The 5 bit phase shifter was designed on two chips one containing 180^0 and 90^0 bits, the other containing the 45^0, 22.5^0 and 11.25^0 bits. The variable gain amplifier is used to control the amplitude of the modulator. The resultant modulator can not cover the full 360^0 range due to digital phase shifters.

2.2.2 Impedance Transformer Technique

The vector modulator is implemented by using impedance transformers and variable gain amplifiers.

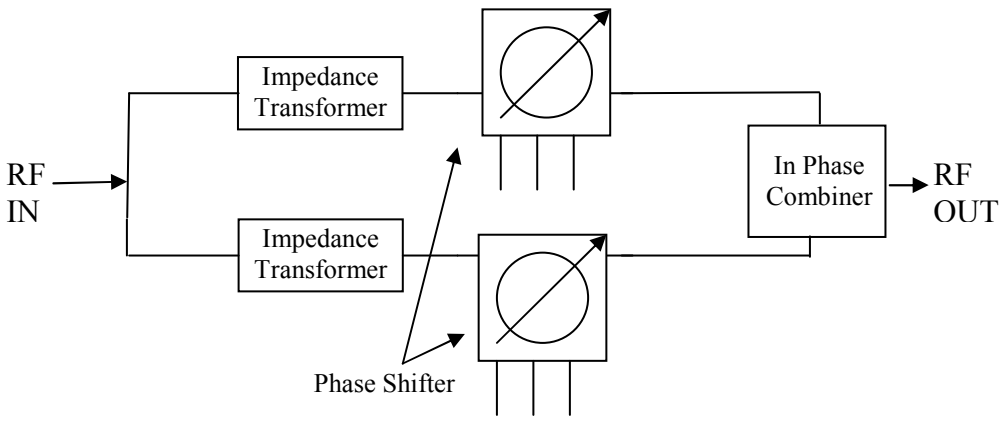

Figure 2.2 Block diagram of the vector modulator using impedance transformer

The impedance transformer is electronically tunable (i.e. it may contain varactor). By the help of this transformer we are able to divide the input signal according to our will [5]. Afterwards we give phase shift to the divided signals by the help of phase shifters and then we combine the signal with an in phase combiner. Like the digital vector modulator case, the resultant modulator can not cover the full 360^0 range due to digital phase shifters.

2.2.3 Analog Phase Shifter and Gain Circuit

As shown in figure 4, the chosen structure consists of a MESFET with a series resonant impedance Z_2 between drain and gate of the transistor and a series resonant impedance Z_1 at the input of the circuit. Each resonant impedance circuit includes a single varactor diode used as a voltage controlled element for the phase shift tuning [6].

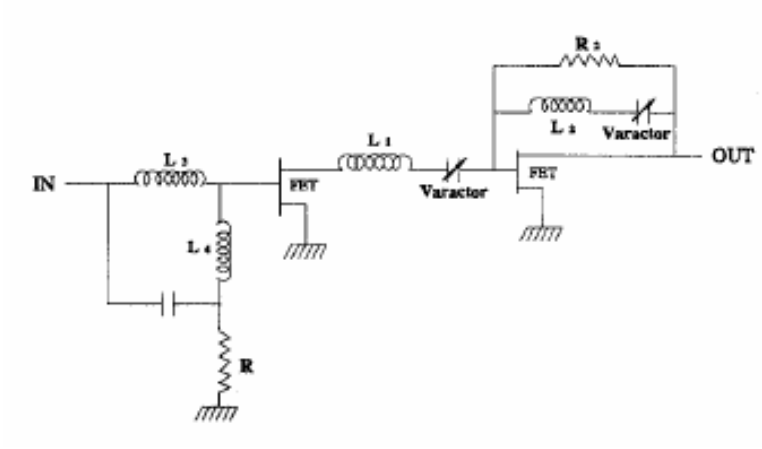

Figure 2.3 Amplifier/Phase shifter structure [6]

The feedback loop between the drain and gate of the transistor is used to control the gain of the circuit and an amplifier is cascaded with the phase shifter compensate for its losses.

By this structure, only a flat phase shift of 75^0 can be obtained. Since we can not cover the full 360^0 range, this structure is not suitable for our case.

2.2.4 Vector Modulator Using Differential Amplifiers

The four basic vectors (0^0, 90^0, 180^0 and 270^0) are generated by the quadrature power splitter and differential amplifiers. Each pair of vectors (0^0, 180^0) and (90^0, 270^0) is then combined linearly by a double balanced mixer function of the input modulation (I, I') and (Q, Q') respectively. The outputs are then summed to generate any vector, amplitude and phase function of the modulation level [7].

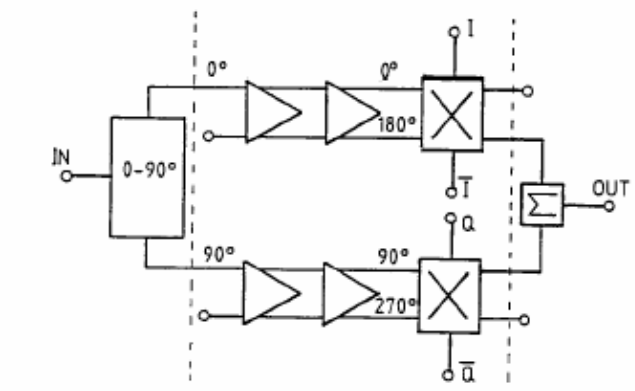

Figure 2.4 Block diagram of the vector modulator [7]

Since the combined signal is summation of two vectors, any amplitude and phase combination can be obtained by giving exact control voltages to the differential amplifier. However, if phase of differential amplifier changes by changing it's gain, the resultant phase changes occur as phase errors at the output, which is not desirable.

2.2.5 Shifted-Quadrant Microwave Vector Modulator

To achieve a good phase and amplitude error at very high frequencies it is often necessary to employ a balanced circuit topology which doubles the number of base band control signals (I, I', Q, Q') and therefore the number of DACs. For high-speed applications the cost of the required DACs is very significant.

However, if one pair of orthogonal channel is generated with variable gain amplifiers (or attenuators) we can solve this problem. This approach creates a single quadrant in the IQ plane, and a third vector is used to shift this quadrant and centre it on the origin. The vector modulator is comprised of several RF components: for the quadrature and in-phase channel, two variable gain amplifiers are used and one auxiliary variable gain amplifier is used to create the fixed quadrant-shifting vector (225^0). The modulator also contains a mechanical phase shifter [1].

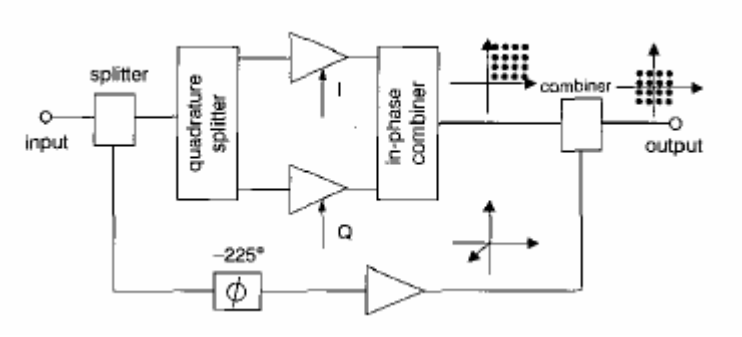

Figure 2.5 Block diagram of shifted-vector modulator [1]

The four channel vector modulator can be reduced to two channels using the "shifted-quadrant" approach. The shifted vector modulator solution needs only simple variable gain amplifiers and has only two variable channels.

2.2.6 I-Q Vector Modulator

A basic vector modulator is shown in figure 7. the first power splitter splits the input signal into two orthogonal components, I and Q. these two vectors are adjusted in amplitude and sense by a pair of modified bi-phase modulators, each one of which comprises a quadrature power splitter and a pair of variable resistance terminations [8].

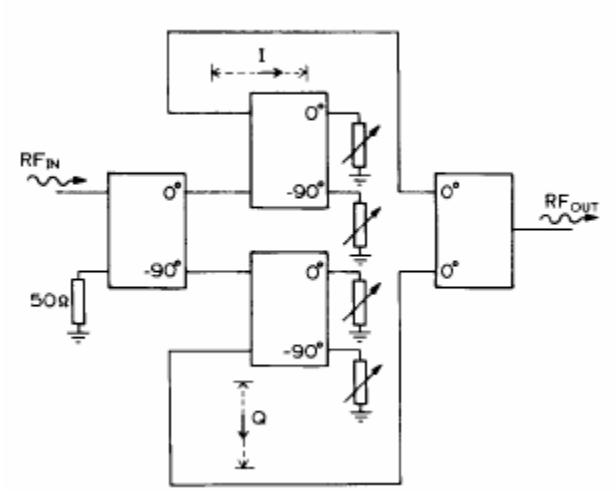

Figure 2.6 I-Q vector modulator [8]

When the terminations of the modulators are at a low resistance, signals are strongly reflected with a phase inversion. When they are high in resistance, signals are strongly reflected with no phase inversion and when the resistances approach to fifty ohms, the reflected signals tend to zero. Combining these two signal components in a simple power combiner completes the modulator function.

Pin-diodes are obvious first choice for the variable resistance elements; however, these are available as discrete devices, they are not generally available in GaAs MMIC. FETs have therefore been used as an alternative and when DC biased with zero drain voltage, they have been shown to be capable of performing the same task.

2.2.7 Vector Modulator-Based Phase Shifter

The majority of the commercial MMIC processes do not feature high quality varactor diodes due to their poor quality factors and capacitance control ranges. However, vector modulator-based phase shifters are well suited for monolithic integration. Their functional principle can be explained as fallows:

The input signal is divided in at least two signals and a phase difference is generated between these signals. Then the amplitudes of these signals are weighted by variable attenuators or variable gain amplifiers. Finally, these signals are combined to obtain a phase-dependent vector sum [9].

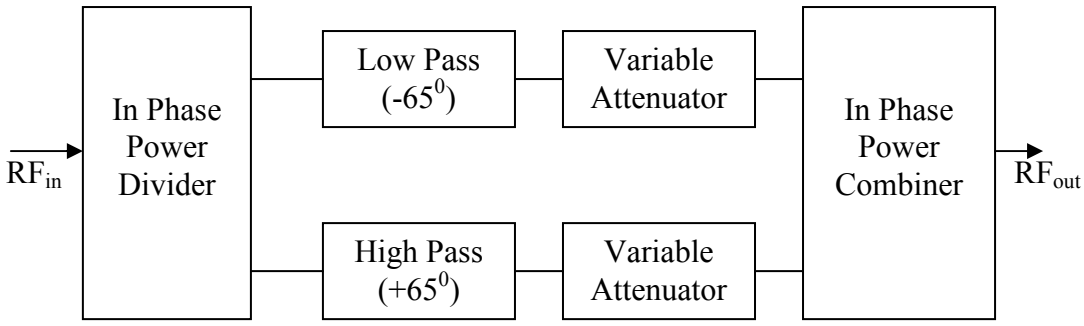

Figure 2.7 Circuit schematics of the vector modulator-based phase shifter

Vector modulator-based phase shifter has a phase control range of 130^0; therefore we have to use three of vector modulator-based phase shifter to cover the full 360^0 range which may cause more phase and amplitude errors.

2.2.8 Basic I-Q Vector Modulator

The operation is as follows: the signal is divided to its in-phase (I) and quadrature phase (Ø) components by means of a quadrature hybrid coupler. Then each component is sent to a biphase modulator followed by an attenuator. Since biphase modulator produces two signals which are exactly out of phase and quadrature coupler produces two signals which are 0° and 90° respectively, at the output of biphase modulator there are four signals which have the phases 0°, 90°, 180° and 270° respectively. Then the attenuator/variable gain amplifier gives the desired attenuation level [10]. By means of this attenuator, one can obtain every vector in a signal constellation diagram. A basic block diagram is shown below:

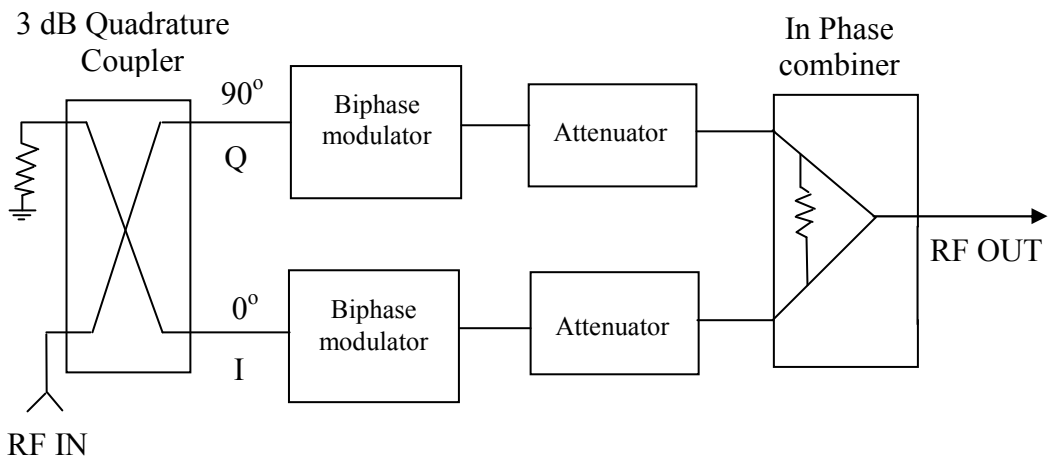

Figure 2.8 Block diagram of Basic I-Q Vector Modulator [10]

2.2.9 Analog Monolithic Vector Modulator

It consists of two artificial transmission lines that are connected by four cascade MESFETs. The MESFETs provide independently controllable amplitude vectors that are separated by 90 degrees. Different attenuation and phase levels are

produced by controlling the amplitude of two quadrature vectors. This vector modulator includes balancing resistors for flat phase variation versus frequency.

The operation is as fallows: the input signal is split off the low pass input filter via cascade connected MESFETs to the high pass output filter. The MESFETs are used as variable gain amplifiers. The LP and HP filters in combination with these MESFETs produce four orthogonal vectors: 0, 90, 180 and 270 degrees. By turning on only two vectors, a signal is produced that is a vector sum. If the amplitude of one of these vectors is varied while the other is constant, then the resultant sum vector will have a different phase. By using only two of the four vectors at a time, the phase can varied from 0 to 360 degrees. Amplitude can also be changed by varying both vectors at the same time [11].

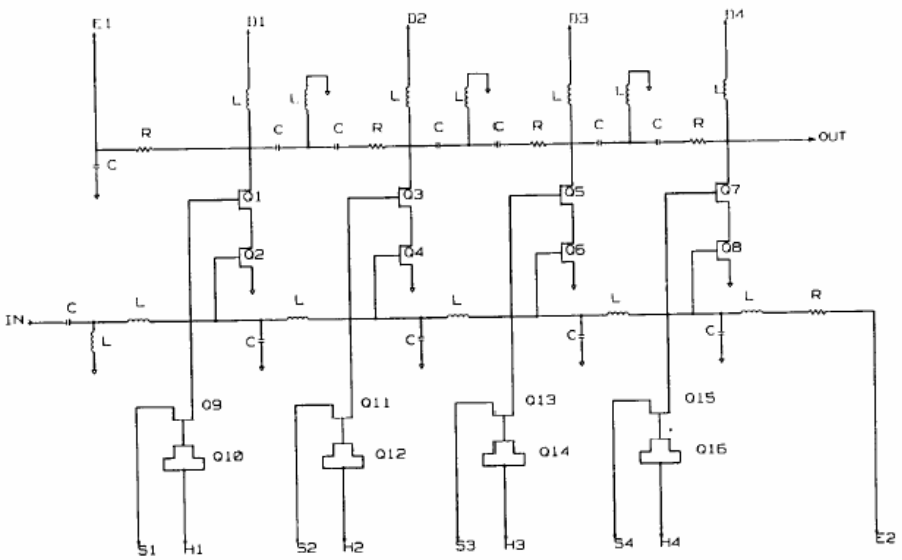

Figure 2.9 Circuit schematics [11]

2.2.10 MMIC Vector Modulator with Summation of Three Vectors

A full 360 degrees phase range is generated by combining two of three vectors which have variable amplitude and 120 degrees apart. When the gain of the amplifier changes the phase of the S_{21} must not change in order to eliminate the phase errors at the output.

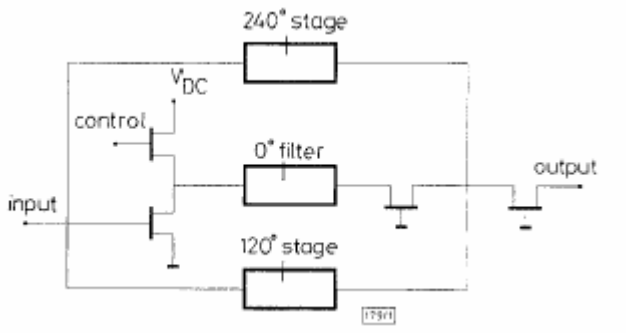

Figure 2.10 Block Diagram of the Vector Modulator [2]

The schematic diagram of one of the three paths is displayed in figure 11. The operation of the whole circuit consists of combining two vectors to obtain any amplitude and phase in the corresponding 120 degrees sector while the third vector is in the off state [2].

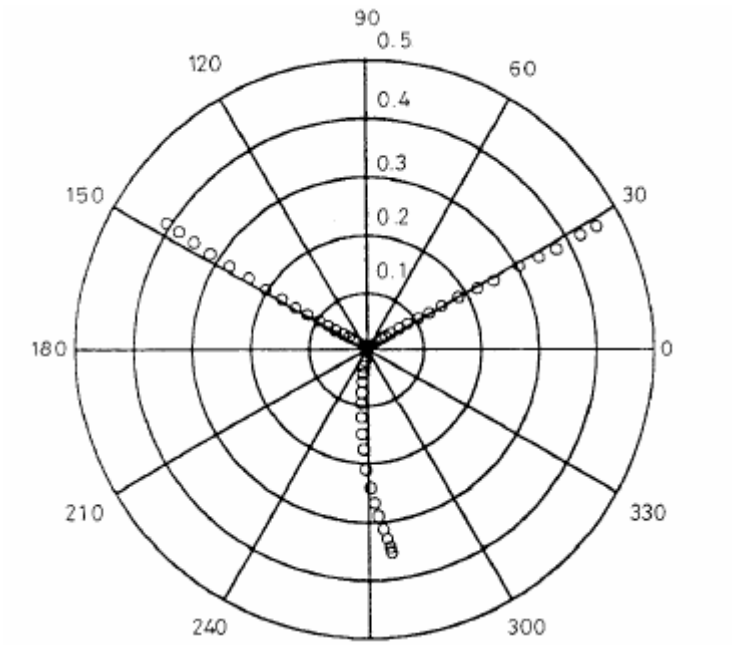

Figure 2.11 Phase of each channel [2]

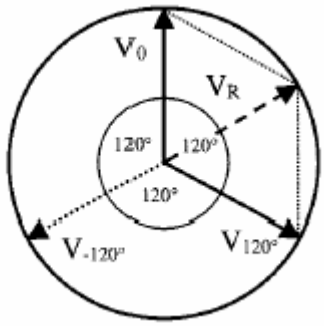

Figure 2.12 Vector addition every phase with amplitude V_R can be obtained by weighting two of the vectors V_0, V_{120}, and V_{-120}. [12]

The three input stages act as an active three way power splitter, isolating three paths. The 120 degrees shifted vectors are achieved through LC filters. Two of them are all pass filters that generate the 0^0 and 240^0 vectors and the third one is a band pass filter which generates a vector 120^0 shifted with respect to the others. This approach allows a broadband design. The three output stages act as a three way power combiner, adding the three vectors and isolating the three paths. The input signals are fed through the gates of the FETs and the signals are added by connecting the drains together. The inputs and outputs are reactively matched to fifty ohm. The gates are biased by resistors, which improve stability and make the circuit broadband. The drains are biased by an inductor.

Among all these types of vector modulators and phase shifters; if we want to cover the full 360 degrees range the best solution is seemed to be the MMIC vector modulator with summation of three vectors; due to its simplicity of realization, wide-band operation and also it seems to have less phase and amplitude errors at the output.

The purpose of this thesis is to design a vector modulator to be operated in the 9-10 GHz band. The basic topology is shown in the Figure 2.13. Since the frequency of operation is high, we constructed the building blocks using lumped elements (they will be also realized with Caswell H-40 linear components) and transistors (Caswell H-40 non-linear model) in MMIC technology.

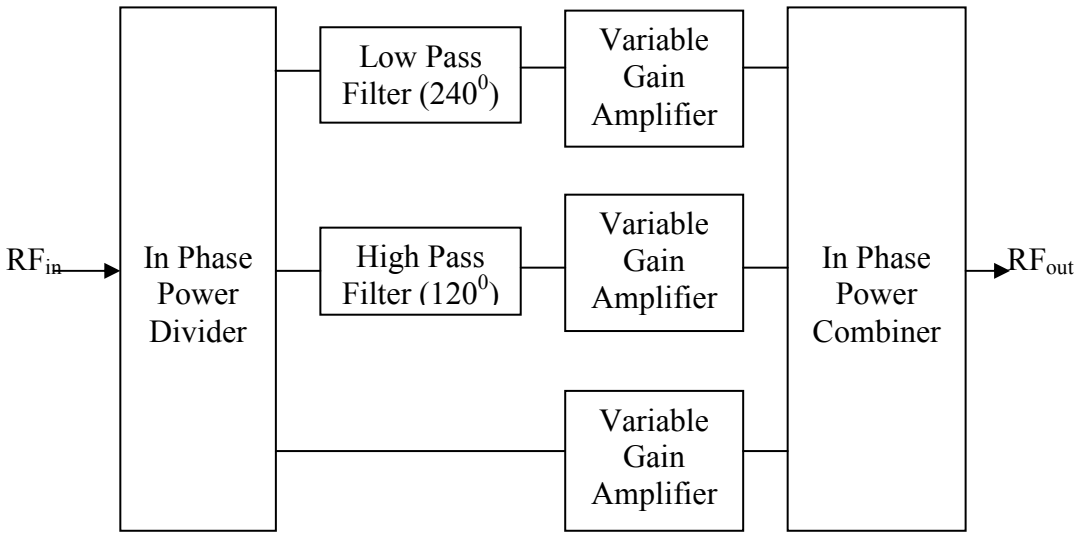

Figure 2.13 Vector modulator topology

CHAPTER 3

4-PORT 120^0 PHASE SHIFT RELATIVE TO THE DEDICATED PORT POWER SPLITTER

3.1 Introduction:

The first part of the vector modulator structure is the 4-port (4.8dB) power splitter and the phase shifting sections. The main purpose of the power splitter section is to divide the input signals into 3 equal phase and equal amplitude signals. We will use lumped elements method for these parts in order to achieve MMIC approach.

For the power splitter part, we will use impedance transformer technique and for the phase shifting parts we will use low pass and high pass filters. Since the frequency is high, we will have the lumped elements of lower value which is quite good for MMIC approach.

Figure 3.1 shows the 4-port power splitter structure using the high-pass and low-pass sections used on the first and the second channel to obtain 120^0 and 240^0 phase differences relative to the third channel which does not have a filter section. Since the filter sections on each channel are in the 50 Ω system and we have to see 50 Ω from the input; we have to use either a modified Wilkinson power divider at the input before the filter sections, or we have to implement three impedance transformers as seen below:

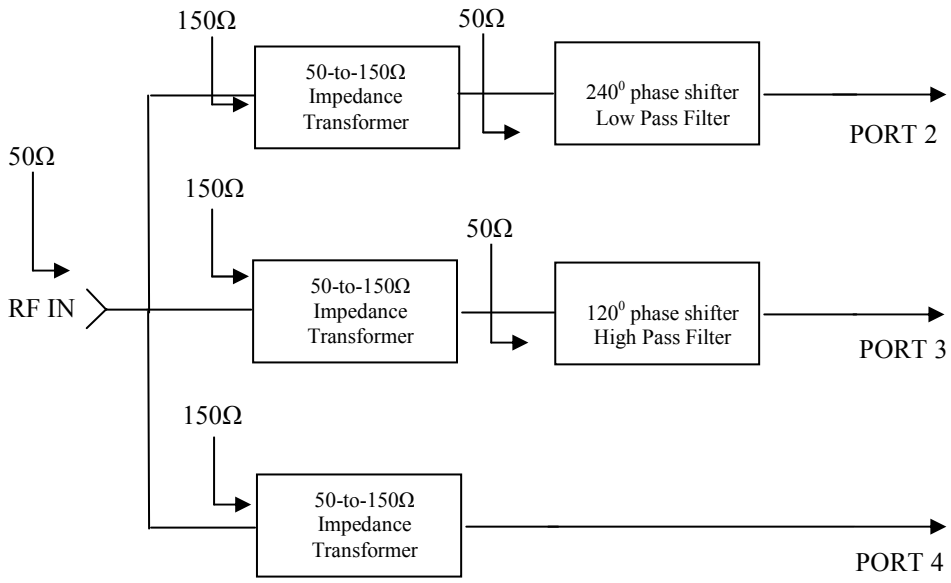

Figure 3.1 4-port Power Splitter with 50-to-150Ω impedance transformers

Now we have to design an impedance transformer which transforms 50Ω at its output to 150Ω at the input ports. The transformer will be in a low-pass filter structure. The required equations to realize the impedance transformer is given below:

$$\omega L = \frac{1}{\omega C} \quad ; \qquad \omega = 2\pi \times 9.5 \times 10^{9} = 5.969 \times 10^{10} \tag{3.1}$$

$$\frac{L}{C} = 50 \times 150 \qquad [10] \tag{3.2}$$

The solution of the equations using the center frequency of 9500 MHz gives the following results:

$$\Rightarrow L \cong 1.4505 \text{ nH} \tag{3.3}$$

$$\Rightarrow C \cong 0.1934 \text{ pF} \tag{3.4}$$

We will realize the phase shifting sections by a structure other than distributed elements due to the very large quarter wave-length sections for MMIC application. The high-pass and low-pass type of phase shifter circuits are the most appropriate circuits for MMIC realization [13]. Therefore we will use these kinds of circuits shown below. And as mentioned before, by using the MMIC approach, the circuit is considerably small enough which is very important for some approaches, like feeding sections of phase arrays.

We have to give a phase delay of 120^0 and phase advance of 120^0 relative to the third channel. Therefore, we will use low-pass and high-pass filter sections.

3.2 Low-pass Phase Shifters:

Figure 3.2 (a)Π-type Low-pass (b)T-type Low-pass

It is obvious from the figure that when the input RF signal passes through the low-pass filter section this signal undergoes a phase delay.

In the above figure, the analysis of the circuits can be carried out using the ABCD matrices of cascaded series and shunt elements. For any reciprocal symmetric passive network, the transmission coefficient S_{21} and the reflection coefficient S_{11} can be obtained in terms of its ABCD parameters as follows:

$$S_{21} = \frac{2}{A + \frac{B}{Z_O} + CZ_O + D} = S_{12} \tag{3.5}$$

$$S_{11} = \frac{\frac{B}{Z_O} - CZ_O}{A + \frac{B}{Z_O} + CZ_O + D} = S_{22} \tag{3.6}$$

For the T-type circuit shown in Fig.3.2(b); the transmission coefficient S_{21} is found as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & jX \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jB & 1 \end{bmatrix} \begin{bmatrix} 1 & jX \\ 0 & 1 \end{bmatrix} \tag{3.7}$$

$$= \begin{bmatrix} (1 - \overline{B}\overline{X}) & jX(2 - \overline{B}\overline{X}) \\ jB & (1 - \overline{B}\overline{X}) \end{bmatrix} \tag{3.8}$$

Using equations 3.1 and 3.4:

$$S_{21}{}^{(1)} = \frac{2}{2(1 - \overline{B}\overline{X}) + j(\overline{B} + 2\overline{X} - \overline{B}\overline{X}^2)} \tag{3.9}$$

Here, $\overline{B}$ is the normalized susceptance and $\overline{X}$ is the normalized reactance given by:

$$\overline{B} = BZ_O = \frac{B}{Y_O}$$

$$\overline{X} = XY_O = \frac{X}{Z_O} \tag{3.10}$$

And note that $\overline{B} \times \overline{X} = B \times X$ (3.11)

From the above equations, the transmission phase is given by:

$$\phi = \arctan\left[-\frac{(\overline{B} + 2\overline{X} - \overline{B}\overline{X}^2)}{2(1 - \overline{B}\overline{X})} \right] \tag{3.12}$$

At this stage, we have to impose another condition on the filter structure. Assuming the phase shifter to be lossless and it is perfectly matched, it turns out that the magnitude of S_{21} is unity. Therefore:

$$S_{21}^{(1)} = \frac{2}{2(1 - \overline{B}\overline{X}) - j(\overline{B} + 2\overline{X} - \overline{B}\overline{X}^2)} = 1$$

$$4 \quad = 4(1 - \overline{B}\overline{X})^2 + \left\langle \overline{B}(1 - \overline{X}^2) + 2\overline{X} \right\rangle^2$$

$$4 \quad = 4 - 8\overline{B}\overline{X} + 4\overline{B}^2\overline{X}^2 + \overline{B}^2(1 - \overline{X}^2)^2 + 4\overline{B}\overline{X}(1 - \overline{X}^2) + 4\overline{X}^2$$

$$0 = -8\overline{B}\overline{X} + 4\overline{B}\overline{X} - 4\overline{B}\overline{X}^3 + 4\overline{X}^2 + 4\overline{B}^2\overline{X}^2 + \overline{B}^2 - 2\overline{B}^2\overline{X}^2 + \overline{B}^2\overline{X}^4$$

$$\overline{B}^2(\overline{X}^4 + 2\overline{X}^2 + 1) - 4\overline{B}\overline{X}(\overline{X}^2 + 1) + 4\overline{X}^2 = 0$$

$$\left\langle \overline{B}(1 + \overline{X}^2) \right\rangle^2 - 4\overline{B}\overline{X}(\overline{X}^2 + 1) + 4\overline{X}^2 = 0$$

$$\left\langle \overline{B}(1 + \overline{X}^2) - 2\overline{X} \right\rangle^2 = 0$$

$$\overline{B} = \frac{2\overline{X}}{\overline{X}^2 + 1} \tag{3.13}$$

Using equation 3.13 in overall phase difference formula (Equation 3.12):

$$\phi = \arctan\left[-\frac{\left(\frac{2\overline{X}}{\overline{X}^2+1} + 2\overline{X} - \frac{2\overline{X}}{\overline{X}^2+1}\overline{X}^2\right)}{2\left(1 - \frac{2\overline{X}}{\overline{X}^2+1}\overline{X}\right)} \right]$$

$$\Delta\phi = \arctan\left[-\frac{2\overline{X}}{\overline{X}^2 - 1} \right] \tag{3.14}$$

From the above equations, the normalized susceptance and reactance values required for a given phase difference is found to be:

$$\overline{X} = \tan\left(-\frac{\Delta\phi}{2}\right) \tag{3.15}$$

$$\overline{B} = \frac{2\tan\left(-\frac{\Delta\phi}{2}\right)}{\tan^2\left(-\frac{\Delta\phi}{2}\right)+1} = \frac{-2\sin\left(\frac{\Delta\phi}{2}\right)\cos\left(\frac{\Delta\phi}{2}\right)}{\cos^2\left(-\frac{\Delta\phi}{2}\right)+\sin^2\left(-\frac{\Delta\phi}{2}\right)} = -\sin(\Delta\phi)$$

$$\Rightarrow \overline{B} = -\sin(\Delta\phi) \tag{3.16}$$

Phase delay of 120^0:

$$\Delta\phi = 240^0 \Rightarrow \overline{X} = \tan\left(-\frac{240}{2}\right) = -\tan(120) \cong 1.732050807; \tag{3.17}$$

$$\Rightarrow \overline{B} = -\sin(240) \cong 0.8660254 \tag{3.18}$$

$$B = \frac{\overline{B}}{Z_O}; \quad X = \overline{X}Z_O \tag{3.19}$$

Also we know that:

X=wL and B=wC (3.20)

$$\Rightarrow L = \frac{X}{\omega}; \quad C = \frac{B}{\omega}$$

$$L = \frac{\overline{X} Z_O}{\omega}; \quad C = \frac{\overline{B}}{\omega Z_O}; \qquad \text{for low-pass filter} \tag{3.21}$$

Our characteristic impedance Z_0 is 50Ω and the center frequency of operation is 9500 MHz ($\omega = 2\pi \times 9.5 \times 10^9 = 5.969 \times 10^{10}$). Therefore we can obtain L and C values from the $\overline{B}$ and $\overline{X}$ values by the help of Eq.3.21 and 3.19.

$\Rightarrow$ L≅1.45086 nH (3.22)

$\Rightarrow$ C≅0.29017 pF (3.23)

3.3 High-pass Phase Shifters:

Figure 3.3 (a)Π-type High-pass (b)T-type High-pass sections

It is obvious from the figure that when the input RF signal passes through the low-pass filter section this signal undergoes a phase advance.

In the above figure, the analysis of the circuits can be again carried out using the ABCD matrices of cascaded series and shunt elements. For any reciprocal symmetric passive network, the transmission coefficient S_{21} and the reflection coefficient S_{11} can be obtained in terms of its ABCD parameters as follows:

$$S_{21} = \frac{2}{A + \frac{B}{Z_O} + CZ_O + D} = S_{12} \tag{3.24}$$

$$S_{11} = \frac{\frac{B}{Z_O} - CZ_O}{A + \frac{B}{Z_O} + CZ_O + D} = S_{22} \tag{3.25}$$

For the T-type circuit shown in Fig.3.3(b); the transmission coefficient S_{21} is found as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & -jX \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ -jB & 1 \end{bmatrix} \begin{bmatrix} 1 & -jX \\ 0 & 1 \end{bmatrix} \tag{3.26}$$

$$= \begin{bmatrix} (1 - \overline{B}\overline{X}) & -jX(2 - \overline{B}\overline{X}) \\ -jB & (1 - \overline{B}\overline{X}) \end{bmatrix} \tag{3.27}$$

Using equations 3.13 and 3.16:

$$S_{21}{}^{(1)} = \frac{2}{2(1 - \overline{B}\overline{X}) - j(\overline{B} + 2\overline{X} - \overline{B}\overline{X}^2)} \tag{3.28}$$

Here, $\overline{B}$ is the normalized susceptance and $\overline{X}$ is the normalized reactance given by:

$$\overline{B} = BZ_O = \frac{B}{Y_O}$$

$$\overline{X} = XY_O = \frac{X}{Z_O} \tag{3.29}$$

And note that $\overline{B} \times \overline{X} = B \times X$ (3.30)

From the above equations, the transmission phase is given by:

$$\phi = \arctan\left[\frac{(\overline{B} + 2\overline{X} - \overline{B}\overline{X}^2)}{2(1 - \overline{B}\overline{X})}\right] \tag{3.31}$$

At this stage, we have to impose another condition on the filter structure. Assuming the phase shifter to be lossless and it is perfectly matched, it turns out that the magnitude of S_{21} is unity. Therefore:

$$S_{21}^{(1)} = \frac{2}{2(1 - \overline{B}\overline{X}) - j(\overline{B} + 2\overline{X} - \overline{B}\overline{X}^2)} = 1$$

If we carry out the same operations, we find $\overline{B}$ same as low-pass case:

$$\overline{B} = \frac{2\overline{X}}{\overline{X}^2 + 1} \tag{3.32}$$

Using equation 3.32 in overall phase difference formula (Equation 3.31):

$$\phi = \arctan\left[\frac{(\frac{2\overline{X}}{\overline{X}^2 + 1} + 2\overline{X} - \frac{2\overline{X}}{\overline{X}^2 + 1}\overline{X}^2)}{2(1 - \frac{2\overline{X}}{\overline{X}^2 + 1}\overline{X})}\right]$$

$$\Delta\phi = \arctan\left[\frac{2\overline{X}}{\overline{X}^2 - 1}\right] \tag{3.33}$$

From the above equations, the normalized susceptance and reactance values required for a given phase difference is found to be:

$$\overline{X} = \tan\left(\frac{\Delta\phi}{2}\right) \tag{3.34}$$

$$\overline{B} = \frac{2\tan\left(\frac{\Delta\phi}{2}\right)}{\tan^2\left(\frac{\Delta\phi}{2}\right)+1} = \frac{2\sin\left(\frac{\Delta\phi}{2}\right)\cos\left(\frac{\Delta\phi}{2}\right)}{\cos^2\left(-\frac{\Delta\phi}{2}\right)+\sin^2\left(-\frac{\Delta\phi}{2}\right)} = \sin(\Delta\phi)$$

$$\Rightarrow \overline{B} = \sin(\Delta\phi) \tag{3.35}$$

Phase advance of 120^0:

$$\Delta\phi = 120^0 \Rightarrow \overline{X} = \tan\left(\frac{120}{2}\right) = \tan(60) \cong 1.732050807; \tag{3.36}$$

$$\Rightarrow \overline{B} = \sin(120) \cong 0.8660254 \tag{3.37}$$

$$B = \frac{\overline{B}}{Z_O}; \quad X = \overline{X}Z_O \tag{3.38}$$

$$B = \frac{1}{\omega L}; \quad X = \frac{1}{\omega C}$$

$$\Rightarrow L = \frac{1}{\omega B}; \quad C = \frac{1}{\omega X}$$

$$L = \frac{Z_O}{\omega \overline{B}}; \quad C = \frac{1}{\omega \overline{X} Z_O} \text{; for high-pass filter} \tag{3.39}$$

Our characteristic impedance Z_0 is 50Ω and the center frequency of operation is 9500 MHz ($\omega = 2\pi \times 9.5 \times 10^9 = 5.969 \times 10^{10}$). Therefore we can obtain L and C values from the $\overline{B}$ and $\overline{X}$ values by the help of Eq.3.38 and 3.39.

$$\Rightarrow L \cong 0.96724 \text{ nH} \tag{3.40}$$

$$\Rightarrow C \cong 0.19345 \text{ pF} \tag{3.41}$$

The equations similar to the above ones can also be derived for the ∏-type phase shifters. However we used T-type phase shifting sections from in our design.

Figure 3.4 Low-pass and High-pass T-type filter section

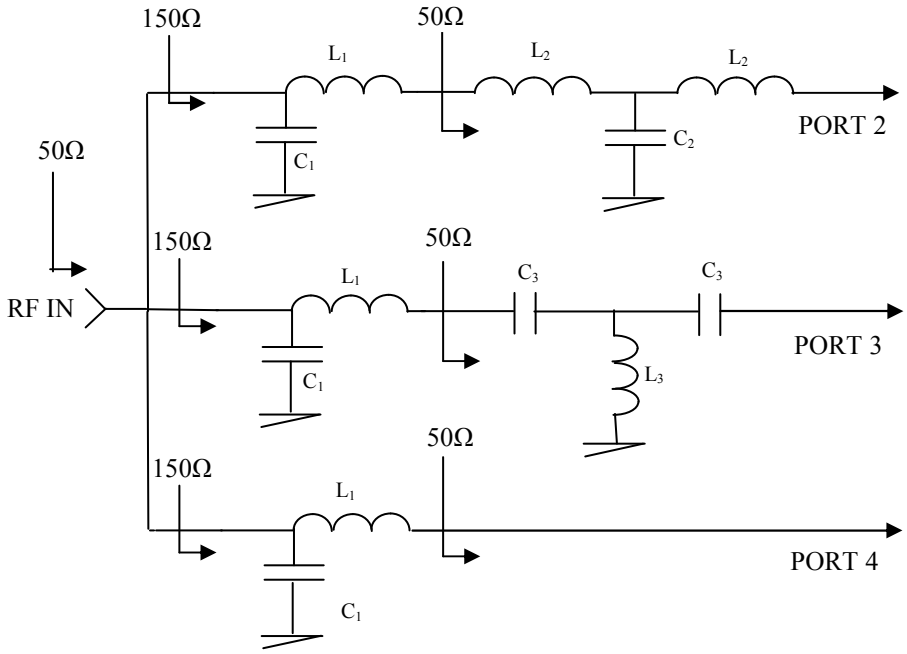

Figure 3.5 The final design of the 4-port 120^0 Phase Shift Relative to the Dedicated Port Power Splitter

Table 3.1: Element values obtained for the ideal circuit

Element	Element Value
L_1	1.451 nH
C_1	0.193 pF
L_2	1.451 nH
C_2	0.290 pF
L_3	0.967 nH
C_3	0.193 pF

3.4 Simulation Results

Simulations and the optimizations of the circuit were done by the ADS (Advanced Design System) simulation and optimization software. Firstly, the entire sub

circuits (impedance transformer, low-pass and high pass filters) are designed. After that, the final circuit is constituted.

However, the performance was not good enough. Therefore, optimization was needed. It was seen that optimization could not improve the performance to the expected values, because of this, the impedance transformer's structure was changed to high-pass type and it was made forth order.

The below simulation performances are the optimization results of Advanced Design System program. All the elements of the 4-port, 4.8 dB, 120^0 Phase Shift Relative to the Dedicated Port Power Splitter were given different names and put into the optimization in order to achieve the best performance.

The following figures represent the optimization results of the final structure with optimized element values:

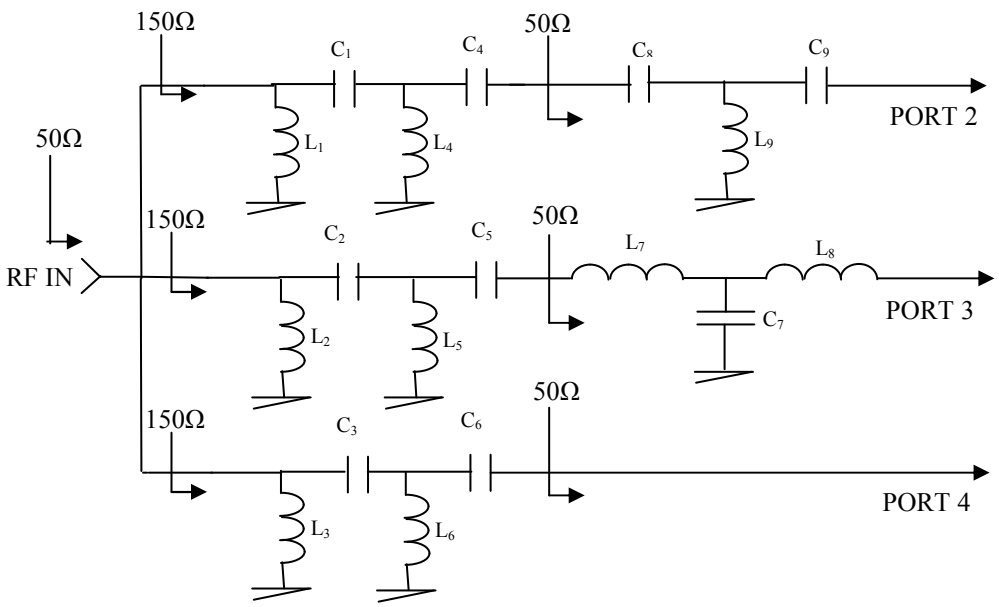

Figure 3.6 4-port 4.8 dB 120^0 Phase Shift Relative to the Dedicated Port Power Splitter with optimized elements

Table 3.2 Element values obtained for the final circuit

Element	Element Value
L_1	4.000 nH
C_1	0.192 pF
L_2	4.000 nH
C_2	0.281 pF
L_3	4.000 nH
C_3	0.177 pF
L_4	1.099 nH
C_4	0.351 pF
L_5	2.356 nH
C_5	0.209 pF
L_6	1.029 nH
C_6	0.420 pF
L_7	1.288 nH
C_7	0.284 pF
L_8	0.780 nH
C_8	0.164 pF
L_9	0.850 nH
C_9	0.175 pF

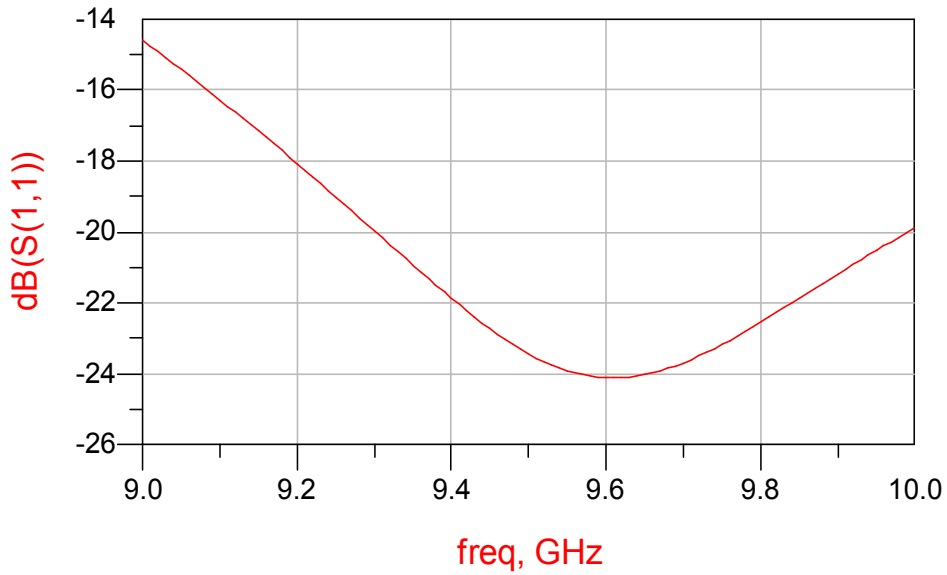

Figure 3.7 Input return loss characteristics of the final circuit

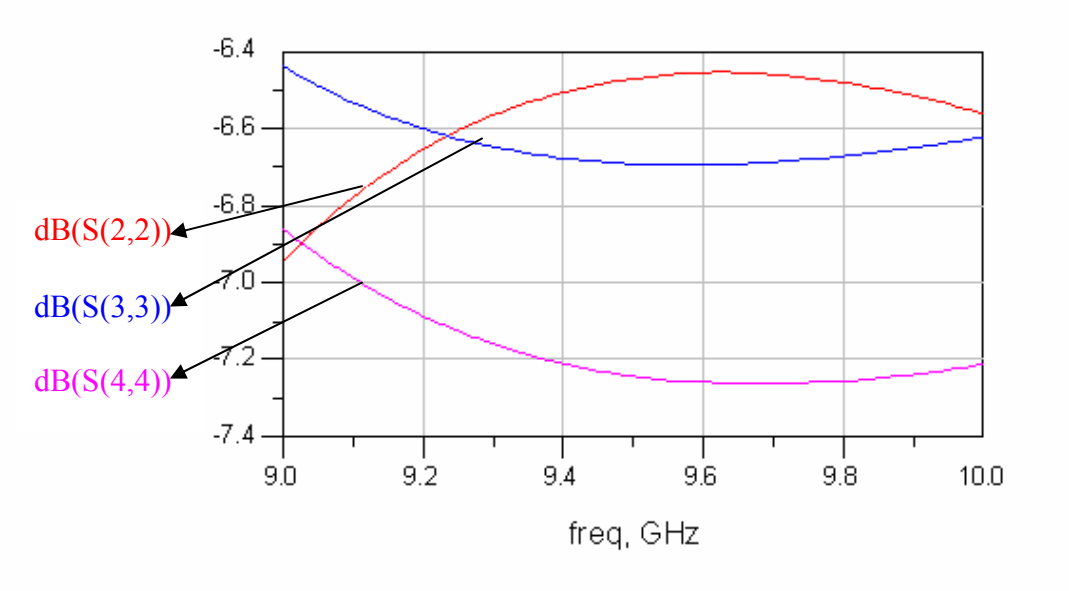

Figure 3.8 Output return loss characteristics of the final circuit

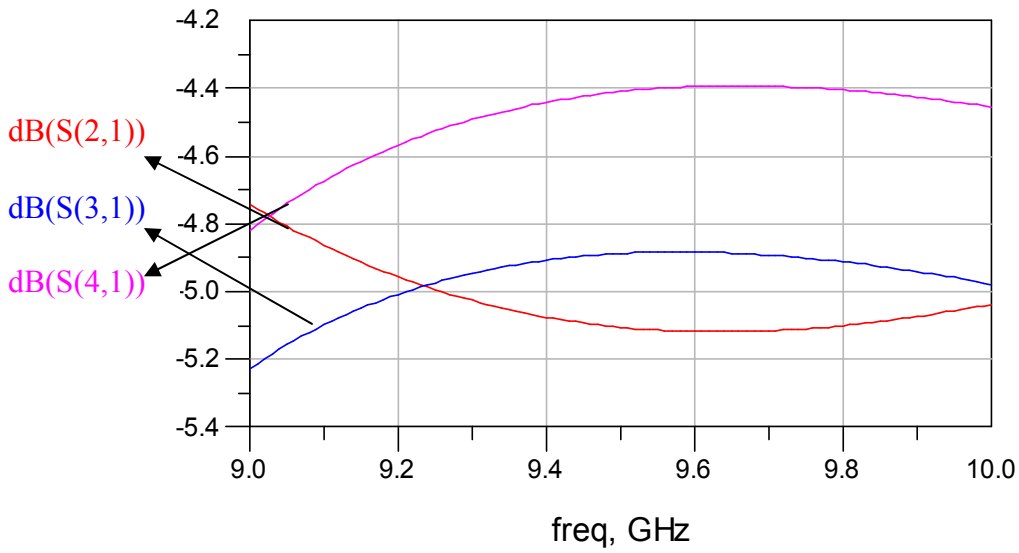

Figure 3.9 Magnitude of S_{21}, S_{31} and S_{41} of the final circuit

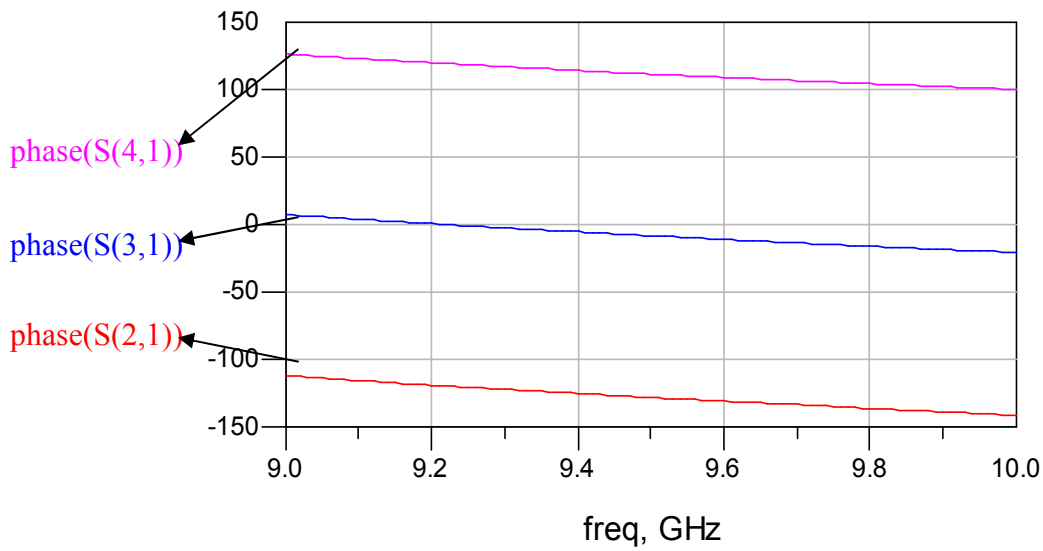

Figure 3.10 Phase of S_{21}, S_{31} and S_{31} of the final circuit.

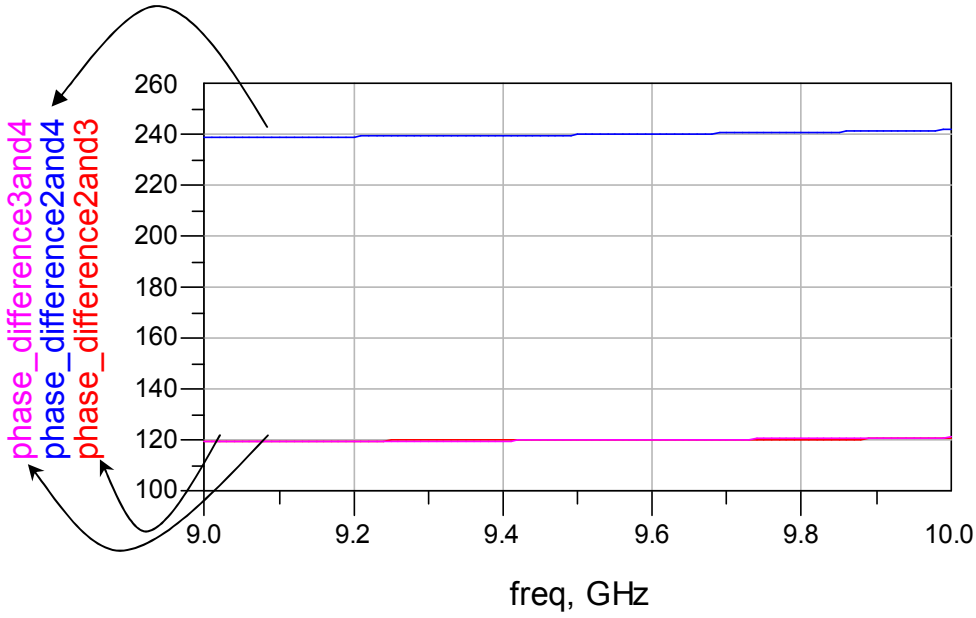

Figure 3.11 Differential phase shift between the output ports of the final circuit

CHAPTER 4

VARIABLE GAIN AMPLIFIER

4.1 Introduction

The next section in the vector modulator structure is the variable gain amplifier. By the help of 4-port 120^0 phase shift relative to the dedicated port power splitter, we made a phase shift in every channel. However, we still did not change the amplitude of the channels. The main purpose of this section is to change the amplitude of each channel.

The amplifier to be used in our vector modulator is in a completely digitally controlled MMIC structure. The alternative of the variable gain amplifier is the variable attenuator.

4.2 Basic Attenuator Topologies:

An attenuator is a network that reduces the input power by predetermined ratio when working between resistive impedances Z_{in} and Z_{out}, which the input and output impedances of the attenuator are matched. In our system, the input and output impedances will be equal to 50Ω [10].

There are two major categories of attenuators: Fixed and variable. Fixed attenuators are those whose attenuation is factory preset at some nominal level. It is a fixed value and cannot be changed. Variable attenuators, on the other hand,

can be controlled by the user to vary the attenuation level of the device. This can be done by a number of different methods.

Mechanically variable attenuators are normally adjusted through the use of a tuning screw or knob adjustment. Electronically variable attenuators respond to the application of either current (current-controlled) or voltage (voltage-controlled) to the device. Mechanically variable attenuators, due to the necessity of mechanical adjustment are generally not suited to system requirements. Electronic attenuators are more applicable to these applications and are used in many systems, test and lab situations.

There are basically two types of resistive electronically controlled networks that can be used as microwave attenuators. These are namely the T and π attenuator structures. The following figures represent these three types of attenuators [14]:

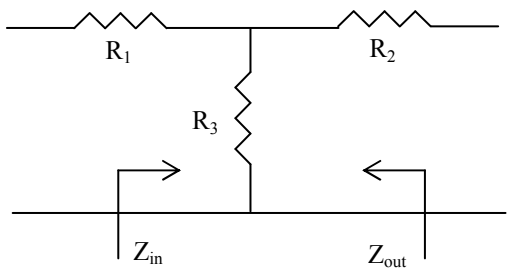

Figure 4.1 T-type attenuator network configuration with resistances

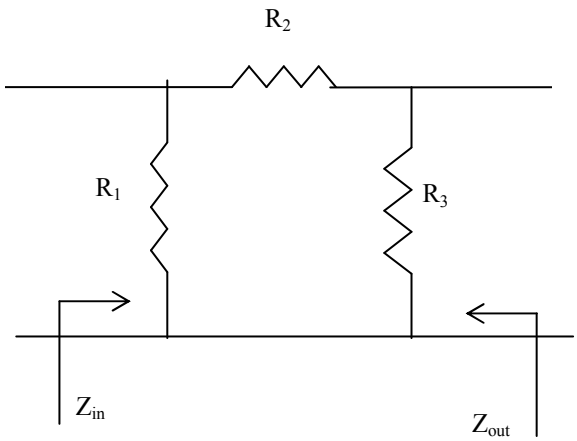

Figure 4.2 π -type attenuator network configuration with resistances

The network configurations above are the basic attenuator topologies. If the resistance values could be varied, then the attenuation value would be variable accordingly; and we would obtain a variable attenuator. In fact, there are variable resistors to implement such a structure. Variable resistors are three-terminal devices where the resistance between two terminals is controlled by a voltage or current applied to the third terminal.

The broadest frequency coverage available is obtained with some form of T-type or π-type attenuator. These are lumped element circuits which function in the microwave frequency range in essentially the same manner as they do at DC.

Although designing a variable attenuator is much more easier than designing a variable gain amplifier, we will use variable gain amplifier in our design. Because variable attenuators are lossy structures. In order to change the amplitude of a channel we have to attenuate the RF signal in that channel. If we want small losses and lower Noise Figure in our vector modulator, we have to use variable gain amplifier. Furthermore, variable gain amplifiers are much more compatible to MMIC applications.

4.3 Basic Variable Gain Amplifier Topologies:

Variable gain amplifiers are used in communication systems in order to control the incoming power level of the received signals. In many systems the received signal varies greatly in amplitude. This requires a variable gain amplifier with wide gain control range and bandwidth capability. Important characteristics of variable gain amplifiers are bandwidth, noise and distortion performance (dynamic range), temperature and supply independence and the form of the gain control characteristics [15].

In our design, variable gain amplifier will change the amplitude of each channel in order to achieve an amplitude shift in each channel. Therefore, it must have an at least 10-15dB dynamic range.

There are basically three types of variable gain amplifiers. These are: Analog emitter-coupled current steering topology, variable resistance feedback amplifier and the variable transconductance amplifier.

4.1.1 Variable Gain Amplifier with Current Steering

In many cases, the gain control is realized by a current-steering pair built of bipolar transistors. Current steering technique is usually designed in an emitter-coupled transistor network where cascade differential stages are used in the loads of a differential amplifier in order to steer current to and from the load resistor (Figure 4.3) [16].

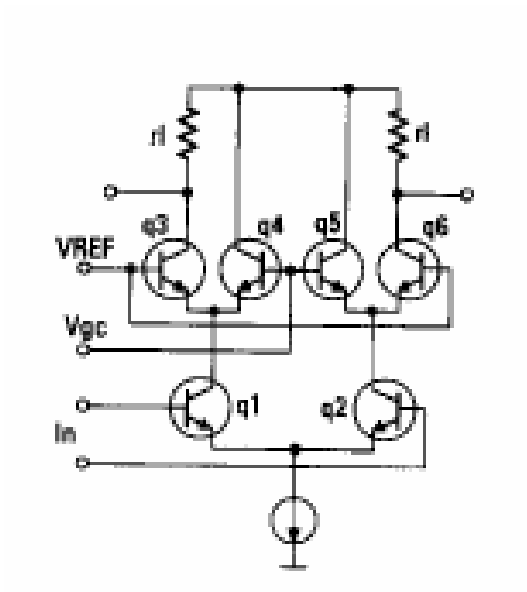

Figure 4.3 Variable gain amplifier with current steering [16]

Gain control is achieved by varying the current through the load resistors which varies the amplitude at the output. The advantage of this approach is that it can achieve high dynamic range. However, due to differential emitter-coupled transistors, its noise figure is high.

4.1.2 Variable Gain Amplifier with Variable Feedback Resistance

The second approach achieves gain control by an electronically variable resistance in the series or parallel feedback path of a common-emitter amplifier.

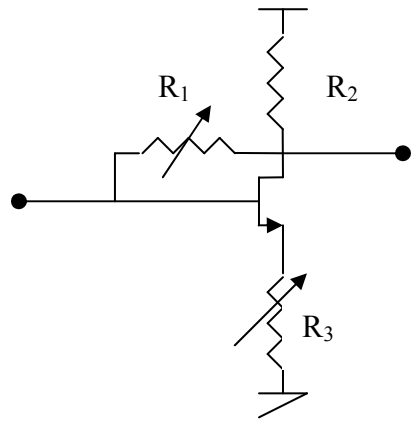

Figure 4.4 Variable gain amplifier with variable feedback resistance

The variable resistance can be realized by a PIN diode or a FET device and is usually integrated as discrete components in a Microwave Integrated Circuit (MIC) hybrid. The advantages of this topology are the potential for high IP3 and low DC power consumption. The disadvantages are stability problems in the design; limitations on bandwidth and gain control range and noise figure sensitivity over the gain control range [16].

4.1.3 Variable Gain Amplifier with Variable Transconductance

The third approach is based on the bias dependent characteristics of the transistor's transconductance [16]. Variable gain amplifiers utilize the V_g or V_{dd} dependence of transconductance. The variable gain is realized by controlling the quiescent current of the transistor to change the g_m. In our design V_g will be variable and V_{dd} will be kept constant.

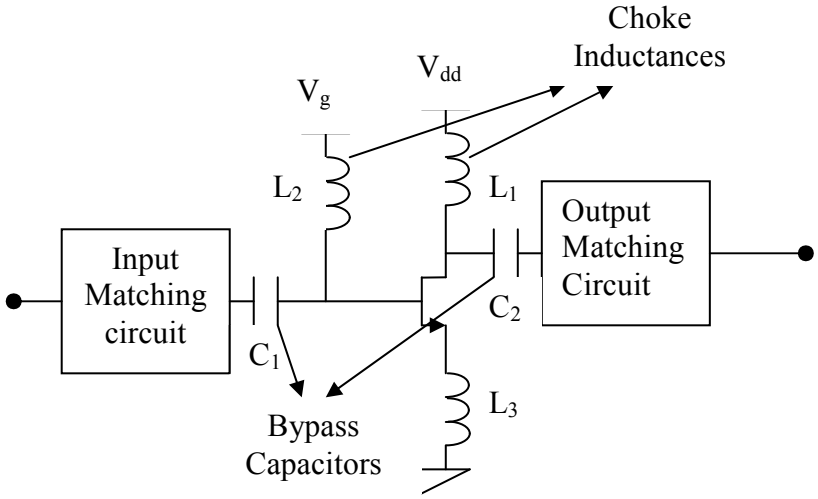

Figure 4.5 Variable gain amplifier with variable transconductance

The advantages of this topology are low noise figure and low DC power consumption on the other hand the disadvantages of the topology are linearity and output power characteristics are strongly dependent on the quiescent bias current of the transistor.

Since low noise figure and high IP3 are required in order to maintain a high signal to noise ratio, the third approach seems to be better than the other topologies. Therefore in our variable gain amplifier design, we will use the third approach.

4.4 Design of Variable Gain Amplifier

A network's behavior at microwave frequencies can be characterized using the scattering parameters (S-parameters). These parameters are defined in terms of traveling waves. Figure 4.6 shows the incident and reflected waves for a two-port network (common-source FET).

The relationship between the S-parameters and the incident and reflected waves can be expressed as follows:

$$b_1=S_{11} \times a_1+ S_{12} \times a_2 \quad (4.1)$$

$$b_2=S_{21} \times a_1+ S_{22} \times a_2 \quad (4.2)$$

where,

a_i and b_i are the incident and reflected waves respectively at port i and can be defined in terms of the voltage wave, as shown in equations (4.3), (4.4), (4.5) and (4.6):

$$a_1=(V_1+I_1 \times Z_0)/(Z_0)^{1/2} \quad (4.3)$$

$$b_1= (V_1-I_1 \times Z_0)/(Z_0)^{1/2} \quad (4.4)$$

$$a_2=(V_2+I_2 \times Z_0)/(Z_0)^{1/2} \quad (4.5)$$

$$b_2= (V_2-I_2 \times Z_0)/(Z_0)^{1/2} \quad (4.6)$$

where, Z_0 is the reference impedance.

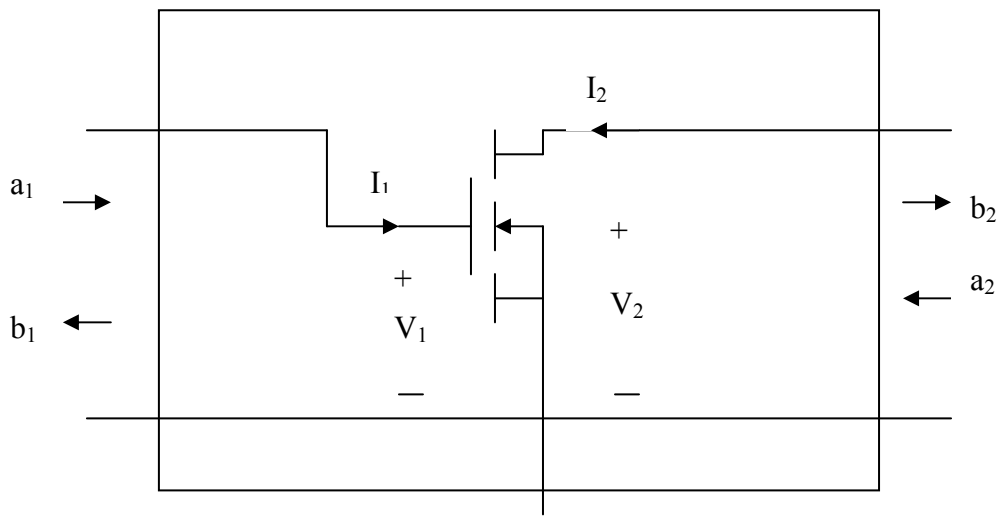

Figure 4.6 A transistor as two-port network

The stability of an amplifier is a very important consideration in a microwave circuit design. Stability or resistance to oscillation in a microwave circuit can be determined by the S-parameters. Oscillations are possible in a two-port network if either or both the input and the output port have negative resistance. This condition

occurs when the magnitude of the input or output reflection coefficients is greater than one,

$|\Gamma_{in}|>1$ or $|\Gamma_{out}|>1$. (4.7)

$\Rightarrow$ if $|S_{11}|<0$dB our circuit is stable. (4.8)

In most of the cases, microwave amplifiers used for narrowband or wideband applications face stability problems at certain frequency ranges. Instability is primarily caused by three phenomena: internal feedback in the transistor, external feedback around the transistor caused by an external circuit, or excess of gain at frequencies outside of the band of operation.

Amplifiers usually need matching networks to achieve the desired goals. The input and output matching networks of the variable gain amplifier is designed to achieve minimum input and output return losses, maximum insertion loss and a stable operation.

The input and output matching networks of the variable gain amplifiers are ideally conjugally matched to the input and output impedance of the amplifier. Matching networks can be implemented using lumped elements, distributed elements (transmission lines), or a combination of lumped and distributed elements. In our design we used lumped elements to achieve a good performance MMIC application.

In our design, CASWELL H-40 non-linear transistor model was used since; the transconductance of the transistor may be changed by the help of this model. Therefore gain of the amplifier may also be changed. The gain and the frequency range considerations of this H-40 model coincide with our vector modulator design. Therefore CASWELL H-40 non-linear transistor model was used in our design.

4.5 Simulation Results of the Variable Gain Amplifier

In order to achieve minimum input and output return losses and maximum insertion loss, I optimize the input and output matching circuits. For stable operation and high insertion loss I put a small inductance from the emitter of the transistor to the ground. Also by pass capacitors and choke inductors are also used in order to prevent the distortion of the RF signal by the DC signal.

Simulations and the optimizations of the circuit were done by the ADS (Advanced Design System) simulation and optimization software. The below simulation performances are the optimization results of Advanced Design System program. All the elements of the Variable Gain Amplifier were given different names and put into the optimization in order to achieve the best performance.

Caswell H-40 transistor model operates well when V_g is between (-1) to (+0.2) V_{DC}. Therefore, SRC2 is swept between (-1.5) to (+0.5) V_{DC} with 50mV steps.

The following figures represent the optimization results of the final structure with optimized element values:

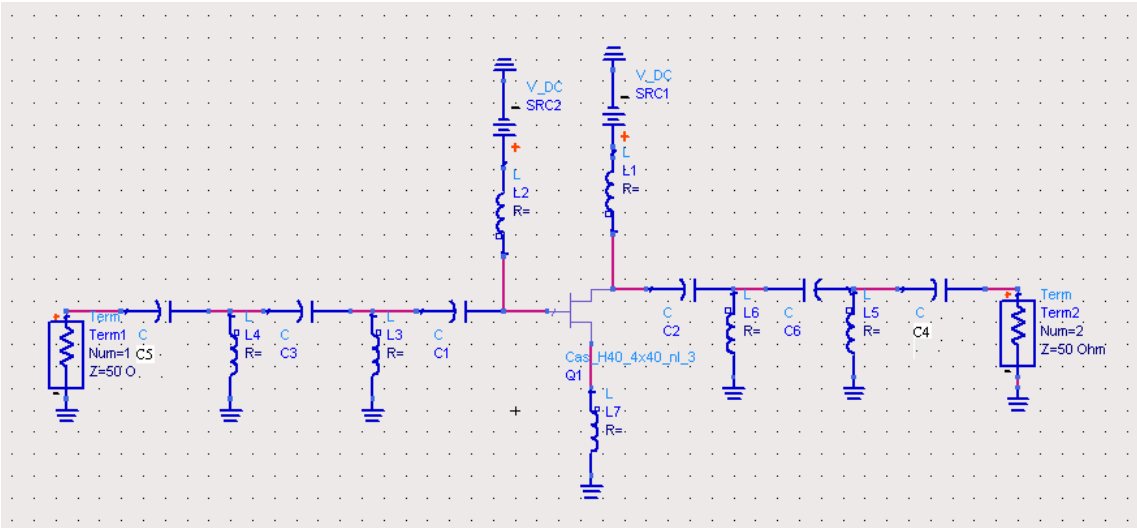

Figure 4.7 Variable gain amplifier

Table 4.1 Element values obtained for the final Variable Gain Amplifier

Element	Element Value
L_1	1.855 uH
L_2	2.434 uH
L_3	0.869 nH
L_4	1.751 nH
L_5	2.258 nH
L_6	3.551 pF
L_7	0.239 nH
C_1	3.201 uF
C_2	4.818 pF
C_3	3.926 pF
C_6	0.262 pF
C_4	0.102 pF
C_5	0.248 pF
SRC1	5 V DC
SRC2	Sweep between (-1.5) to(+0.5) V DC

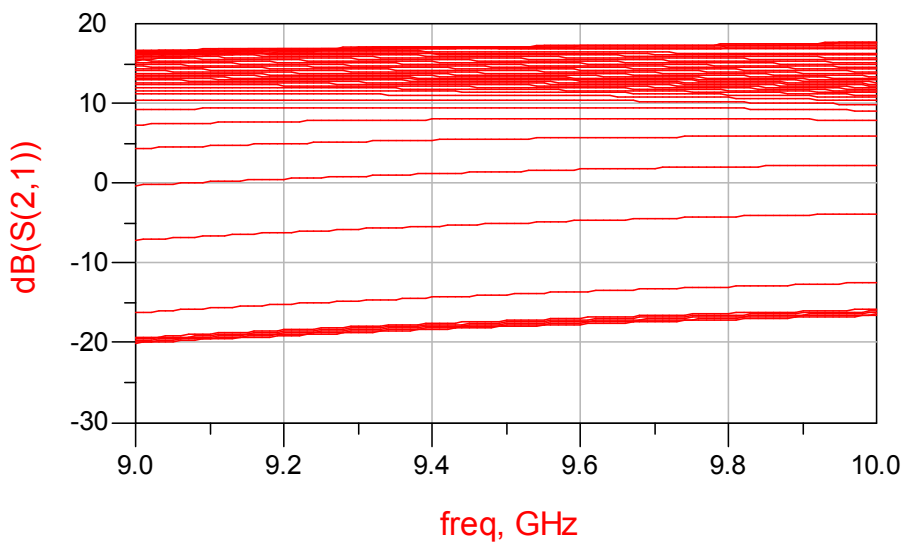

Figure 4.8 Insertion loss of the variable gain amplifier

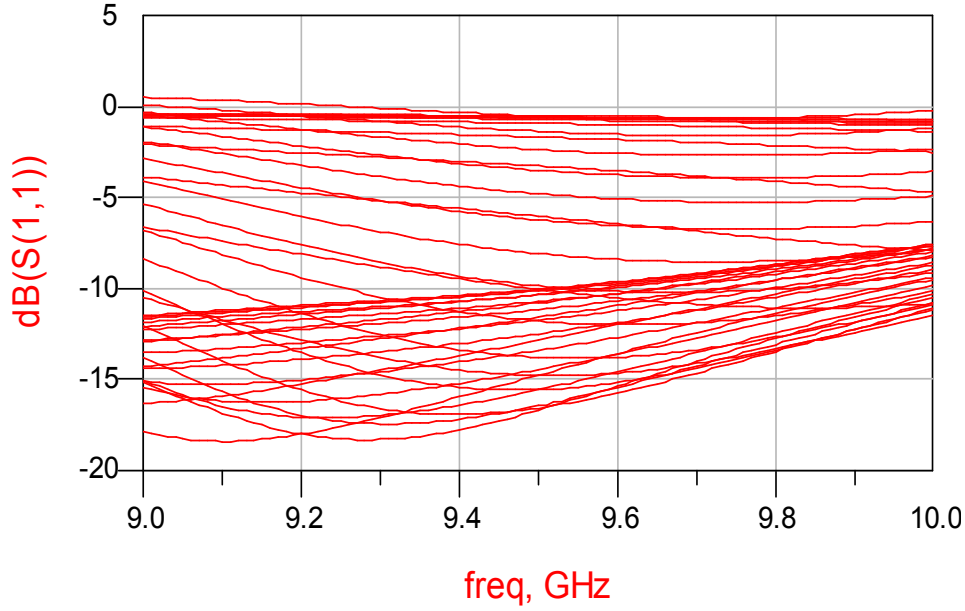

Figure 4.9 Input return loss of the variable gain amplifier

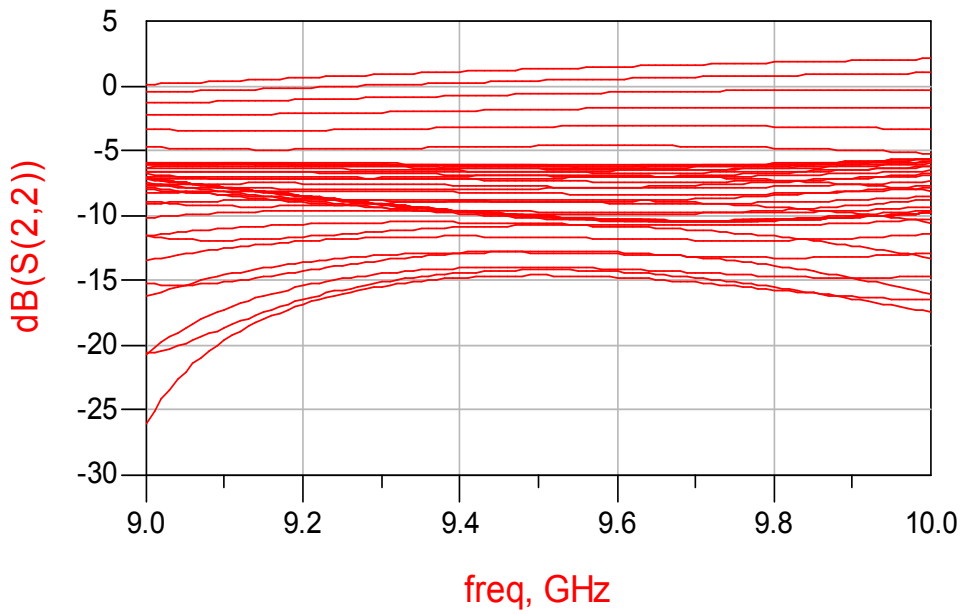

Figure 4.10 Output return loss of the variable gain amplifier

Table 4.2 Insertion loss, input return loss and output return loss of the variable gain amplifier at 9GHz

V_g (V, DC)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
-1,50	-20,050	-0,351	-7,102
-1,45	-19,900	-0,372	-7,114
-1,40	-19,736	-0,398	-7,125
-1,35	-19,558	-0,430	-7,135
-1,30	-19,365	-0,467	-7,142
-1,25	-16,183	-0,597	-7,233
-1,20	-7,088	-1,066	-7,482
-1,15	-0,228	-2,065	-7,842
-1,10	4,380	-3,843	-8,003
-1,05	7,391	-6,616	-7,736
-1,00	9,285	-10,483	-7,196
-0,95	10,462	-15,148	-6,667
-0,90	11,217	-17,845	-6,278
-0,85	11,734	-16,314	-6,038
-0,80	12,119	-14,297	-5,922
-0,75	12,431	-12,930	-5,908
-0,70	12,704	-12,098	-5,980
-0,65	12,956	-11,647	-6,133
-0,60	13,196	-11,481	-6,366
-0,55	13,429	-11,550	-6,685
-0,50	13,656	-11,826	-7,101
-0,45	13,885	-12,270	-7,628
-0,40	14,136	-12,841	-8,283
-0,35	14,406	-13,543	-9,106
-0,30	14,683	-14,347	-10,169
-0,25	14,958	-15,100	-11,572

Table 4.2 (continued)

V_g (V, DC)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
-0,20	15,227	-15,463	-13,490
-0,15	15,487	-15,037	-16,273
-0,10	15,733	-13,766	-20,686
-0,05	15,959	-12,014	-26,041
0	16,158	-10,153	-20,652
0,05	16,321	-8,382	-15,218
0,10	16,440	-6,773	-11,571
0,15	16,508	-5,345	-8,891
0,20	16,516	-4,096	-6,805
0,25	16,635	-2,841	-4,700
0,30	16,519	-1,905	-3,346
0,35	16,345	-1,110	-2,218
0,40	16,108	-0,448	-1,283
0,45	15,812	0,093	-0,517
0,50	15,458	0,523	0,104

Table 4.3 Insertion loss, input return loss and output return loss of the variable gain amplifier at 9.5GHz

V_g (V, DC)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
-1,50	-17,988	-0,486	-10,039
-1,45	-17,820	-0,523	-10,052
-1,40	-17,638	-0,567	-10,063
-1,35	-17,440	-0,620	-10,072
-1,30	-17,227	-0,685	-10,077
-1,25	-13,939	-0,897	-10,132

Table 4.3 (continued)

V_g (V, DC)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
-1,20	-5,017	-1,656	-10,224
-1,15	1,501	-3,258	-9,913
-1,10	5,617	-6,005	-8,996
-1,05	8,103	-10,028	-7,935
-1,00	9,578	-14,784	-7,124
-0,95	10,479	-16,678	-6,605
-0,90	11,069	-14,758	-6,305
-0,85	11,490	-12,843	-6,155
-0,80	11,817	-11,576	-6,111
-0,75	12,092	-10,784	-6,147
-0,70	12,337	-10,315	-6,252
-0,65	12,565	-10,078	-6,420
-0,60	12,782	-10,021	-6,651
-0,55	12,991	-10,116	-6,949
-0,50	13,193	-10,348	-7,322
-0,45	13,398	-10,698	-7,774
-0,40	13,623	-11,155	-8,310
-0,35	13,869	-11,743	-8,946
-0,30	14,124	-12,486	-9,709
-0,25	14,381	-13,396	-10,618
-0,20	14,640	-14,457	-11,681
-0,15	14,900	-15,573	-12,861
-0,10	15,159	-16,453	-13,988
-0,05	15,417	-16,563	-14,626
0	15,671	-15,563	-14,216
0,05	15,916	-13,790	-12,749
0,10	16,148	-11,786	-10,784

Table 4.3 (continued)

V_g (V, DC)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
0,15	16,362	-9,848	-8,773
0,20	16,552	-8,075	-6,900
0,25	16,892	-6,215	-4,643
0,30	17,030	-4,773	-3,154
0,35	17,133	-3,485	-1,817
0,40	17,189	-2,343	-0,630
0,45	17,185	-1,347	0,406
0,50	17,109	-0,497	1,293

Table 4.4 Insertion loss, input return loss and output return loss of the variable gain amplifier at 10GHz

V_g (V, DC)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
-1,50	-16,613	-0,709	-9,784
-1,45	-16,438	-0,767	-9,794
-1,40	-16,249	-0,839	-9,802
-1,35	-16,047	-0,925	-9,807
-1,30	-15,833	-1,029	-9,808
-1,25	-12,455	-1,355	-9,803
-1,20	-3,778	-2,483	-9,583
-1,15	2,286	-4,703	-8,777
-1,10	5,873	-7,910	-7,666
-1,05	7,924	-10,826	-6,763
-1,00	9,123	-11,462	-6,184
-0,95	9,874	-10,525	-5,850
-0,90	10,389	-9,486	-5,676

Table 4.4 (continued)

V_g (V, DC)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
-0,85	10,775	-8,712	-5,609
-0,80	11,088	-8,186	-5,620
-0,75	11,360	-7,848	-5,692
-0,70	11,607	-7,652	-5,821
-0,65	11,840	-7,566	-6,003
-0,60	12,063	-7,569	-6,241
-0,55	12,279	-7,648	-6,541
-0,50	12,489	-7,792	-6,912
-0,45	12,702	-7,993	-7,360
-0,40	12,937	-8,249	-7,893
-0,35	13,196	-8,566	-8,533
-0,30	13,466	-8,946	-9,310
-0,25	13,741	-9,378	-10,262
-0,20	14,021	-9,850	-11,438
-0,15	14,306	-10,333	-12,897
-0,10	14,598	-10,774	-14,665
-0,05	14,894	-11,085	-16,526
0	15,195	-11,146	-17,422
0,05	15,498	-10,845	-16,035
0,10	15,799	-10,144	-13,308
0,15	16,094	-9,106	-10,541
0,20	16,378	-7,861	-8,087
0,25	16,860	-6,287	-5,228
0,30	17,124	-4,895	-3,389
0,35	17,368	-3,556	-1,745
0,40	17,572	-2,302	-0,282
0,45	17,714	-1,162	1,003

Table 4.4 (continued)

V_g (V, DC)	S_{21} (dB)	S_{11} (dB)	S_{22} (dB)
0,50	17,772	-0,162	2,106

As can be seen from the figures and the tables, variable gain amplifier operates well in the 9-10GHz bandwidth. However, V_g voltage must be swept between (-1.1) to (+0.2) Volts in order to get an input return loss of maximum (-6) dB and output return loss of maximum (-5.6) dB and a dynamic range of better than 12 dB for insertion loss.

4.6 Simulations Results of the Power Splitter Stage, Filter Stage and Variable Gain Amplifier Stage

In this section, power splitter, low pass filter, high pass filter and variable gain amplifiers are simulated and optimized altogether in order to get good matching, high insertion loss and 120 degrees phase shifts.

Simulations and the optimizations of the circuit were done by the ADS (Advanced Design System) simulation and optimization software. All the elements were given different names and put into the optimization in order to achieve the best performance.

The below simulation performances are the optimization results of Advanced Design System program. When one channel's gate voltage was swept the other gate voltages were set to 0 V. The following figures represent the optimization results of the final structure with optimized element values:

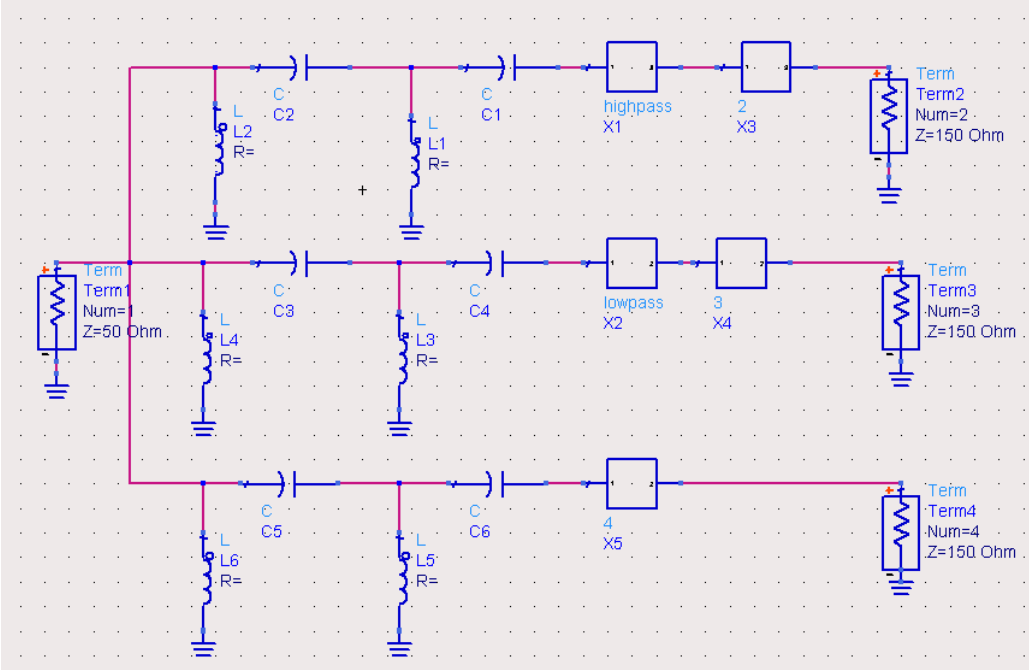

Figure 4.11 Power Splitter Stage, Filter Stage and Variable Gain Amplifier Stage

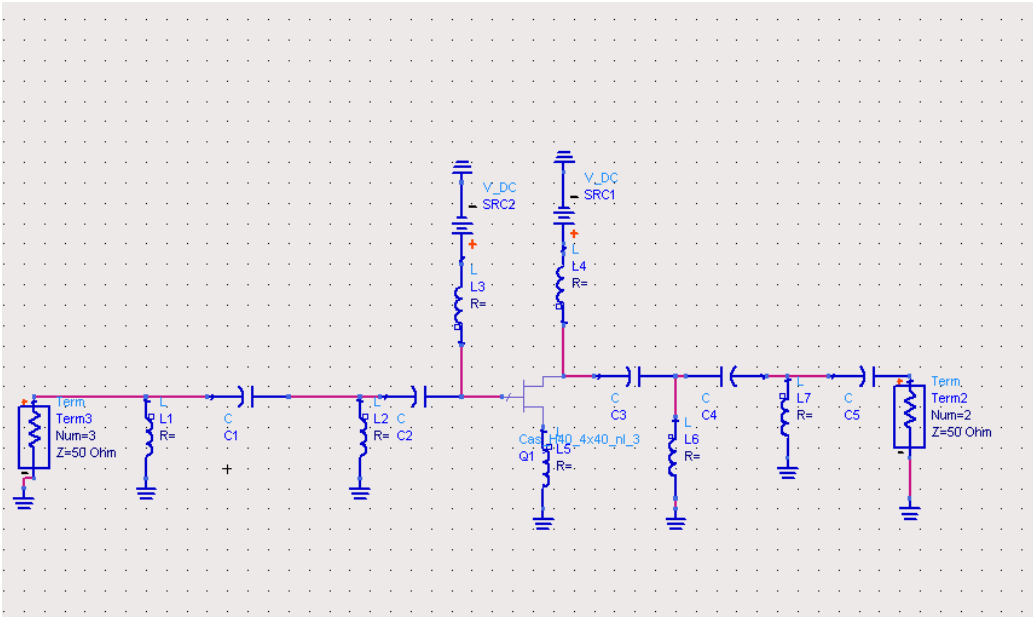

Figure 4.12 Variable gain amplifier section (every channel's element values are different than each other, due to optimization, however all the VGA circuit schematics are the same)

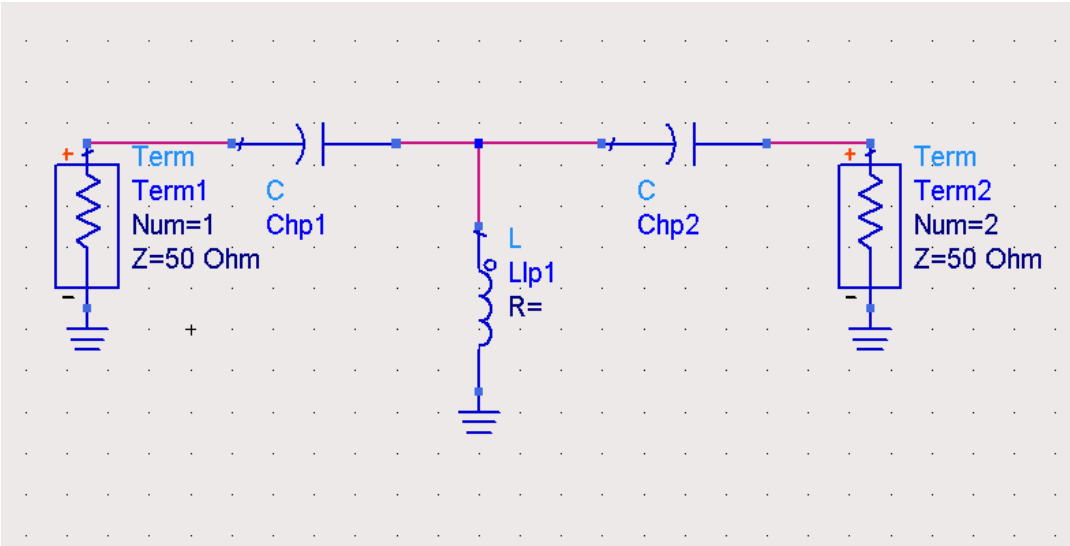

Figure 4.13 High pass filter section

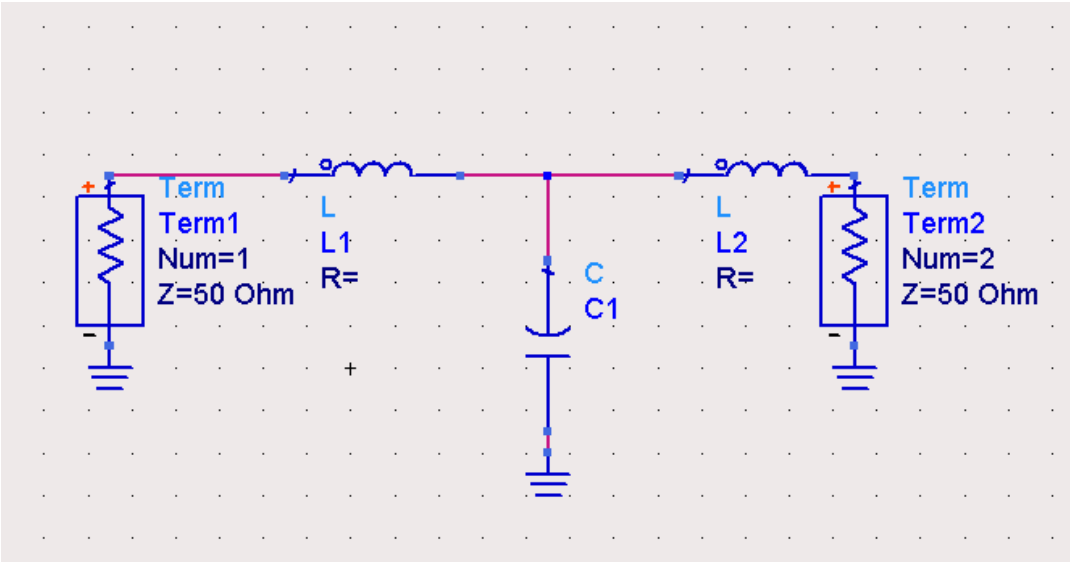

Figure 4.14 Low pass filter section

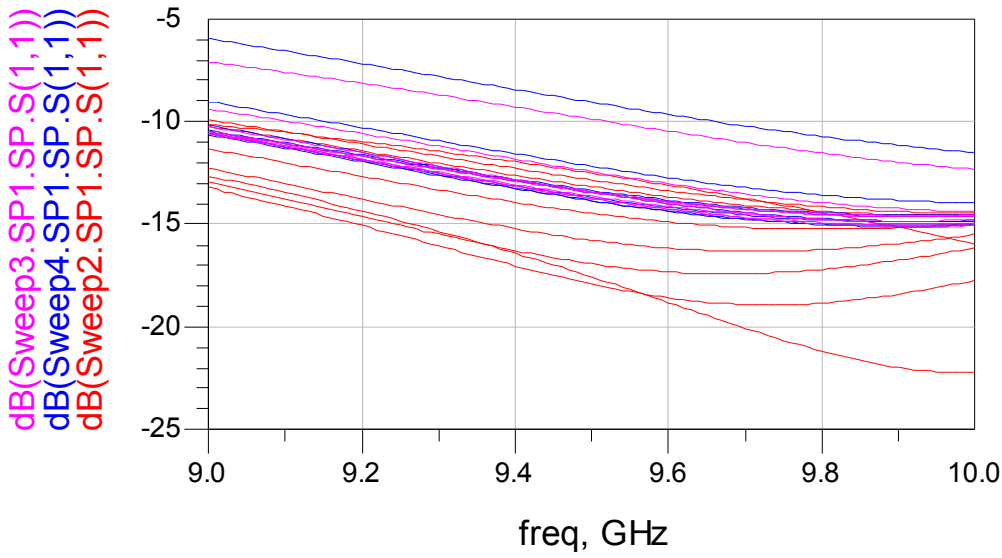

Figure 4.15 Input return losses with different gate voltage sweeps

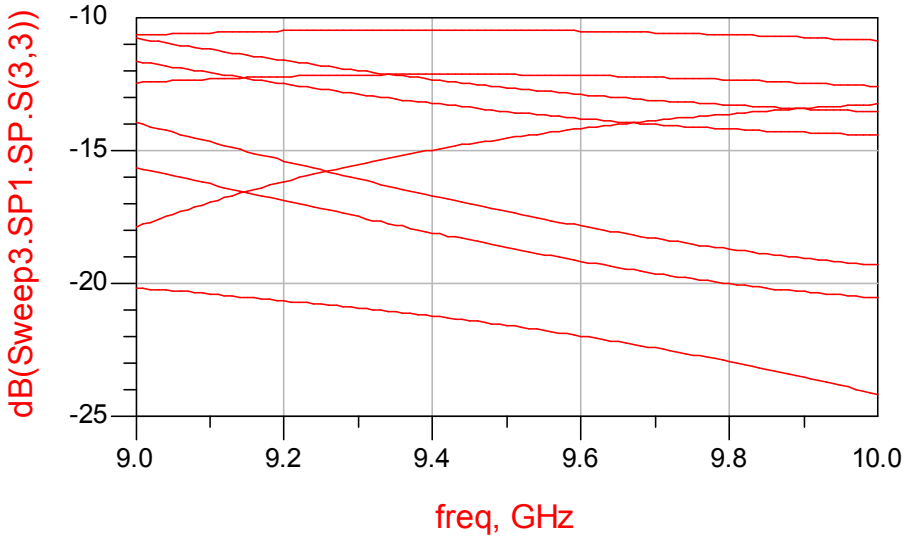

Figure 4.16 Second channel's output return loss with second gate voltage sweep

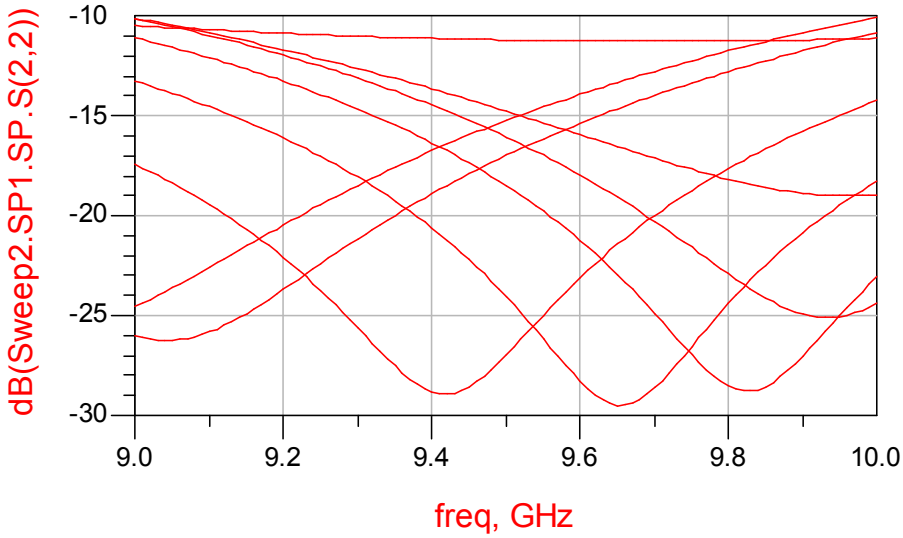

Figure 4.17 First channel's output return loss with first gate voltage sweep

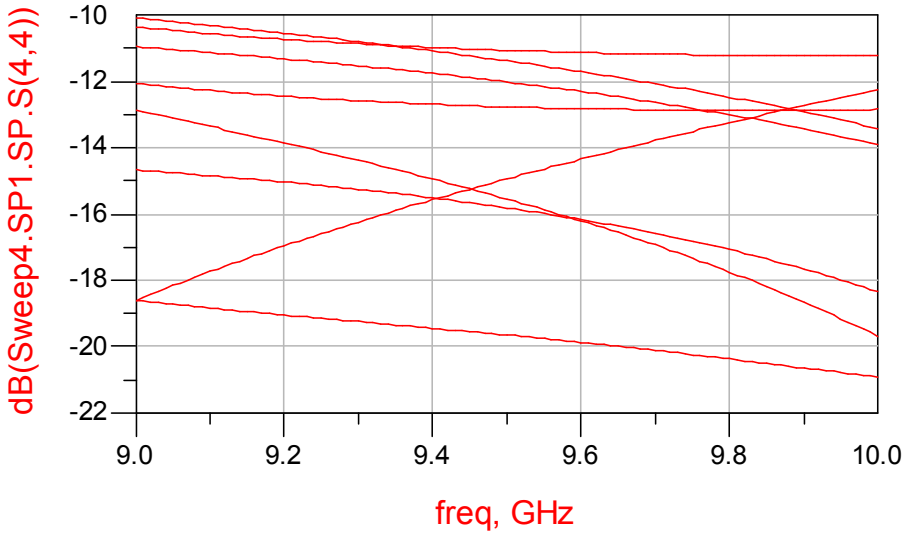

Figure 4.18 Third channel's output return loss with third gate voltage sweep

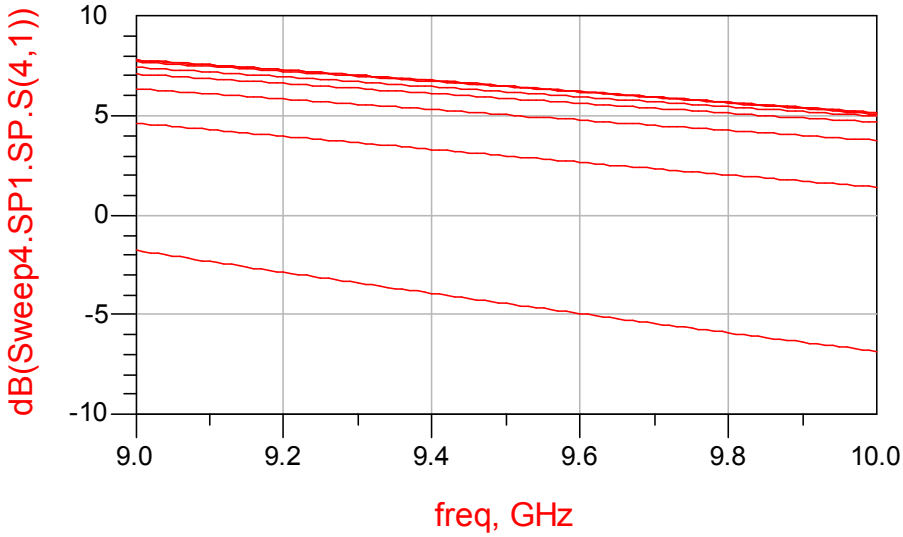

Figure 4.19 Third channel's insertion loss with third gate voltage sweep

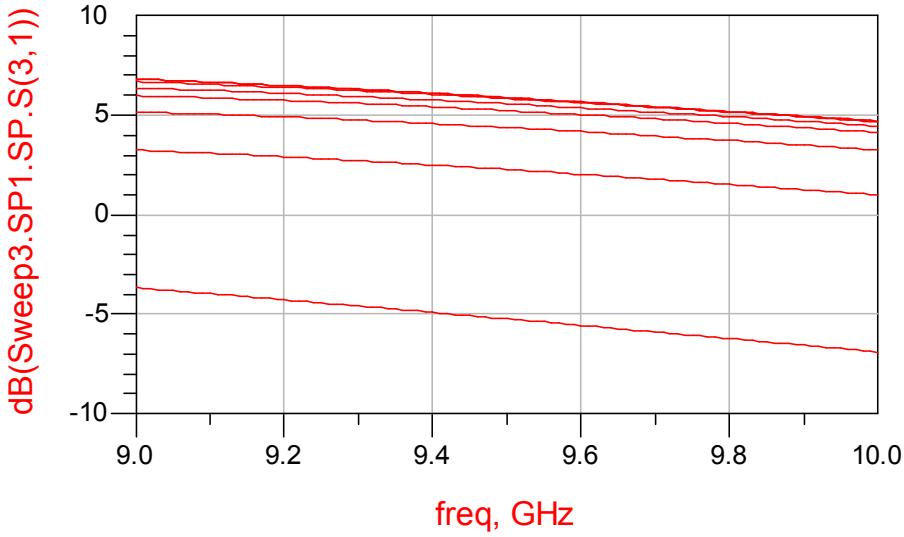

Figure 4.20 Second channel's insertion loss with second gate voltage sweep

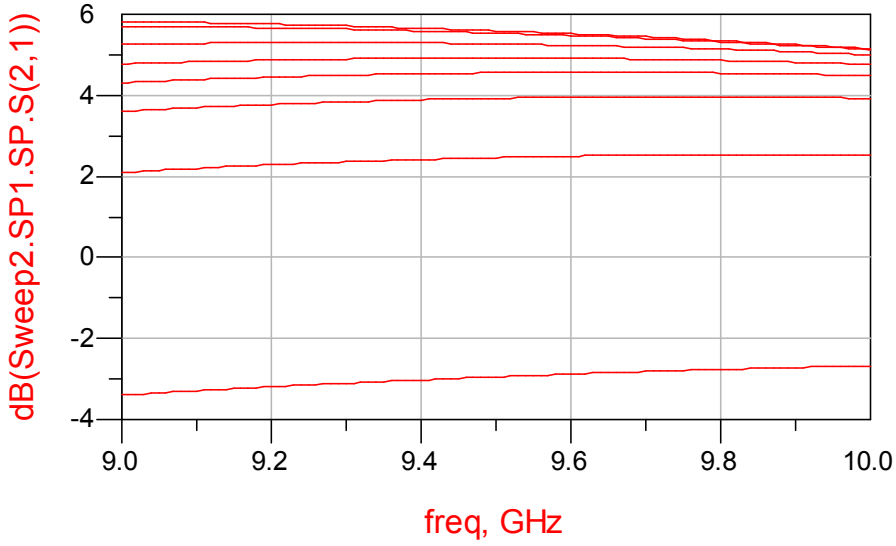

Figure 4.21 First channel's insertion loss with first gate voltage sweep

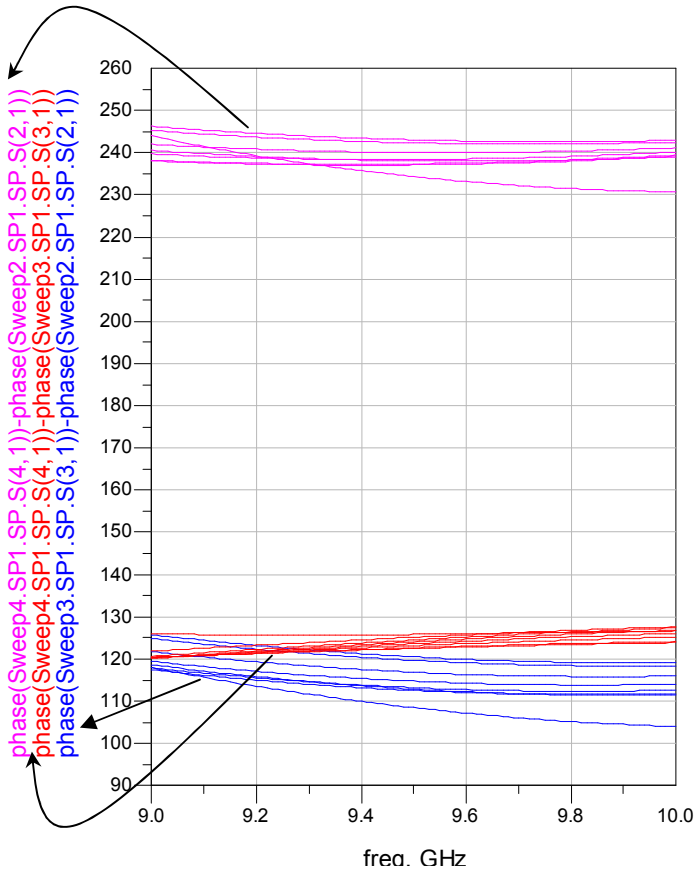

Figure 4.22 Phase differences of the channels when only one channel's gate voltage is swept and the others are set to 0 Volt.

For ease of operation, gate voltages are swept between (-1.1) to (+0.3) V in 200 mV steps. The results show that insertion loss has a better than 10 dB dynamic range and the output and input return losses are better than -10dB and phase differences between the channel's are almost 120 degrees.

Table 4.5 Element values obtained for the power splitter stage, filter stage and variable gain amplifier stage

Element	Element Value	Element	Element Value
L_1	4.000 nH	1st channel VGA C_5	0.129 pF
C_1	3.961 pF	1st channel VGA L_6	3.738 nH
L_2	4.000 nH	1st channel VGA L_7	3.485 nH
C_2	0.195 pF	2nd channel VGA L_1	3.783 nH
L_3	3.991 nH	2nd channel VGA C_1	3.559 pF
C_3	0.723 pF	2nd channel VGA L_2	3.993 nH
L_4	Open circuit	2nd channel VGA C_2	1.201 uF
C_4	0.176 pF	2nd channel VGA L_3	2.435 uH
L_5	Open circuit	2nd channel VGA C_3	4.818 uF
C_5	3.969 pF	2nd channel VGA L_4	1.855 uH
L_6	4.000 nH	2nd channel VGA C_4	0.126 pF
C_6	2.972 pF	2nd channel VGA L_5	0.271 nH
Low pass L_1	2.714 nH	2nd channel VGA C_5	0.303 pF
Low pass C_1	0.148 pF	2nd channel VGA L_6	1.344 nH
Low pass L_2	1.918 nH	2nd channel VGA L_7	0.921 nH
High pass C_1	1.575 pF	3rd channel VGA L_1	3.976 nH
High pass L_1	3.000 nH	3rd channel VGA C_1	3.855 pF
High pass C_2	2.331 pF	3rd channel VGA L_2	3.392 nH
1st channel VGA L_1	3.917 nH	3rd channel VGA C_2	3.201 uF
1st channel VGA C_1	3.059 pF	3rd channel VGA L_3	2.435 uH
1st channel VGA L_2	3.954 nH	3rd channel VGA C_3	3.818 uF
1st channel VGA C_2	3.201 uF	3rd channel VGA L_4	1.855 uH

Table 4.5 (continued)

Element	Element Value	Element	Element Value
1st channel VGA L_3	2.435 uH	3rd channel VGA C_4	0.190 pF
1st channel VGA C_3	3.818 uF	3rd channel VGA L_5	0.180 nH
1st channel VGA L_4	1.855 uH	3rd channel VGA C_5	0.832 pF
1st channel VGA C_4	3.392 pF	3rd channel VGA L_6	1.321 nH
1st channel VGA L_5	1.710 nH	3rd channel VGA L_7	1.505 nH
1st channel SRC2	Sweep between (-1.1) to (+0.3) V or set to 0 V DC		
2nd channel SRC2	Sweep between (-1.1) to (+0.3) V or set to 0 V DC		
3rd channel SRC2	Sweep between (-1.1) to (+0.3) V or set to 0 V DC		
1st channel SRC1	5 V DC		
2nd channel SRC1	5 V DC		
3rd channel SRC1	5 V DC		

CHAPTER 5

IN PHASE POWER COMBINER and the FINAL ANALYSIS of the VECTOR MODULATOR

5.1 In Phase Power Combiner

Power splitters are used to divide the input power into a number of smaller amounts of power for exciting the radiating elements in an array antenna. They are also used in balanced power amplifiers both as power splitters and power combiners [17].

The last section of our vector modulator is a 4-port (4.8 dB) in phase power combiner. In chapter two, we designed a low pass impedance transformer. However, in the simulations, we changed the second order low pass impedance transformer to a forth order high pass impedance transformer in order to get good phase shifting and matching. We can also use that optimized power splitter as a power combiner by taking its mirror image. However, we may need optimization in order get good matching. We will use that in phase power combiner after the variable gain amplifier section.

As mentioned in the earlier chapters realizing the MMIC structure with lumped elements is much easier than realizing it with distributed elements. Therefore, we again used lumped elements in the design. Furthermore, for wide band match we used forth order high pass impedance transformer.

5.2 Simulations Results of the In Phase Power Combiner

Simulations and the optimizations of the circuit were done by the ADS (Advanced Design System) simulation and optimization software. Firstly, we get the mirror image of the 150 Ω to 50 Ω high pass forth order impedance transformer designed and optimized in chapter two, however the results were not good enough. Therefore optimization was done.

The below simulation performances are the optimization results of Advanced Design System program. The following figures represent the optimization results of the final structure with optimized element values:

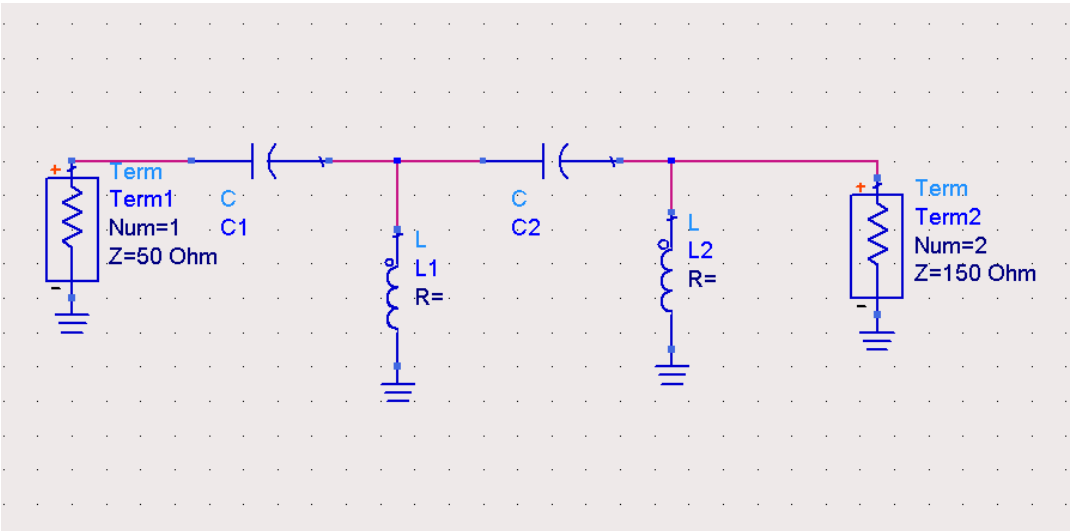

Figure 5.1 50 Ω to 150 Ω high pass forth order impedance transformer

Table 5.1 Element values obtained for the impedance transformer

Element	Element Value
C_1	0.351106 pF
L_1	1.09911 nH
C_2	0.192483 pF
L_2	4.0 nH

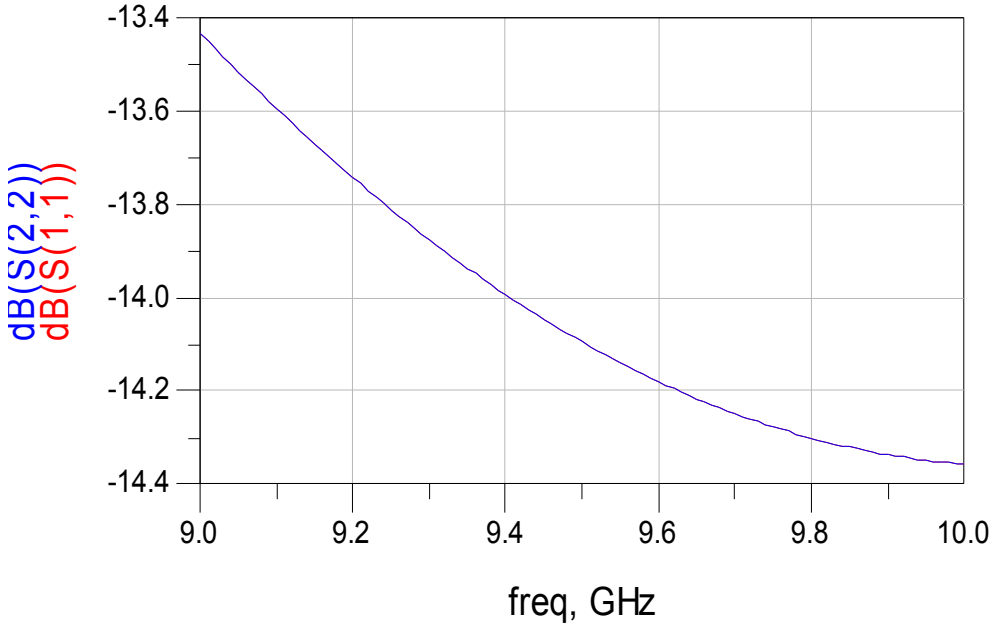

Figure 5.2 Input and output return losses of the impedance transformer

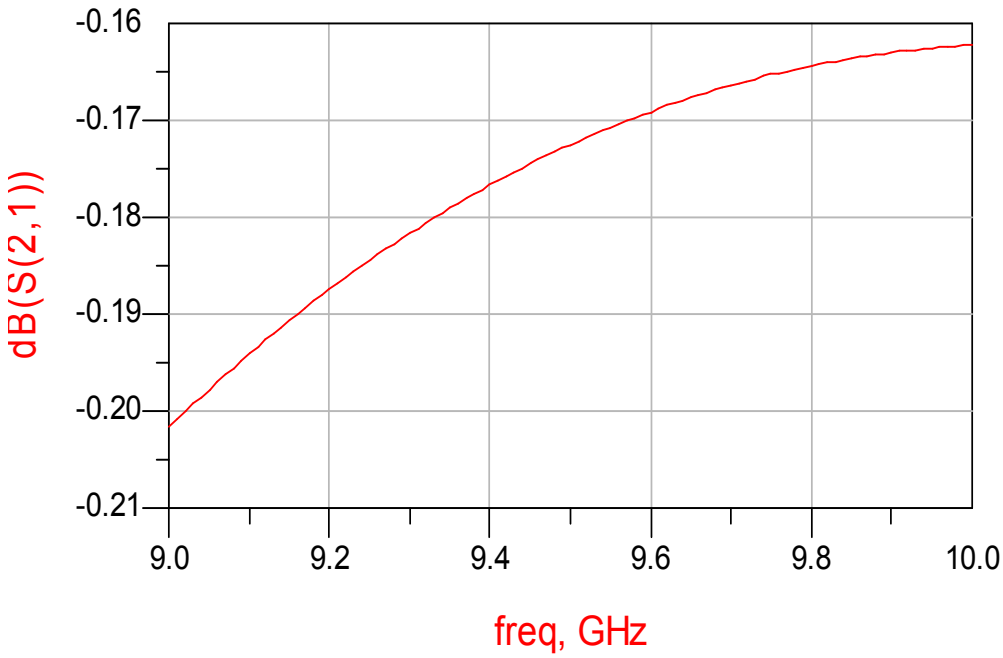

Figure 5.3 Insertion loss of the impedance transformer

5.3 Simulations Results of the Vector Modulator

In this section, all the section of the vector modulator is simulated and it was seen that optimization was needed. Therefore all the circuit elements were optimized.

Simulations and the optimizations of the circuit were done by the ADS (Advanced Design System) simulation and optimization software. All the elements were given different names and put into the optimization in order to achieve the best performance.

The below simulation performances are the optimization results of Advanced Design System program. The following figures represent the optimization results of the final structure with optimized element values:

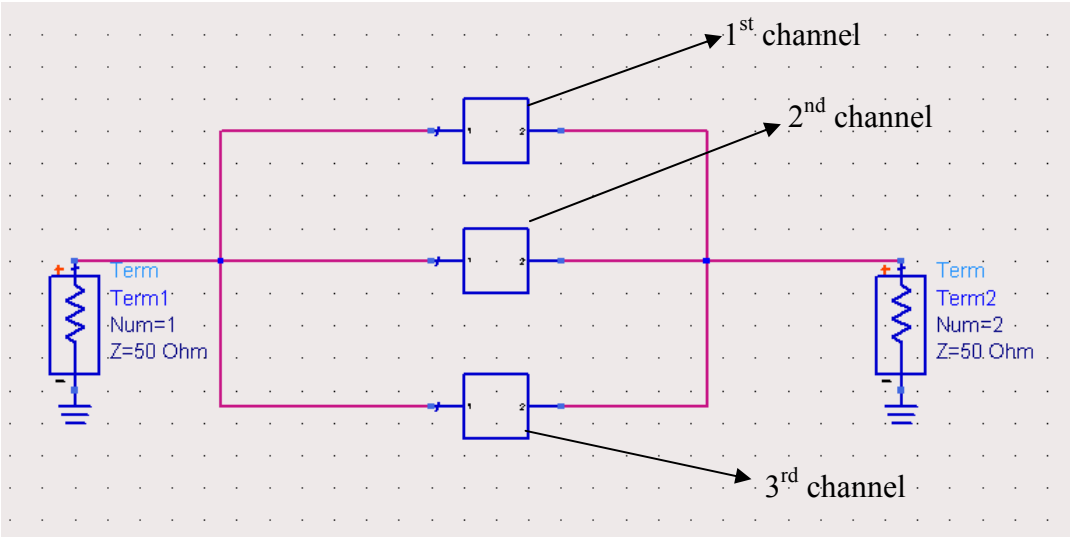

Figure 5.4 Vector Modulator

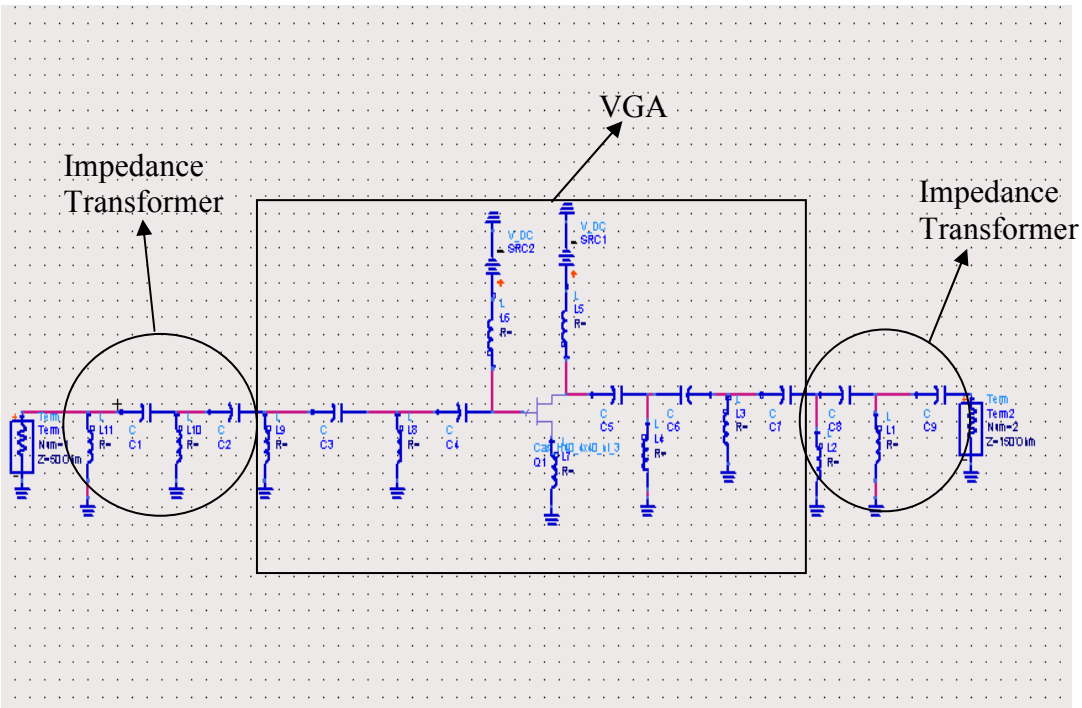

Figure 5.5 1st channel's circuit diagram

Table 5.2 Element values obtained after the optimization for the first channel

Element	Element Value	Element	Element Value
L_1	3.375 nH	L_6	2.435 uH
C_1	0.609 pF	C_6	0.381 pF
L_2	2.982 nH	L_7	1.069 nH
C_2	0.100 pF	C_7	1.343 pF
L_3	2.670 nH	L_8	3.931 nH
C_3	1.480 pF	C_8	0.393 pF
L_4	1.749 nH	L_9	2.888 nH
C_4	3.201uF	C_9	0.390 pF
L_5	1.855 nH	L_{10}	3.300 nH
C_5	3.818 uF	L_{11}	3.370 nH
SRC1	5 V, DC		
SRC2	Sweep between (-1.5) to (+0.5) V, DC		

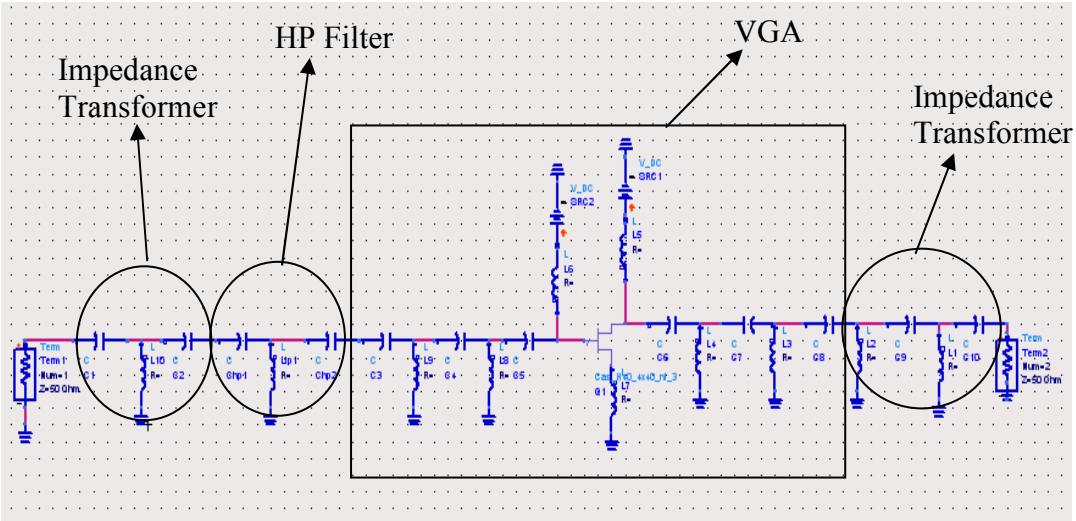

Figure 5.6 2nd channel's circuit diagram

Table 5.3 Element values obtained after the optimization for the second channel

Element	Element Value	Element	Element Value
L_1	1.356 nH	L_7	0.340 nH
C_1	2.619 pF	C_7	0.768 pF
L_2	2.982 nH	L_8	1.658 nH
C_2	0.976 pF	C_8	0.088 pF
L_3	2.917 nH	L_9	0.800 nH
C_3	0.600 pF	C_9	0.395 pF
L_4	2.995 nH	L_{10}	1.495 nH
C_4	1.098 pF	C_{10}	0.426 pF
L_5	1.855 uH	C_{hp1}	1.058 pF
C_5	1.201 uF	L_{hp1}	0.106 nH
L_6	2.435 uH	C_{hp2}	0.373 pF
C_6	3.818 uF		
SRC1	5 V, DC		
SRC2	Sweep between (-1.5) to (+0.5) V, DC		

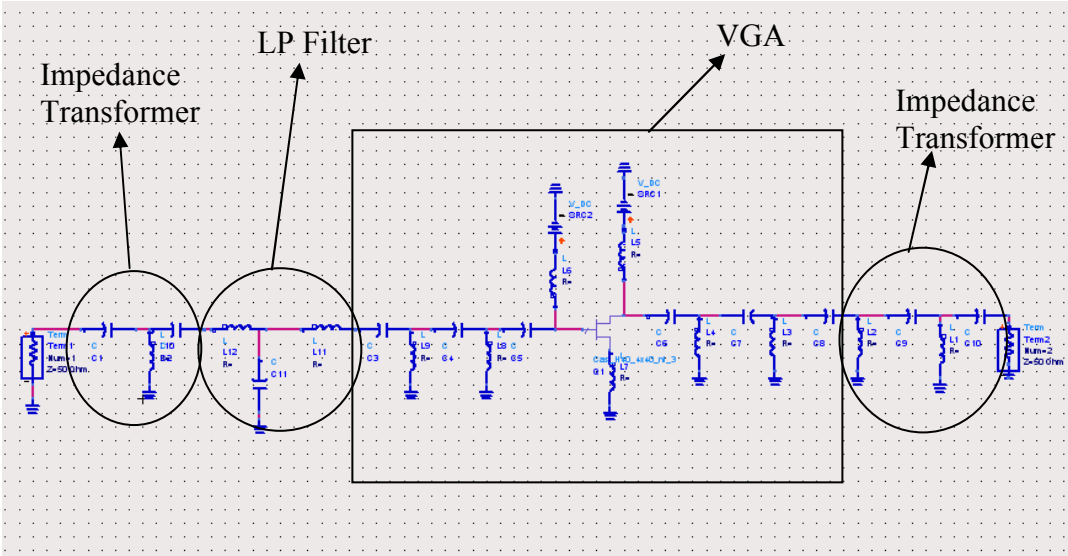

Figure 5.7 3rd channel's circuit diagram

Table 5.4 Element values obtained after the optimization for the third channel

Element	Element Value	Element	Element Value
L_1	3.372 nH	L_7	0.108 nH
C_1	2.859 pF	C_7	0.135 pF
L_2	2.982 nH	L_8	2.700 nH
C_2	2.950 pF	C_8	0.188 pF
L_3	1.119 nH	L_9	1.600 nH
C_3	0.305 pF	C_9	0.410 pF
L_4	1.172 nH	L_{10}	2.965 nH
C_4	0.876 pF	C_{10}	0.429 pF
L_5	1.855 uH	L_{11}	3.097 nH
C_5	3.201 uF	C_{11}	0.316 pF
L_6	2.435 uH	L_{12}	0.789 nH
C_6	3.818 uF		
SRC1	5 V, DC		
SRC2	Sweep between (-1.5) to (+0.5) V, DC		

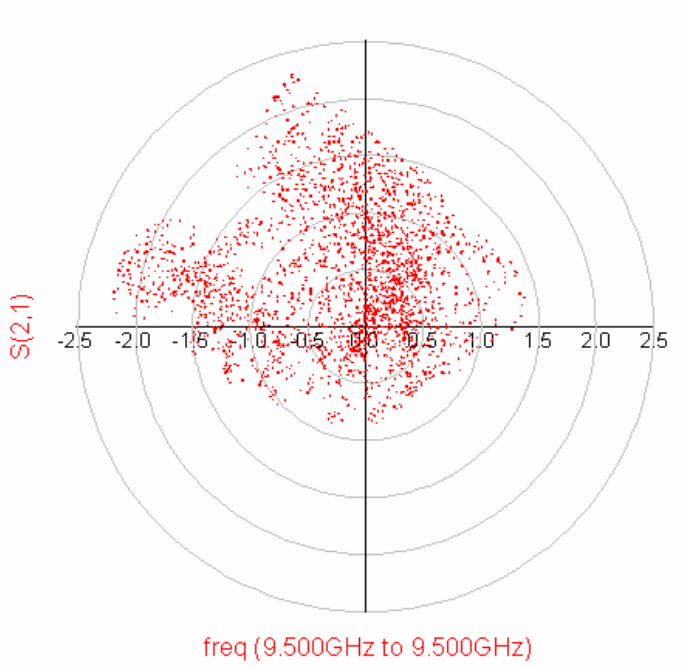

Figure 5.8 Insertion loss of the vector modulator in polar coordinate at 9.5 GHz (Dynamic range of -36dB to 8dB)

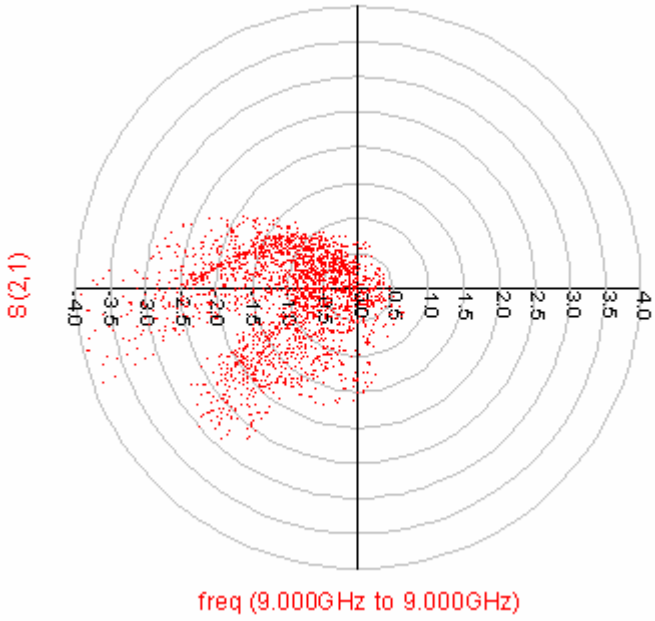

Figure 5.9 Insertion loss of the vector modulator in polar coordinate at 9 GHz (Dynamic range of -36dB to 12dB)

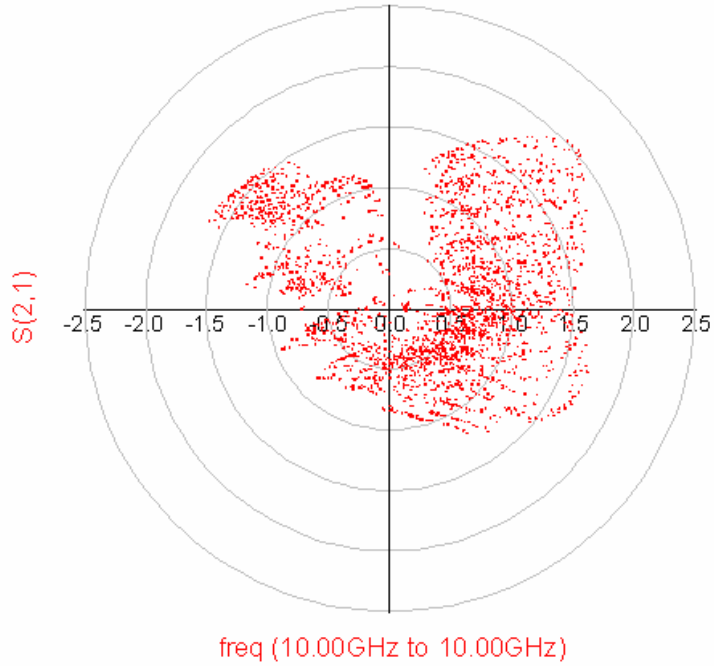

Figure 5.10 Insertion loss of the vector modulator in polar coordinate at 10 GHz (Dynamic range of -28dB to 8dB)

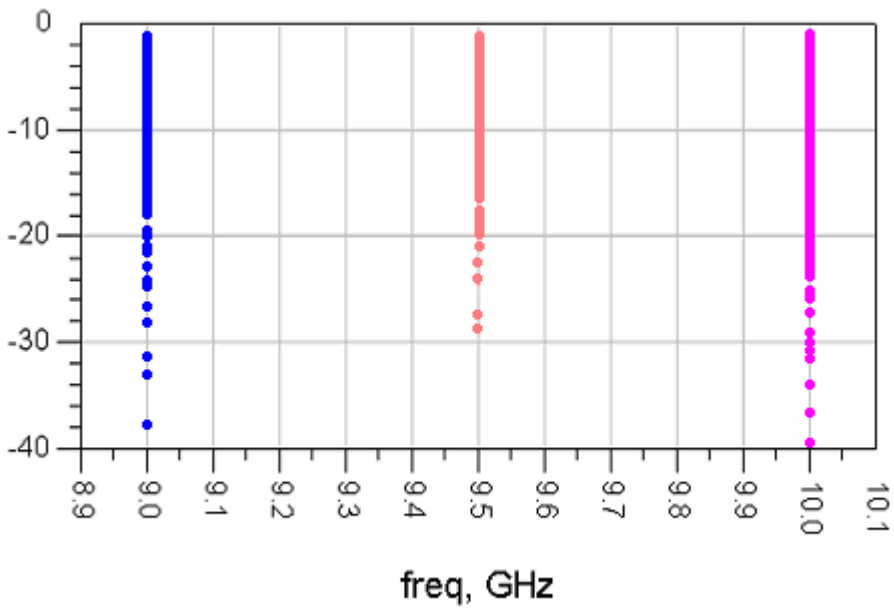

Figure 5.11 Input return loss of the vector modulator in Cartesian coordinate at 9GHz, 9.5GHz and 10 GHz

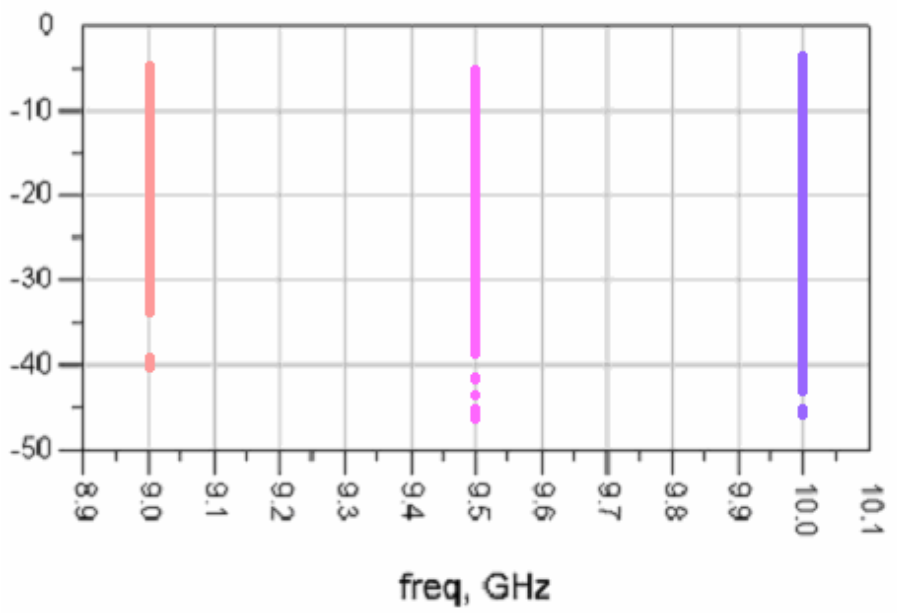

Figure 5.12 Output return loss of the vector modulator in Cartesian coordinate at 9GHz, 9.5GHz and 10 GHz

As can be seen from the figures our vector modulator operates well in the 9-10 GHz bandwidth. For ease of operation gate voltages of the variable gain amplifiers were swept between (-1.5) to (0.5) V with 125 mV steps.

By looking at the figures we can easily comment that vector modulator's insertion loss has at least 15 dB dynamic range. Since the step voltage is very high, 125 mV, we can not see full 360 degrees coverage for some amplitude values. However, if we change the step voltage to lower values, it is possible to see full 360 degrees coverage for all amplitude values.

Some of the input and output insertion losses seem to be high. However, these are the values when one or more variable gain amplifiers are in off region. Also we can say that in these regions insertion losses are very small, therefore these regions will not be used. Except for those regions, insertion loss has at least 15dB dynamic range and input and output return losses are better than 5-6 dB which are reasonable values.

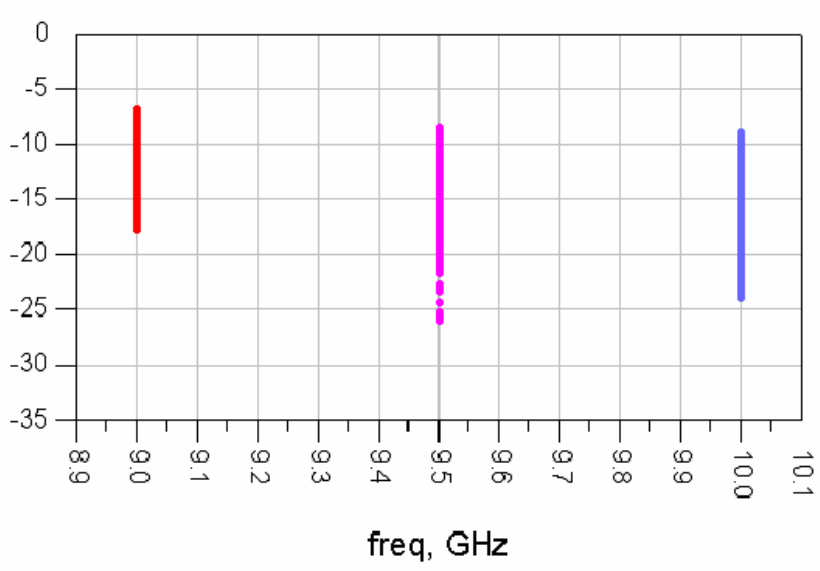

Figure 5.13 Input return loss of the vector modulator when none of the amplifiers are in off stage at 9GHz, 9.5 GHz and 10GHz (gate voltage is swept between (-1.1) to (+0.15) V in 125mV steps

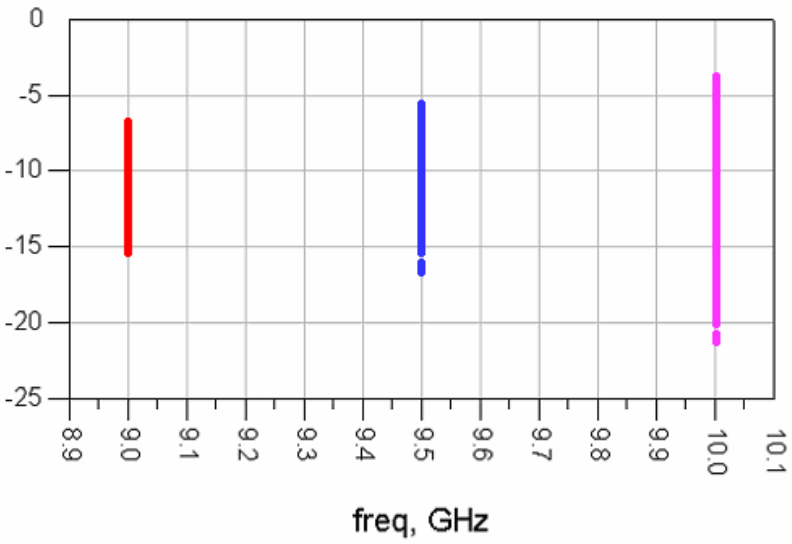

Figure 5.14 Output return loss of the vector modulator when none of the amplifiers are in off stage at 9GHz, 9.5 GHz and 10GHz (gate voltage is swept between (-1.1) to (+0.15)V in 125mV steps

CHAPTER 6

CASWELL MODEL and LAYOUT of the FINAL CIRCUIT

6.1 Caswell H-40 Model:

In this section, all the lumped element models are replaced with Caswell H-40 Models in order to achieve MMIC vector modulator. Capacitance values are optimized by changing the distances between the layers or changing the type of the Caswell H-40 Capacitance Model. Higher values (by-pass capacitances) are realized with transmission lines. Inductance values are optimized by changing the turn of the Caswell H-40 Inductance Model. Lower values are realized with transmission lines. Choke inductances are not replaced with Caswell H-40 model, because they will be not be in the final layout. They will be given from outside the circuit. The Final circuit is simulated and it was seen that optimization (tuning) was needed. Therefore all the circuit elements were optimized (tuned).

Simulations and the optimizations of the circuit were done by the ADS (Advanced Design System) simulation and optimization software. All the elements were given different names and put into the optimization in order to achieve the best performance.

The below simulation performances are the optimization results of Advanced Design System program. The following figures represent the optimization results of the final structure with optimized element values:

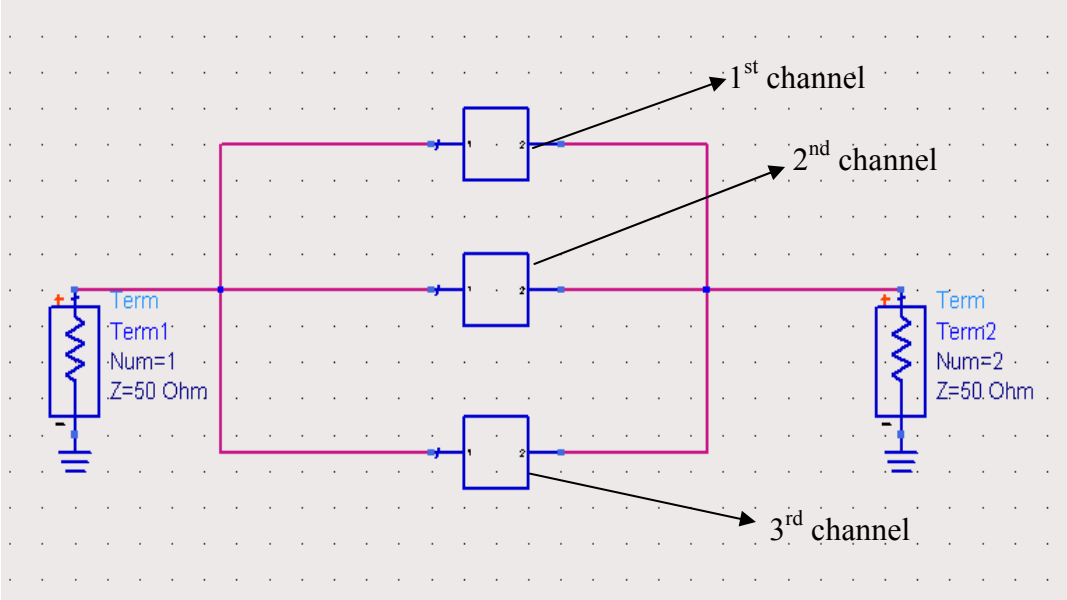

Figure 6.1 MMIC Vector Modulator

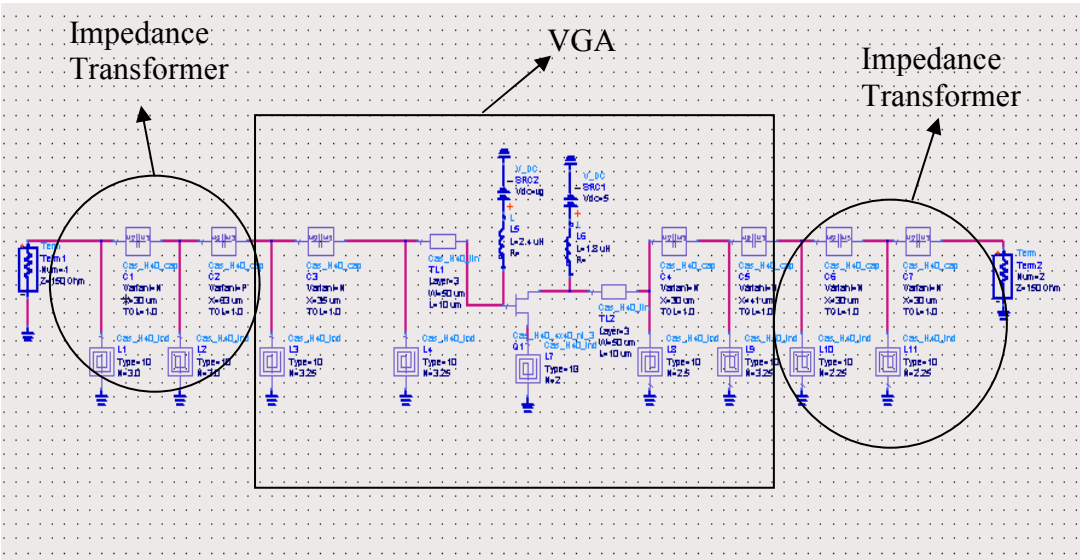

Figure 6.2 1st channel's circuit diagram

Table 6.1 Element values obtained after the optimization for the first channel

Element	Element Value	Element	Element Value
L_1	3 turn	L_6	1.8 uH
C_1	X=30 um Type N	C_6	X=30 um Type N
L_2	3 turn	L_7	2 turn
C_2	X=63 um Type P	C_7	X=30 um Type N
L_3	3.25 turn	L_8	2.5 turn
C_3	X=35 um Type N	L_9	3.25 turn
L_4	3.25 turn	L_{10}	2.25 turn
C_4	X=30 um Type N	L_{11}	2.25 turn
L_5	2.4 nH	TL_1	W= 50 um L=10 um
C_5	X=41 um Type N	TL_2	W= 50 um L=10 um
SRC2	Sweep between (-1.5) to (+0.5) V, DC		
SRC1	5 V, DC		

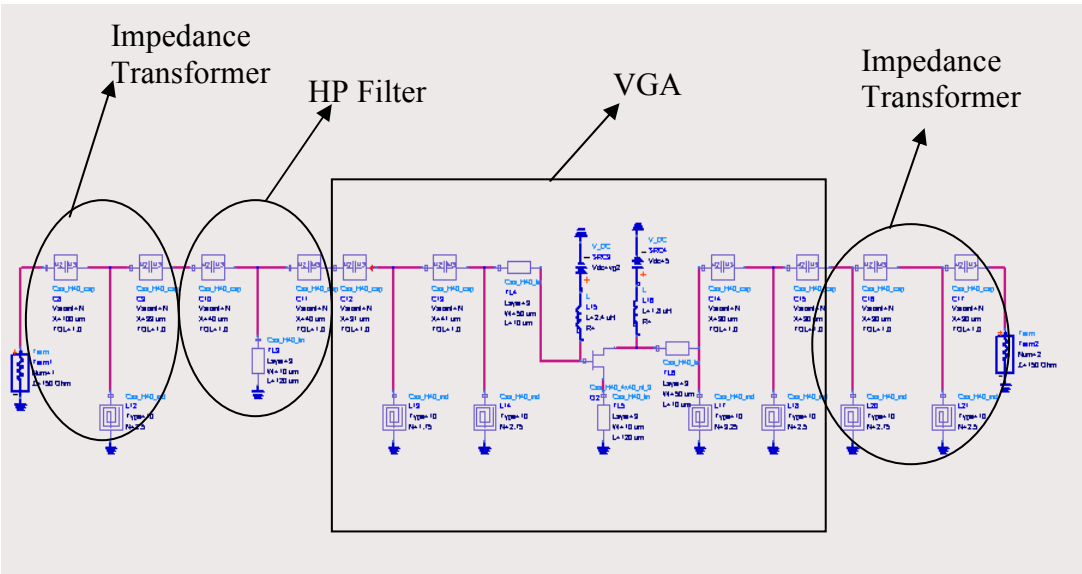

Figure 6.3 2nd channel's circuit diagram

Table 6.2 Element values obtained after the optimization for the second channel

Element	Element Value	Element	Element Value
L_{12}	2.5 turn	L_{18}	2.5 turn
C_8	X=100 um Type N	C_{14}	X=30 um Type N
L_{13}	1.75 turn	L_{20}	2.75 turn
C_9	X=33 um Type N	C_{15}	X=30 um Type N
L_{14}	2.75 turn	L_{21}	2.5 turn
C_{10}	X=40 um Type N	C_{16}	X=30 um Type N
L_{15}	2.4 nH	C_{17}	X=30 um Type N
C_{11}	X=40 um Type N	TL_3	W= 10 um L=120 um
L_{16}	1.8 uH	TL_4	W= 50 um L=10 um
C_{12}	X=31 um Type N	TL_5	W= 10 um L=120 um
L_{17}	3.25 turn	TL_6	W= 50 um L=10 um
C_{13}	X=41 um Type N		
SRC3	5 V, DC		
SRC4	Sweep between (-1.5) to (+0.5) V, DC		

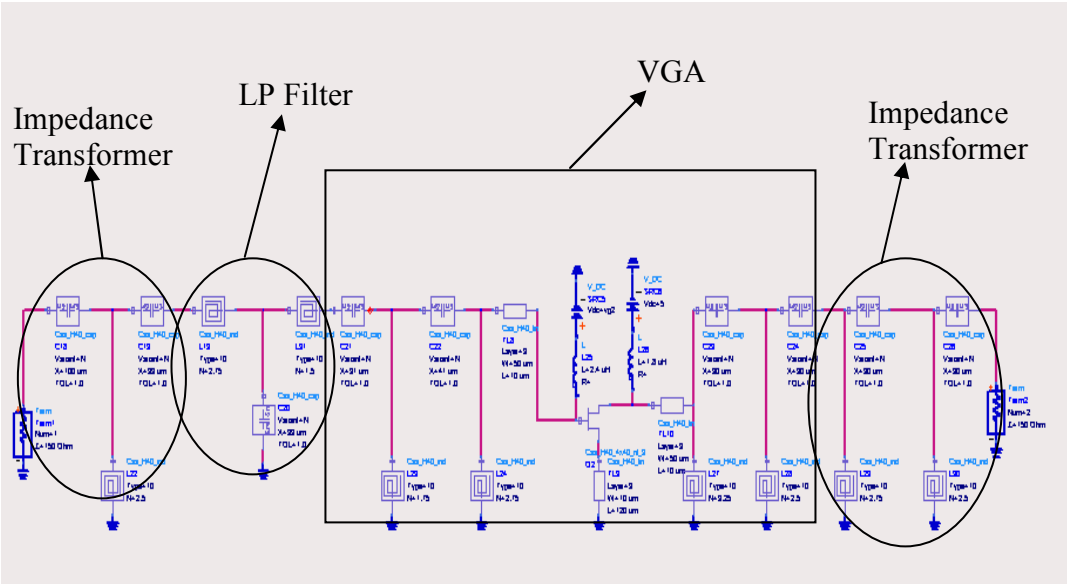

Figure 6.4 3rd channel's circuit diagram

Table 6.3 Element values obtained after the optimization for the third channel

Element	Element Value	Element	Element Value
L_{22}	2.75 turn	L_{26}	1.8 uH
C_{18}	X=100 um Type N	C_{24}	X=82 um Type P
L_{19}	2.75 turn	L_{27}	2.25 turn
C_{19}	X=100 um Type N	C_{25}	X=30 um Type N
L_{31}	1.5 turn	L_{28}	2 turn
C_{20}	X=33 um Type N	C_{26}	X=30 um Type N
L_{23}	2.25 turn	L_{29}	2.75 turn
C_{21}	X=30 um Type N	L_{30}	3 turn
L_{24}	2 turn	TL_8	W= 50 um L=10 um
C_{22}	X=38 um Type N	TL_9	W= 15 um L=120 um
L_{25}	2.4 uH	TL_{10}	W= 50 um L=10 um
C_{23}	X=71 um Type P		
SRC5	5 V, DC		
SRC6	Sweep between (-1.5) to (+0.5) V, DC		

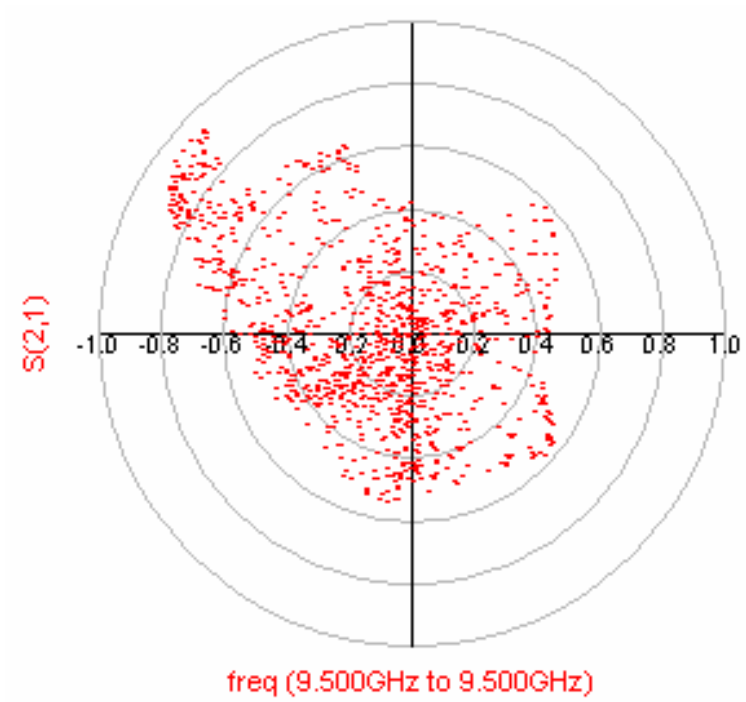

Figure 6.5 Insertion loss of the vector modulator in polar coordinate at 9.5 GHz (Dynamic Range of -48dB to 0 dB)

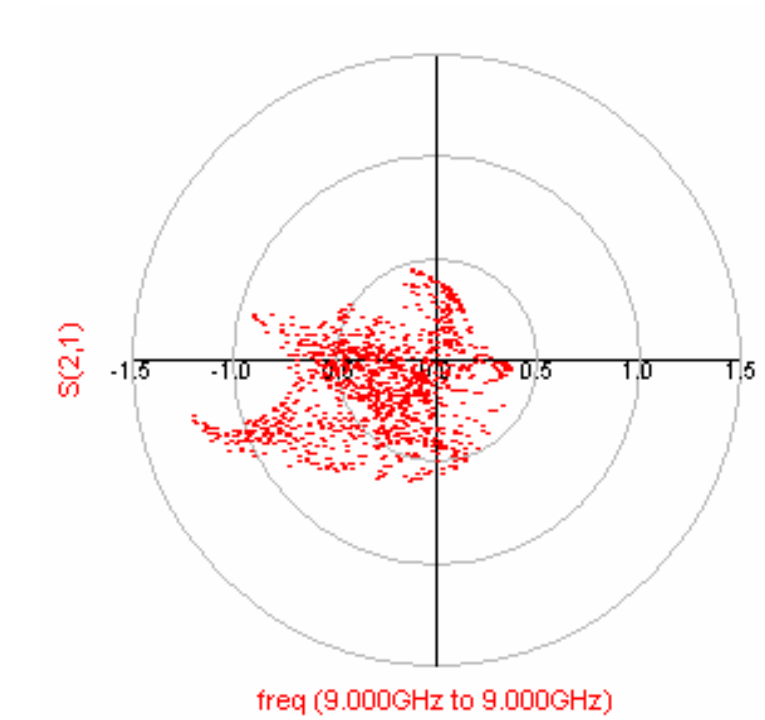

Figure 6.6 Insertion loss of the vector modulator in polar coordinate at 9 GHz (Dynamic Range of -45dB to 3 dB)

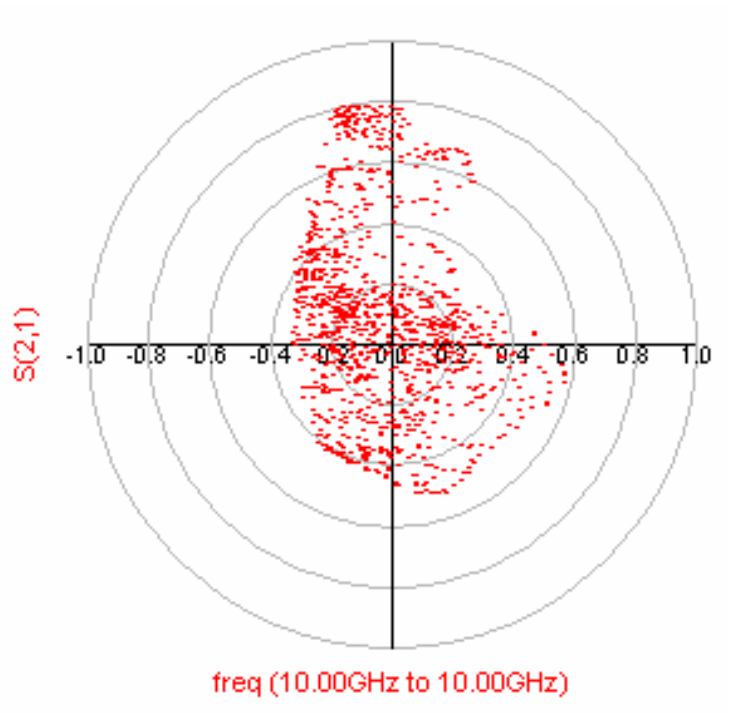

Figure 6.7 Insertion loss of the vector modulator in polar coordinate at 10 GHz (Dynamic Range of -38dB to -2 dB)

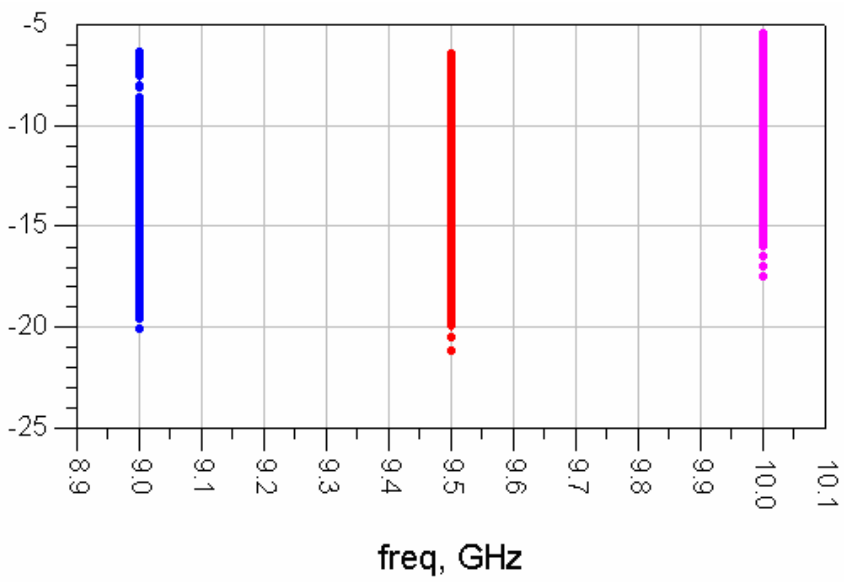

Figure 6.8 Input return loss of the vector modulator in Cartesian coordinate at 9GHz, 9.5GHz and 10 GHz

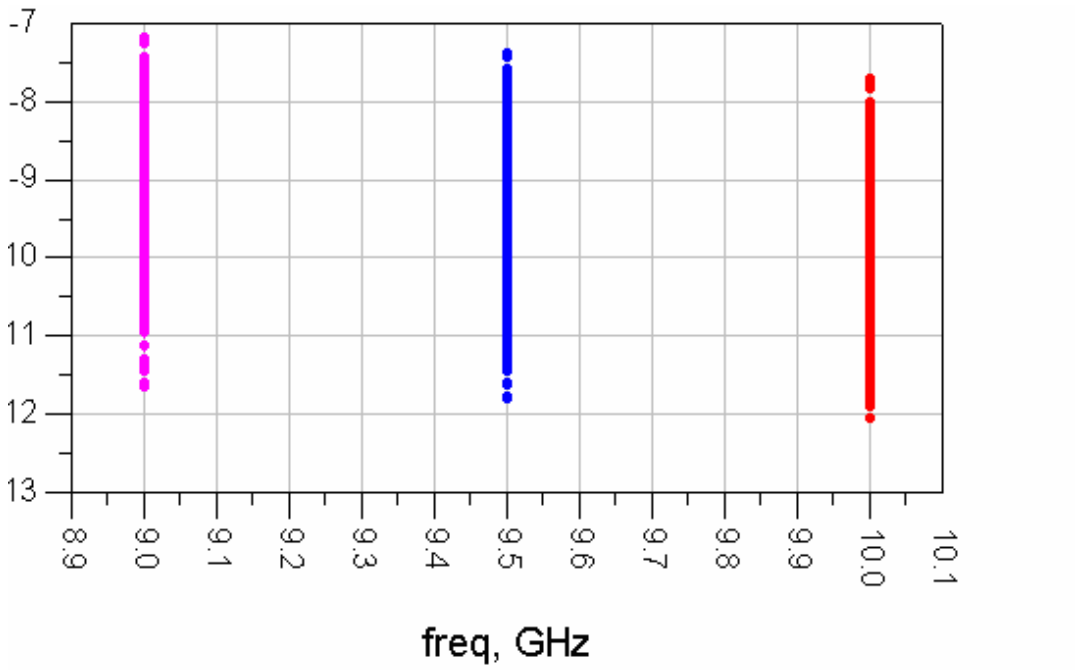

Figure 6.9 Output return loss of the vector modulator in Cartesian coordinate at 9GHz, 9.5GHz and 10 GHz

6.2 Layout

In this section, the layout of the MMIC vector modulator is drawn and simulated. Simulations were done by the ADS (Advanced Design System) simulation and optimization software. The following figures represent the simulation results of the final structure with layout. Since the schematic of the full circuit is very large, I only give the schematic of the 1st channel. Other channel's schematics are almost in the same format of the first channel.

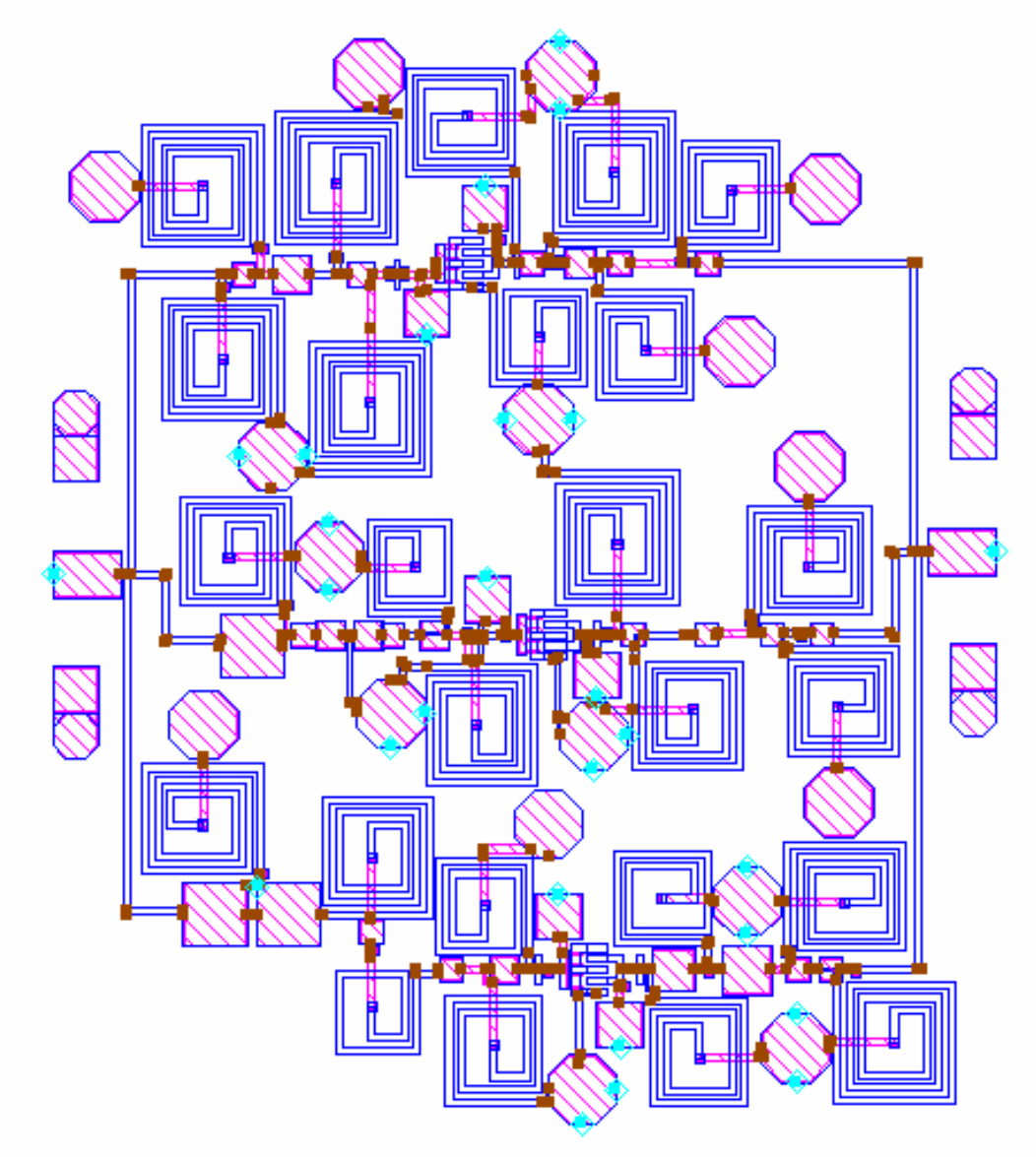

Figure 6.10 Layout of the final MMIC Vector Modulator

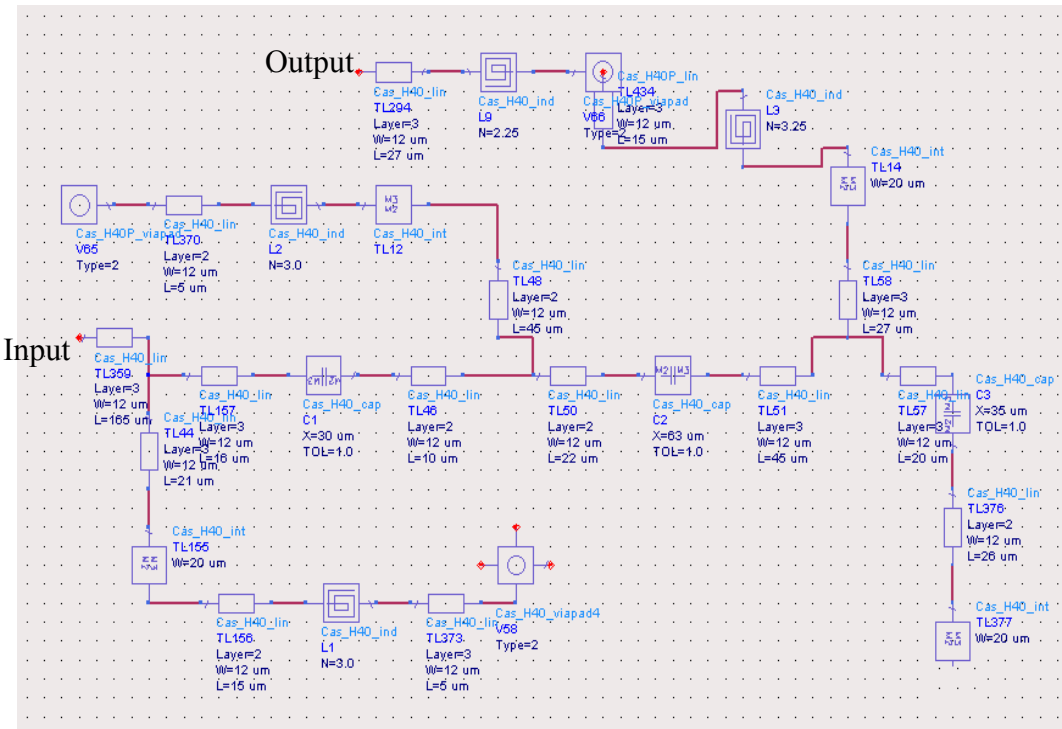

Figure 6.11 Schematic of the 1st channel's layout

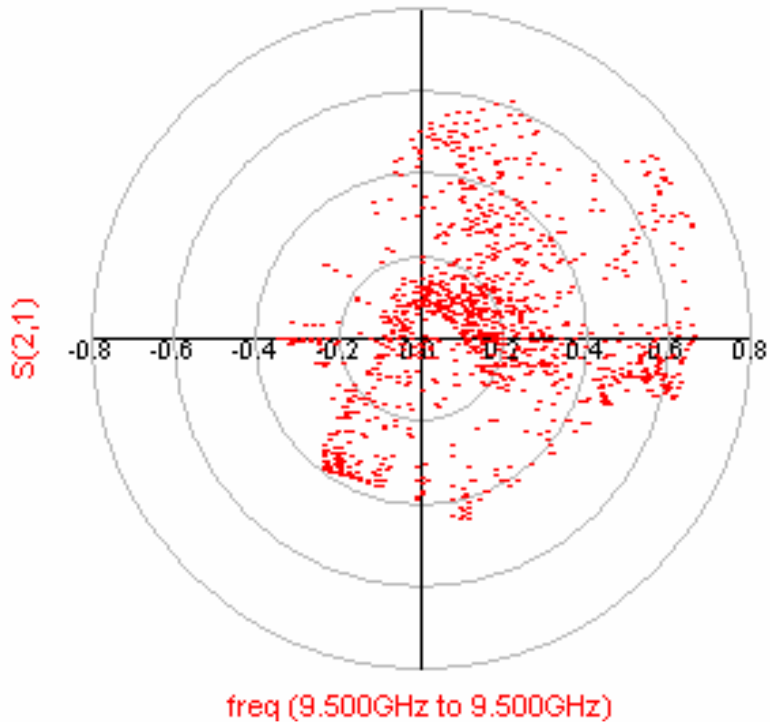

Figure 6.12 Insertion loss of the vector modulator in polar coordinate at 9.5 GHz

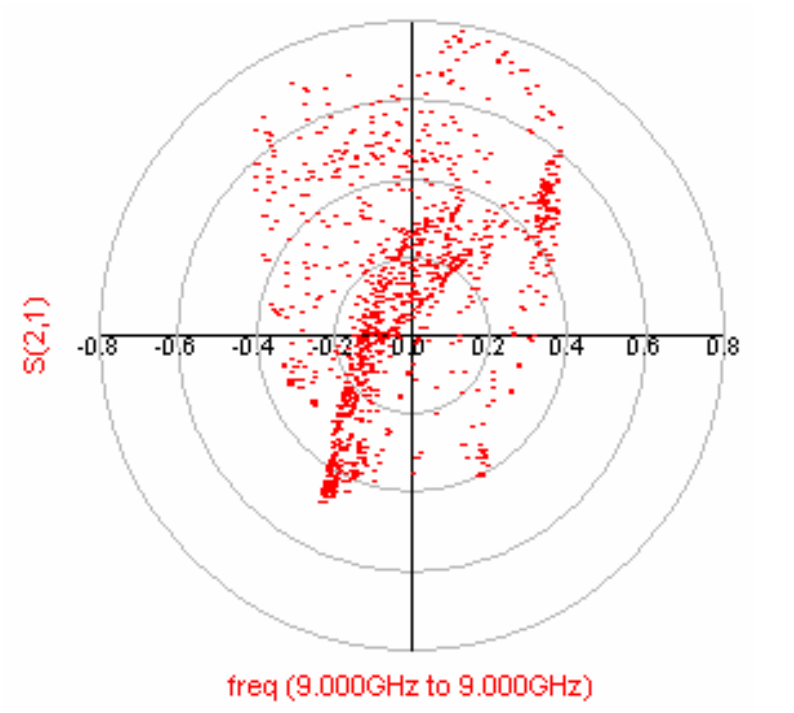

Figure 6.13 Insertion loss of the vector modulator in polar coordinate at 9 GHz

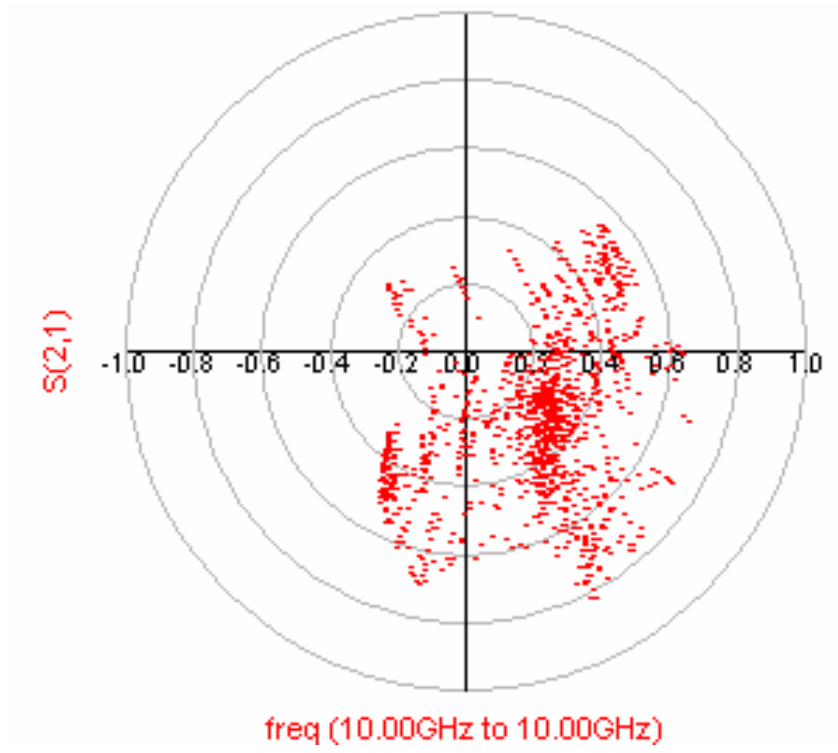

Figure 6.14 Insertion loss of the vector modulator in polar coordinate at 10 GHz

As can be seen from the figures our vector modulator operates well in the 9-10GHz bandwidth. For ease of operation gate voltages of the variable gain amplifiers were swept between (-1.5) to (0.5) V with 125 mV steps.

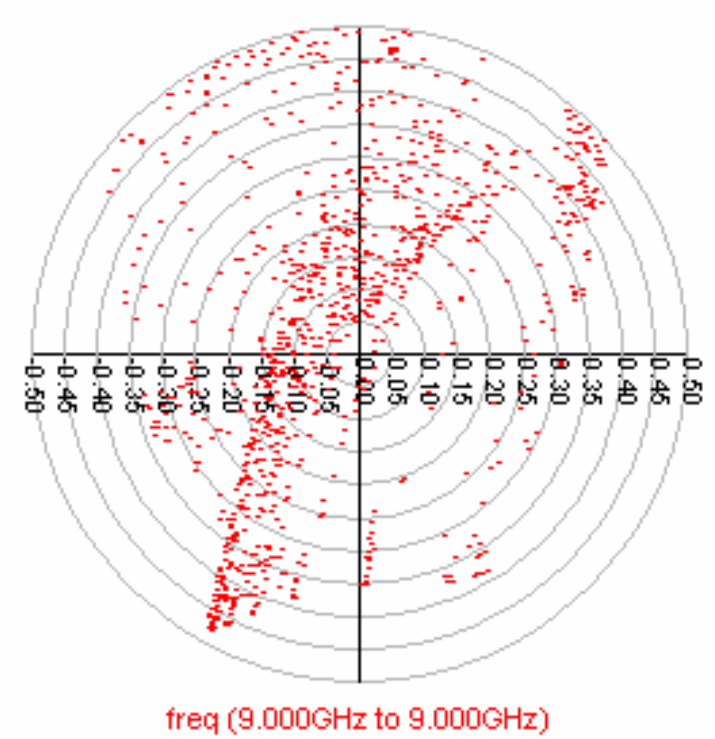

Figure 6.15 Dynamic range of the vector modulator in polar coordinate at 9 GHz (0.04 (-28dB) to 0.4(-8dB))

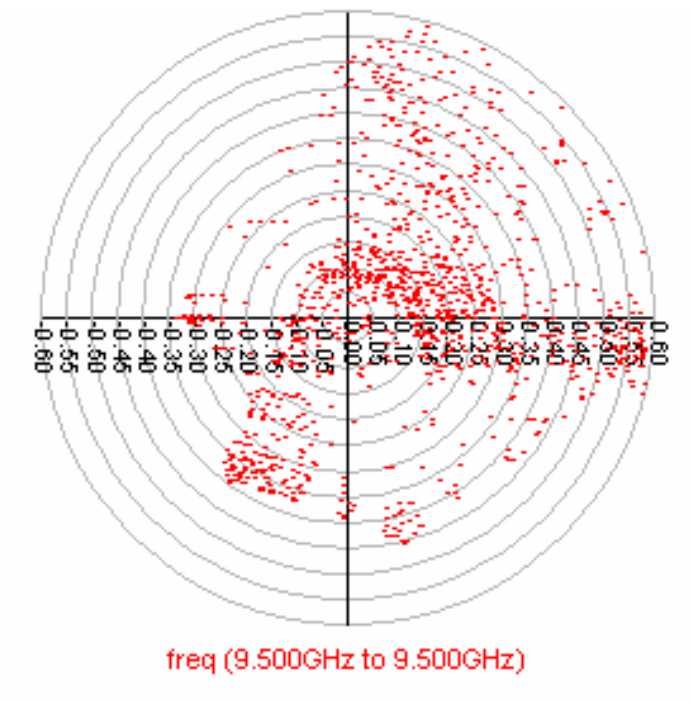

Figure 6.16 Dynamic range of the vector modulator in polar coordinate at 9.5 GHz (0.04 (-28dB) to 0.5(-6dB))

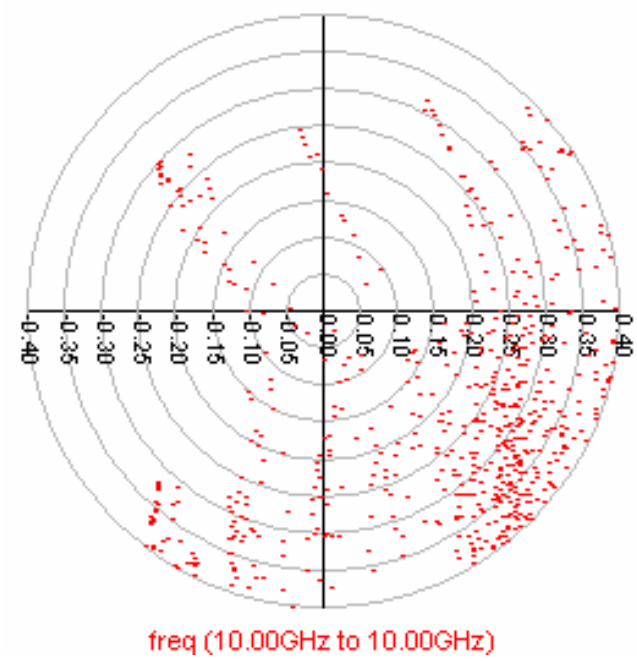

Figure 6.17 Dynamic range of the vector modulator in polar coordinate at 10 GHz (0.05 (-26dB) to 0.35(-9dB))

Table 6.4 Some Amplitude and Phase values for different control voltages at 9.5 GHz.

Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase	Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase
-1,38	-1,38	-1,00	-14,11	-178,76	-1,00	0,50	-0,75	-13,18	10,04
-1,13	-1,25	-0,13	-13,23	-174,81	-1,00	0,50	-0,38	-14,12	15,37
-1,13	-1,25	-0,75	-13,48	-172,41	-0,50	-0,25	0,25	-14,04	20,04
-1,13	-1,38	0,13	-13,49	-164,80	-1,00	0,38	-0,50	-14,10	25,14
-1,13	-1,38	-0,88	-14,05	-160,91	0,13	-0,13	0,13	-14,83	30,05
-1,00	-1,25	-0,25	-13,34	-150,14	-0,88	-0,13	-0,75	-13,27	35,17
-1,00	-1,25	-0,75	-13,73	-145,93	-1,13	0,50	-0,50	-14,55	40,28
0,38	-1,13	-0,25	-13,50	-139,77	-0,88	-0,13	-0,38	-13,50	45,09
-0,75	-1,13	-0,38	-13,88	-135,10	-1,25	0,50	-0,75	-13,56	50,47
0,25	-1,13	0,00	-13,79	-129,75	0,50	-0,25	0,00	-14,52	54,82
0,38	-1,13	0,13	-14,80	-125,41	-1,25	0,50	-0,50	-14,24	60,32
0,38	-1,13	-0,88	-14,55	-121,02	-1,38	0,50	-0,38	-13,70	65,03
-0,63	-1,13	0,13	-13,44	-115,53	-0,88	-0,63	-0,25	-14,03	69,65
-0,75	-1,13	-0,88	-14,64	-111,32	-0,88	-0,63	-0,50	-14,77	75,97
0,00	-1,13	0,38	-13,26	-106,00	-1,00	-0,88	-0,13	-13,53	80,13
-0,63	-1,13	0,38	-13,35	-99,96	-1,00	-0,88	-0,25	-13,76	85,02
0,38	-1,13	-1,00	-14,66	-95,85	-1,00	-0,88	-0,63	-14,55	88,42
-0,75	-1,13	0,50	-14,53	-87,42	-1,00	-0,88	-0,50	-14,19	91,11
-1,00	-1,50	-1,13	-14,47	-82,86	-1,13	-1,00	-0,75	-13,68	100,23
0,25	-1,00	-1,13	-13,26	-42,16	-1,25	-1,13	0,50	-14,76	112,64
0,38	-1,00	-1,13	-13,61	-37,55	-1,38	-1,13	0,50	-13,59	116,45
-0,25	0,50	-0,50	-14,41	-34,97	-1,25	-1,13	0,38	-14,17	119,15
-0,13	0,50	-0,75	-13,23	-30,73	-1,25	-1,13	0,25	-13,55	125,19
-0,25	0,38	-0,75	-14,23	-25,67	-1,38	-1,13	-0,88	-13,42	130,05
-0,50	0,38	-0,25	-14,60	-20,72	-1,13	-1,13	-0,38	-14,78	146,49

Table 6.4 (continued)

Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase	Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase
0,00	0,38	-0,13	-14,73	-15,67	-1,13	-1,13	-0,50	-14,56	148,27
0,13	0,38	0,00	-13,91	-10,28	-1,38	-1,25	0,50	-13,84	167,92
-0,63	0,25	-0,13	-14,80	-5,23	-1,25	-1,25	0,38	-13,99	170,88
-0,88	0,38	-0,75	-13,24	0,04	-1,25	-1,25	-0,88	-13,19	173,93
-0,13	-0,50	-1,00	-14,83	5,20					

Table 6.5 Some Amplitude and Phase values for different control voltages at 9 GHz.

Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase	Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase
-1,00	-1,00	-0,25	-14,22	-179,67	0,38	-0,75	-1,13	-14,69	39,95
-1,00	-1,00	-0,38	-14,47	-175,97	0,50	-0,75	-1,13	-14,16	44,68
-1,13	-1,25	0,50	-14,26	-169,00	-0,88	-0,88	-1,13	-13,20	46,64
-1,13	-1,25	0,38	-13,34	-165,77	-0,50	0,50	-0,63	-13,55	55,48
-1,00	-1,13	0,00	-13,62	-161,59	-0,75	-0,13	-1,00	-13,30	60,05
-1,13	-1,38	0,50	-13,98	-154,84	0,50	0,25	-0,88	-13,54	65,11
-0,88	-1,00	-0,13	-14,21	-150,96	-0,75	0,38	-0,25	-13,42	70,15
0,50	-0,88	-0,25	-13,56	-145,04	-0,88	-0,13	-0,88	-13,85	74,82
0,00	-0,88	0,13	-13,77	-140,02	-0,88	0,00	-0,75	-14,84	78,26
-0,50	-0,63	-0,50	-13,63	-134,60	-0,88	0,13	-0,38	-14,27	85,06
0,50	-1,13	0,38	-13,96	-130,04	-1,00	-0,88	-1,00	-14,58	90,39
-0,75	-1,13	0,38	-13,77	-125,20	0,50	0,13	0,13	-13,25	94,89
0,25	-1,13	0,50	-14,09	-120,97	-0,25	-0,13	0,50	-14,22	99,95
-1,00	-1,38	-1,00	-13,59	-115,10	0,13	-0,25	0,50	-14,20	105,23
-1,00	-1,50	-1,00	-13,67	-113,73	0,38	-0,25	0,38	-13,78	110,17

Table 6.5 (continued)

Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase	Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase
0,38	-1,13	-1,00	-14,33	-105,39	0,50	-0,50	0,50	-13,95	114,94
-0,75	-1,13	-1,00	-14,49	-101,77	-1,00	-0,50	-0,63	-14,26	118,97
-0,88	-1,25	-1,13	-14,06	-79,42	-1,00	-0,50	-0,38	-13,21	124,49
0,00	-1,13	-1,13	-14,29	-70,20	-1,00	-0,63	-0,63	-14,84	128,82
-0,63	-1,13	-1,13	-14,57	-65,92	-1,00	-0,63	-0,50	-14,37	133,83
-1,00	-1,38	-1,25	-14,31	-49,27	-1,00	-1,00	0,38	-13,66	141,07
-1,00	-1,50	-1,25	-14,16	-47,22	-1,00	-0,75	-0,38	-14,22	145,37
-1,00	-1,50	-1,38	-13,18	-40,20	-1,00	-1,00	0,25	-14,00	151,31
-1,00	-1,50	-1,50	-13,21	-38,85	-1,00	-0,88	-0,13	-13,61	154,32
-1,00	-1,25	-1,50	-14,32	-25,25	-1,00	-1,00	0,13	-14,06	160,60
0,50	-1,13	-1,25	-13,19	-19,50	-1,00	-1,00	0,00	-14,08	168,62
-1,00	-1,13	-1,25	-13,36	25,92	-1,00	-1,00	-0,13	-14,10	175,25
-0,50	-0,63	-1,13	-14,40	30,83	-1,13	-1,13	-0,75	-13,40	179,92
-0,63	-0,63	-1,13	-13,59	34,99					

Table 6.6 Some Amplitude and Phase values for different control voltages at 10 GHz.

Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase	Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase
-1,00	-1,38	0,13	-14,76	-119,87	0,13	-0,75	0,13	-13,53	-30,22
-1,00	-1,38	0,25	-14,07	-115,92	0,25	-0,75	-0,88	-13,58	-25,06
-1,00	-1,50	0,38	-13,25	-111,51	-1,00	-1,00	0,13	-13,65	-19,64
-1,00	-1,25	0,38	-14,09	-105,45	-1,00	-1,00	0,00	-14,02	-14,34
-1,00	-1,25	0,50	-13,30	-102,40	0,50	-0,75	-0,88	-13,40	-10,18
-0,25	-1,00	-0,38	-13,33	-91,89	0,25	-0,75	-0,63	-14,68	-5,04

Table 6.6 (continued)

Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase	Vg3 (Volt)	Vg2 (Volt)	Vg (Volt)	A (dB)	Phase
0,00	-1,00	0,00	-13,62	-90,28	0,38	-0,75	-0,25	-14,12	0,53
0,13	-1,00	-0,88	-13,58	-86,31	0,38	-0,75	-0,50	-14,24	4,96
0,25	-1,00	0,25	-14,09	-84,09	0,50	-0,75	-0,38	-13,77	9,88
0,38	-1,00	0,38	-14,05	-79,64	0,50	-0,75	-0,50	-13,79	11,79
0,50	-1,00	0,50	-13,99	-75,18	-1,13	-1,00	-0,88	-13,24	20,81
-0,75	-1,00	-0,50	-13,32	-70,73	-1,25	-1,13	0,00	-14,34	89,92
-0,38	-0,88	-0,75	-13,40	-65,47	-1,50	-1,13	0,13	-13,49	94,38
-0,50	-0,88	-0,50	-13,81	-60,06	-1,25	-1,25	-0,75	-13,43	132,00
-0,63	-0,88	-0,50	-13,28	-55,41	-1,25	-1,25	0,13	-13,93	135,76
-0,88	-1,00	-0,13	-13,58	-50,89	-1,50	-1,25	0,50	-14,32	140,49
-0,88	-1,00	-0,50	-14,53	-45,05	-1,25	-1,50	-0,88	-14,01	145,29
-0,38	-0,75	-0,63	-13,54	-40,15	-1,25	-1,38	0,38	-14,25	150,07
-0,25	-0,75	-0,50	-14,21	-35,14					

In above tables for a +/- 0.8 dB amplitude ripple and constant frequency, control voltages versus phase values are given. For 10 GHz, since the control voltage resolution is high (125mV), some phase values could not be obtained.

By looking at the figures and tables we can easily comment that vector modulator's insertion loss has at least 15 dB dynamic range. Since the step voltage is very high, 125 mV, we can not see full 360 degrees coverage for some amplitude values. However, if we change the step voltage to lower values, it is possible to see full 360 degrees coverage for all amplitude values. Furthermore, layout has a dimension of (1.6mm*1.9mm=3.04mm^2) which is quite small for a MMIC application.

6.2.1 Coupling Effects of the Layout

Since the coupling effects can not be included into the simulation, in this section coupling effects are investigated. Firstly, the CW (clockwise turn) inductors are put closer and the couplings are examined and these are done for a CW and a CCW (counter-clock wise) inductor and the worst case inductor settlement of my layout. Furthermore, effects of closer transmission lines are investigated

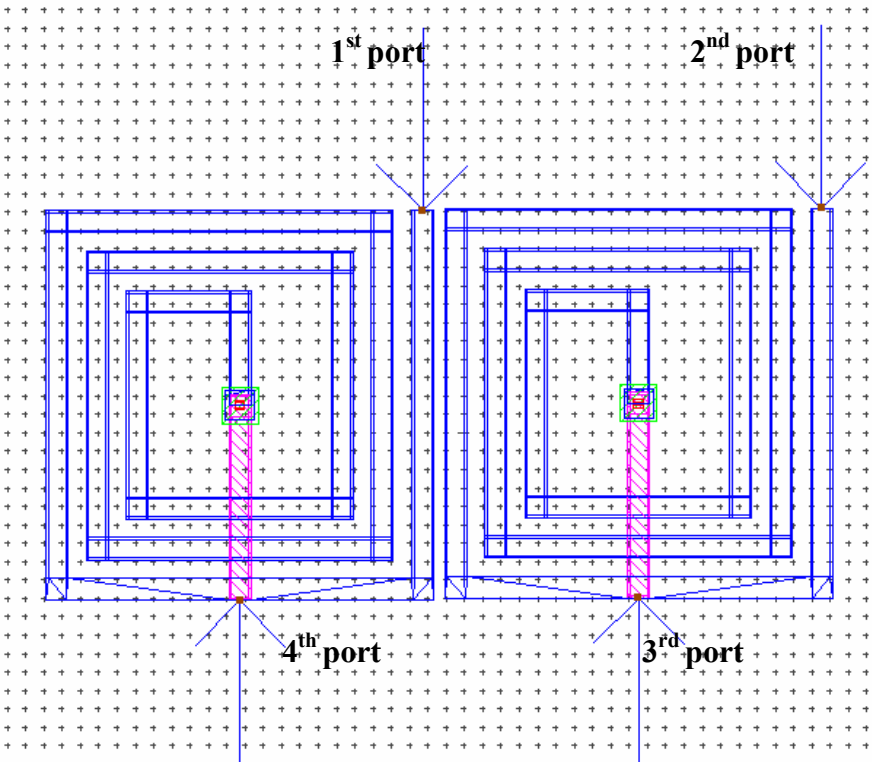

Figure 6.18 Layout of three turn CW inductors

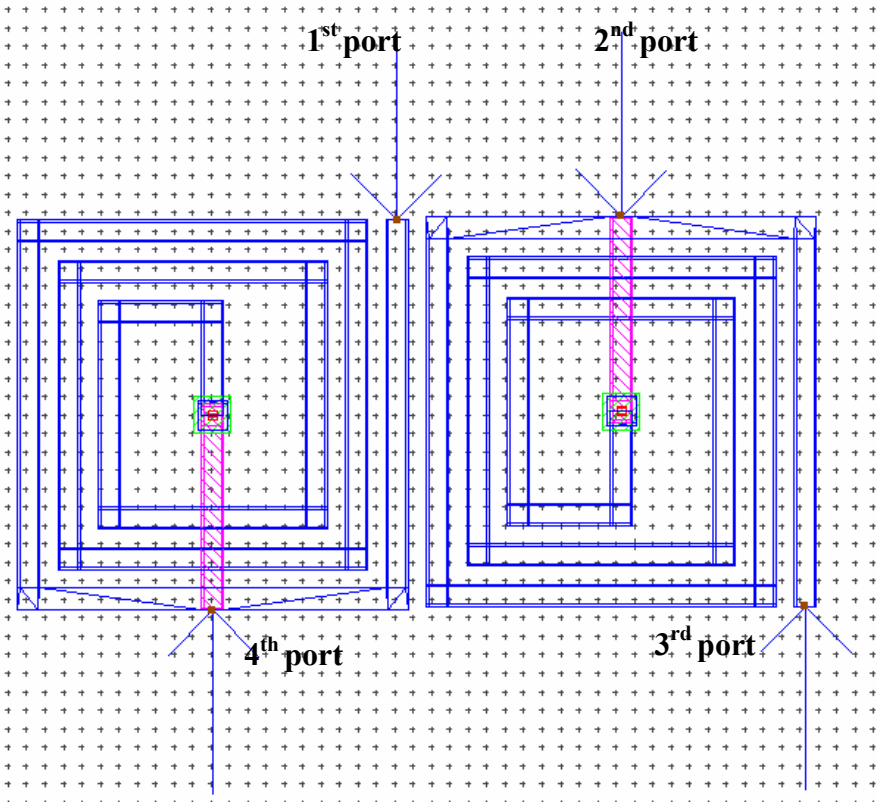

Figure 6.19 Layout of three turn CW and CCW inductor

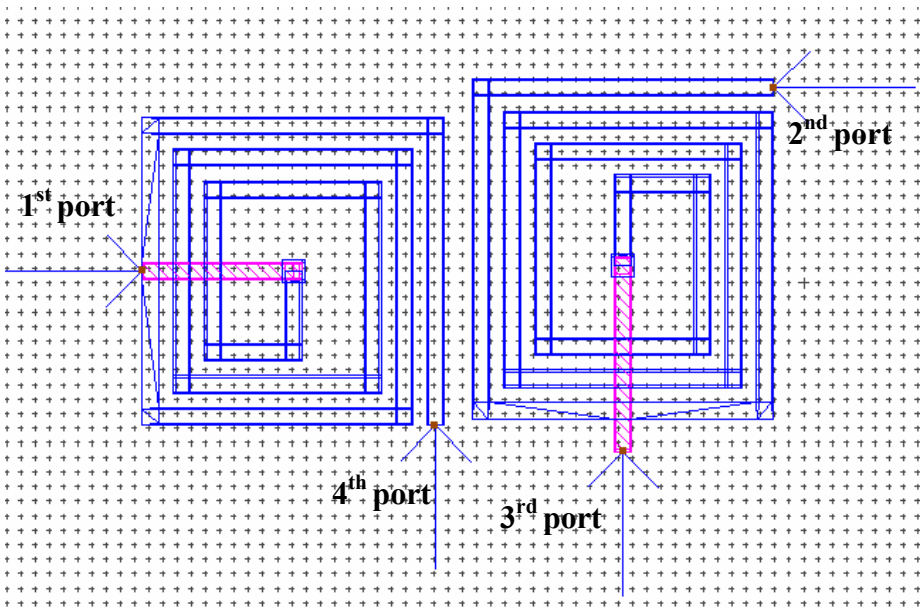

Figure 6.20 Layout of the worst case inductor settlement of the layout

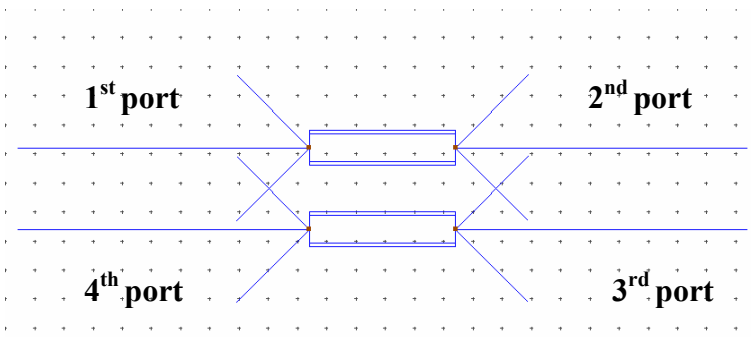

Figure 6.21 Layout of 12 um height, 50 um length, 16 um distant transmission lines

For the first case (figure 6.18), coupling of first port to second port is -15dB and the coupling of the first port to the third port is -25dB. The distance between the first and the second port is 215 um and the distance between the first port and the third port is 242 um. For the second case (figure 6.19), coupling of the first port to the second port is -22dB and the coupling of first port to third port is -30dB. The distance between the first and the second port is 117 um and the distance between the first port and the third port is 306 um. For the third case (figure 6.20), coupling of the first port to the second port is -23dB and the coupling of the first port to the third port is -31dB. The distance between the first and the second port is 445 um and the distance between the first port and the third port is 350 um. For the transmission line case (figure 6.21), the coupling of the first port to the fourth port is -38dB and the coupling of first port to third port is -42dB. Therefore, we may conclude that couplings are very small, because of this, ignoring the coupling effects are acceptable.

CHAPTER 7

CONCLUSION

Throughout this thesis, a MMIC vector modulator structure operating in the 9GHz-10GHz band was designed by using CASWELL H-40 models. Firstly, a research on the MMIC and vector modulator technology was done, secondly lumped element simulations and optimizations were accomplished by using Advanced Design System (ADS) and Microwave Office, lastly lumped element structure was replaced with CASWELL H-40 model and after that, layout was drawn. CASWELL H-40 structure was optimized and tuned in order to achieve a better performance.

The aim of the thesis was to realize the MMIC vector modulator structure. We found a proper MMIC foundry for ADS, therefore all the simulations and optimizations were done by the help of ADS tool. However, the foundry was closed its MMIC department during our design. Because of this, realization of the final design could not be achieved.

The first part of the design is a 4-port (4.8dB) 120^0 phase shift relative to the dedicated port power splitter. The main purpose of the power splitter section is to divide the input signals into 3 equal phase and equal amplitude signals. We used lumped elements method for these parts in order to achieve MMIC approach. There are high-pass and low-pass structures in the circuit. The circuit is composed of three channels. Also an impedance transformer was used to obtain 150 ohm at the input of each channel in order to achieve 50 ohm at the input port of the vector modulator.

The next section in the vector modulator structure is the variable gain amplifier. By the help of 4-port 120^0 phase shift relative to the dedicated port power splitter, we made a phase shift in every channel. The main purpose of this section is to change the amplitude of each channel in order to achieve an amplitude shift in each channel. The amplifier used in our vector modulator is in a completely digitally controlled MMIC structure and it has 12 dB dynamic range which is good enough to achieve amplitude shift in each channel.

The last section of the MMIC vector modulator is a 4-port (4.8 dB) in phase power combiner. The power splitter designed in chapter two can also be used as a power combiner by taking its mirror image. However, optimization was done in order get good matching. The in phase power combiner was used after the variable gain amplifier section. Realizing the MMIC structure with lumped elements is much easier than realizing it with distributed elements. Therefore, we again used lumped elements in the design. Furthermore, for wide band match we used forth order high pass impedance transformer.

Having designed all sections of vector modulator, we had to replace the lumped elements with CASWELL H-40 model in order achieve a MMIC structure. The Final circuit is simulated and it was seen that optimization (tuning) was needed. Therefore all the circuit elements were optimized (tuned). After that, the layout of the finalized circuit was drawn. Final layout has a dimension of ($1.6mm*1.9mm=3.04mm^2$) which is quite small for a MMIC application.

In the layout simulations, coupling effects can be included into the simulation; therefore coupling effects were examined separately. The results of the coupling effects were small enough to be ignored. Furthermore, throughout this thesis, choke inductances were 1.8uH and 2uH. However, if those are replaced with 10nH, the total performance of the circuit is not affected.

The aim of this thesis was to realize a MMIC vector modulator operating between 9GHz-10GHz. All the sections of the vector modulator were designed with lumped

elements and afterwards they were replaced with CASWELL H-40 model in order achieve a MMIC structure. By looking at the figures and tables we can easily comment that vector modulator's insertion loss has at least 15 dB dynamic range. Since the step voltage is very high, 125 mV, we can not see full 360 degrees coverage for some amplitude values. If we change the step voltage to lower values, it is possible to see full 360 degrees coverage for all amplitude values. However, simulating the circuit with lower step voltages (like 10mV) is very difficult; we could only give the simulation results of the step voltage of 125mV.

In conclusion, this thesis generally gives us the necessary information and experience to design and realize a vector modulator using MMIC technology. Furthermore, this development study can be a reference to implement overall vector modulator structure by the aid of a MMIC foundry as a future work.

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