CMOS CLASS E POWER AMPLIFIER MODELLING AND DESIGN INCLUDING CHANNEL RESISTANCE EFFECTS

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İBRAHİM DEMİR

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_____

Prof. Dr. Canan Özgen
Director

I certify that this thesis satisfies all the requirements as a thesis for the degree of Master of Science.

_____

Prof. Dr. İsmet Erkmen
Head of Department

This is to certify that we have read this thesis and that in our opinion it is fully adequate, in scope and quality, as a thesis for the degree of Master of Science.

_____	_____
Prof. Dr. Canan TOKER Co-Supervisor	Assist. Prof. Dr. Şimşek DEMİR Supervisor

Examining Committee Members

Prof. Dr. Altunkan HIZAL	(METU,EE)	_____
Assist. Prof. Dr. Şimşek DEMİR	(METU,EE)	_____
Prof. Dr. Canan TOKER	(METU,EE)	_____
Prof. Dr. Murat AŞKAR	(METU,EE)	_____
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İbrahim Demir

ABSTRACT

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DEMİR, İbrahim

M.S., Department of Electrical and Electronics Engineering
Supervisor : Assist. Prof. Dr. Şimşek DEMİR
Co-Supervisor : Prof. Dr. Canan TOKER

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CMOS is the favorite candidate process for the high integration of the wireless communication IC blocks, RF frontend and digital baseband circuitry. Also the design of the RF power amplifier stage is the one of the most important part of the RF CMOS circuit design. Since high frequency and high power simultaneously exists on this stage, devices works on the limits of the process. Therefore standard device models may not be valid enough for a successful design. In the thesis high frequency passive device and MOS transistor models for the CMOS process searched though the literature and presented. Besides, different structures of the inductors are investigated for the best quality factor for the chosen process.

Class E power amplifiers can reach very high efficiencies and they are very suitable for the low power applications. After the derivation of the classical Class E equations is presented, a new Class E circuit model including MOS transistor's channel resistance is developed and new sets of equations are obtained for the model. Circuit parameters are determined using numerical methods. Class E circuit simulations with these new parameters and earlier parameters are compared.

Finally, a 100mW 2.4GHz Class E power amplifier is designed and simulated targeting Bluetooth applications. In this design, Class E circuit parameters are determined for AMS CMOS 0.35um process MOS transistor including the channel resistance. Simulations are performed using Cadence/BSIM3v3 and OrCad PSPICE.

Keywords: Class E Amplifier, Power Amplifier, RF CMOS, Modeling, Channel Resistance Effects

ÖZ

CMOS E-SINIFI GÜÇ YÜKSELTECİNİN KANAL DİRENÇ ETKİLERİNİ İÇEREN MODELLEMESİ VE TASARIMI

DEMİR, İbrahim

Yüksek Lisans,Elektrik ve Elektronik Mühendisliği Bölümü
Tez Yöneticisi : Yar.Doç. Dr. Şimşek DEMİR
Ortak Tez Yöneticisi : Prof. Dr. Canan TOKER

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CMOS süreci, radyo frekansı ön uç ve sayısal temel band devreleri gibi kablosuz haberleşme tümdevre birimlerinin bileştirilmesi için en uygun adaydır. Radyo frekansı güç yülselteç katı tasarımı ise RF CMOS tümdevre tasarımındaki en önemli kısımlardan biridir. Bu katta hem yüksek frekans hem de yüksek güç bir arada bulunduğundan, devre elemanları kullanılan sürecin limitlerinde çalışırlar. Bu nedenden standart modeler başarılı bir tasarım için yeterli olmayabilir. CMOS süreci için yüksek frekansta pasif eleman ve MOS transistor modelleri araştırıldı ve toplandı. Ayrıca seçilen süreçde en uygun kalite faktörü için değişik bobin yapıları incelendi.

E sınıfı güç yükselticileri çok yüksek verimlilikte çalışabilirler ve düşük güç uygulamaları için çok uygundurlar. Bu tezde klasik E sınıfı güç yükselteçlerinin literatürde yer alan denklemlerinin çıkarılması verildikten sonra MOS transistörünün kanal direncini de içeren yeni bir model geliştrildi ve bir denklem seti elde edildi. Devre elemanlarının değerleri numerik yöntemler kullanılarak hesaplandı. Yeni değerlerle ve eski değerlerle yapılan simulasyonlar karşılaştırıldı.

Son olarak MOS transistor kanal direncini hesaba katan bu yeni yöntem kullanılarak, Bluetooth uygulamalarına yönelik 100mW 2.4GHz E sınıfı bir güç yükselteci AMS CMOS 0.35um süreci kullanılarak tasarlandı ve similasyonu gerçekleştirildi. Similasyonlarda Cadence/BSIM3v3 ve OrCad PSPICE programları kullanıldı.

Anahtar Kelimeler: E Sınıfı Güç Yükselteci, Güç Yükselteci, RF CMOS, Modelleme, Kanal Direnç Etkileri

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CHAPTER 1

INTRODUCTION

1.1 Scope and Objective

There is an increasing demand for the higher integration of wireless communication ICs in sake of small size, low cost and low power consumption. A complete communication system requires the use of both analog RF front end and digital baseband circuitry. These two parts must be manufactured in the same process for a complete integration. As the requirements of the communication systems increases digital parts of the wireless systems get more and more complicated, and therefore get bigger in size. Most suitable technology for the manufacturing of the very large-scale digital circuits is CMOS, since it is low cost, widespread, well known and industry's de-facto standard for digital circuits. For the very high speed RF circuitry most suitable processes are GaAs and Si-bipolar processes. However these processes are very expensive for the manufacturing of the very large-scale digital circuits. On the other hand as the scaling of the CMOS process is improved, high frequency characteristics of the CMOS become suitable for the manufacturing of the high frequency RF circuits.[1] So, a complete communication system can be integrated into same chip using CMOS process.

However standard models of the CMOS devices may not be valid for very high speed circuits. Not only parasitic resistance, inductance and capacitance effects considerably increase at very high frequencies but also high speed effects arise in the semiconductor devices. For a realistic simulation of the CMOS operation at high frequencies device models must be improved. These improved models are used to simulate the circuit operation and design can be verified before manufacturing. This

helps to decrease the number of the prototype chips and the initial cost of the manufacturing. There are many models in the literature for increasing the valid frequency region of the CMOS device models. Most of them add extrinsic components to a base model to develop a new model. Values of these extrinsic components are obtained by parameter extraction methods [2-10].

Class-E power amplifies are firstly introduced by Sokals [11] in 1975. Theoretically they offer %100 efficiency. They are commonly used for high efficiency applications, because they have simple circuit topology, are easy to implement and are not very sensitive to changes to component values. In 1977 Raab presented the derivation of the circuit equations based on the infinite quality factor assumption [12]. Even though a few exact analyses at any quality factor are published afterwards, previously presented design equations are preferred, because they make the design straightforward and valid enough for the obtainable quality factors.

In the derivation of the equations, channel resistance of the MOS transistor is assumed to be zero. However this resistance may not be so small especially for small sized transistors in low power applications. This resistance affects the operation of the circuit in two ways. Firstly it causes power dissipation when current is flowing through the device. Secondly it causes the Class-E amplifier to be miss-tuned, decreasing the efficiency of the amplifier. First effect cannot be avoided but if the Class-E amplifier is tuned according to channel resistance, second effect can be suppressed.

1.2 Organization of the Thesis

In Chapter 2, properties of the RF CMOS technology are investigated and presented. High-speed characteristics of the MOS transistor together with the effects of the parasitic elements are discussed. Different models for better modeling MOS transistor at high frequencies are studied and compared.

In Chapter 3, reasons of the power dissipation in amplifies are discussed. The theory of the Class-E high efficiency operation of is given and the derivation of the

classical Class-E equations from the literature is presented. Potential sources of the power dissipation are discussed using more realistic Class-E circuit model.

In Chapter 4, derivation of the Class-E circuit equations taking into account the channel resistance is given. Solution is performed using a numerical method. Simulation results are compared with the classical equations. These simulations are performed by OrCad PSPICE.

In Chapter 5, a 100mW 2.4GHz Class-E power amplifier for AMS CMOS 0.35um process is designed using the method presented in chapter 4 and simulations are performed in Cadence/BSIM3v3 using MOS RF model.

In Chapter 6, obtained results are discussed and intended future works are presented. This the conclusion part of the thesis.

CHAPTER 2

RF CMOS TECHNOLOGY

2.1 Introduction

The scaling of CMOS has resulted in a strong improvement in the RF performance of MOS devices. Consequently, CMOS has become a viable option for analog RF applications and RF system-on-chip. Performance metrics such as cutoff frequency, maximum oscillation frequency, and minimum noise figure are very important for RF Analog circuit design [1].

First-order equations for the RF figure of merit such as the cutoff frequency f_t, the maximum oscillation frequency $f_{\max}$ based on the maximum available gain (MAG), minimum noise figure $NF_{\min}$, and third harmonic intercept voltage V_{IP3} are given below [1]

$$f_t = \frac{1}{2\pi} \cdot \frac{g_m}{C_{gg} + C_{par} + C_{gso} + C_{gdo}} \tag{2.1}$$

$$f_{\max} = \frac{f_t}{2\sqrt{(R_g + R_i)(g_{ds} + 2\pi f_t C_{gdo})}} \tag{2.2}$$

$$NF_{\min} = 1 + K \cdot \frac{f}{f_t} \sqrt{g_m (R_g + R_i + R_s)} \tag{2.3}$$

$$V_{IP3} = \sqrt{\frac{24 \cdot g_m}{g_{m3}}} \tag{2.4}$$

where g_m is the transconductance; g_{m3} is the third-order derivative of the drain current versus gate bias; and V_{IP3} is the extrapolated input voltage amplitude at which the first- and third-order output amplitudes are equal. The capacitances C_{gg}, C_{par}, C_{gso} and C_{gdo} are the intrinsic input capacitance, parasitic gate-bulk capacitance, and the gate-source and gate-drain overlap capacitances. R_g is the gate resistance and R_i is the real part of the input impedance due to non-quasistatic effects. R_s and g_{ds} are the source series resistance and output conductance. The above equations give an indication of the impact of technology parameters on the RF figure of merit. For linearity figure of merit V_{IP3} is used as a first-order parameter, a large V_{IP3} is required for high linearity. V_{IP3} is easily obtained from the dc characteristics. It gives a good indication of the device linearity even at high frequencies.

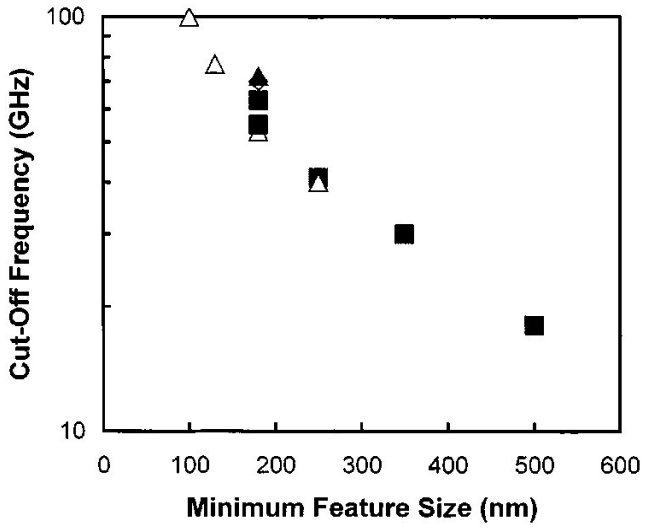


Figure 2-1 Measured f_t data versus nominal gate length[1]

Figure the measured maximum f_t of 350-nm, 250-nm, and 180-nm NMOS devices are plotted in Figure 2-1. The total device width was either 160um or 192 um. For the 180-nm technology f_t exceeds 60 GHz. A strong improvement with scaling is observed due to an increased g_m.

2.2 Passive Components

One of the most important parts of the RF circuits regarding its performance is the passive components. However, the CMOS technology process is mainly optimized to satisfy the demands of the digital electronics and therefore high quality passive components are relatively hard to obtain in CMOS especially at high frequencies. RF CMOS circuits have to be build using these limited set of passive components. Modeling of the passive devices becomes very important for the simulation accuracy.

Due to the parasitic effects, at some certain frequencies, capacitors may behave as inductors, inductors may behave as capacitors and resistors may behave as a little of both [9].

As an example for the limitations of the CMOS process, inductors larger than about 10nH consume significant die area and have relatively poor Q (typically below 10) and low self-resonant frequency. Capacitors with high Q and low temperature coefficient are available, but tolerances are relatively loose (e.g. order of 20% or worse). Additionally, the most area-efficient capacitors also tend to have high loss and poor voltage coefficients. Resistors with low self capacitance and temperature coefficient are hard to come by, and one must also occasionally contend with high voltage coefficients, loose tolerances, and a limited range of values [9].

2.2.1 Interconnects

Polysilicon or metal layers can be used for the interconnection of the integrated circuit. There may be more than one polysilicon or metal layers. Especially more metal layers are required if the integrated circuit is complicated. Main routing layer is generally metal layers, where polysilicon is used for short connections, since its resistance is much higher than metal layers'.

Various considerations exist for the interconnections, especially for high frequency operation. Most obvious ones are the parasitic capacitance and inductance of the interconnection lines. They are called parasitic since they are not intended. However similar structures can be used for building capacitors and inductors, which

are studied in depth in sections 2.2.3 and 2.2.4, respectively. So called parasitic capacitance and inductance of the interconnection lines can be calculated using the same equations.

Another high frequency effect is the "Skin Effect". It is effective on any type of conductors such as wires, capacitors, resistors, or inductors. A high frequency electromagnetic wave is attenuated very rapidly from the surface to the center of a good conductor. Fields and currents can be considered as confined in a very thin layer of the conductor surface. The depth into the conductor at which current density falls to e^{-1} or 0.368 of this value at the surface is called as "skin depth". Due to the skin depth effective cross section of the conductor is decreased and the ac resistance is increased.

$$\delta = \sqrt{\frac{2}{w \cdot \mu \cdot \sigma}} \tag{2.5}$$

where δ is the skin depth, w is the frequency, μ is the permeability and σ is the conductivity of the material.

For the CMOS process skin depth is on the order of sub millimeters for N-well, few tens of micrometers for poly and a few micrometers for metal layers. [9]

Current handling in metal lines is another issue. Maximum allowable dc current over an interconnection line is limited by the metal migration. Normally diffusion process is random, but with dc current, metal atoms are bombarded more from one side than from the other. This causes the movement of the metal atoms, which is referred to as metal migration. Sufficient movement in the metal can create gaps or open circuits appearing in metal and results in subsequent circuit failure. For 1μm thick aluminum, a typical value for maximum current would be 1 mA of dc current for every micrometer of metal width. The ac current component can be as larger as typically 4 times [9].

2.2.2 On Chip Resistors

There are many sources for resistors in CMOS technology; poly layer, diffusion areas, well areas, metal layers, even MOS transistors. Since the thickness is constant for the resistive materials, resistivity is given in terms of sheet resistance, R_{sh}.

$$R_{sh} = \frac{\sigma}{t} \tag{2.6}$$

and the resistance is calculated by multiplying the sheet resistance by the aspect ratio $\frac{L}{W}$.

$$R = R_{sh}\frac{L}{W} \tag{2.7}$$

Resistor dependence to temperature is modeled using temperature coefficients (TCR, TCR_2) and voltage dependence is modeled using voltage coefficient (VCR).

In pspice temperature dependence is modeled as

$$R(T) = R_{To}\left[1 + TCR.(T - T_0) + TCR_2(T - T_0)^2\right] \tag{2.8}$$

and voltage dependence is modeled as

$$R(V) = R_{V0}\left[1 + VCR.V\right] \tag{2.9}$$

2.2.2.1 Polysilicon Resistor

Interconnect material polysilicon is suitable for small valued resistances. It is more resistive than other interconnect metal layers, thus they occupy less space for the same valued resistances. However, most polysilicon layers these days are silicided specifically to reduce resistance. Resistivities tend to be in the vicinity of roughly 5-10 ohms per square [13], however it is 20-80 ohm per square in the unsilicided polysilicon [9].

Its tolerance is poor (35%), and temperature coefficient is typically in the neighborhood of 1000 ppm/°C. Despite their poor tolerance, poly resistors have low parasitic capacitance per unit area (due to oxide layer under the polysilicon) and lowest voltage coefficient of all the resistor materials available in a standard CMOS technology [9].

2.2.2.2 Diffused Resistor

Source/drain diffusion regions can be used as resistors in CMOS. The resistivities and temperature coefficients are generally similar to those of silicided polysilicon. There is also significant parasitic (junction) capacitance, which limits the useful frequency range of the resistor and a noticeable voltage coefficient, which limits the dynamic range of voltages that may be applied. Both terminals of the resistor must not be forward biased to the bulk.

2.2.2.3 Well Resistor

Lightly doped well regions can be used for high valued resistors. Their resistivity is in the rage of 1-10Kohm per square. Despite their high resistivity they suffer from high capacitance per square, poor initial tolerance (±50-80%), large temperature coefficient (typically 3000-5000 ppm/°C) and high voltage coefficient.

2.2.2.4 MOS Transistor Resistor

MOS transistor in linear region can be used as resistor since drain current changes linearly with respect to drain-source voltage. Channel resistance can be given as,

$$r_{ds} = \left[\mu C_{OX} \frac{W}{L} (V_{GS} - V_T - V_{DS}) \right]^{-1} \tag{2.10}$$

MOS transistor resistor can provide typically 5-10Kohm per square, but suffers from non-linearity, high temperature coefficient and loose tolerance due to the variations on threshold and mobility.

2.2.2.5 Metal Resistor

Metal layer can be used for small valued resistors, since its typical resistance value is 50 mohm per square. Aluminum has a temperature coefficient of about 3900 ppm/°C. Resistances up to 10 ohms are reasonable.

2.2.3 On Chip Capacitors

A general complicated model for the on chip capacitors is shown in Figure 2-2. This model includes all of the possible parasitic elements. C is the desired capacitance between terminals A and B. Rp represents the leakage in the capacitance's dielectric material. L and Rs are the parasitic inductance and resistance of the capacitance structure. Csub1 and Csub2 are the capacitance between the terminals and the substrate below the structure. However these capacitances are connected to bulk substrate via substrate resistance and capacitance.

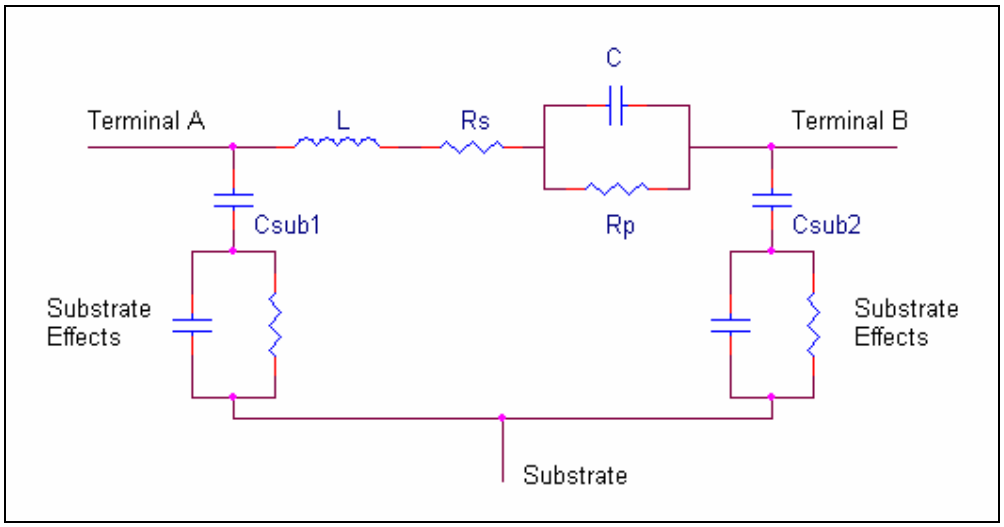


Figure 2-2 On chip capacitance model

Due to parasitic elements real capacitor's characteristics deviate from the ideal capacitor. At low frequencies Csub1 and Csub2 are open circuit and L is short circuit. Rs is a small and Rp is a large resistance. Real capacitor behaves like ideal capacitor. When the frequency is increased, effects of the parasitic elements start to dominate. Impedance of the inductance starts to increase. This decreases the effective capacitance seen at terminal. At some point inductance's impedance becomes equal

to the capacitance's impedance, after this point structure behaves more like an inductor. This frequency point is called as the resonance frequency of the capacitance.

Ideally capacitor only stores energy. But in reality due to parasitic resistances, some of the energy is dissipated. Quality factor of a capacitor is a measure of the capacitance's energy storage capacity over its energy dissipation. It is defined as the ratio of the net energy stored in the capacitor to energy lost in one ac cycle.

$$Q = 2\pi \frac{|Net\ energy\ stored\ in\ one\ ac\ cycle|}{Energy\ dissipated\ in\ one\ ac\ cycle} \quad (2.11)$$

It is required to note that the net energy stored in the whole structure is equal to difference between the net energy stored in the capacitance C and inductance L in one ac cycle. This is because energy stored in inductance L on one half ac cycle is transferred to capacitance C on the other half ac cycle. This means that since the net energy stored on the real capacitance decreases as the frequency increases and becomes zero at the resonance frequency, quality factor decreases with increasing frequency and becomes zero at the resonance frequency. So the resonance frequency can be defined as maximum usable frequency of the capacitance.

2.2.3.1 Parallel Plate Capacitor

Parallel plate capacitors are made of any parallel interconnection layers, metal-oxide-metal, metal-oxide-poly and poly-oxide-poly. Since the oxide between the layers is intentionally made thick (0.5-1μm) to reduce the parasitic capacitance between the interconnection line, capacitance per unit area is small (typically $5x10^{-5}$ pF/μm^2). Capacitance between the bottom plate and the substrate can be as large as 10-30% of the main capacitance and often severely limits circuit performance. Temperature coefficient of the metal-oxide-metal capacitors are quite low, usually in the range of 30-50 ppm/°C [9]. Parallel plate capacitors are highly linear but may be exposed to oxide break down when high voltages are applied. More capacitance per unit area can be obtained by using multiple layers.

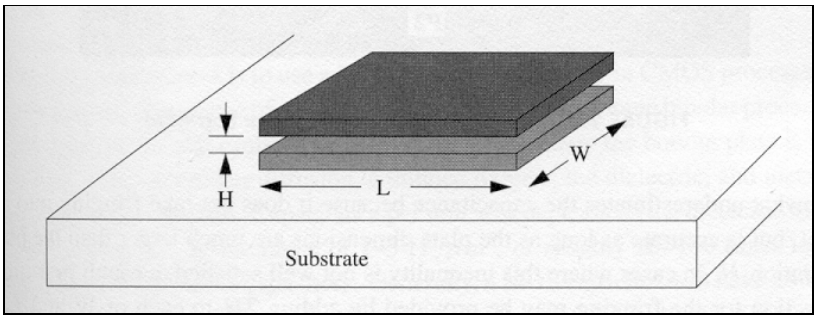


Figure 2-3 Parallel plate capacitor

$$C = \varepsilon \frac{W.L}{H} \tag{2.12}$$

Standard capacitance formula assumes uniform electric field between the parallel plates. But for the real structures electric field is not uniform at the edges of the parallel plates, fringing of the electric field occurs. In some cases this fringing electric field can be comparable to the uniform electric field in the middle of the conductors. In those cases standard capacitance formula can not be used. A rough first order correction for the fringing may be provided by adding 2H to each of W and L in computing the area of the planes [9].

$$C \approx \varepsilon \frac{(W+2H).(L+2H)}{H} \approx \varepsilon \left[\frac{WL}{H} + 2W + 2L \right] \tag{2.13}$$

This formula is adequate for most of the cases when $\frac{W}{H}$ ratio is high. But below values of about 2-3 (e.g. in case of capacitance of an interconnection line), fringing becomes more effective and capacitance error grows. Equation developed by v.d. Meijs and Fokkema can be used with an accuracy within 1%.

$$C \approx \varepsilon \left[\frac{W}{H} + 0.77 + 1.06 \left[\left(\frac{W}{H} \right)^{0.25} + \left(\frac{T}{H} \right)^{0.25} \right] \right] \cdot L \tag{2.14}$$

2.2.3.2 Lateral Capacitor

Lateral capacitors make use of the capacitance between two adjacent conductors and use the advantage of the scaling. Since the spacing between two

adjacent conductor decreases with the scaling, maximum obtainable capacitance per unit area increases with the scaling. However scaling does not change the thickness of the oxide, so the parallel plate capacitance.

Since the capacitance is proportional to length of the adjacent conductors, capacitance per unit area can be increased by using different geometries.

Figure 2-4 Figure shows the interdigitated lateral capacitance geometry. This geometry suffers from high parasitic inductance since currents are all in the same direction.

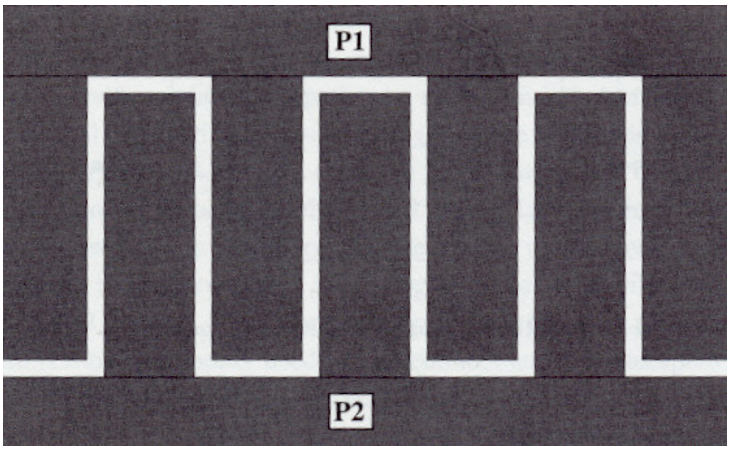


Figure 2-4 Interdigitated lateral capacitor

Fractals can enclose finite area with infinite perimeter. Because of photolithographic limitations, infinite perimeter is unattainable but large increases are possible. In certain cases, capacitance increases of a factor of 10 or more can be achieved. Fractals geometries have lower series inductance since currents are not in the same direction [9].

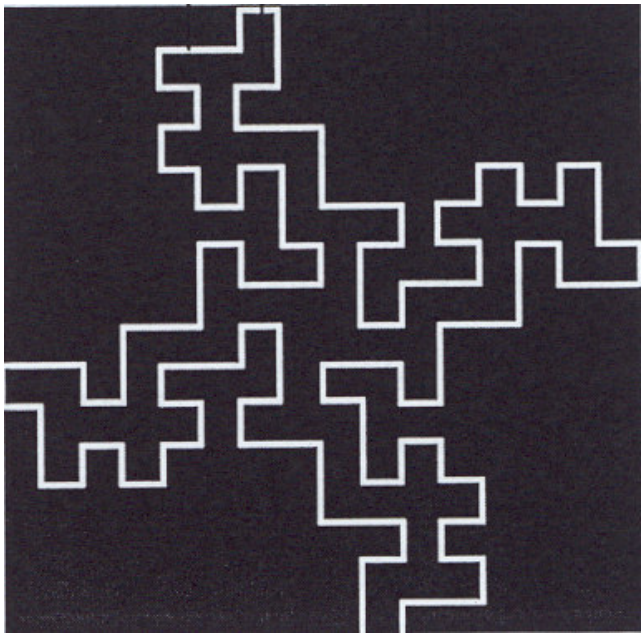


Figure 2-5 Fractal lateral capacitor

2.2.3.3 Gate (MOS) Capacitor

Gate to channel capacitance can be used as a useful capacitance. Since the oxide under the poly (gate) is thinner than the isolator oxide layer, higher capacitance per unit area can be obtained. Capacitance unit area is typically in the range of 1-5pF, 20-100 times larger than ordinary interconnect capacitors [9].

Channel must be on for the operation of the capacitor, therefore gate must be biased well above the threshold voltage. Otherwise the capacitance will be small, lossy and highly nonlinear. If accumulation type MOSFET is used there is no need to bias the capacitance since channel is on at zero bias level at the gate. Since channel is series to the capacitance effects the capacitance's Q. Series resistance can be taken quarter of the channel. In order to maximize the Q minimum length device must be used [13].

2.2.3.4 Junction Capacitors

P-N junction capacitance can be used as a useful capacitance as well. p+ region in an n-well forms a junction capacitance. This capacitance depends on the applied bias; therefore it is used in electrically tuned circuits. Capacitance is

$$C \approx \frac{C_{j0}}{(1 - V_F / \phi)^n} \quad (2.15)$$

where C_{j0} is the incremental capacitance at zero bias, V_F is the applied bias voltage across the junction, ϕ is the built in potential (typically several tenths of a volt, and n is a parameter that depends on the doping profile, which is typically 1/2.

Junction capacitances have large temperature coefficients in the range of 200 ppm/°C to 1000 ppm/°C. The Q of the junction capacitance is inversely proportional with the tuning range. Wider range results in smaller Q, narrower range results higher Q [9].

2.2.4 On Chip Inductors

On chip inductance model is given in Figure 2-6. This model includes many parasitic elements that may be effective in the characteristics of the on chip inductor. L is the desired inductance between the terminals A and B. Distributed resistance in the conductor of the inductor is modeled with series lumped resistance Rs. C is the capacitance between the windings of the inductor. Independent of the geometry of inductor, somehow windings reside on the substrate. Capacitances of the windings to the substrate are modeled with Csub1 and Csub2. These capacitances are not directly connected to bulk substrate but via substrate capacitance and resistance.

Due to the parasitic elements characteristics of the real inductor deviates from the ideal one at high frequencies, however characteristics are similar at low frequencies. This is due to most of the parasitic elements are effective at high frequencies and therefore limits the operation of the device. At low frequencies C, Csub1 and Csub2 are open circuit since their values are very small. There is only L and Rs left between the terminals. It should be mentioned that value of the Rs is frequency dependent as a result of the skin effect.

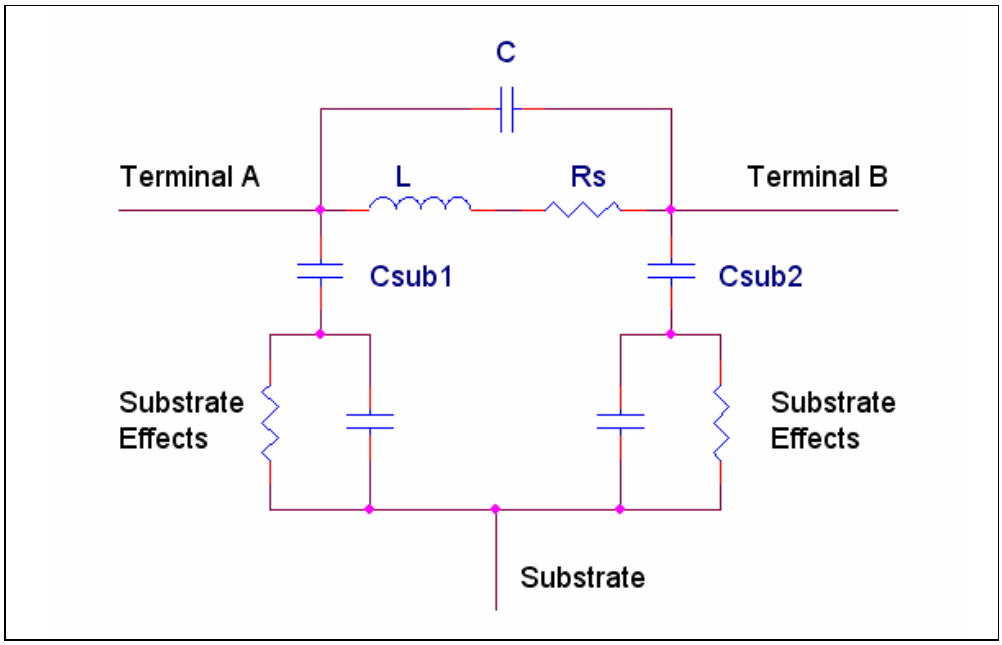


Figure 2-6 On chip inductance model

However as the frequency increases impedance of the C starts to decrease, whereas impedance of the inductance increases. At the resonance frequency their impedances becomes equal. If the frequency is further increased, impedance of the capacitance becomes more effective and device behaves more like a capacitance.

Quality factor of an inductor is a measure of the energy storage capacity over its energy dissipation.

$$Q = 2\pi \frac{|Net\ energy\ stored\ in\ one\ ac\ cycle|}{Energy\ dissipated\ in\ one\ ac\ cycle} \tag{2.16}$$

The quality factor Q in an ideal inductance, increases with the increasing frequency. However in the on chip inductance, quality factor decreases with the frequency due to parasitic capacitances. Parallel impedance of the capacitance cancels the impedance of the inductors. At the resonance frequency quality factor is zero.

On chip inductors consume very large areas. So the number of the inductors must be kept minimum or external inductors must be used. Generally inductors above 10nH are not realizable.

On chip inductors are made of looping the interconnect layers. This loop may be parallel to the surface of the chip which forms planar spiral inductors, perpendicular which forms planar solenoidal inductors or they may be made on the bond wires.

2.2.4.1 Planar Spiral Inductors

Planar spiral inductors are very widely used. Since circle shaped versions has longer turns than the square shaped version in the same area, they produce higher inductance. However circular shapes are not permitted in most processes. Because of this, hexagonal and octagonal shapes are preferred.

Direction of the resultant magnetic flux is into the lossy silicon substrate, and they consume very large area. They must be implemented in the topmost available metal in order to increase the distance between the inductor and the substrate. This is effective in two ways. Firstly this decreases the capacitance to the substrate. Second the flux doesn't go directly into the substrate but instead loops under the inductor.

An approximate formula for the calculation of the inductance value is given in [9]. This equation results within 5% of the correct value. For shapes other than square spirals, multiply the value given by the equation by the square root of the area ratio to obtain a crude estimate of the correct value.

$$L \approx \mu_0 n^2 r = 4\pi.10^{-7} n^2 r \qquad (2.17)$$

As an alternative to this equation a more complicated and accurate one can be given as:

$$L \approx \frac{37.5\mu.n^2.a^2}{22r - 14a} \qquad (2.18)$$

where a is the square spiral's mean radius. This equation holds within percentage error of ±10%. This formula accurately predicts the inductance of the "hollow inductors", in which one of the most inner turns have been removed to improve quality factor Q [9]. Area occupied by the most inner turns are relatively small compared to outer turns and their contribution to the total flux is small. However

additional resistance caused by the inner turns are comparable to resistance of others turns. Therefore removing internal turns and making the inductor hollow improves the quality factor, Q.

Long turns of the inductor cause a large series resistance in the inductor which is the main reason for the decrease of the quality factor Q. At the high frequencies this resistance increases because of the "skin effect". This is the cause of the further decrease in the quality factor at the higher frequencies.

Another reason for the decrease in the quality factor Q is the parasitic capacitances as described in section 2.2.4. There are two main parasitic capacitances. One is the capacitance between the terminals of the inductors as a result of the series connection of the capacitances among the winding. Other is the winding capacitance to substrate. Actually because of the series connection of the winding capacitances, capacitance at the terminals of the inductor is very small and in most cases negligible. Generally most effective capacitance in the decrease of the quality factor is the capacitance to substrate. This capacitance is quite large since the inductor is very close to substrate, about 2-5 μm. Resonance frequency of the combination of the capacitance and the inductance is the highest usable frequency of the inductance. Another term decreasing the quality factor Q is the energy coupled to the substrate [13].

In [9] handy equations for the calculation of the parasitic elements in the model circuit Figure 2-6 are given for initial design calculations.

Series resistance R_S is given as

$$R_S \approx \frac{1}{w.\sigma.\delta(1-e^{-t/\delta})} \tag{2.19}$$

where σ is the conductivity of the material, l is the total length of the winding, w and t are the width and thickness of the interconnect, and the δ is the skin depth.

Parallel winding capacitance C is given as

$$C \approx n \cdot w^2 \cdot \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.20}$$

where t_{ox} is the thickness of the oxide.

Oxide capacitance C_{ox} is given as

$$C_{ox} \approx w \cdot l \cdot \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.21}$$

Substrate loss resistance models two effects; current flowing through the C_{ox} and the current coupling to the substrate. An approximate equation based on the fitting can be given as

$$R \approx \frac{2}{w \cdot l \cdot G_{sub}} \tag{2.22}$$

where G_{sub} is the fitting parameter. It has a typical value of about $10^{-7}\, S / \mu m^2$.

Lastly substrate loss capacitance equation is given as

$$C \approx \frac{w \cdot l \cdot C_{sub}}{2} \tag{2.23}$$

where C_{sub} is the fitting parameter which is generally between 10^{-3} and $10^{-2}\ fF / \mu m^2$.

Patterned ground shields under the inductor may prevent the capacitive coupling to the lossy substrate and improve the quality factor Q. In depth discussion about the solid and patterned ground shield can be found in [13]. Using improvement techniques, quality factor can be increased by 50% [9]. It is also possible to use multi-layer inductors to obtain higher value inductors.

2.2.4.2 Planar Solenoidal Inductors

Inductors can be constructed by looping the conductor perpendicular to the surface of the substrate. This is done using two interconnect layers. One loop is formed as connecting two parallel lines at different layers by via contacts; more loops can be formed by connecting these loops one after other.

Since the flux is parallel to the substrate, substrate losses are much more less than planar spiral inductors. However due to many contacts series resistance is higher.

2.2.4.3 Bond Wire Inductors

Additionally bond wires can be used to make inductors. These inductors have much more inductance per wire length since their wires surround more area. As they are close to substrate they have small substrate capacitances and small substrate losses.

Inductance formula of the bond wire inductances are given as

$$L \approx 2.10^{-7} l \left[\ln\left(\frac{2l}{r}\right) - 0.75 \right] \tag{2.24}$$

According to this formula inductance per millimeter length is 1nH/mm. Quality factor Q values on the order of 50 – 100 is possible to obtain in the 1GHz – 5GHz frequency range. Series resistance can be calculated and quality factor can be predicted by the formula,

$$\frac{R}{l} \approx \frac{1}{2\pi \cdot r \cdot \delta \cdot \sigma} \tag{2.25}$$

2.3 Active Components: MOSFET Devices

MOSFETs are the main active components of the CMOS process. Normally resistivity is very high between the two diffusion regions on an opposite type semiconductor. (e.g. n+ diffusions in p-substrate or p-well, p+ diffusions in n-substrate or n-well) When an electric field is applied to the region between the

diffusions, opposite type carries are attracted and a low resistivity channel is formed. A general structure of the nMOS transistor is shown in Figure 2-7.

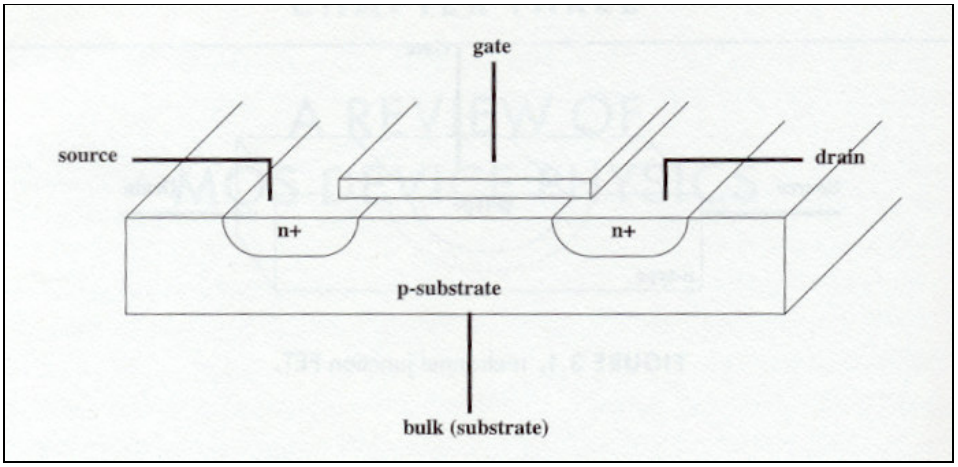


Figure 2-7 N-channel MOSFET

When the voltage between the terminals of the transistor is zero, electric field through the channel is constant. However when a voltage difference is applied to the terminals of the transistor, a lateral electric field is formed for the movements of the carriers. Additionally potential through the channel decreases from voltage applied to the drain terminal to the zero. Therefore, the potential difference between the channel and the gate terminal increases with the strength of the electric field.

Current density at the inversion layer channel can be expressed as

$$Q_n(y) = -C_{ox}\left[\left(V_{gs} - V(y)\right) - V_t\right] \tag{2.26}$$

where $Q_n(y)$ is the charge density at position y and, C_{ox} is ε_{ox}/t_{ox}, and $V(y)$ is the channel potential at position y.

2.3.1 Linear Region

When gate voltage is sufficiently high (especially compared to drain voltage) whole channel remains in the inversion layer. Gate voltage must be higher than threshold voltage plus drain voltage in order to keep the whole channel in the inversion layer. This is called as linear (triod) region of the MOSFET.

(2.27) $V_G > V_D + V_T$

In the linear region drain current depends on the gate voltage and drain voltage. It works as if voltage controlled resistor, control voltage of which is the gate voltage. The expression for the drain current of the MOSFET in the linear region is

(2.28) $$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{gs} - V_T) - \frac{V_{ds}}{2}\right]V_{ds}$$

For the small voltages of the V_{ds} ($\frac{V_{ds}}{2} << V_{gs} - V_T$), current can be expresses a linear function of the V_{ds} since

(2.29) $$I_D = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_T)V_{ds}$$

and a linear R_{ON} resistance can be formulated as,

(2.30) $$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_T)}$$

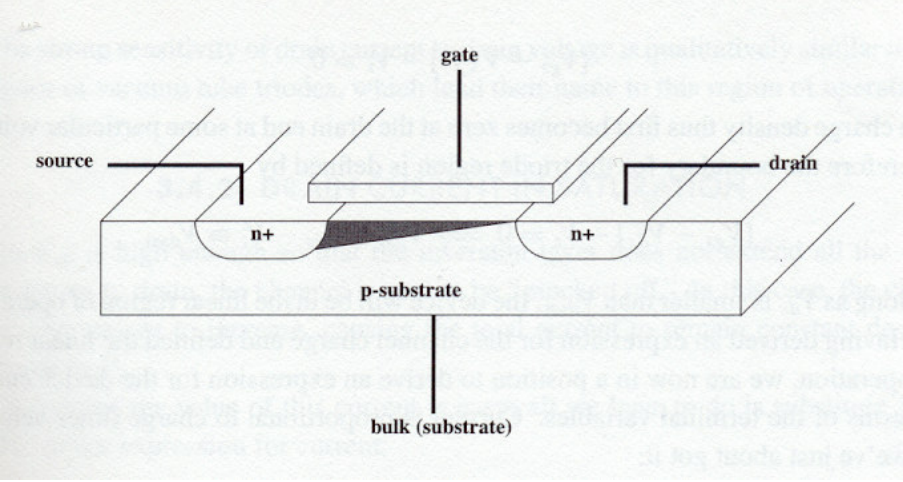


Figure 2-8 N-channel MOSFET at the boundary of the linear region and saturation region

2.3.2 Saturation Region

If the gate voltage is higher than threshold voltage plus the source voltage but is less than threshold voltage plus drain voltage, channel at the source will be open but channel at the drain will be closed. This is called "pinched off" channel and transistor is in the saturation mode.

Current expression for saturation mode of the MOSFET is;

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{gs} - V_T)^2 \tag{2.31}$$

Transconductance of MOSFET in saturation region is

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_T) \tag{2.32}$$

or

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{2.33}$$

2.3.3 Channel Length Modulation

Unfortunately as the drain to source voltage increases effective channel length does not remain the same. As the voltage increases at the drain terminal, pinch-off in the channel occurs closer to the source terminal, decreasing the effective channel length, which increases the drain current. This effect is called "channel length modulation".

Channel length modulation creates a dependence of output current on the output voltage, which means a nonzero output conductance, limiting the maximum voltage gain.

2.3.4 Body Effect

If there is a positive difference between the source terminal and the body, junction between the channel (n-channel) and the body (p-substrate) will be more

reverse biased. This will decrease the negative charges in the channel, and more voltage will be needed at the gate terminal to the keep the inversion layer at the same level. As a result threshold voltage increases. This effect is called “body effect” or “back-gate bias”. Expression for the dependence of the threshold voltage to the source to bulk voltage can be given as;

$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{2.34}$$

where V_{T0} is the zero substrate voltage threshold voltage, γ is the body effect parameter and 2ϕ is the surface potential parameter.

Because of the dependence of the drain current to the body voltage, this terminal can be taken as the second control terminal of the MOSFET. Therefore there is a transconductance term due to the body effect, whose expression is;

$$g_{mb} = \frac{\gamma}{2\sqrt{V_{SB} + 2\phi_F}}\, g_m \tag{2.35}$$

2.3.5 Capacitance Model

In the MOSFET device various intrinsic and extrinsic capacitances exist. Intrinsic capacitances are the capacitances already existing in the ideal operation of the MOSFET due to semiconductor properties. However extrinsic capacitances are due to parasitic effects of the structure and the geometry.

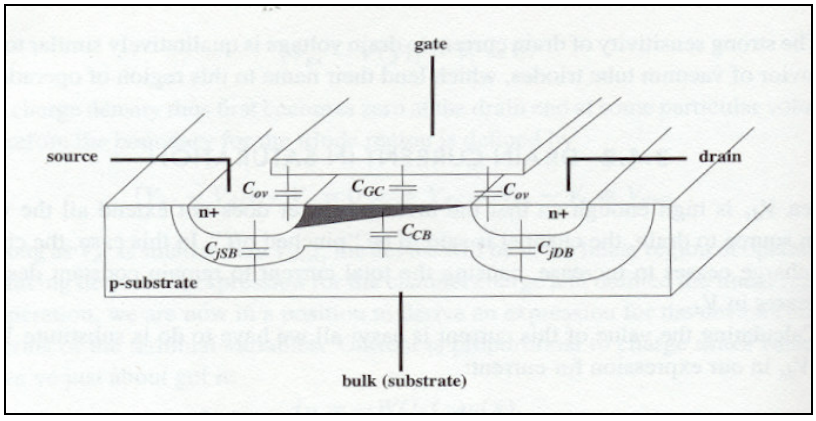


Figure 2-9 MOSFET capacitances

In the diffusion process of the drain and source, they diffuse by a small amount under the gate. This creates the overlap capacitance C_{OV}. Lateral diffusion under the gate is proportional to the depth of the source and drain diffusions by 2/3 to 3/4. C_{OV} can be formulated as [9],

$$C_{ov} \approx \frac{\varepsilon_{ox}}{t_{ox}} W L_D = 0.7 x_j C_{ox} W \tag{2.36}$$

where x_j is the depth of the source-drain diffusions. Occasionally thickness of the gate is larger than the width of the channel and fringing capacitance dominates. Thus overlap capacitance changes little with scaling [9].

Another capacitance is the gate-to-channel capacitance, C_{gc}, which is a parallel plate capacitor. This capacitance is given by

$$C_{gc} = C_{ox} W (L - 2L_D) \tag{2.37}$$

Channel-to-bulk capacitance is the capacitance between the inversion layer channel and the bulk, which behaves like a junction capacitance. Its value is given as

$$C_{cb} \approx \frac{\varepsilon_{Si}}{x_d} W (L - 2L_D) \tag{2.38}$$

where x_d is the depth of the depletion layer, whose value is given by

$$x_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_{sub}} \left| \phi_S - \phi_F \right|} \tag{2.39}$$

Additionally there are two junction capacitances between source and bulk and drain and bulk. These junction capacitances are normally reverse biased and their value can be given as

$$C_{db} \approx \frac{C_{j0}}{(1 - V_F / \phi)^n} \tag{2.40}$$

where C_{j0} is the incremental capacitance at zero bias, V_F is the applied bias voltage across the junction, ϕ is the built in potential (typically several tenths of a volt), and n is a parameter that depends on the doping profile, which is typically 1/2.

2.3.6 High Frequency Figures of Merits

There are two figures of merit for the high frequency operation of the MOSFET transistor; w_T and $w_{\max}$, which are the frequencies at which current gain and power gain, respectively, falls to unity.

w_T stands for the maximum frequency of operation, considering the current gain. However a device below a unit current gain can produce quite fine power gains, if it can transfer current to large impedances, by giving very low impedance at its input. Therefore $w_{\max}$ defines the usable frequencies of the device better than w_T. Expressions $w_{\max}$ and $w_{\max}$ can be given as [9],

$$w_T = \frac{g_m}{C_{gs} + C_{gd}} \tag{2.41}$$

$$w_{\max} \approx \frac{1}{2}\sqrt{\frac{w_T}{r_g C_{gd}}} \tag{2.42}$$

2.3.7 Short Channel Effects

With the scaling, device dimensions (especially channel width) decrease, which causes very high electric fields in the channel.

Because of scattering by high–energy ("optical") phonons, carrier velocities eventually cease to increase with the increasing electric field. In silicon, as the electric field approaches to about 10^5 V/m, electron drift velocity displays a progressively weakening dependence on the field strength and eventually saturates at a value of about 10^5m/s [9]. This will also cause degradation on the drain current. Drain current expression taking account the velocity saturation is,

$$I_D = \frac{\mu_n C_{ox}}{2} W (V_{GS} - V_T) E_{sat} \quad (2.43)$$

where E_{sat} is the electric field where the velocity saturation occurs. This equation holds where the electric field in the channel is large compared to E_{sat}, which can be expressed roughly as,

$$\frac{V_{GS} - V_T}{L} >> E_{sat} \quad (2.44)$$

One important consequence of the short channel effect is on the high frequency of merit, w_T, since the g_m depending on the drain current changes. Expression for the w_T can be given as [9]:

$$w_T \approx \frac{g_m}{C_{gs}} \approx \frac{\frac{1}{2}(\mu_n C_{ox}) W E_{sat}}{\frac{2}{3} W L C_{ox}} = \frac{3}{4} \frac{\mu_n E_{sat}}{L} \quad (2.45)$$

2.3.8 Small Signal Model of the MOSFET

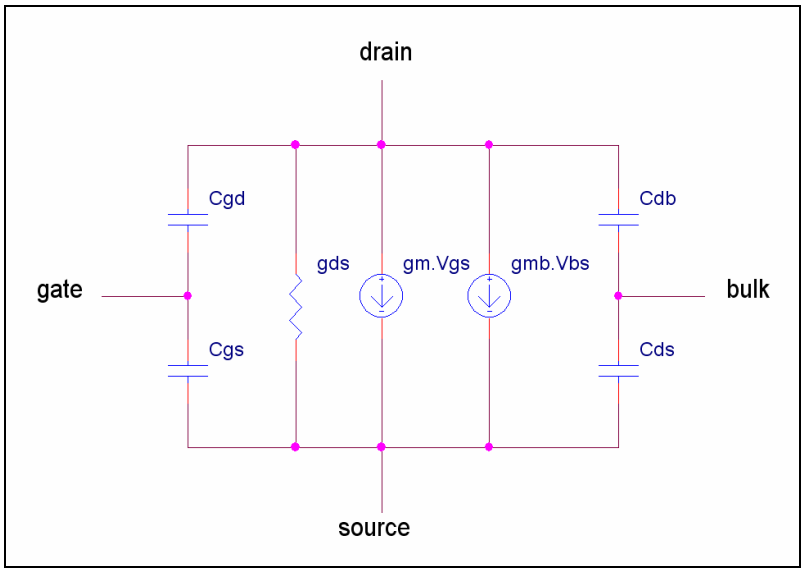


Figure 2-10 Small signal model of the MOSFET

Figure 2-10 shows the small signal model of the MOSFET. Drain current depends on gate voltage via g_m, bulk voltage via g_{mb}, and drain to source voltage via g_{ds}.

2.3.9 Developing High Frequency Simulation Models of the MOSFET

So far we have examined the simple operation of the MOSFET, however actual characteristics of the MOSFET is much more complicated than that can be modeled by such simple equations. These complicated characteristics can be modeled with very complex equations and those equations are not useful for the initial design calculations. Instead these equations are used for computer simulation of the circuits.

There are some simulation models that can model the MOSFET operation very accurately at relatively low frequencies. However real device measurements and the simulation results differ at high frequencies. This is because the parasitic components exist in structure and geometry of the device. The analysis of these parasitics is very difficult.

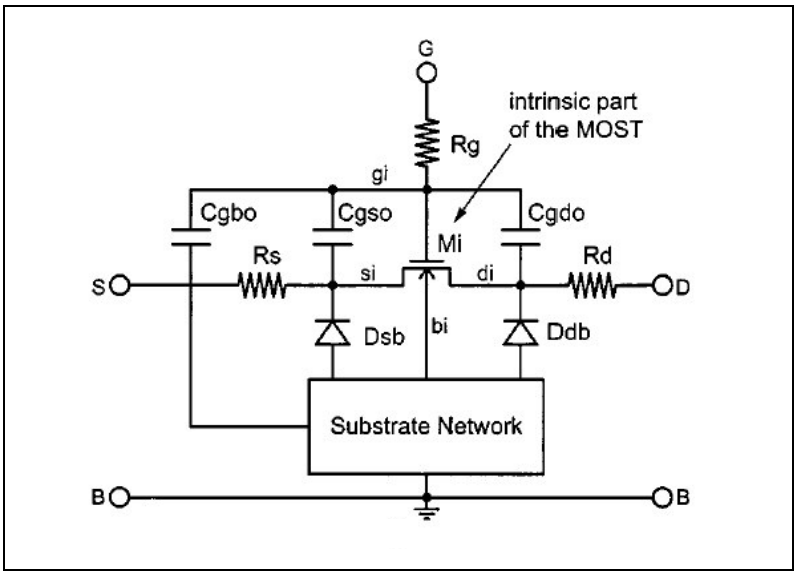


Figure 2-11 MOSFET model with high frequency parasitics

Validity of the simulation model can be extended to very high frequencies by placing parasitic components around the intrinsic device model, then determining the values of these parasitics by the parameter extraction methods from the measured data of the real device valid up to 10GHz [6][8][10].

CHAPTER 3

CLASS E POWER AMPLIFIERS

3.1 Introduction

Compared to other types of amplifiers, efficiency is a very important parameter in power amplifiers. Since large amounts of power is needed to be delivered to the load, increase of efficiency can greatly save the dissipated power on the output transistors, reduce the heat sink volume, battery size and total weight/size of the device. For this reason efficiency parameter for the power amplifiers is especially more important for the immerging mobile device market as the device sizes are getting smaller and smaller.

Major reason of the power dissipation of an amplifier is the existence of voltage and current on the active device simultaneously. This energy is converted to heat and dissipated. In order to obtain a high efficiency amplifier, simultaneous voltage and current on the active device (in fact on the every component of the amplifier other than the load) must be decreased. In this section we will examine the reasons of the simultaneous voltage and current on the active devices and the ways of minimizing this power dissipation according to different power amplifier topologies.

Main idea behind the power amplification is to control high power signals using low power signals. Active devices convert DC power to high frequency signal using this principle. Devices used in amplifiers have three important region of operation: High impedance cutoff region, linear low impedance region and high impedance controlled current source region. In the high impedance cutoff region,

very small or no current exists when voltage is applied on the device. In the linear low impedance region, very small voltage exists when current is applied on the device. In these two operation region, power dissipation is very small or doesn't exist. But in order to use the active device in the current source region, certain amount of voltage must exist on the device, and this makes certain amount of dissipation unavoidable.

Amplifiers of type class A, B, AB, C uses active devices as controlled current source. These types of amplifiers modulate DC power using controlled current source and delivers to the load. Since certain amount of voltage must exist to keep the device in the current source mode, there is always a certain power dissipation on the device. But power dissipation can be decreased by using the device as a current source only some part of the period and forcing the device to cutoff on the other parts of the period (Class B, AB, C). This is done by decreasing the bias level. Driving signal forces the device to the cutoff on the lower levels of the period automatically.

Other types of amplifiers use active devices switching between linear low impedance region and cutoff region to obtain a high efficiency. This type of operation is similar to operation of an ideal switch, linear low impedance region as on state and cutoff region as off state. Since a switch ideally dissipates no power, i.e. there is either zero voltage across it or zero current through it, it is theoretically possible to obtain 100% efficiency [11].

At a first glance it seems there is no reason for loss of energy with an ideal switch. However, even if with an ideal switch, finite parasitic inductances and capacitances on the terminals may cause some power to be dissipated during on/off transitions. Any non-zero charge on the output capacitance at the time of turn on is discharged with an impulsive current over the switch. Similarly any none-zero current stored on the inductances over the terminals of the switch is dissipated with an impulsive voltage at the time of turn off. In the case of non-ideal switch, with non-zero on resistance, finite off resistance and none zero switching time, impulsive voltage and currents are limited and spread to time, keeping the dissipated power same, reasoning the simultaneous voltage and currents on the switch at the on/off transitions. The switching time of the device may be considerable fraction of the ac

cycle, and considerable power may be dissipated in the active device during switching [11].

3.2 High Efficiency Switching Power Amplifiers

Current and voltage must be zero at the time of on/off transitions to obtain 100% efficiency power amplifier. Such an optimum waveform proposed in [11] by Sokals in 1975. In these current and voltage waveforms, voltage drops to zero before active device turns on and current drops to zero before device turns off.

The following conditions are met by those waveforms [11]:

1) 2) *Minimizing; the voltage across the device when current flows through it, the current through the device when voltage exists across it:* Those conditions are well known, and require only that the active device be chosen and the driver be designed so as to minimize the switch "on" voltage and "off" leakage current, respectively. Those conditions are substantially independent of the design of the load network.

3) *The switching time of the switch is minimized:* This condition is also well known and may also be fulfilled by proper choice of the active device and proper design of the driver. This condition is somewhat dependent on the design of the load network.

4) *Voltage delay at switch turnoff:* In the time interval during which the switch makes its transition from the "on" state to the "off" state, the voltage across the switch remains low for a time long enough that the current through the switch has by then reduced substantially to zero. Then the voltage increases. This assures that high voltage does not exist across the switch while the current through it is nonzero, thereby avoiding the energy loss, which would have existed if the voltage has been allowed to start to increase before the current decrease to zero had been substantially completed.

5) *Voltage return to zero at switch turn-on:* During the switch turn "off" state, the load network input-port transient response carriers the voltage across the switch first upwards, and then downwards towards to zero; this voltage reaches zero

just before the current begins to flow in the switch. This avoids the energy dissipation which would have occurred if the switch current had begun flowing while the voltage across the switch was still high, and had thereafter discharged to ground, through the switch, the capacitance at the load network input port.

6) *Zero voltage slope at the switch turn-on:* When the "off" state transient response reaches zero voltage across the switch, i.e. just before the beginning of the "on" state, it does so with approximately zero slope. This permits accidental slight mistuning of the amplifier without severe loss of efficiency, i.e. there is a time interval during which the switch turn-on can occur while still substantially meeting the condition of $v = 0$. Moreover, moderately slow turn-on of the switch does not cause the switch to experience high power dissipation during turn-on, because voltage across the switch is not increasing rapidly during the time that the switch is turning on. Furthermore, the conditions $v = 0$ and $dv/dt = 0$ at the end of the "off" state together imply that the switch current at the start of the "on" state will be zero, and that during the "on" state the switch current need increase from zero only gradually. In the view of the limited dv/dt capabilities of the actual active-device switches, this zero starting current is desirable because it helps to minimize dissipation during the turn-on transient. Avoiding a substantial negative value of dv/dt at turn-on time avoids imposing on the switch a requirement to conduct substantial current then in the reverse on the usual direction.

7) 8) *The voltage and current transient response waveforms each have a flat top:* It can be shown that the optimum voltage and current waveforms are flat topped with short rise and fall times, the peak values being equal to or less than the maximum which the switch is able to withstand reliably, for the usual case in which the switch peak voltage and current capabilities define the allowable limits of operation.

Such a waveform can only be accomplished by appropriate design of a non-resistive load network. Class E and Class F amplifiers use tuned load networks to obtain such similar voltage and current waveforms to decrease power dissipation.

3.3 Class E Power Amplifier Circuit Topology

A common Class E circuit is shown in Figure 3-1. Q1 active device is driven so highly that it completely turns on and turns off each cycle, in other words works like a switch. L1 is very high inductance choke for biasing and can be seen as a short circuit at DC and open circuit at RF.

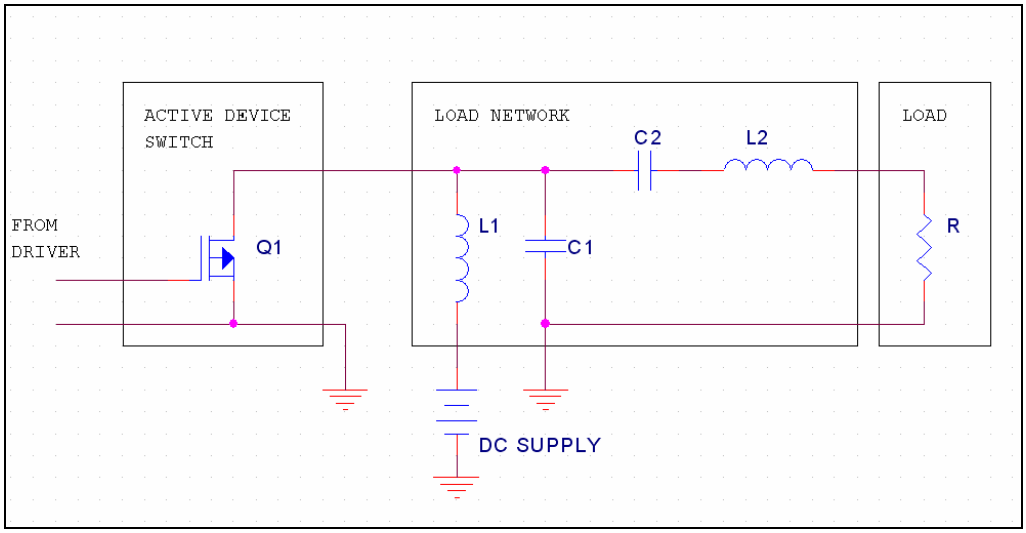


Figure 3-1 Classical class-E circuit topology

C1 is shunt to the terminals of the active device and output capacitance can be absorbed into it. C2 and L2 form a band pass filter at the desired operating frequency. R is the load, as well as it can be the real load, it can represent the input impendence of a band pass filter or a load transmission network.

3.4 Basic Circuit Equations

A simple equivalent circuit of this amplifier can be seen in Figure 3-2. This simplification is based on the following five assumptions [12]:

- The RF choke allows only a constant (dc) input current and has no series resistance.
- The Q of the series-tuned output circuit is high enough that the output current is essentially a sinusoid at the carrier frequency.

- Switching action of the transistor is instantaneous and lossless (except when discharging the shunt capacitor); the transistor has zero saturation voltage, zero saturation resistance and infinite off resistance.
- The total shunt capacitance is independent of the collector voltage.
- The transistor can pass negative current and withstand negative voltage (this is inherent in MOS devices, but requires a combination of bipolar transistors and diodes).

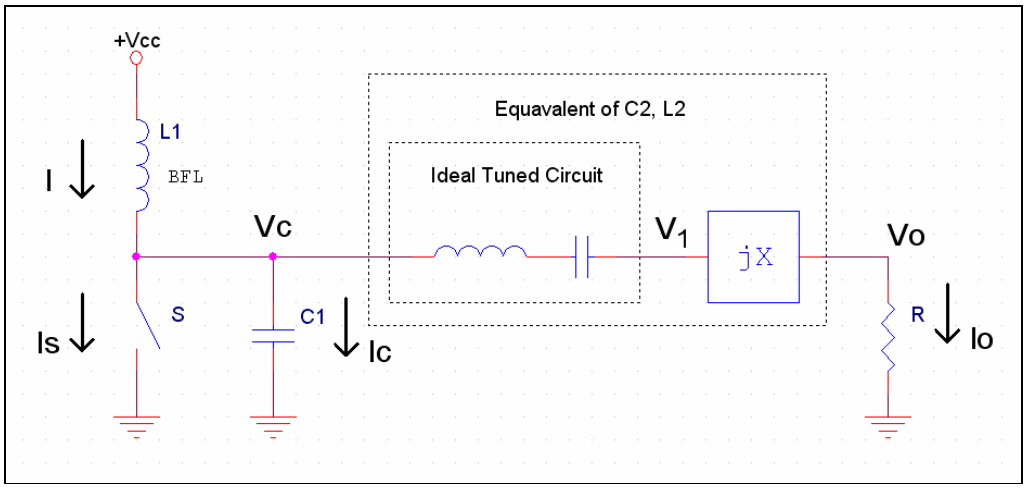


Figure 3-2 Simplified Equivalent Circuit of Class E Amplifier

The series reactance *jX* is actually produced by the difference in the reactance of the inductor and capacitor of the series-tuned circuit. The voltage $v_1(\theta)$ is actually fictitious; however, it is a convenient reference point to use in the analysis.

Analysis of the class E amplifier is straightforward but quite tedious. There is no clear source of voltage or current, as in classes A, B, C and D amplifiers. The collector voltage waveform is a function of the current charging capacitor, and the current is the function of the voltage on the load, which in turn a function of the collector voltage. All parameters are interrelated. The analysis begins by determining the collector voltage waveform as a function of the dc input current and the sinusoidal output current. Next, the fundamental frequency component of the collector voltage is related to the output current, and the dc component of the collector current is related to the supply voltage. These relationships result in a

nonlinear equation, which can be solved analytically or numerically. Finally, input and output power and efficiency can be calculated.

The slope of the collector voltage at turn-on and the pulse width (duty cycle) of the transistor switch are two design options. It is shown that for the maximum output power and output power capability slope must be zero and the duty cycle must be 50-percent [12]. Because of this reason, all of the equations will be derived for the 50-percent duty cycle operation.

3.4.1 Basic Relationships

The output voltage and current are sinusoidal and have the forms

$$v_0(\theta) = c\sin(\omega t + \varphi) = c\sin(\theta + \varphi) \tag{3.1}$$

and

$$i_0(\theta) = \frac{c}{R}\sin(\theta + \varphi) \tag{3.2}$$

where θ is an "angular time" used for mathematical convenience. The parameters c and φ are to be determined. c is the magnitude of the output voltage, φ is the phase difference of the output voltage.

The hypothetical voltage $v_1(\theta)$ is also a sinusoid, but has a different phase because of reactance jX

$$v_1(\theta) = v_0(\theta) + v_x(\theta) \tag{3.3}$$

$$= c\sin(\theta + \varphi) + X\frac{c}{R}\cos(\theta + \varphi) \tag{3.4}$$

$$= c_1\sin(\theta + \varphi_1) \tag{3.5}$$

where

(3.6) $$c_1 = c\sqrt{1+\frac{x^2}{R^2}} = \rho c$$

and

(3.7) $$\varphi_1 = \varphi + \psi = \varphi + \arctan(\frac{X}{R})$$

Since the RF choke forces a dc input current and the series-tuned output circuit forces a sinusoidal output current, difference between those two currents must flow into (or out of) the switch-capacitor combination. When switch S is open, difference flows into capacitor C1; when switch S is closed, the current difference flows through switch S. If a capacitor voltage of other then zero volts is present at the time switch closes, switch discharges that voltage to zero volts, dissipating the stored energy of $\frac{1}{2}CV^2$.

For the purposes of this analysis, the discharge of the capacitor may be assumed to be a current impulse $q\delta(\theta-\theta_C)$, where θ_C is the time at which the switch closes. However, on a real amplifier, discharge of the capacitor requires a nonzero length of time, during which the collector voltage and current are simultaneously nonzero. In any case, however, the total dissipation is the energy stored in the capacitor, and does not depend on the particulars of the discharge waveforms. The model remains valid as long as the time required to discharge the capacitor is a relatively small fraction of the RF cycle.

When S is off, the collector voltage is produced by the charging of capacitor C by the difference current, hence

(3.8) $$v(\theta) = \frac{1}{\omega C}\int_{\theta_0}^{\theta} i_c(u)du$$

where θ_0 indicated the time at which S opens.

For a 50-percent duty cycle switch opens at the beginning of the period and closes at angular time π. The collector voltage at time θ can now be evaluated by expanding (3.8)

$$v(\theta) = \frac{1}{B}\int_0^{\theta}\left[I - \frac{c}{R}\sin(u+\varphi)\right]du \tag{3.9}$$

$$= \frac{I}{B}\theta + \frac{c}{BR}\cos(\theta+\varphi) - \frac{c}{BR}\cos(\varphi) \tag{3.10}$$

where

$$B = \omega C \tag{3.11}$$

Since the tuned circuit has zero impedance to the fundamental frequency current, there can be no fundamental frequency voltage drop across it. This means that the fundamental frequency component of the collector voltage must be the hypothetical voltage $v_1(\theta)$. The magnitude of this component can be calculated by a Fourier integral. Unfortunately, the collector voltage is not symmetrical around $\pi/2$, which makes the phase φ an unknown.

3.4.2 Fourier Analysis

The magnitude c_1 of the fundamental frequency component of the collector voltage is then

$$c_1 = \frac{1}{\pi}\int_0^{2\pi} v(\theta)\sin(\theta+\varphi_1)d\theta \tag{3.12}$$

$$= -2\frac{c}{\pi BR}\cos(\varphi)\cos\varphi_1 - 2\frac{I}{\pi B}\sin(\varphi_1) + \frac{I}{B}\cos(\varphi_1) + \frac{c}{2BR}\sin(\psi) \tag{3.13}$$

It is now possible to solve for c by substituting pc for c_1 and collecting terms

$$\rho c + c\left[\frac{-\sin(\psi)}{2BR} + \frac{2\sin(\frac{\pi}{2}-\varphi)\cos(\varphi_1)}{\pi BR}\right] \tag{3.14}$$

$$= \frac{I}{\pi B}\left[\pi\cos(\varphi_1) - 2\sin(\varphi_1)\right]$$

Thus

$$c = IR\frac{\pi\cos(\varphi_1) - 2\sin(\varphi_1)}{\pi BR\rho - \frac{\pi}{2}\sin(\psi) + 2\sin(\frac{\pi}{2}-\theta)\cos(\varphi_1)} \tag{3.15}$$

$$= IRh(\varphi,\psi,B,R,\rho) \tag{3.16}$$

This relationship will be useful later in finding φ. Since the fundamental frequency component of the collector voltage is by definition a sine wave of phase φ_1, there can be no cosine and or quadrature component with respect to phase φ_1. A second relationship among the parameters is then found from

$$0 = \frac{1}{\pi}\int_0^{2\pi} v(\theta)\cos(\theta+\varphi_1)d\theta \tag{3.17}$$

$$= \frac{2c}{\pi BR}\cos\varphi\sin\varphi_1 - 2\frac{I}{\pi B}\cos\varphi_1 - \frac{I}{B}\sin\varphi_1 + \frac{c\cos\psi}{2BR} \tag{3.18}$$

$$c = IR\frac{\pi\sin\varphi_1 + 2\cos\varphi_1}{-2\sin(\varphi-\pi/2)\sin\varphi_1 + \frac{\pi}{2}\cos\psi} \tag{3.19}$$

$$= IRg(\varphi,\psi) \tag{3.20}$$

Similarity of (3.16) and (3.20) requires that

$$g(\varphi,\psi) = h(\varphi,\psi,B,R,\rho) \tag{3.21}$$

When component values and switch duty cycle have been specified, φ is the only unknown in (3.21). Finding the operating parameters of a class E amplifier then begins by finding φ. It is possible to solve (3.21) analytically in most cases. In the event that an analytical solution is difficult or impossible, one can resort to brute force numerical solution to find φ.

3.4.3 Power and Efficiency

The relationship of the supply voltage V_{CC} to the other parameters has yet to be determined. It can be found by observing that there is no dc voltage drop across the RF choke, thus using (3.10) and (3.20), and abbreviating $g(\varphi,\psi,y)$ as g

$$V_{CC} = \frac{1}{2\pi}\int_0^{2\pi} v(\theta)d\theta \tag{3.22}$$

$$V_{CC} = \frac{I}{2\pi B}\int_0^{\pi}\left[\theta + g\cos(\theta+\varphi) - g\cos(\varphi)\right]d\theta \tag{3.23}$$

$$= \frac{I}{2\pi B}\left[\frac{\pi^2}{2} - 2g\sin\varphi - \pi g\cos(\varphi)\right] \tag{3.24}$$

$$= IR_{dc} \tag{3.25}$$

R_{dc} is the resistance (load) that the amplifier shows to the power supply. It is now possible to compute input and output power and efficiency. Output power is

$$P_O = \frac{1}{2}\frac{c^2}{R} = \frac{I^2 g^2 R}{2} = \frac{V_{cc}^2 g^2 R}{2R_{dc}^2} \tag{3.26}$$

The input power is simply

$$P_i = V_{cc} I = \frac{V_{cc}^2}{R_{dc}} \tag{3.27}$$

so the efficiency is

$$\eta = \frac{P_o}{P_i} = \frac{g^2}{2}\frac{R}{R_{dc}} \tag{3.28}$$

3.4.4 Device Stress

To determine the peak collector voltage, it is first necessary to determine the time at which it occurs. This is accomplished by differentiating the waveform and setting the result equal to zero. Since $I = V_{CC}/R_{dc}$, and

$$c = IRg = \frac{Vcc}{R_{dc}}Rg \tag{3.29}$$

the collector voltage waveform may be described by

$$v(\theta) = \frac{V_{cc}}{R_{dc}B}\left[\theta + g\sin(\varphi - \frac{\pi}{2}) + g\cos(\theta + \varphi)\right] \tag{3.30}$$

Now

$$0 = \frac{dv(\theta)}{d\theta}\Big|_{\theta=\theta_{c\max}} = \frac{V_{cc}}{R_{dc}B}\left[1 - g\sin(\theta_{c\max} + \varphi)\right] \tag{3.31}$$

From this

$$\theta_{c\max} = \arcsin\frac{1}{g} - \varphi \tag{3.32}$$

and the peak voltage v max can then be found by using $\theta_{v\max}$ in (3.30). In the event that there is a negative collector voltage, its peak value can be determined similarly using

$$\theta_{v\min} = \pi - \arcsin\frac{1}{g} - \varphi \tag{3.33}$$

provided that it occurs before the time of turn-on.

The peak collector current is more easily determined, since it must occur at a peak of the output current.

$$(3.34) \qquad i_{S\max} = \frac{c}{R} + I = \frac{IRg}{R} + I = I(1+g)$$

In the event that the peak output current occurs outside of the interval in which the transistor is turned on, (3.34) no longer applies, and $i_{S\max}$ is the value at either turn-on or turn-off. One should be careful, however, to note that unless the voltage on the capacitor is zero at the time of turn-on, $i_{S\max}$ is theoretically infinite, and in practice considerably larger than that given by (3.34).

The power output capability $P_{\max}$ provides a means of comparing different designs with each other and other types of amplifiers. It is convenient to define this as the output power produced when the device has a peak collector voltage of 1 V and a peak collector current of 1 A. It may be determined from any set of values based on this same supply and load according to

$$(3.35) \qquad P_{\max} = \frac{P_o}{v_{\max} i_{S\max}}$$

If the capacitor voltage is not zero at the time the switch closes, $P_{\max}$ will be zero in theory and greatly reduced from that given by (3.35) in practice.

3.4.5 High-Efficiency Operation

The ideal-circuit model of the Class-E amplifier used in that paper contains only lossless elements (other than the load). Consequently, the only loss mechanism is discharge of the shunt capacitor when the transistor is turned on. High efficiency operation will then be possible if the circuit parameters can be chosen to cause the collector voltage to drop to zero at the instant the transistor turns on.

The requirement for efficiency of 100 percent can now be expressed by setting (3.30) equal to zero at time $\theta = \pi$, which produces

(3.36) $$0 = \pi - 2g\cos\varphi$$

Thus

(3.37) $$\cos\varphi = \frac{\pi}{2g}$$

which is the first constraint on g and φ.

The slope of the waveform at the time of turn-on must also be zero.

(3.38) $$0 = \frac{1}{V_{CC}}\frac{dv(\theta)}{d\theta}\Big|_{\theta=\pi}$$

(3.39) $$= \frac{1}{R_{dc}B}\left[1 - g\cos(\frac{\pi}{2} + \varphi)\right]$$

Rearrangement of (3.24) produces

(3.40) $$R_{dc}B = \frac{\frac{\pi^2}{2} + \pi g\sin(\varphi - \frac{\pi}{2}) - 2g\sin\varphi}{2\pi}$$

Substitution of this into (3.39) followed by expansion of the trigonometric functions and rearrangement to separate $\cos\varphi$ and $\sin\varphi$ produces

(3.41) $$\sin\varphi = -\frac{1}{g}$$

Dividing by (3.37)

(3.42) $$\tan\varphi = -\frac{2}{\pi}$$

Now φ is determined.

(3.43) $$\varphi = -32.482° = -0.56691 rad$$

Using trigonometric relationships g can be found from (3.40)

$$\sin(\varphi) = \frac{-1}{\sqrt{1+\pi^2/4}} \tag{3.44}$$

$$g = \sqrt{1+\pi^2/4} = 1.8621 \tag{3.45}$$

Substitution of the efficiency of unity in (3.28) and rearrangement yields

$$R_{dc} = \frac{g^2 R}{2} = 1.7337R \tag{3.46}$$

and substitution of this into (3.40)

$$B = \frac{\frac{\pi^2}{2} + \pi g \sin(\varphi - \frac{\pi}{2}) - 2g\sin\varphi}{\pi g^2 R} = \frac{1}{5.4466R} \tag{3.47}$$

which is used to obtain the value of the capacitor shunting the switch. In an actual application, the capacitance inherent in the transistor would comprise some of the shunt capacitance.

By recalling (3.21)

$$g = \frac{\pi\sin\varphi_1 + 2\cos\varphi_1}{-2\sin(\varphi - \pi/2)\sin\varphi_1 + \frac{\pi}{2}\cos\psi} \tag{3.48}$$

Applying trigonometric expansion to $\varphi_1 = \varphi + \psi$ term and collecting $\sin\psi$ and $\cos\psi$ terms

$$\tan\psi = \frac{\sin\psi}{\cos\psi} = \frac{\pi\sin\varphi + 2\cos\varphi - 2g\cos\varphi\sin\varphi - \frac{\pi}{2}g}{2\sin\varphi - \pi\cos\varphi + 2g\cos\varphi\cos\varphi} \tag{3.49}$$

substituting (3.37) and (3.41) into this

(3.50) $$\tan \psi = \frac{\pi}{8}(\frac{\pi^2}{2} - 2)$$

thus ψ is

(3.51) $$\psi = \arctan\left[\frac{\pi}{8}(\frac{\pi^2}{2} - 2)\right]$$

(3.52) $$= 49.052° = 0.85613 rad$$

The series reactance is then

(3.53) $$X = R\tan\psi = 1.1525R$$

The output voltage, obtained from (3.31), is

(3.54) $$c = \frac{2}{\sqrt{1+\pi^2/4}} V_{cc} \approx 1.074 V_{cc}$$

and the output power may be obtained from the above or (3.45). Substitution of these values into (3.32), (3.30) and (3.34) produces a peak voltage of $3.56V_{cc}$ and a peak current of $2.84I$. This results in $P_{\max} = 0.0981$ (for class B and class D, $P_{\max}$ is 0.125 and 0.318 respectively).

CHAPTER 4

CLASS E CHANNEL RESISTANCE MODEL

4.1 Introduction

In the previous chapter derivation of the classical Class-E equations are given. Those derivations are based on five assumptions:

1. The RF choke allows only a constant (dc) input current and has no series resistance.
2. The Q of the series-tuned output circuit is high enough that the output current is essentially a sinusoid at the carrier frequency.
3. Switching action of the transistor is instantaneous and lossless (except when discharging the shunt capacitor); the transistor has zero saturation voltage, zero saturation resistance and infinite off resistance.
4. The total shunt cappacitance is independent of the collector voltage.
5. The transistor can pass negative current and withstand negative voltage. (this is inherent in MOS devices, but requires a combination of bipolar transistors and diodes).

In this chapter a more realistic model will be developed and analysis will be done on this model. Afterwards these equations will be numerically solved for the circuit element values.

In our model first assumption will be substituted with:

- The RF choke allows only a constant (dc) input current and has a constant (dc) resistance.

Since RF choke only conducts constant current a constant voltage drop exists on the choke. This will only affect the circuit as if supply voltage was dropped by the voltage on the choke. Voltage on the drain of the transistor is equal to

(4.1) $$V_{cc}^{'} = V_{cc} - IR_{choke,dc}$$

We will keep the second, forth and fifth assumptions as it is but third assumption will be changed to:

- Switching action of the transistor is instantaneous and lossless (except when discharging the shunt capacitor); the transistor has zero saturation voltage, *non-zero saturation resistance* and infinite off resistance.

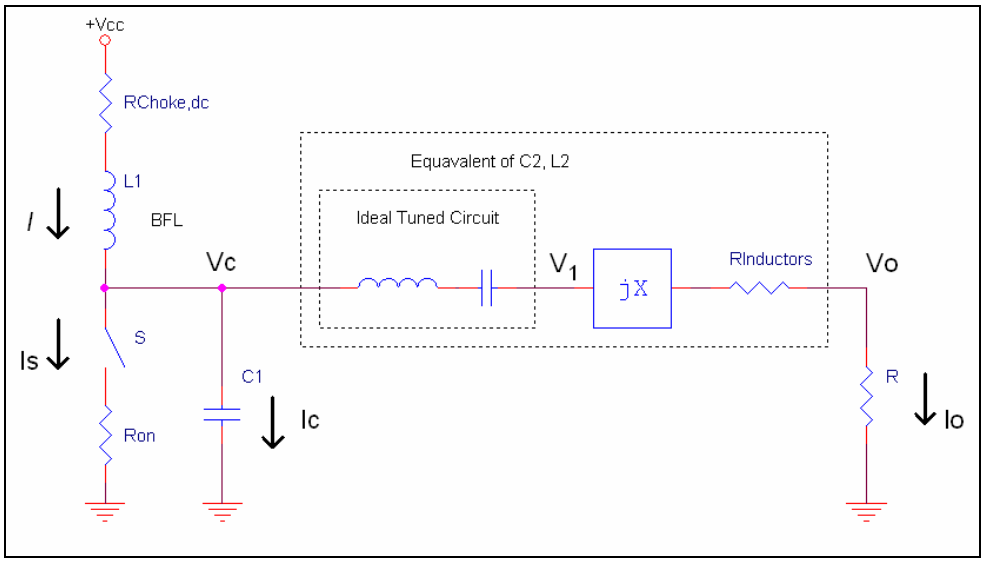


Figure 4-1 Lossy simplified model of the Class-E circuit

Besides those assumptions series parasitic resistance of the L2 inductor is included into the model ($R_{inductors}$). This resistance is series to the load and can be moved near to the load resistance R. If this resistance is included in the load resistance an equivalent load resistance seen by the output of the circuit can be obtained.

(4.2) $$R_{eq} = R + R_{inductors}$$

Figure 4-1 shows the lossy simplified model of the Class-E circuit drawn according to these assumptions.

If $V_{cc}^{'}$ and R_{eq} is used for the supply voltage and the load resistance, only difference is the channel resistance of the transistor (R_{ON}) between this circuit and the circuit given in Chapter 3.

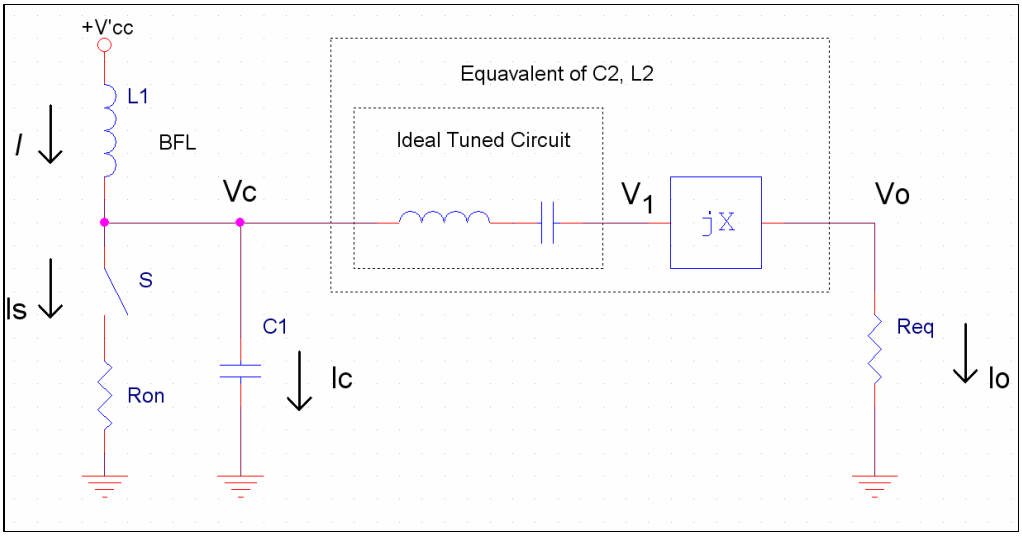


Figure 4-2 Equivalent lossy simplified model

Therefore if previous equations are modified to include the channel resistance (R_{ON}) of the transistor, equations for the lossy model (Figure 4-1) can be obtained by substituting $V_{cc}^{'}$ and R_{eq} .

4.2 Deriving Equations

Derivation of the equations is similar to the derivations in the previous chapter. Due to the ideally tuned circuit, a sinusoidal current at the fundamental frequency exists through the load resistance. First capacitor voltage is obtained by integrating the current through it. Then the Fourier transform of the Vc is calculated to obtain the fundamental component of the voltage which is the source of the sinusoidal current. These equations are simplified by substituting the high efficiency conditions.

4.2.1 Base Equations

Capacitor voltage and its slope must be zero at the transistor turn on to obtain the maximum efficiency. These two conditions are set at the capacitor voltage to obtain the desired solution.

When the switch is off, there is no effect of the resistor and $V_{C,OFF}$ is equal to (3.10). However, when the switch is on, $V_{C,ON}$ voltage is non-zero and equal to R_{on} times the current on the switch. Capacitor can be ignored in this situation.

$$V_{C,OFF} = \frac{I}{B}\theta + \frac{c}{BR}\cos(\theta + \varphi) - \frac{c}{BR}\cos(\varphi) \tag{4.3}$$

$$V_{C,ON} = I.R_{on} - \frac{c}{R}R_{on}\sin(\theta + \varphi) \tag{4.4}$$

It is important to note that $V_{C,OFF}$ contains the implicit assumption that $V_{C,OFF}$ is zero at $\theta = 0$. But this is not the case for this situation because $V_{C,ON}$ and $V_{C,OFF}$ must be equal to each other at the boundaries.

$$V_{C,OFF}(0) = V_{C,ON}(2\pi) \tag{4.5}$$

$$V_{C,ON}(\pi) = V_{C,OFF}(\pi) = 0 \tag{4.6}$$

Therefore $V_{C,OFF}$ is equals to

$$V_{C,OFF} = \frac{I}{B}\theta + \frac{c}{BR}\cos(\theta + \varphi) - \frac{c}{BR}\cos(\varphi) + I.R_{on} - \frac{c}{R}R_{on}\sin(\varphi) \tag{4.7}$$

Previously introduced variable g is equal to the ratio of the ac load current and the dc supply current.

$$g = \frac{I_{ac}}{I} = \frac{c}{I.R} \tag{4.8}$$

Due to the ideally tuned circuit fundamental frequency component of the V_C is short circuited to the jX and the R load. Fundamental frequency component of the V_C is equal to

$$v_1(\theta) = v_0(\theta) + v_x(\theta) \tag{4.9}$$

$$= c\sin(\theta+\varphi) + X\frac{c}{R}\cos(\theta+\varphi)$$

$$= c_1\sin(\theta+\varphi_1) \tag{4.10}$$

where

$$c_1 = c\sqrt{1+\frac{x^2}{R^2}} = \rho c \tag{4.11}$$

and

$$\varphi_1 = \varphi + \psi = \varphi + \arctan(\frac{X}{R}) \tag{4.12}$$

4.2.2 Sine Transformation

c_1 and φ_1 can be calculated using sine and cosine transformations of the capacitor voltage. Sine transformation at phase φ_1 must be equal to c_1 and the cosine transformation must be zero.

$$c_1 = \frac{1}{\pi}\int_0^{2\pi} V_C(\theta)\sin(\theta+\varphi_1)d\theta \tag{4.13}$$

$$c_1 = \frac{1}{\pi}\int_{\pi}^{2\pi} V_{C,OFF}(\theta)\sin(\theta+\varphi_1)d\theta + \frac{1}{\pi}\int_0^{\pi} V_{C,ON}(\theta)\sin(\theta+\varphi_1)d\theta \tag{4.14}$$

Eq. (3.13) is the sine integral of the V_C without initial condition. Initial condition is the constant term of the $V_{C,OFF}$. So sine integral can be calculated by

replacing the constant term of the V_C with initial condition term in the sine integral Eq. (3.13).

$$c_1 = \frac{1}{\pi}\int_0^{2\pi} V_C(\theta)\sin(\theta+\varphi_1)d\theta \tag{4.15}$$

$$= \frac{I}{B}\cos(\varphi_1) - 2\frac{I}{\pi B}\sin(\varphi_1) + \frac{c}{2BR}\sin(\psi) + \frac{2}{\pi}\left(-\frac{c}{BR}\cos(\varphi)\right)\cos\varphi_1 \tag{4.16}$$

$-\frac{c}{BR}\cos(\varphi)$ is the constant term in V_C. Replacing this term with the initial condition term we can obtain the sine transform of the $V_{C,OFF}$.

$$\frac{1}{\pi}\int_0^{\pi} V_{C,OFF}(\theta)\sin(\theta+\varphi_1)d\theta = \tag{4.17}$$

$$\frac{I}{B}\cos(\varphi_1) - 2\frac{I}{\pi B}\sin(\varphi_1) + \frac{c}{2BR}\sin(\psi) \tag{4.18}$$

$$+\frac{2}{\pi}\left(-\frac{c}{BR}\cos(\varphi) + I.R_{on} - \frac{c}{R}R_{on}\sin(\varphi)\right)\cos\varphi_1 \tag{4.19}$$

Sine integral of the $V_{C,ON}$ is calculated by integrating from π to 2π.

$$= \frac{1}{\pi}\int_{\pi}^{2\pi}\left(I.R_{ON}\sin(\theta+\varphi_1) - \frac{c}{R}R_{ON}\sin(\theta+\varphi)\sin(\theta+\varphi_1)\right)d\theta \tag{4.20}$$

using trigonometric relations

$$= \frac{1}{\pi}\int_{\pi}^{2\pi}\left(I.R_{ON}\sin(\theta+\varphi_1) - \frac{c}{R}R_{ON}\left[\cos(2\theta+\varphi+\varphi_1) - \cos(\psi)\right]\right)d\theta \tag{4.21}$$

since the integral of the 2θ term is zero, we ignore it.

$$= \frac{1}{\pi}\left|_{\pi}^{2\pi} - I.R_{ON}\cos(\theta+\varphi_1) - \frac{c}{2R}R_{ON}\theta\cos(\psi)\right. \tag{4.22}$$

(4.23) $$= -\frac{2}{\pi} I.R_{ON} \cos(\varphi_1) - \frac{c}{2R} R_{ON} \cos(\psi)$$

by adding the two equations

(4.24) $$c_1 = \frac{1}{\pi} \int_{\pi}^{2\pi} V_{C,OFF}(\theta) \sin(\theta + \varphi_1) d\theta + \frac{1}{\pi} \int_{0}^{\pi} V_{C,ON}(\theta) \sin(\theta + \varphi_1) d\theta$$

(4.25) $$= \frac{I}{B} \cos(\varphi_1) - 2\frac{I}{\pi B} \sin(\varphi_1) + \frac{c}{2BR} \sin(\psi) - \frac{2c}{\pi BR} \cos(\varphi) \cos(\varphi_1)$$

(4.26) $$-\frac{2}{\pi} \frac{c}{R} R_{on} \sin(\varphi) \cos\varphi_1 - \frac{c}{2R} R_{ON} \cos(\psi)$$

substitute eq. (4.4) into this and by arranging the terms we can obtain c.

(4.27) $$c = I.R \frac{\pi \cos(\varphi_1) - 2\sin(\varphi_1)}{p\pi BR - \frac{\pi}{2} \sin(\psi) + 2\cos(\varphi)\cos(\varphi_1) + 2BR_{ON} \sin(\varphi)\cos(\varphi_1) + \frac{\pi}{2} BR_{ON} \cos(\psi)}$$

4.2.3 Cosine Transformation

Quadrature component of the V_C must be zero in order to obtain a sine at phase φ_1.

(4.28) $$0 = \frac{1}{\pi} \int_{0}^{\pi} V_{C,OFF}(\theta) \cos(\theta + \varphi_1) d\theta + \frac{1}{\pi} \int_{\pi}^{2\pi} V_{C,ON}(\theta) \cos(\theta + \varphi_1) d\theta$$

cosine integral of the $V_{C,OFF}$ equals to

(4.29) $$\frac{1}{\pi} \int_{0}^{\pi} V_{C,OFF}(\theta) \cos(\theta + \varphi_1) d\theta =$$

(4.30) $$= -\frac{I}{B} \sin\varphi_1 - 2\frac{I}{\pi B} \cos\varphi_1 + \frac{c}{2BR} \cos\psi$$

(4.31) $$-\frac{2}{\pi}\left(-\frac{c}{BR}\cos\varphi + I.R_{on} - \frac{c}{R}R_{on}\sin(\varphi)\right)\sin\varphi_1$$

and cosine integral of the $V_{C,ON}$ equals to

(4.32) $$=\frac{2}{\pi}I.R_{ON}\sin(\varphi_1) + \frac{c}{2R}R_{ON}\sin(\psi)$$

and the sum of the two equations equals to zero.

(4.33) $$0 = -\frac{I}{B}\sin\varphi_1 - 2\frac{I}{\pi B}\cos\varphi_1 + \frac{c}{2BR}\cos\psi + \frac{2c}{\pi BR}\cos\varphi\sin\varphi_1$$

(4.34) $$+\frac{2c}{\pi R}R_{on}\sin(\varphi)\sin(\varphi_1) + \frac{c}{2R}R_{ON}\sin(\psi)$$

collecting c terms and arranging we get

(4.35) $$c = I.R\frac{\pi\sin(\varphi_1) + 2\cos(\varphi_1)}{\frac{\pi}{2}\cos(\psi) + 2\cos(\varphi)\sin(\varphi_1) + 2BR_{ON}\sin(\varphi)\sin(\varphi_1) + \frac{\pi}{2}BR_{ON}\sin(\psi)}$$

4.2.4 High Efficiency Conditions

Our first condition for the high efficiency operation is $V_C(\pi) = 0$ at the instant that the transistor turns on. Substituting this condition into V_C equation

(4.36) $$V_{C,OFF}(\pi) = 0$$

(4.37) $$0 = \frac{I}{B}\theta + \frac{c}{BR}\cos(\theta + \varphi) - \frac{c}{BR}\cos(\varphi) + I.R_{on} - \frac{c}{R}R_{on}\sin(\varphi)$$

Note that when we substitute $c = g \cdot I \cdot R$, I term can be eliminated. This means this condition is independent of the supply current, so as the supply voltage.

Collect g terms and arrange to get g

(4.38) $$g = \frac{\pi + R_{ON} B}{R_{ON} B \sin(\varphi) + 2\cos(\varphi)}$$

Second condition for the high efficiency operation is $\frac{dV_C(\pi)}{d\theta} = 0$ at the instant the transistor turns on.

(4.39) $$\frac{dV_{C,OFF}(\pi)}{d\theta} = \frac{I}{B} - \frac{c}{BR}\sin(\pi + \varphi)$$

Again when $c = g \cdot I \cdot R$ is substituted, supply current can be eliminated from the equation. Similarly $\frac{dV_C(\pi)}{d\theta} = 0$ condition is independent of the supply current and voltage. We get

(4.40) $$g = \frac{-1}{\sin(\varphi)}$$

If we substitute this into previous one

(4.41) $$\frac{-1}{\sin(\varphi)} = \frac{\pi + R_{ON} B}{R_{ON} B \sin(\varphi) + 2\cos(\varphi)}$$

collecting sine and cosine terms and dividing we get

(4.42) $$\tan(\varphi) = \frac{-2}{\pi + 2R_{ON} B}$$

In this equation only unknown is B. R_{ON} is the design choice.

Again substitute second condition on *g* into eq. (3.15).

(4.43) $$\frac{-1}{\sin(\varphi)} = \frac{\pi \sin(\varphi_1) + 2\cos(\varphi_1)}{\frac{\pi}{2}\cos(\psi) + 2\cos(\varphi)\sin(\varphi_1) + 2BR_{ON}\sin(\varphi)\sin(\varphi_1) + \frac{\pi}{2}BR_{ON}\sin(\psi)}$$

Using trigonometric expansions and collecting $\sin(\psi)$ and $\cos(\psi)$ terms, then dividing one by one we can obtain $\tan(\psi)$.

$$\tan(\psi) = \frac{\frac{\pi}{2}\cos(2\varphi) - 2\sin(2\varphi) - \pi - R_{ON}B + R_{ON}B\cos(2\varphi)}{\frac{\pi}{2}\sin(2\varphi) + 2\cos(2\varphi) + \frac{\pi}{2}R_{ON}B + R_{ON}B\sin(2\varphi)} \tag{4.44}$$

Right side unknowns are B and φ. R_{ON} is the design parameter. Note that this equation neither depends on supply current nor supply voltage.

Similarly, when (4.40) is substituted into (4.27)

(4.45)

$$\frac{-1}{\sin(\varphi)} = \frac{\pi\cos(\varphi_1) - 2\sin(\varphi_1)}{p\pi BR - \frac{\pi}{2}\sin(\psi) + 2\cos(\varphi)\cos(\varphi_1) + 2BR_{ON}\sin(\varphi)\cos(\varphi_1) + \frac{\pi}{2}BR_{ON}\cos(\psi)}$$

is obtained. Applying trigonometric expansions and arranging terms, following equation is obtained.

(4.46)

$$\cos(2\varphi)\left[2\cos(\psi) + (B.R_{ON} + \frac{\pi}{2})\sin\psi\right] + \sin(2\varphi)\left[-2\sin(\psi) - (B.R_{ON} - \frac{\pi}{2})\cos(\psi)\right]$$

$$= \frac{-\pi B.R_{ON}}{2}\cos(\psi) + (\pi + B.Ron)\sin(\psi) - p.\pi.B.R$$

4.2.5 Obtaining The High Efficiency Solution

So far we obtained the closed form equations of the lossy circuit model. These closed form equations are not suitable for obtaining a solution. We will use a numerical solution technique to obtain the desired circuit element values.

Equations (4.11), (4.42), (4.44) and (4.46) forms a system of equations that is suitable for a numerical solution using iteration technique. R and R_{ON} are the design parameters. Iteration starts with an initial guess of the variable B. φ is obtained

using (4.42). Then B and φ is substituted into (4.44) to obtain ψ. p is calculated using (4.11). And all these variables are substituted into (4.27). If the equation is not satisfied, B is swept and the iteration goes on like this until (4.27) is satisfied in an error range.

For the numerical solution, MATLAB function *fzero* is used. *fzero* finds a zero of a function of one variable. A starting point is supplied as a parameter to *fzero.* This starting point is the solution of B without R_{ON} resistance because of the reason that the new solution is close to the solution without R_{ON} resistance.

Following drawings are obtained using drawPlots function in M-File 1 DrawPlots.m for the load resistance of 20 ohm.

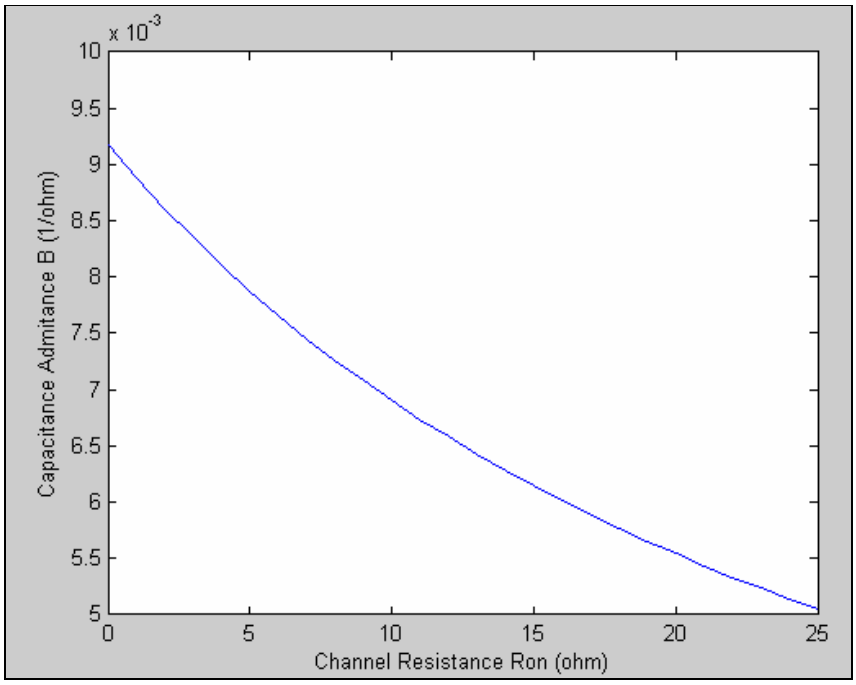


Figure 4-1 Capacitance Admittance vs. Channel Resistance

In Figure 4-1 capacitance admittance change with respect to channel resistance can be seen. Effect of the channel resistance dramatically changes the capacitance admittance satisfying the high efficiency conditions. Capacitance admittance value for zero ohm channel resistance is equal to the solution eq. (3.46) in the previous chapter for 20 ohm load resistance. This also verifies the numerical solution.

(4.47) $$\frac{1}{5.4466R} = 9.18x10^{-3}\,siemens$$

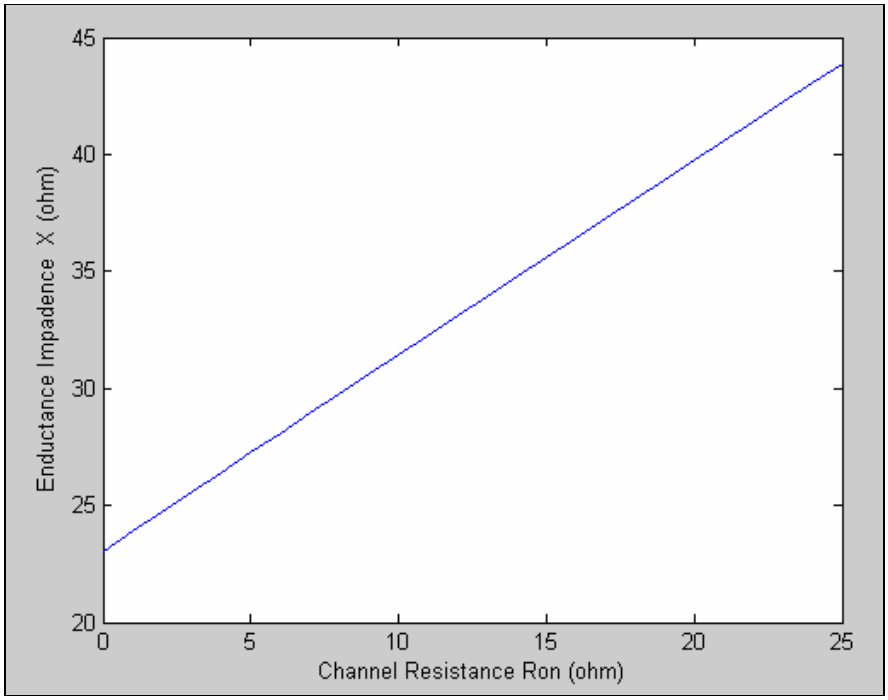


Figure 4-2 Inductance Impedance vs. Channel Resistance

Figure 4-2 shows the dependence of the inductance impedance to channel resistance. Again inductance impedance at zero channel resistance matches to the solution in the previous chapter eq. (3.51), which verifies the numerical solution.

(4.48) $$X = R\tan\psi = 1.1525R = 23.05 ohms$$

Figure 4-3 and Figure 4-4 show the dependence of the phi and ksi angles to channel resistance. Their values at zero channel resistance are equal to solutions in the previous chapter.

(4.49) $$\varphi = -32.482° = -0.56691 rad$$

(4.50) $$\psi = \arctan\left[\frac{\pi}{8}\left(\frac{\pi^2}{2} - 2\right)\right] = 49.052° = 0.85613 rad$$

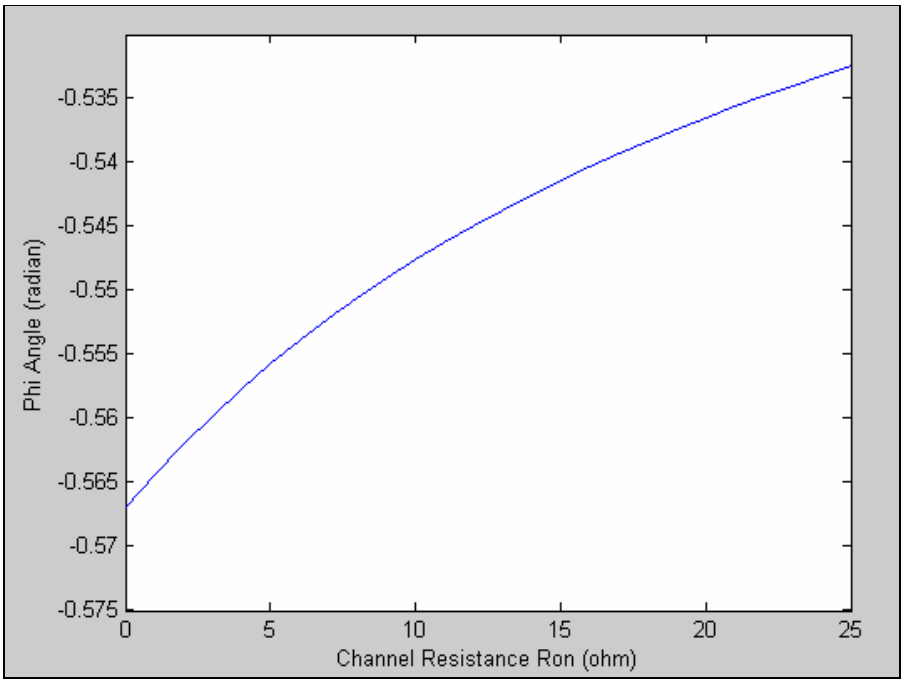


Figure 4-3 Phi angle vs. Channel Resistance

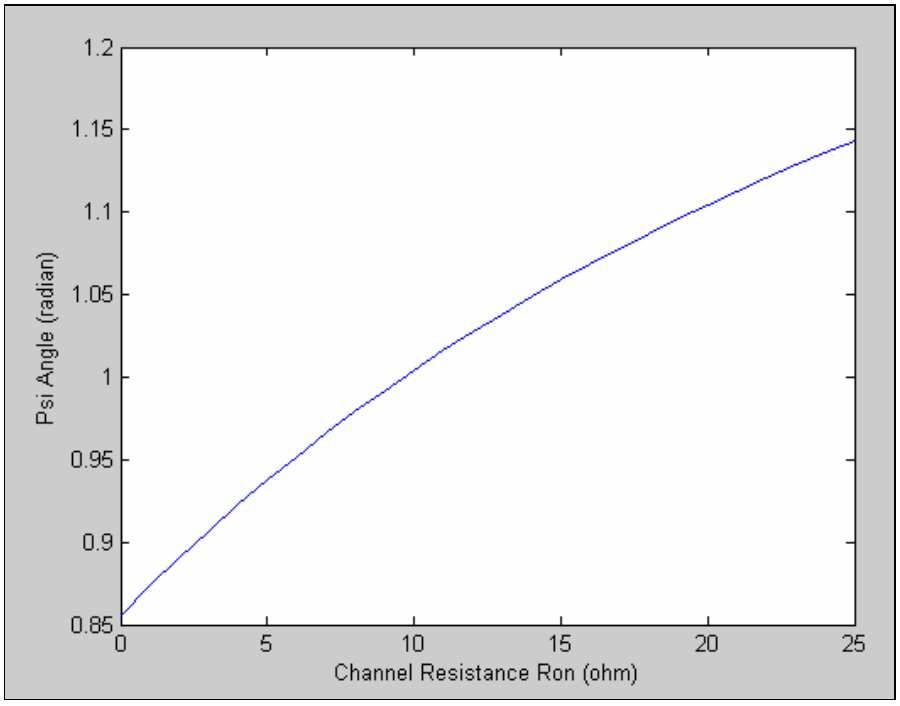


Figure 4-4 Psi angel vs. Channel Resistance

4.2.6 The Efficiency

So far we talked about the high efficiency but never figured it out. Efficiency is the ratio of the output power to the input power and can be calculated as in the previous chapter eq.(3.28)

$$\eta = \frac{P_o}{P_i} = \frac{g^2}{2}\frac{R}{R_{dc}} \tag{4.51}$$

and R_{dc} is calculated as

$$R_{dc} = \frac{V_{cc}}{I} \tag{4.52}$$

since dc resistance of the L1 BFL is zero, V_{cc} is equal to the dc component of the capacitor voltage and it is calculated by integrating the capacitance voltage through the whole cycle.

$$V_{CC} = \frac{1}{2\pi}\int_0^{\pi} V_{C,OFF} + \frac{1}{2\pi}\int_{\pi}^{2\pi} V_{C,ON} \tag{4.53}$$

for the $V_{C,OFF}$

$$\frac{1}{2\pi}\int_0^{\pi} V_{C,OFF} = \frac{I}{2\pi B}\int_0^{\pi}\left[\theta + g\cos(\theta+\varphi) - g\cos(\varphi) + B.R_{on} - g.B.R_{on}\sin(\varphi)\right]d\theta \tag{4.54}$$

$$= \frac{I}{2\pi B}\left[\frac{\pi^2}{2} - 2g\sin\varphi - \pi.g\cos(\varphi) + \pi.B.R_{on} - \pi.g.B.R_{on}\sin(\varphi)\right] \tag{4.55}$$

and for the $V_{C,ON}$

$$\frac{1}{2\pi}\int_{\pi}^{2\pi} V_{C,ON} = \frac{I}{2\pi B}\int_{\pi}^{2\pi}[B.R_{on} - g.B.R_{on}\sin(\theta+\varphi)]d\theta \tag{4.56}$$

$$= \frac{I}{2\pi B}\left[\pi.B.R_{ON} + 2g.B.R_{ON}\cos(\varphi)\right] \tag{4.57}$$

by summing these two

$$V_{CC} = \frac{I}{2\pi.B}\left[2\pi.B.R_{ON} + \frac{\pi^2}{2} - g\sin(\varphi)(2+\pi.B.R_{ON}) - g\cos(\varphi)(\pi - 2B.R_{ON})\right] \tag{4.58}$$

(4.59)

$$R_{eq} = \frac{V_{CC}}{I} = \frac{1}{2\pi.B}\left[2\pi.B.R_{ON} + \frac{\pi^2}{2} - g\sin(\varphi)(2+\pi.B.R_{ON}) - g\cos(\varphi)(\pi - 2B.R_{ON})\right]$$

and by substituting (4.40)

$$R_{eq} = \frac{1}{2\pi.B}\left[2 + 3\pi.B.R_{ON} + \frac{\pi^2}{2} + \frac{\cos(\varphi)}{\sin(\varphi)}(\pi - 2B.R_{ON})\right] \tag{4.60}$$

4.2.7 Solution Results

Figure 4-5 shows the equivalent DC resistance vs. channel resistance (Ron) plot. It has a linear dependence to channel resistance Ron.

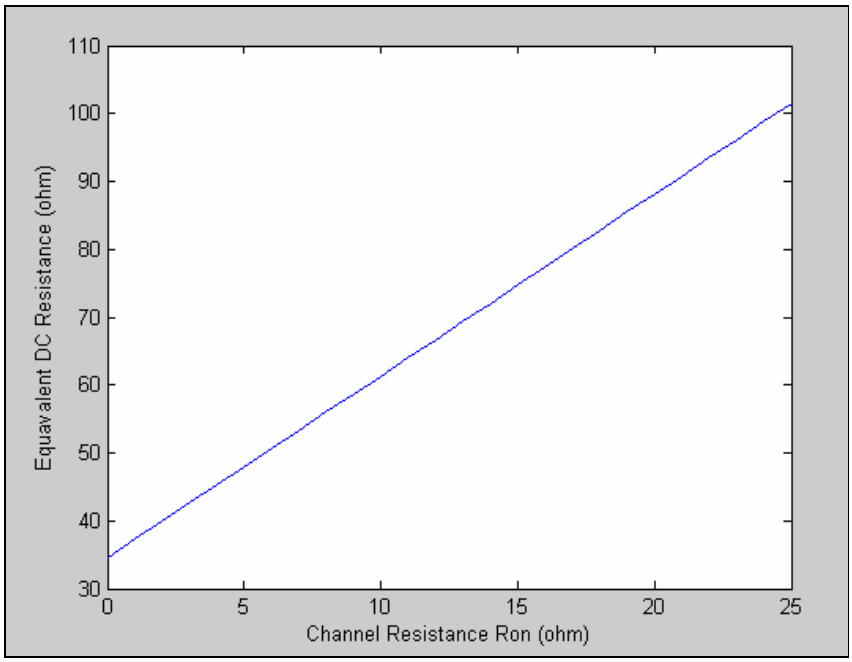


Figure 4-5 Equivalent DC Resistance vs. Channel Resistance Ron

DC supply current plot can be easily obtained using (4.59)

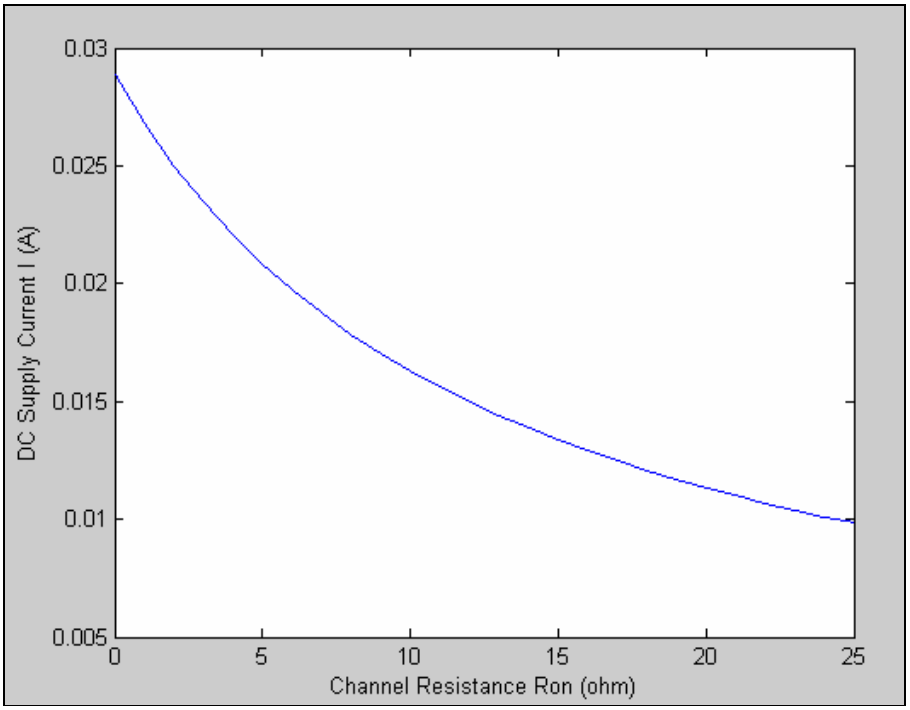


Figure 4-6 DC Supply Current vs Channel Resistance

As the R_{ON} channel resistance increases, voltage on the drain node of the transistor increases in the ON phase for a particular output voltage. This increases the average voltage on the drain node for a particular DC current, which causes the increase of the equivalent DC resistance.

Fundamental component of the drain voltage decreases as the voltage level in the ON phase increases with the increasing channel resistance. This causes a decrease on the output voltage shown in Figure 4-7.

Figure 4-8 shows the channel resistance dependence of the efficiency. In fact only source of the dissipation is the channel resistance since the high efficiency conditions are satisfied. Input output and the dissipated power plots are shown in Figure 4-9.

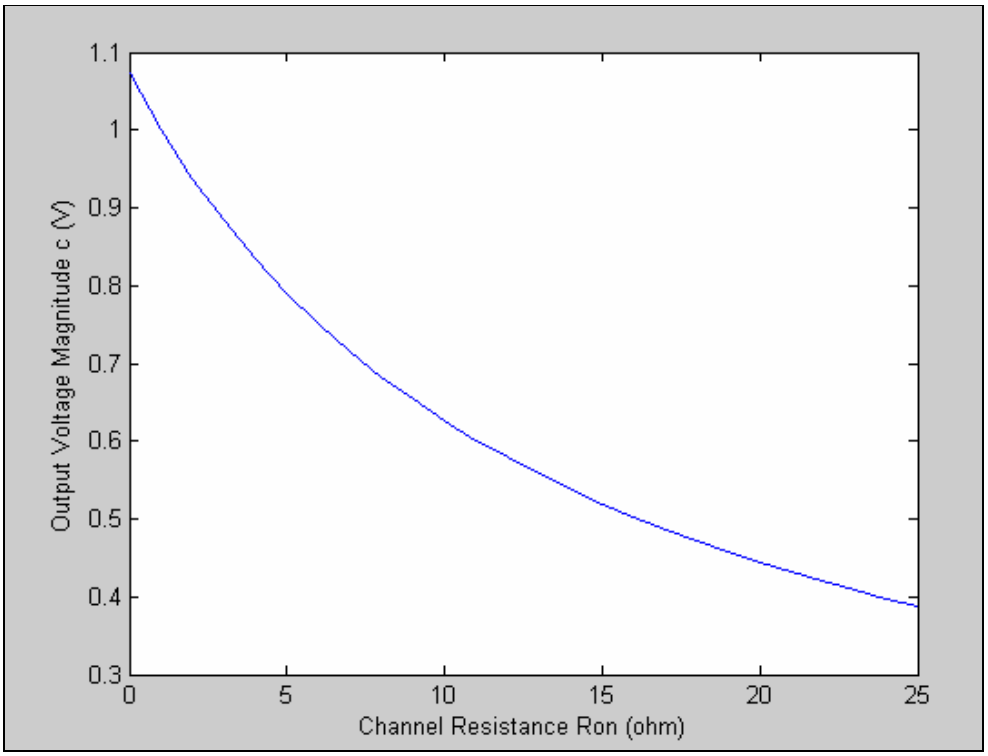


Figure 4-7 Output Voltage Magnitude vs. Channel Resistance

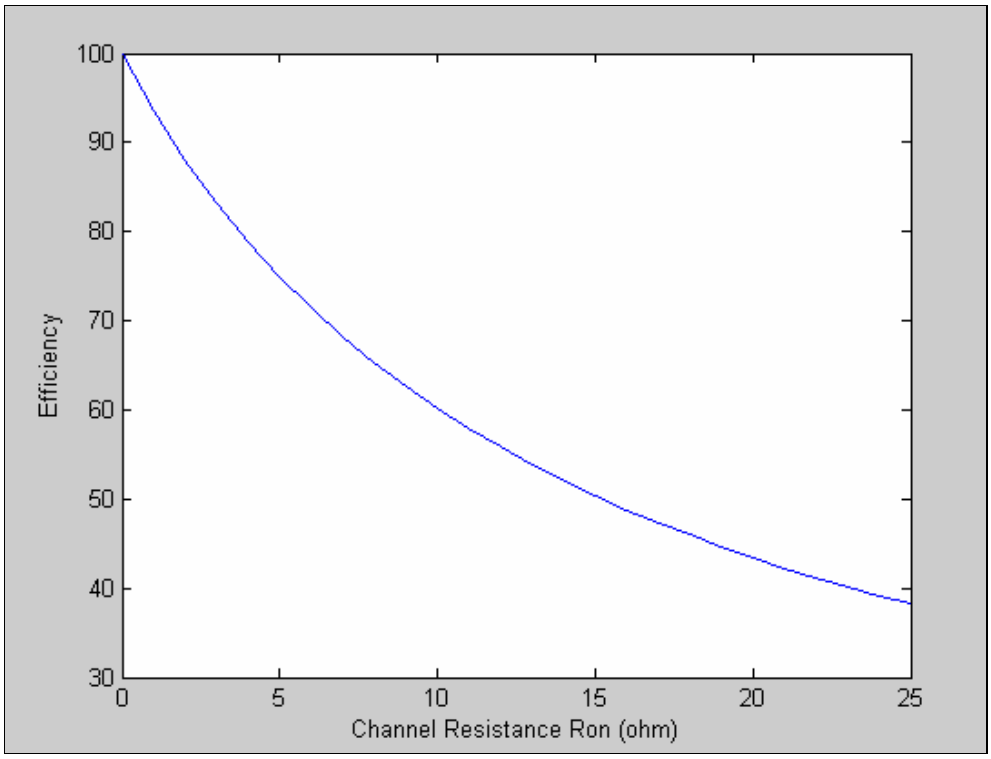


Figure 4-8 Efficiency (%) vs. Channel Resistance (ohm)

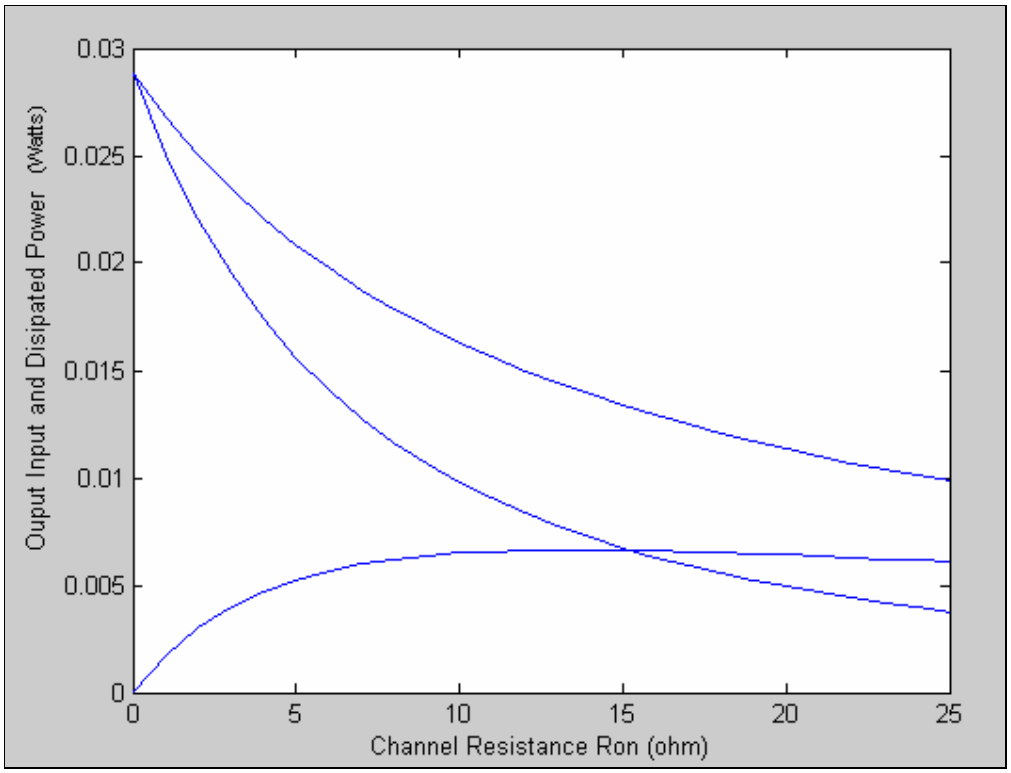


Figure 4-9 Input Output and Dissipated Power vs. Channel Resistance

Channel resistance decreases the efficiency. This is an expected result. As the channel resistance is increased the efficiency is decreased. This is because channel resistance dissipates power on itself when the transistor is ON.

Input power decreases since the equivalent DC resistance of the circuit increases as the channel resistance increases. This causes less power to be drawn from the voltage source. Since the efficiency decreases too, output power is further decreased. This means high voltage source is needed for a particular output power as the channel resistance increases.

MATLAB solutions of the equations are given as tabulated in Table (4-1). This table shows the solutions of the admittance of the capacitor and impedance of the X. Capacitor and the inductor values are given for the frequency of 100 MHz.

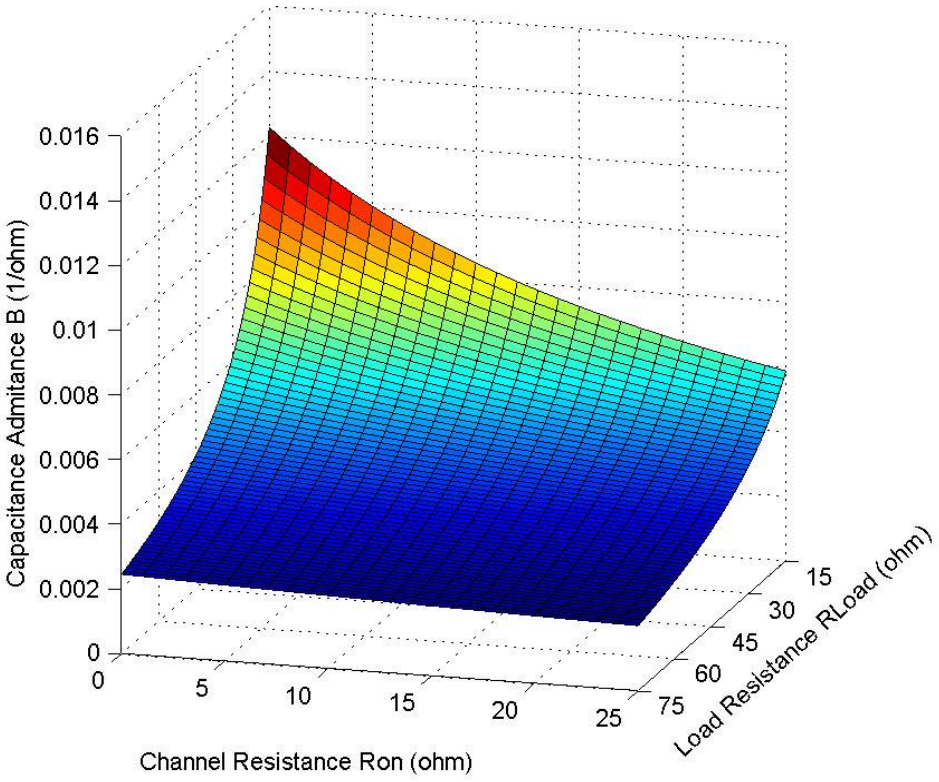


Figure 4-10 Capacitance Admittance (B) vs Channel Resistance (Ron) and Load Resistance (Rload)

In the Figure 4-10 the relation of the channel resistance and load resistance can be seen. For the small values of the load resistance channel resistance changes the values of the capacitance admittance very much. However for the higher values of the load resistance, change in the capacitance admittance is very small. This means that in order the channel resistance to affect the circuit operation, its value must be comparable to the value of the load resistance.

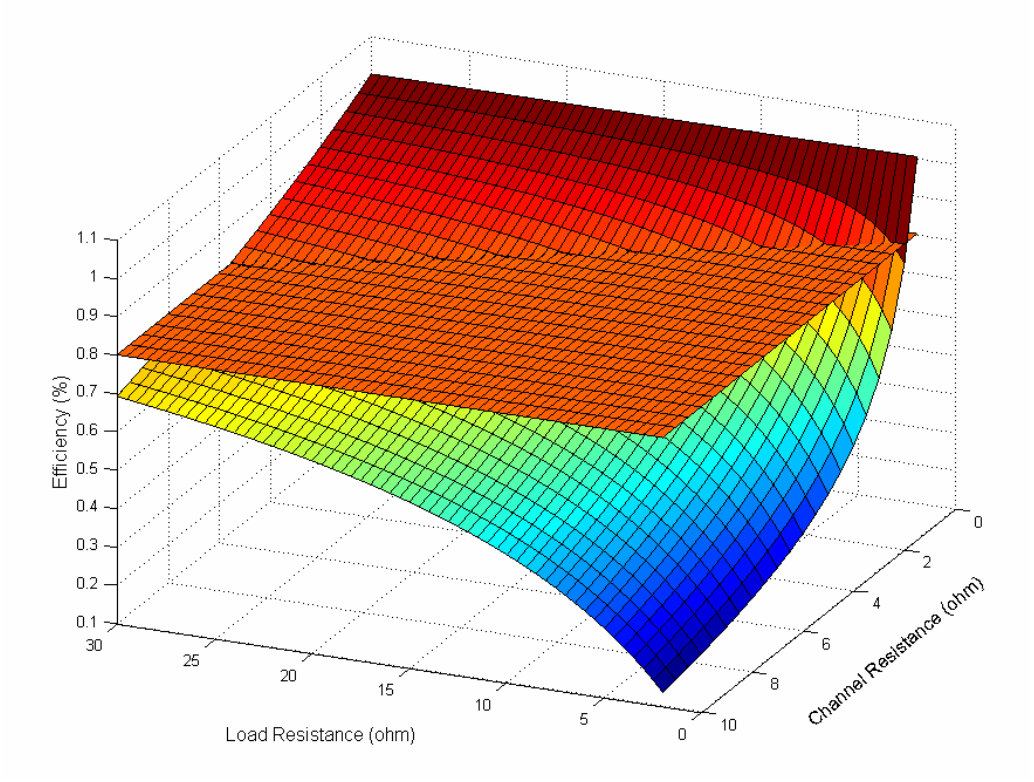


Figure 4-11 Efficiency (%) vs Load Resistance (ohm) and Channel Resistance (ohm) with the intersection of constant %80 efficiency surface

Figure 4-11 shows the efficiency dependence on channel resistance and load resistance. As it can be easily noticed, efficiency dramatically drops with channel resistance at small load resistances. However at higher load resistance values efficiency decreases slower with the increasing channel resistance. A constant efficiency surface at 80% is also drawn in the Figure 4-11. In order to obtain efficiency higher than 80%, load resistance and channel resistance values must be behind the intersection line of the two surfaces. Projection of the intersection of the efficiency plot with various constant efficiencies are shown in Figure 4-12.

Area under the lines represents higher efficiencies and area above the lines represents lower efficiencies. For a particular load resistance, channel resistance is limited by the desired efficiency. Figure 4-12 can be used in rough estimation of the efficiency from load and channel resistances.

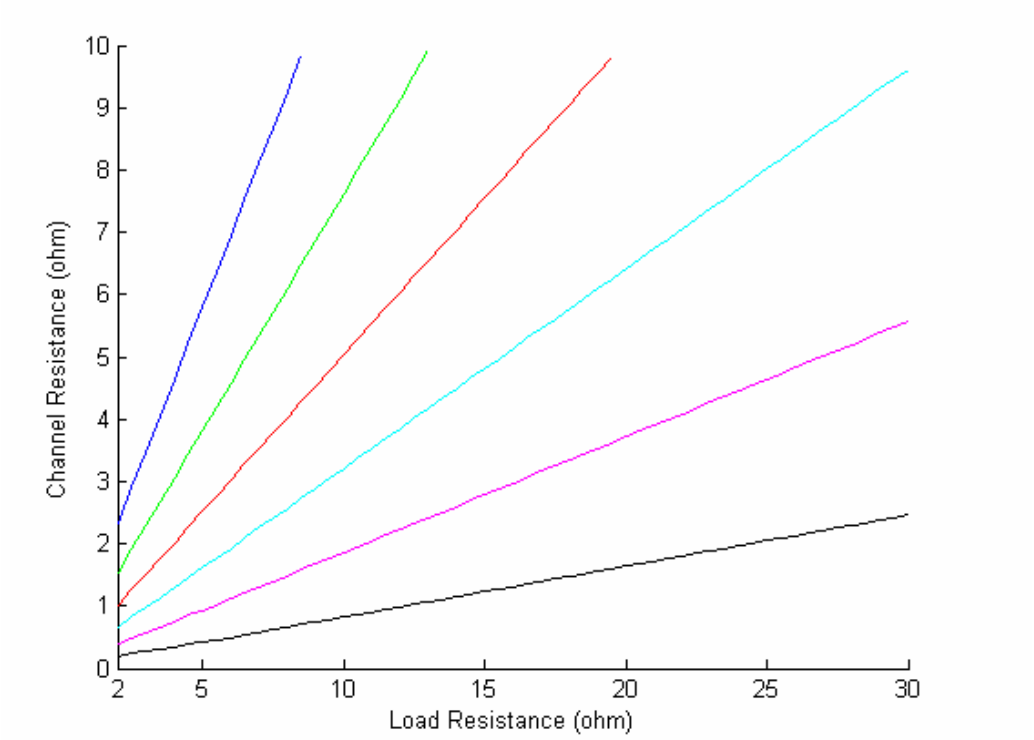


Figure 4-12 Load Resistance (ohm) vs Channel Resistance (ohm) for constant efficiencies, blue %40, green %50, red %60, cyan %70, purple %80, black %90

4.3 Simulation Results

In order to verify the solutions found in this chapter, the model circuit has been simulated at 100 MHz for the gray shaded values of the Ron resistance in Table 4-1. Tabulated capacitance and inductance values in Table 4-1 have been used for 9 different simulation runs.

To be able to compare the obtained results with the solution ignoring the effect of the Ron resistance, circuit has been simulated for the same values of the Ron resistance, but using capacitance and inductance values from the solution assuming zero channel resistance.

Table 4-1 Tabulated Solution of the Component Values for 100MHz

Ron	B (mS)	X (ohm)	C (pF)	L (nH)
0	9,180	23,05	14,61	36,69
1	8,884	23,89	14,14	38,03
2	8,608	24,74	13,70	39,37
3	8,349	25,58	13,29	40,71
4	8,105	26,42	12,90	42,05
5	7,876	27,26	12,53	43,38
6	7,659	28,10	12,19	44,72
7	7,455	28,93	11,86	46,05
8	7,261	29,77	11,56	47,38
9	7,077	30,60	11,26	48,71
10	6,903	31,44	10,99	50,04
11	6,737	32,27	10,72	51,36
12	6,579	33,10	10,47	52,69
13	6,429	33,94	10,23	54,01
14	6,285	34,77	10,00	55,34
15	6,148	35,60	9,785	56,66
16	6,016	36,43	9,576	57,98
17	5,891	37,26	9,376	59,30
18	5,770	38,09	9,184	60,62
19	5,655	38,92	9,000	61,94
20	5,544	39,75	8,823	63,26
21	5,437	40,57	8,653	64,58
22	5,334	41,40	8,490	65,89
23	5,236	42,23	8,333	67,21
24	5,140	43,06	8,181	68,53
25	5,049	43,88	8,035	69,84

Figure 4-3 shows the circuit diagram used for the simulations. S1 switch is used to model the switching transistor behavior. R6 resistance models the channel resistance. A 100 MHz signal source is used as the driving signal. In order to obtain the normalized currents and voltages 1V voltage supply is used. C1 and L2 are the tuning capacitance and inductance. C2 and L3 form the tank circuit tuned at the operating frequency. For obtaining the closer results to solutions, an exaggerated high Q value has been used. Load resistance has been chosen as 20 ohms. Colored voltage and current markers show the measurement points.

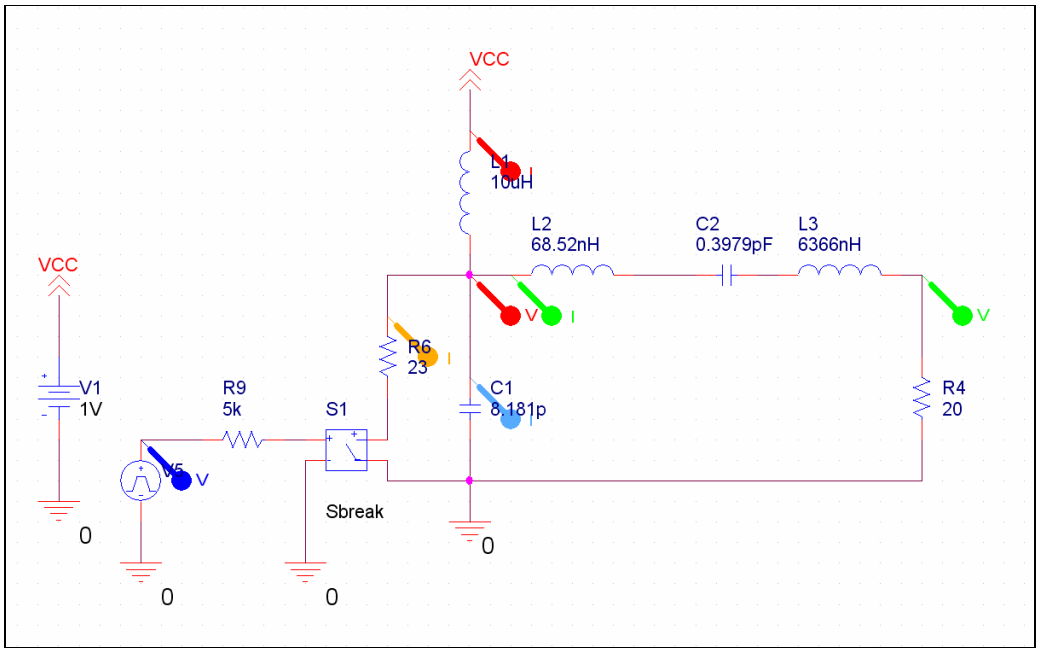


Figure 4-3 Simulation Circuit Diagram

Figure 4-13 shows the simulated current and voltages in the circuit for the 24 ohm channel resistance. The plots of the currents are on the top and the plots of the voltages are on the bottom. Blue voltage plot shows the driving signal. Switch is closed at zero volt and open at 1 volt. Voltage on the terminals of the switch (meanwhile on the terminals of the capacitance) is drawn red. When the switch is on this is the voltage on the channel resistance due to the sinusoidal output current. (yellow current plot). However, the switch is off this current flows into the capacitance (blue current plot). This is the charge and the discharge current of the capacitor. As can be seen, this voltage excellently drops to zero at the time of the switch turn on. Meanwhile capacitor current, which is the slope of the capacitor voltage, is zero. This verifies our solution for the 24 ohm channel resistance.

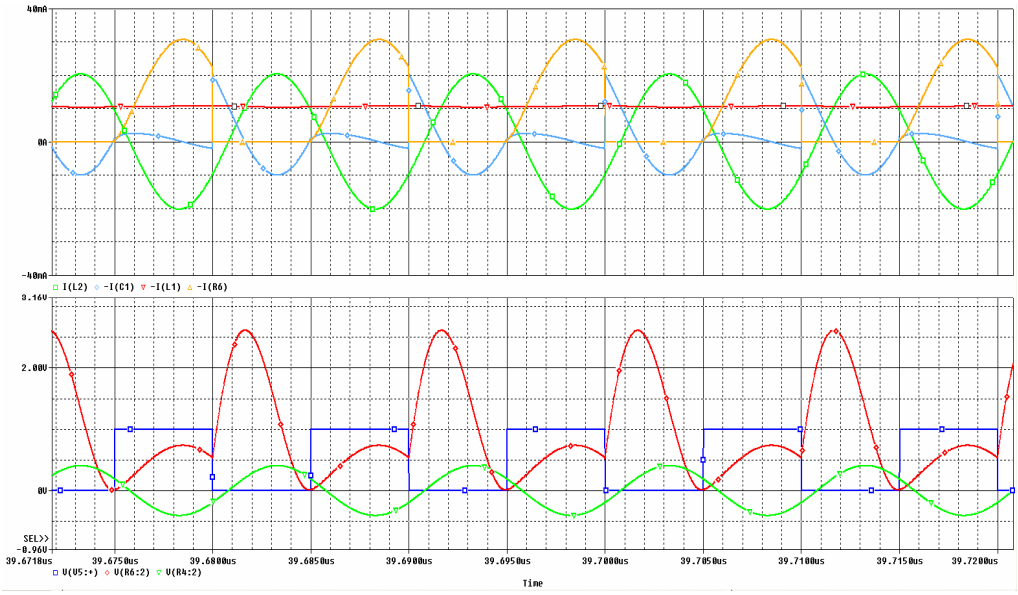


Figure 4-13 Simulated currents and voltages for 24 ohm channel resistance vs. time

Simulations are performed for the 9 different channel resistance values from 1 ohm to 25 ohms. In these simulations calculated tuning capacitance and inductance values, tabulated in Table 4-1, are used.

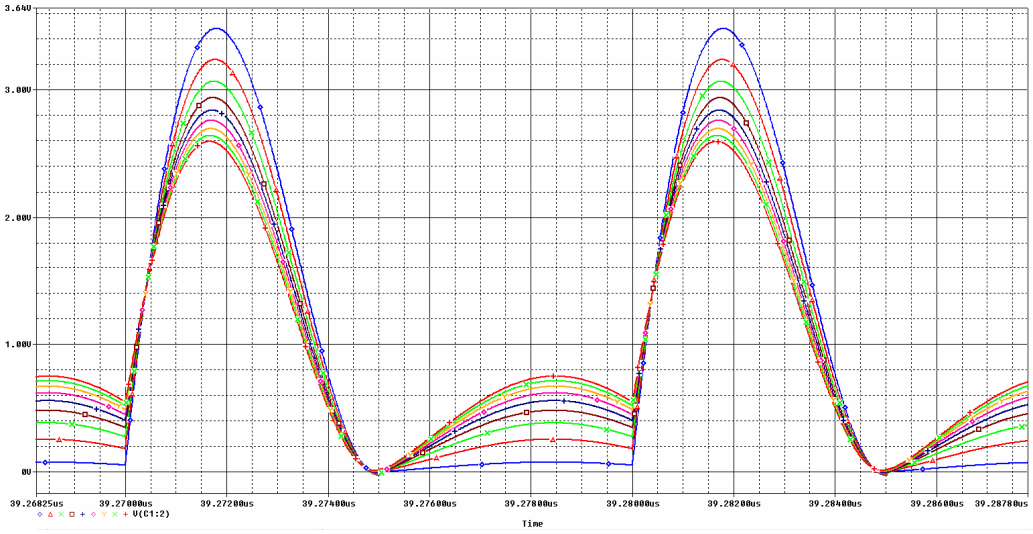


Figure 4-14 Capacitor voltage for different channel resistance values vs. time

Figure 4-14 shows the voltage on the terminals of the switch (meanwhile on the terminals of the capacitor). Even if the capacitor voltage is not zero at the time of the switch turn off, it excellently drops to zero with zero-slope at the time of turn on,

which satisfies our high efficiency conditions for every value of the channel resistance.

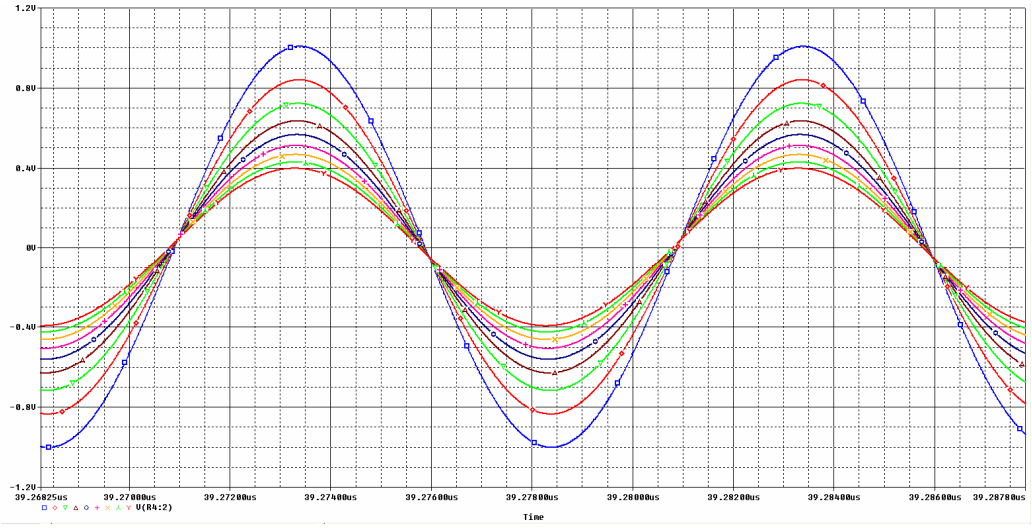


Figure 4-15 Output voltage for different channel resistance values vs. time

Figure 4-15 shows the output of the circuit for the different channel resistance values. Output voltage decreases as the channel resistance is increased. Phase lags very little.

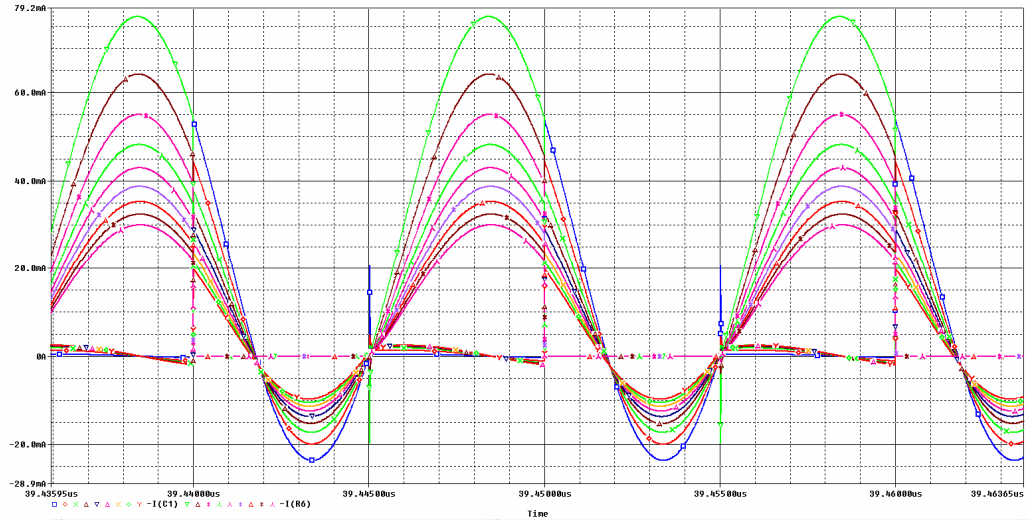


Figure 4-16 Capacitor and switch currents for different channel resistance values vs. time

Figure 4-16 capacitor and switch currents are plotted together. These two currents completes each other and forms a smooth sine curve with a dc offset, where the dc offset is the supply current and sine current is the load current. When switch is

open, this current flows into capacitor and when the switch is closed this current flows into switch and the channel resistance. At the time of the switch turn on, capacitor current, in fact, the slope of the capacitor voltage, is zero. In this plot it is evident that there is a close relation among ac current, dc current and the phase of the ac current in order to satisfy zero current condition at the device turn on. This relation was given as Equation (4.40).

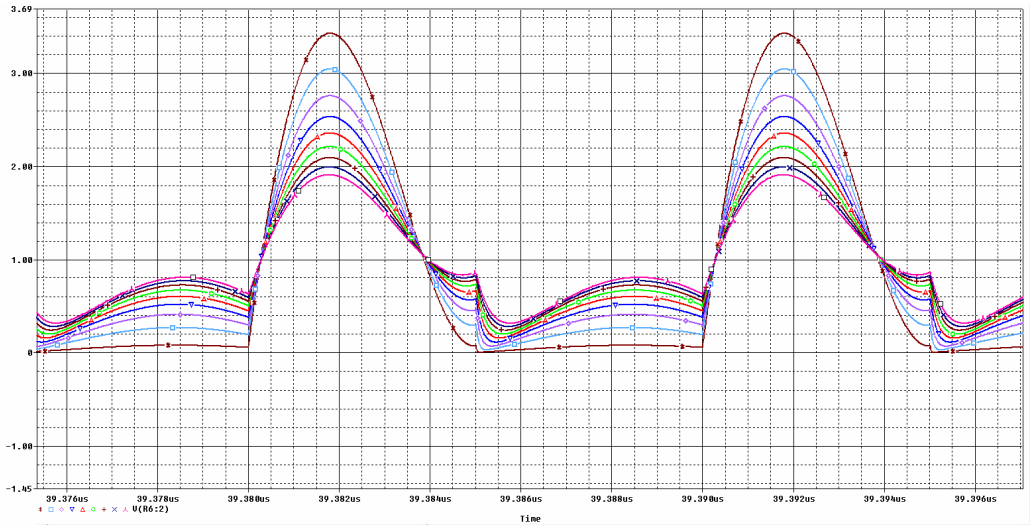


Figure 4-17 Capacitor voltage for different channel resistance values when channel resistance is ignored in class-E calculations

Another set of simulations performed is simulating different channel resistance values with the classical class-E calculations. In these calculations channel resistance is assumed to be zero, and therefore when the switch is turned off capacitor voltage is taken to be zero. However, this is not the case when a channel resistance exists in the switch, which leads to miss operation of the circuit.

Figure 4-17 shows the simulations of the circuit designed using classical class-E equations with the different channel resistance values. Capacitor voltage does not drop to zero at the time of the switch turn on, since the capacitor voltage at the turn off is none zero due to the none zero voltage drop on the channel resistance. This none zero voltage on the device turn on discharges over the device which leads to power dissipation on the switch. Figure 4-18 shows the current through the switch when the switch is ON. Current peaks when the switch is turn ON, this is the discharge current of the capacitor.

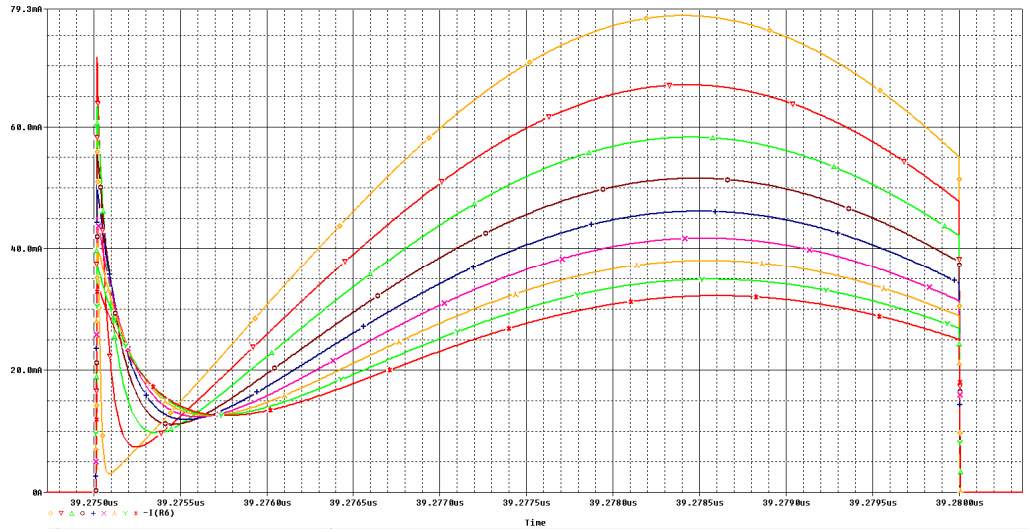


Figure 4-18 Switch current for different channel resistance values when channel resistance is ignored in class-E calculations

In Figure 4-19 capacitor and the switch currents are plotted together. Again these two plots complete each other and form a sine plot, which is the sum of the supply current and the ac load current.

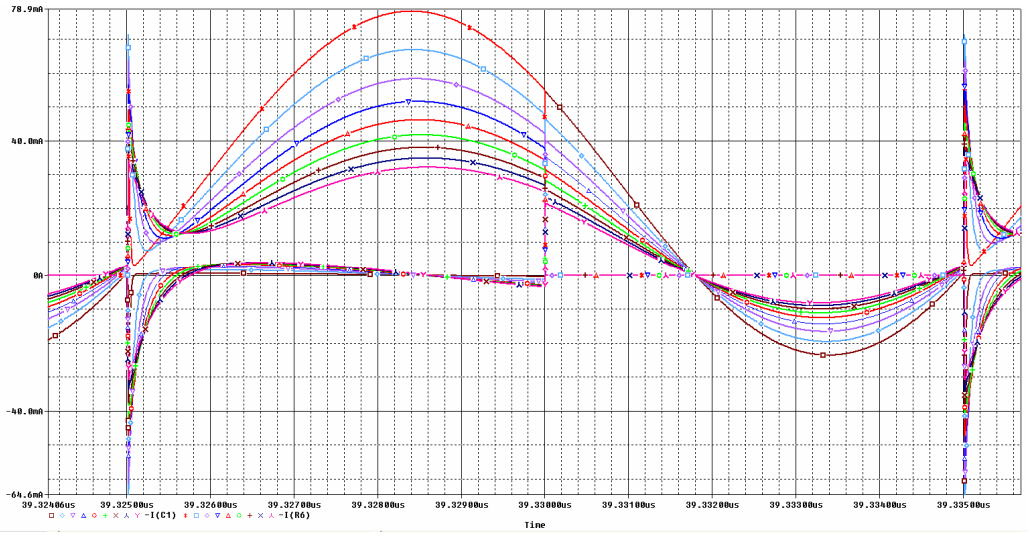


Figure 4-19 Capacitor and Switch currents for different channel resistance values when channel resistance is ignored in class-E calculations

Simulation results collected from simulations with new class-E design calculations and classical class-E design calculations are plotted together with the plots of the MATLAB equations. Straight blue lines are the plots of the MATLAB equations. Points marked with red circles are the simulation results of the circuits

designed with new equations which includes the effect of the channel resistance. Points marked with green triangles are the simulation results of the circuits designed with classical class-E equations.

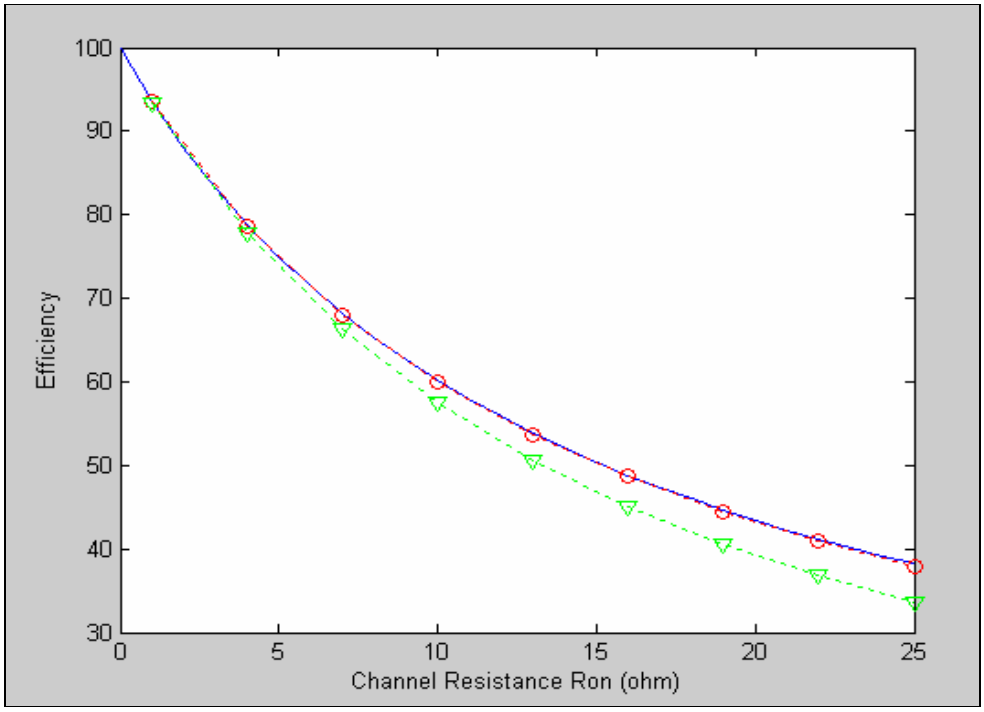


Figure 4-20 Efficiency: MATLAB solution plot (blue straight line), Simulation using class-E calculations with channel resistance (red circle) , Simulation using class-E calculations without channel resistance (green triangle)

Figure 4-20 is the plot of the efficiency vs. channel resistance. Efficiency is higher in the circuits designed with equations including channel resistance effect. Improvement on the efficiency is more effective when the channel resistance is comparable with the load. MATLAB solutions and the simulation results perfectly match for the efficiency calculations.

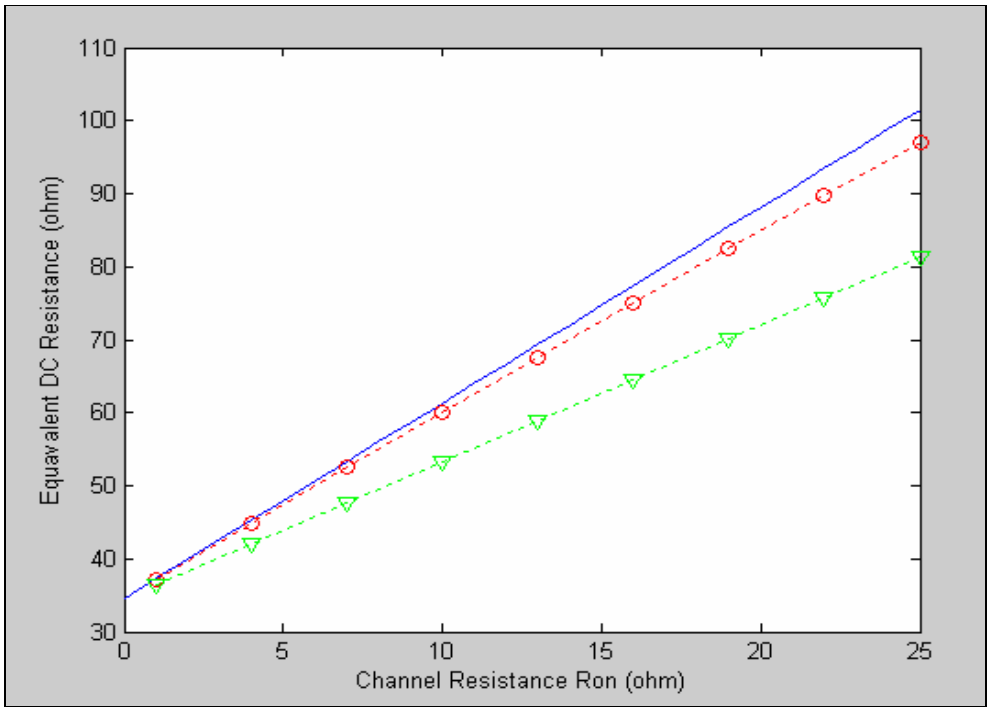


Figure 4-21 Equivalent DC Resistance: MATLAB solution plot (blue straight line), Simulation using class-E calculations with channel resistance (red circle) , Simulation using class-E calculations without channel resistance (green triangle)

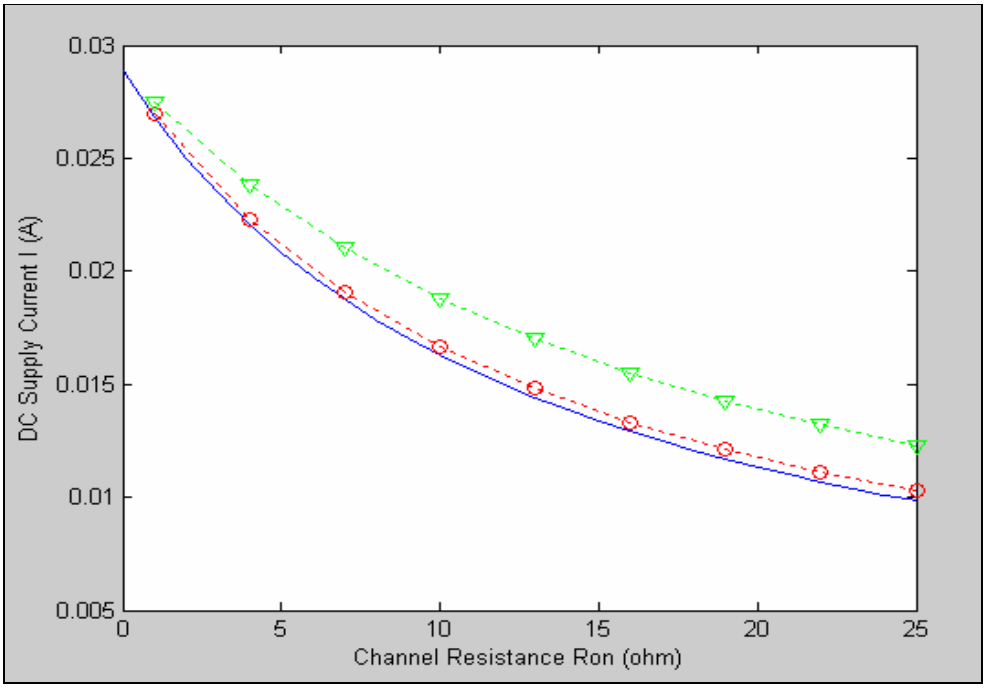


Figure 4-22 DC Supply Current : MATLAB solution plot (blue straight line), Simulation using class-E calculations with channel resistance (red circle) , Simulation using class-E calculations without channel resistance (green triangle)

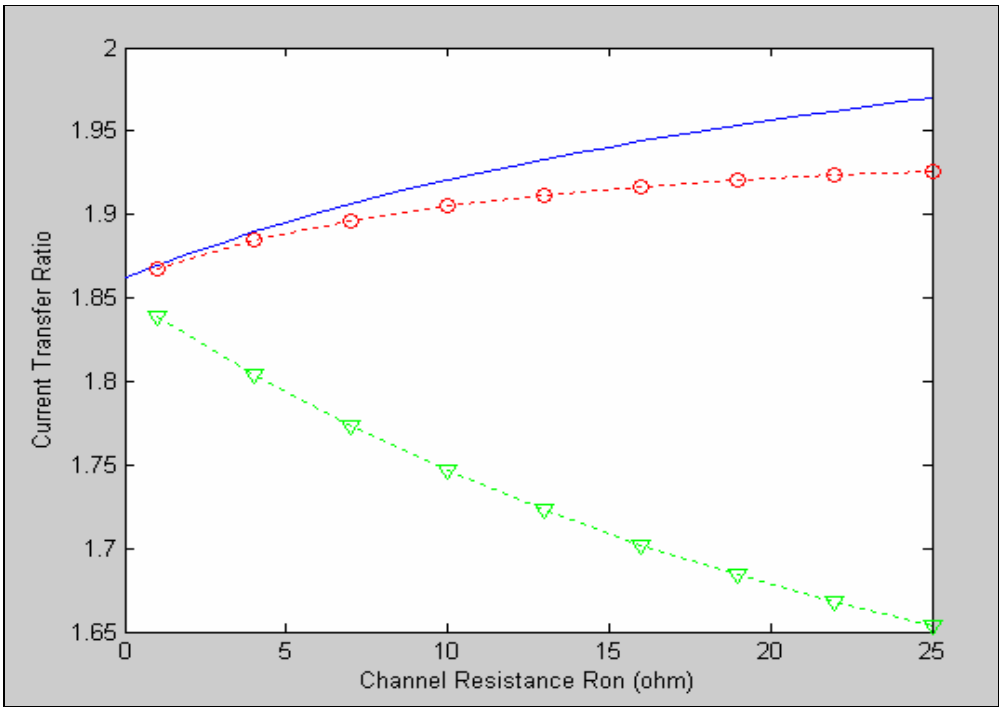


Figure 4-23 Current Transfer Ratio: MATLAB solution plot (blue straight line), Simulation using class-E calculations with channel resistance (red circle) , Simulation using class-E calculations without channel resistance (green triangle)

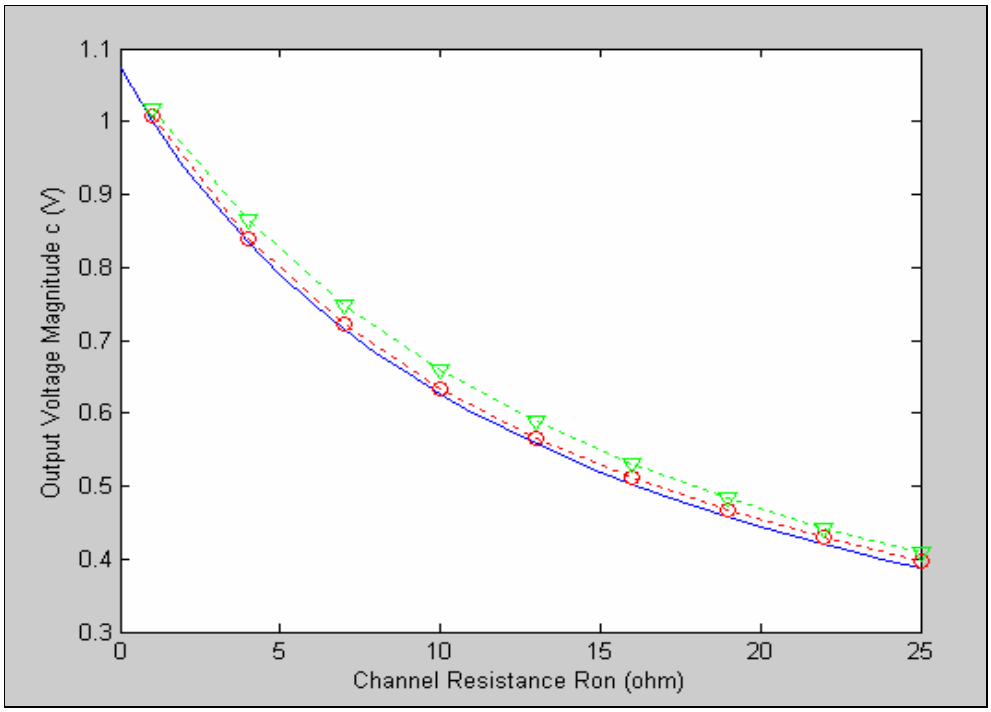


Figure 4-24 Output Voltage Magnitude: MATLAB solution plot (blue straight line), Simulation using class-E calculations with channel resistance (red circle) , Simulation using class-E calculations without channel resistance (green triangle)

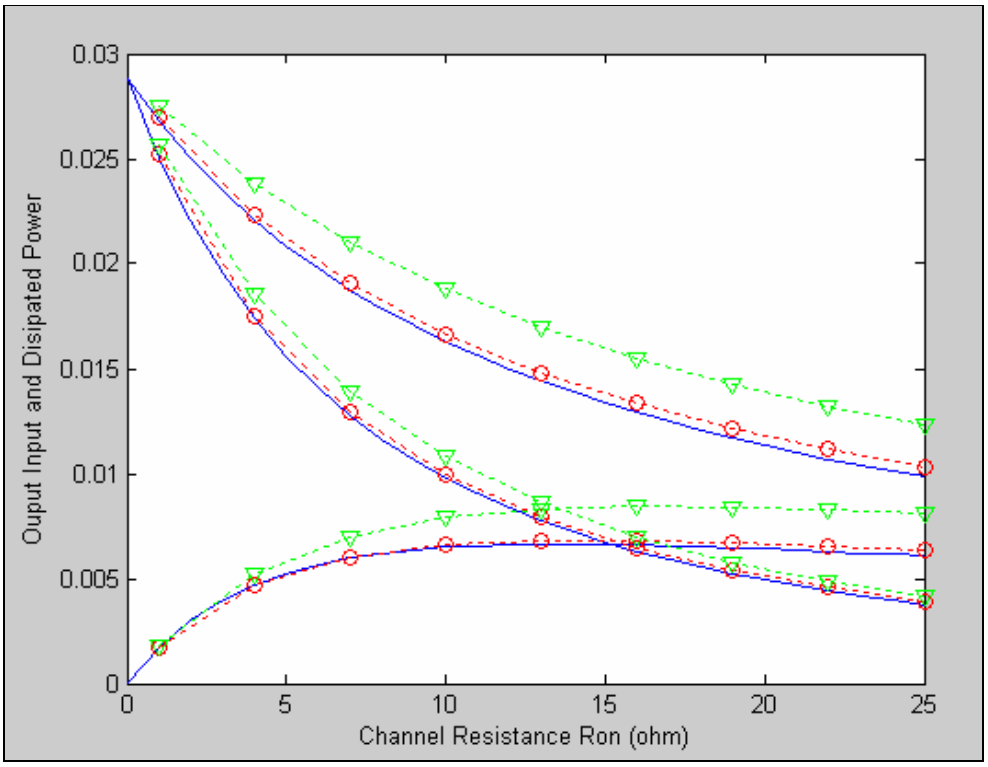


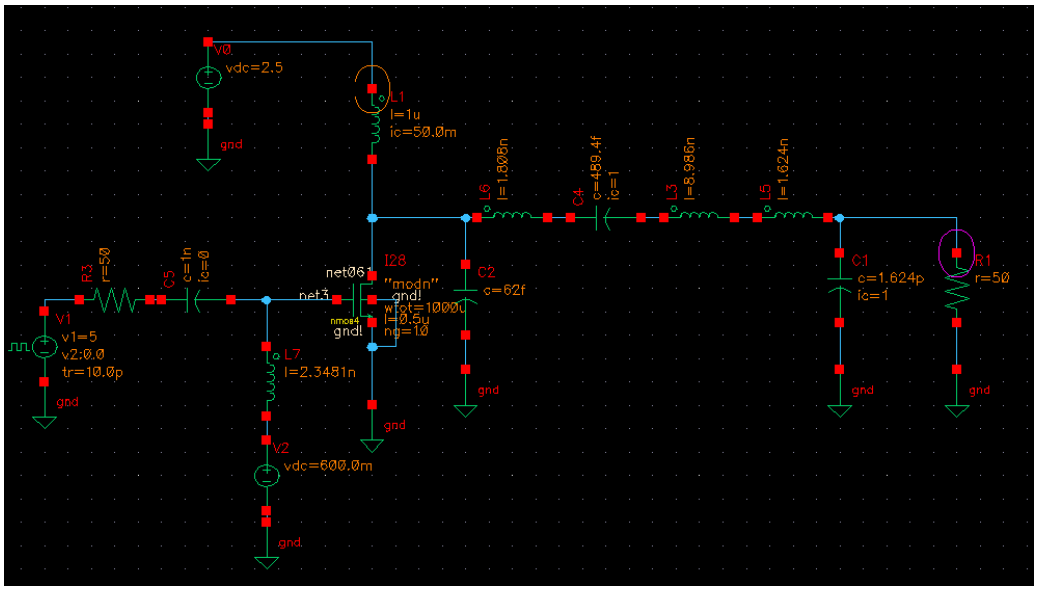
Figure 4-25 Input Output and Dissipated power: MATLAB solution plot (blue straight line), Simulation using class-E calculations with channel resistance (red circle) , Simulation using class-E calculations without channel resistance (green triangle)

CHAPTER 5

CMOS CLASS E AMPLIFIER DESIGN

5.1 Design of the Amplifier

A 0.1W 2.4 GHz power amplifier is designed and simulated for the AMS 0.35 CMOS process. Amplifier is designed to operate from a 2.5V power supply in order to demonstrate a method of design using the equations in Chapter 4. It must be noted that in this design some properties of the process are omitted for the sake of the simplicity of this demonstration. One of them is the oxide break down, others may exist.



Design process started with using classical class-E design equations since they are practical and straight forward to solve. According to voltage supply, output power and the estimated efficiency, load resistance value is determined, which is

then transformed to 50 ohm load resistance. Then approximate component values are obtained from the classical class-E equations [11][12]. Size of the transistor is selected according to the power requirements. Transistor's output capacitance and channel resistance is calculated. Calculated channel resistance is then used in the solution described in Chapter 4 and component values are obtained from this solution, Circuit is simulated in a BSIM3v3 simulator (spectre) with AMS 0.35 CMOS process parameters using these values.

L1 DC feed inductor which is supposed to be infinite will be made off chip, therefore it can be chosen as high as 1μH.

Gate terminal of the MOSFET is tuned with L7 which is connected to 600mV dc voltage supply. L7 resonates with the gate to source capacitance of the MOSFET and provides a means of matching.

We need to deliver 0.1W to the load using a 2.5 V power supply. Using (3.26) and (3.54)

$$P_O = \frac{1}{2}\frac{c^2}{R} = \frac{1}{2}\frac{(1.074)^2 V_{cc}^2}{R} = 0.5767\frac{V_{cc}^2}{R} \tag{5.1}$$

Assuming efficiency around 60%-70% target P_O is chosen around 0.12W-0.18 W and R is chosen as 20 ohm. This means that the Q of the transformation network will be small.

$$Q = \sqrt{\frac{50}{R} - 1} = 1.2247 \tag{5.2}$$

But load resistance can not be chosen smaller since this will increase the output power. Therefore we will put an additional tank circuit to increase the quality factor. But the loss in the tank circuit's inductor is a problem.

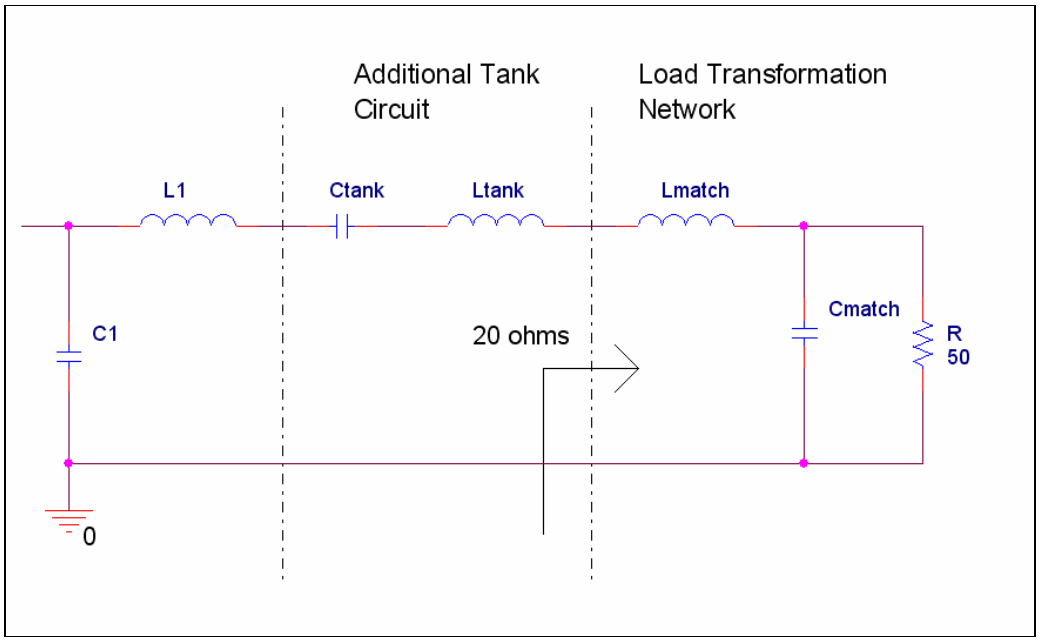


Figure 5-1 Output Network of the Class E Amplifier

Ratio of the loss in the parasitic resistance of the tank circuit's inductor to the output power is,

$$\frac{P_{Loss,TankInductor}}{P_{Output}} = \frac{R_{L,Tank}}{R_{Load}} \tag{5.3}$$

Quality factor of the tank circuit is

$$Q = \frac{wL_{Tank}}{R_{Load} + \frac{wL_{Tank}}{Q_{L,Tank}}} \tag{5.4}$$

where $Q_{L,Tank}$ is the quality factor of the tank circuit's inductor. Manipulating the equation and leaving the wL_{Tank} alone on the right side we get;

$$wL_{Tank} = \frac{QR_{Load}}{1 - \frac{Q}{Q_L}} \tag{5.5}$$

Since

$$R_{L,Tank} = \frac{wL_{Tank}}{Q_L} = \frac{\frac{Q}{Q_L} R_{Load}}{1 - \frac{Q}{Q_L}} \tag{5.6}$$

then the ratio of the loss in the parasitic resistance of the tank circuits inductor to the output power is;

$$\frac{P_{Loss,TankInductor}}{P_{Output}} = \frac{R_{L,Tank}}{R_{Load}} = \frac{\frac{Q}{Q_L}}{1 - \frac{Q}{Q_L}} \tag{5.7}$$

As a design criteria, this ratio mustn't be higher than 20%, even which is a very high loss.

$$\frac{P_{Loss,TankInductor}}{P_{Output}} < 0.2 \tag{5.8}$$

$$\frac{\frac{Q}{Q_L}}{1 - \frac{Q}{Q_L}} < 0.2 \tag{5.9}$$

which results with

$$Q < \frac{Q_L}{6} \tag{5.10}$$

which means quality factor of the tank circuit can be maximum of the quality factor of the inductor. Austriamicrosystems provides some ready inductor with their simulation models in their analog development kit. In [16] these inductor values and quality factors are given. However even the high quality thick metal inductors give maximum quality factor of 11.9 which results quality around 2 in the tank circuit. Additionally these inductors are very small which requires small load resistances.

Bond wire inductors have a constant resistance to inductance ratio of 0.1ohm/nH, they have a quality factor of

$$Q_L = 2 \cdot \pi \cdot 2.4 \cdot 10^9 \cdot 1 \cdot 10^{-9} / 0.1 = 150$$

at 2.4GHz. Therefore bond wire inductors can produce quality factor up to 150/6=26.67 in the tank circuit. However this value requires very high inductor values for the load resistance of 20 ohm. Limiting the quality factor at 8 is sufficient, since it will produce errors less than 10 percent in the operation of the class E amplifier [17][18].

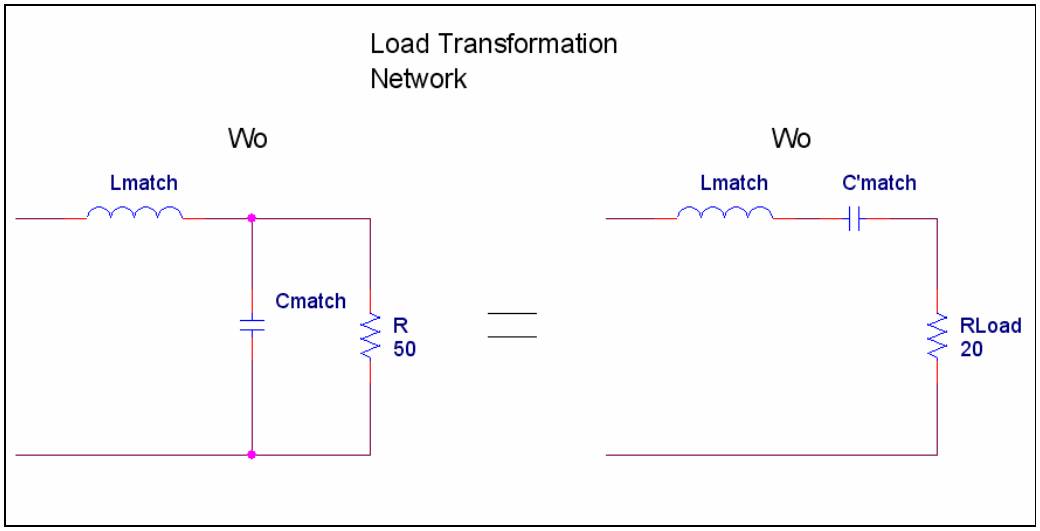


Figure 5-2 Load Transformation Network

Load transformation ratio is equal to

$$M = \frac{R}{R_{Load}} = \frac{50}{20} = 2.5 \tag{5.11}$$

Transformation inductance value is

$$wL_{match} = \sqrt{M - 1} R_{Load} = 24.49 \tag{5.12}$$

(5.13) $L_{match} = 1.624nH$

Transformation capacitance is

(5.14) $wC_{match} = \frac{\sqrt{M-1}}{R} = 24.49 \cdot 10^{-3}$

(5.15) $C_{match} = 1.624pF$

Considering the equivalent circuit of the transformation network, L_{match} - $L_{\tan k}$ and C_{match} - $C_{\tan k}$ are in series. Since they resonate individually at 2.4GHz, their series combination also resonates at 2.4GHz. This forms a tank circuit with a load of R_{Load}. Therefore total quality factor of the transformation circuit and the tank circuit is

(5.16) $wL_{Total} = \frac{Q_{Total} R_{Load}}{1 - \frac{Q_{Total}}{Q_L}}$

For $Q_{Total} = 8$, $L_{\tan k}$ is found as 8.986nH, and therefore $C_{\tan k} = 489.4fF$.

Size of the transistor is selected as 1000µm/0.5µm.

The drain junction-to-bulk capacitance of nMOS devices in a modern high-performance CMOS n-well process is the dominant parasitic [19]. Drain junction to bulk capacitance can be calculated using junction capacitance formula (2.15):

(5.17) $C \approx \frac{C_{j0}}{(1 - V_F / \phi)^n}$

Required process parameters are found in AMS 0.35µm CMOS process parameters document [20]. Area junction capacitance $AC_{j0} = 0.94fF / \mu m^2$, area grading coefficient $n = 0.34$, junction potential $\phi = 0.69V$. Junction capacitance highly depends on the junction potential, but here we will use capacitance at the average junction potential which is the supply voltage 2.5V. However this is reverse junction voltage so it must be taken as negative. So capacitance is

(5.18) $$C \approx \frac{1000\mu m \cdot 0.5\mu m \cdot 0.94 fF/\mu m^2}{(1-(-2.5V/0.69V))^{0.34}} = 279.3 fF$$

But there is also another capacitance C_{gd}, which is parallel to this capacitance when C_{gs} capacitance is tuned out with inductor L_7. The value of the capacitance can be calculated using overlap capacitance per channel width parameter supplied by AMS [20] .

(5.19) $$C_{gs} = C_{ox,ov}.W$$

(5.20) $$C_{gs} = 0.12 \cdot 1000 = 120 fF$$

So the total output capacitance is

(5.21) $$C_{total} = 400 fF$$

For the small drain to source resistance channel resistance can be formulated as follows.

(5.22) $$Ron = \frac{1}{KPN \cdot \frac{W}{L} \cdot (V_{GS} - V_{TN})}$$

Again using [20], process parameters are gain factor $KPN = 170\mu A/V$, threshold voltage $V_T = 0.59V$. Threshold voltage measured in the linear region is used because the nMOS transistor operates at the linear region.

(5.23) $$R_{on} = 2.0 ohms$$

Using the solution given in Chapter 4, C_1 and L_1 values are obtained at the operating frequency 2.4GHz. Table 5-1 shows the C_1 and L_1 values for different channel resistance value. According to the Table 5-1

(5.24) $$C_1 = 570 fF$$

and

(5.25) $L_1 = 1.64nH$

Table 5-1 C1 and L1 values for different channel resistance values at 2.4 GHz

Ron	B (mS)	X (ohm)	C (pF)	L (nH)
0	9,180	23,05	0,6088	1,5286
1	8,884	23,89	0,5892	1,5846
2	8,608	24,74	0,5708	1,6405
3	8,349	25,58	0,5537	1,6963
4	8,105	26,42	0,5375	1,7521
5	7,876	27,26	0,5223	1,8077
6	7,659	28,10	0,5079	1,8633
7	7,455	28,93	0,4944	1,9188
8	7,261	29,77	0,4815	1,9742
9	7,077	30,60	0,4693	2,0296
10	6,903	31,44	0,4578	2,0849
11	6,737	32,27	0,4468	2,1401
12	6,579	33,10	0,4363	2,1954
13	6,429	33,94	0,4263	2,2505
14	6,285	34,77	0,4168	2,3057
15	6,148	35,60	0,4077	2,3608
16	6,016	36,43	0,3990	2,4158
17	5,891	37,26	0,3907	2,4709
18	5,770	38,09	0,3827	2,5259
19	5,655	38,92	0,3750	2,5808
20	5,544	39,75	0,3676	2,6358
21	5,437	40,57	0,3606	2,6907
22	5,334	41,40	0,3538	2,7456
23	5,236	42,23	0,3472	2,8004
24	5,140	43,06	0,3409	2,8553
25	5,049	43,88	0,3348	2,9101

L_1, L_{match}, $L_{\tan k}$ will be implemented as a single bond wire inductor with value:

(5.26) $L_{Total} = L_1 + L_{match} + L_{\tan k}$

(5.27) $L_{Total} = 1.64nH + 8.986nH + 1.624nH = 12.25nH$

279.3fF of the C_1 will be inside the transistor. Rest of the C_1 (290.7fF) and $C_{\tan k} = 489.4\,fF$ will be implemented as poly capacitors, and C_{match} 1.624pF match will be made off-chip.

One simulation using these values is performed. In this simulation run, channel resistance and output capacitance of the transistor is measured.

(5.28) $R_{ON} = 5.2 ohms$

(5.29) $C_{ds} = 460\,fF$

are found. Calculated capacitance value is quite close to simulation result but R_{ON} differs very much. This may be due to some short channel effects, which are not included in the equations. Afterwards using these new values C_1 and L_1 is chosen from the Table 5-1:

(5.30) $C_1 = 522.3\,fF$

and

(5.31) $L_1 = 1.808 nH$

Therefore new value of the shunt capacitance is equal to 66fF.

5.2 Simulation of the Amplifier

Simulation of the amplifier is performed using Cadence with the AMS HitKit 3.4 using 0.35µm CMOS process parameters. Following results have obtained from the simulation results;

(5.32) $P_{out} = 118.5 mW$

(5.33) $I_{dc} = 57.6 mA$

(5.34) $P_{\sup ply} = 144 mW$

$$\eta = \frac{P_{out}}{P_{\sup ply}} = \%82.3 \qquad (5.35)$$

This is a very good efficiency for an amplifier operating at very high frequency but it is required to mention that no parasitic losses are included in the simulation. This efficiency is consistent with the expected values which can be seen in Figure 4-8. Plot of the simulation result is shown in Figure 5-3.

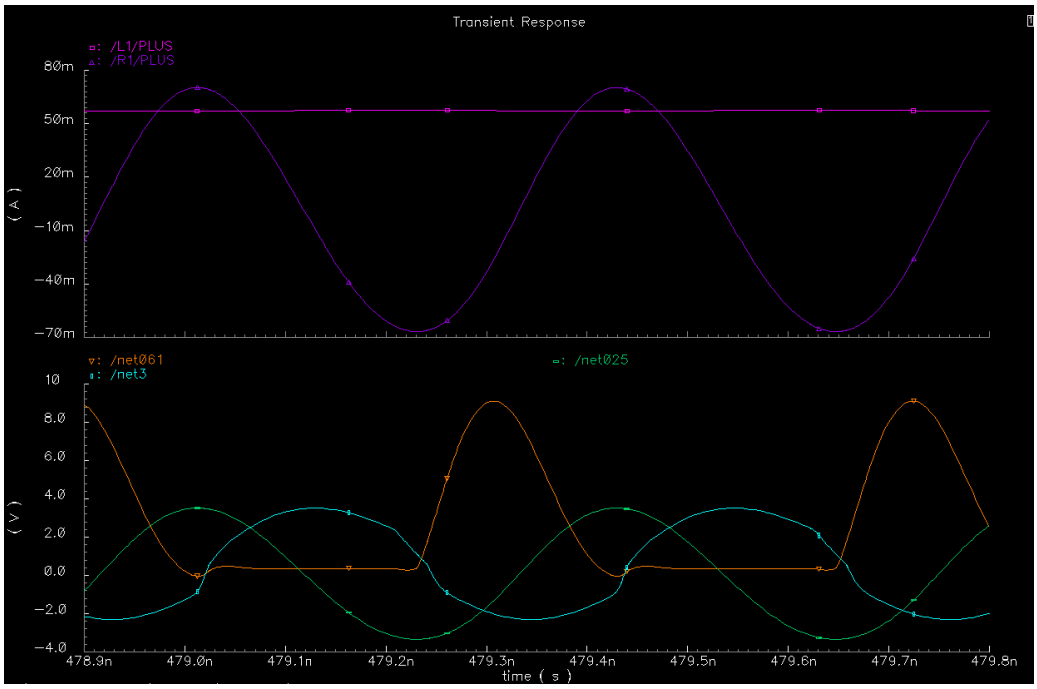


Figure 5-3 Plot of the simulation results

Net3 is the voltage on the gate, which turns ON and OFF the switch. Drain to source voltage (net061) successfully drops to zero volt at the turn on time with a zero slope. However there is a small increase when the gate voltage increase due to the gate to drain capacitance. Net025 is output voltage whose peak voltage is 3.5 V.

CHAPTER 6

CONCLUSIONS

In the scope of this thesis, information required to realize a high frequency CMOS Class E power amplifier has gathered and presented in the chapters 2 and 3. In chapter 4 complete analysis of the channel resistance in the operation of the class-E amplifier is made, which is not presented in the literature so far. Afterwards in chapter 5, a CMOS class-E power amplifier is designed based on the analysis made in the chapter 4.

Chapter 2 focuses on the CMOS process, which will be the target process in the design of the power amplifier. CMOS process is well known for its poor performance at high frequencies. As with the scaling operating frequency of the active devices (most commonly MOSFETs) increases day by day. Thus high frequency applications are becoming possible along with the integration of the digital and RF components. However availability of the high frequency MOSFETs is not enough for a successful design, unless their high frequency characteristics are well known. High frequency characteristics of MOSFET are mostly affected by the parasitic components, such as gate, drain and source resistances, drain to bulk and source to bulk capacitances, which are very hard to analyze and model. However computer simulation models, such as BSIM3V3, can be expanded using parameter extraction methods from the measurements of the real physical devices [1-8]. These modifications to models can increase the valid frequency range of the model up to 10GHz [10]. These models can then be used for the design verification and valid performance estimation of the design before the run.

Today it is possible to integrate all components of an RF transceiver including the passive components into an IC. Passive components realized in the CMOS process mostly suffer from the lossy behavior of the CMOS substrate and unintended parasitic components. Energy coupled to the lossy substrate can cause very high power losses and the effects of the parasitics may make the component useless at high frequencies. However it is still possible to use these components in successful designs, which are made in aware of these effects [15][21][22]

Chapter 4 focuses on class E power amplifiers. Class-E with its 100% power efficiency has a very widespread usage. Although classical equations gives very rough estimation of the component values for the class-E operation, they have many ideal case assumptions, which is very hard to satisfy in real circuits.

Infinite quality tank circuit is one of those assumptions. Most of the cases, especially in the CMOS process class-E amplifier must operate with quality factors below 10, even sometimes below 5. Many analysis done so far have shown that it is possible to obtain class-E operation at any Q [17][18]. However those analyses are very complex and are not practical. So still increasing the quality factor up to what is needed for the operation of the class-E amplifier with classical equations is preferred, and practical equations are used.

Another issue with the classical class-E equations is the assumption of the infinite dc feed inductance. Especially for the on-chip designs high value, low loss inductors are hard to realize. Some works have done to obtain high efficiency class-E operation using finite dc inductance [23-27]. Most practical and preferred one is to use an inductor, which resonates with the capacitance on the drain of the switch [24].

Zero channel (ON) resistance of the MOSFET is another assumption made in the derivation of the classical equations. Non-zero channel resistance does not only cause the power dissipation, but also disturb the tuning of the class-E amplifier. Non-zero channel resistance causes non-zero drain voltage at the time switch turns ON, this discharges the capacitance at the drain over the Ron resistance and causing another power loss. It is possible to retune the circuit to have the drain voltage drop to zero at the moment transistor turns ON, in the existence of a channel resistance.

Thus, eliminating the secondary loss mechanism, which is caused by the channel resistance.

In chapter 4 classical class-E equations are modified to include the channel resistance and closed form equations are obtained. These closed form equations are solved using numerical methods. Obtained results are presented in the same chapter to show the dependence of the circuit parameters to the channel resistance. Figure 4-1 and Figure 4-2 shows that capacitance admittance decreases and inductance impedance increases respectively with the channel resistance in order to maintain class-E operation. Linear dependence of equivalent DC resistance to the channel resistance is shown in Figure 4-5, which means that input power of the circuit decreases inversely proportional to. Effect of the channel resistance gets higher as the load resistance gets smaller; this is because currents are getting larger as the load resistance gets smaller. This is shown in Figure 4-10. Most of the IC class-E designs use small load resistances. This decreases the tank circuit's inductance value to obtain high quality factor. However channel resistance is more effective in such designs. Using a bigger transistor may be a solution by decreasing the channel resistance but in the cases where channel resistance couldn't be decreased more, it must be taken account in the design equations.

Verification of the solution is done by performing SPICE simulations. Circuit parameters are calculated using the equations in chapter 4. Figure 4-17 shows the drain voltage for different channel resistances. For every value of the channel resistance, high efficiency conditions of the class-E amplifier is satisfied at the switch turn ON time. This verifies the solutions successfully.

In chapter 5, a 2.5V 0.1W 2.4GHz power amplifier design is performed to demonstrate a design using the new equations derived in chapter 4. Simulation of the design is done. Simulation results are quite satisfactory with a drain efficiency of 82.3%. But it must be noted that no parasitic losses is included in the simulation since the objective of the design is to show validity of the solution in the presence of a nonlinear output capacitor [19], with an accurate MOSFET model, like BSIM3V3.

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APPENDIX A

MATLAB M-FILES

```
% File DrawPlots.m
% Function DrawPlots takes parameters
% R : Load Resistance in ohms
% Draws B, Y, phi and X for R chanell resistance from 0 to 100 ohm

function DrawPlots(R)
B = 0.0001:0.0001:0.0200 ;
Ron = 0:5:100 ;
for k = 1:21 , B_res(k) = fzero(@fitFunction,B(20),[],Ron(k),R);, end ;
figure('Name','Capacitance Admitance Value B (1/ohm)');

plot(Ron,B_res);
ylabel('Capacitance Admitance B (1/ohm)');
xlabel('Channel Resistance Ron (ohm)');

Y = YEquation_2_3(Ron,B_res);
figure('Name','Landa Value');
plot(Ron,Y) ;
ylabel('Landa Angle (radian)');
xlabel('Channel Resistance Ron (ohm)');

phi = PhiEquation_2_1(Ron,Y,B_res);
figure('Name','Phi Value');
plot(Ron,phi);
ylabel('Phi Angle (radian)');
xlabel('Channel Resistance Ron (ohm)');

X = R*tan(phi);
figure('Name','Enductance Impadence Value');
plot(Ron,X) ;
ylabel('Enductance Impadence  X (ohm)');
xlabel('Channel Resistance Ron (ohm)');
```

M-File 1 DrawPlots.m

```
% File fitFunction.m
% Function fitFunction takes parameters
% B : Cappacitance admittance
% Ron : Channel Resistance
% R : Load Resistance
% Calculates the value of the equation (4.25) This equation must be zero
% for the desired solution. MATLAB fzero function is used to calculate
% the zero of this function based on the B variable.

function fit=fitFunction(B,Ron,R)
Y = YEquation_2_3(Ron,B);              % Calculate lambda
phi = PhiEquation_2_1(Ron,Y,B);        % Calculate phi
fit = fitEquation_2_2(Ron,Y,B,phi,R);  % Try to satisfy equation (4.25)
```

M-File 2 fitFunction.m

```
% File fitEquation_2_2.m
% Function fitEquation_2_2 takes parameters
% Ron : Channel Resistance
% Y : Lamda Angle
% B : Cappacitance Admintance
% phi : Phi Angle
% R : Load Resistance
% This the equation (4.25) which must be satisfied (with equal to zero) for
% the numerical solution.

function fit=fitEquation_2_2(Ron,Y,B,phi,R)
p = 1./cos(phi);
U = cos(2.*Y).*(2.*cos(phi) + (B.*Ron + pi/2).*sin(phi));
L = sin(2.*Y).*(-2.*sin(phi) - (B.*Ron - pi/2).*cos(phi));
T = (-1.*(pi/2).*B.*Ron).*cos(phi) + (pi + B.*Ron).*sin(phi) - p.*pi.*B.*R ;
fit = U + L - T;
```

M-File 3 fitEquation_2_2.m

```
% File phiEquation_2_1.m
% Function phiEquation_2_1 takes the parameters
% Ron : Channel resistance
% Y : Lambda angle
% B : Cappacitance admittance
% Caulculates the phi angle based on the euqation (4.42)

function phi=phiEquation_2_1(Ron,Y,B)
U = Ron.*B.*cos(2*Y) + (pi/2).*cos(2*Y) - Ron.*B - pi - 2*sin(2*Y);
L = Ron.*B.*sin(2.*Y) + (pi/2).*sin(2.*Y) + ((pi/2).*Ron.*B) + 2.*cos(2.*Y);
phi = atan(U./L);
```

M-File 4 phiEquation_2_1.m

```
% File YEquation_2_3.m
% Function YEquation_2_3 takes the parameters
% Ron : Channel Resistance
% B : Cappacitance Admittance
% Calcultes the lamda angle based on the equation (4.40)

function Y = YEquation_2_3(Ron,B)
Y = atan(-2 ./ ( pi + 2.*Ron.*B ));
```

M-File 5 YEquation_2_3.m

APPENDIX B

SIMULATION RESULTS

Table C-1 Simulation results of circuits designed with equations including channel resistance

Ron	C (pF)	L (nH)	Idc	Vout	Pin	Pout	Pron	Efficiency	g	Vc,peak
1	14,14	38,03	26,93	1,007	26,96	25,22	1,719	93,55	1,8679	3,479
4	12,90	42,05	22,31	0,8401	22,29	17,54	4,718	78,68	1,8845	3,237
7	11,86	46,05	19,05	0,7224	19,05	12,96	6,049	68,04	1,8963	3,066
10	10,99	50,04	16,65	0,6344	16,65	9,991	6,615	60,02	1,9056	2,938
13	10,23	54,01	14,80	0,5663	14,81	7,955	6,813	53,71	1,9118	2,840
16	9,576	57,98	13,33	0,5117	13,35	6,491	6,813	48,64	1,9171	2,760
19	9,000	61,94	12,13	0,4669	12,15	5,402	6,711	44,45	1,9210	2,695
22	8,490	65,89	11,14	0,4295	11,16	4,569	6,555	40,93	1,9239	2,641
25	8,035	69,84	10,30	0,3978	10,33	3,917	6,371	37,93	1,9261	2,595

Table C-2 Simulation results of circuits designed with classical class-E equations

Ron	C (pF)	L (nH)	Idc	Vout	Pin	Pout	Pron	Efficiency	g	Vc,peak
1	14,61	36,69	27,50	1,017	27,51	25,67	1,768	93,31	1,8393	3,429
4	14,61	36,69	23,82	0,8638	23,82	18,52	5,212	77,77	1,8045	3,047
7	14,61	36,69	21,01	0,7488	21,01	13,92	6,999	66,28	1,7738	2,760
10	14,61	36,69	18,79	0,6596	18,79	10,81	7,904	57,49	1,7468	2,537
13	14,61	36,69	17,00	0,5884	17,00	8,602	8,318	50,60	1,7230	2,360
16	14,61	36,69	15,52	0,5305	15,52	6,994	8,447	45,07	1,7021	2,216
19	14,61	36,69	14,27	0,4826	14,27	5,788	8,411	40,55	1,6838	2,097
22	14,61	36,69	13,21	0,4423	13,21	4,862	8,277	36,81	1,6677	1,998
25	14,61	36,69	12,29	0,4080	12,29	4,138	8,087	33,67	1,6536	1,913