## PERFORMANCE OF A DYNAMIC VOLTAGE RESTORER FOR A PRACTICAL SITUATION

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I hereby declare that all information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

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#### ABSTRACT

# PERFORMANCE OF A DYNAMIC VOLTAGE RESTORER FOR A PRACTICAL SITUATION

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Among most severe power system disturbances those degrading power quality are voltage sags and transient interruptions. Even voltage sags lasting only a few tens of milliseconds are enough to bring entire production lines to standstill, causing considerable economic damage as well as endangering the production equipment. Therefore necessary measures have to be taken to protect sensitive loads which are susceptible to these voltage disturbances. Among the solution candidates such as, Uninterruptible Power Supplies, Motor-Generator Sets, etc, Dynamic Voltage Restorer (DVR) which is an effective custom power device has been proposed to mitigate such bus voltage sags on sensitive loads with its excellent dynamic performance.

In this study, load side connected shunt converter topology was chosen for the implementation of DVR. The performance DVR was tried to be improved by improving the control strategy used. Super Film located in Gaziantep which is one of the SANKO subsidiary company was chosen to simulate the operation of DVR as actual case of Turkish industry. All the simulations in this study were carried on PSCAD/EMTDC Software.

Keywords: Voltage Sag, Series Device, Dynamic Voltage Restorer

## BİR DİNAMİK GERİLİM DÜZENLEYİCİSİNİN UYGULANABİLİR BİR DURUM İÇİN BAŞARIMI

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Güç kalitesini düşüren en ciddi güç sistemi bozuklukları arasında gerilim düşmeleri ve kısa süreli kesintiler gelmektedir. Sadece bir kaç mili saniye süren gerilim düşmeleri tüm üretim hatlarını, önemli ekonomik zarara sebep olmanın yanı sıra, üretim ekipmanına tehlikeye atarak durdurmaya yeterlidir. Bu yüzden, bu gerilim bozulmalarına maruz kalabilecek hassas yükleri korumak için gerekli tedbirler alınmalıdır. Kesintisiz Güç Kaynağı, Motor-Jeneratör Seti, gibi çözüm adaylarının arasından, etkili bir tasarlanan güç cihazı olan Dinamik Gerilim Düzenleyicisi (DGD) üstün dinamik başarımı ile hassas yükler üzerindeki bu türlü bara gerilim düşmelerinin azaltılması için önerilmiştir.

Bu çalışmada yük tarafından şönt bağlı çevirici topolojisi DGD uygulaması için seçilmiştir. DGD'nin başarımı kullanılan kontrol stratejisinin geliştirilmesi ile iyileştirilmeye çalışılmıştır.

#### ÖZ

SANKO holding iştiraki olan Gaziantep'te yer alan SANKO, DGD'nin çalışmasının simülasyonu için Türk Endüstrisi'nden gerçek bir durum olarak seçilmiştir. Bu çalışmada yer alan tüm simülasyonlar PSCAD/EMTDC yazılımı kullanılarak yapılmıştır.

Anahtar Kelimeler: Gerilim Düşümü, Seri Cihaz, Dinamik Gerilim Düzenleyicisi

to my beloved family, and sweetheart

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#### LIST OF ABBREVIATIONS

- DVR : Dynamic Voltage Restorer
- PCC : Point of Common Coupling
- PLL : Phase Locked Loop
- PWM : Pulse Width Modulation
- SPWM: Sinusoidal Pulse Width Modulation
- RMS : Root Mean Square
- SCO : Short Circuit Operation
- VSI : Voltage Source Inverter
- THD : Total Harmonic Distortion
- IGBT : Integrated Gate Bipolar Transistor
- FFT : Fast Fourier Transform

#### CHAPTER1

#### **INTRODUCTION**

Power quality issues are of vital concern in most industries today, because of the increase in the number of loads sensitive to power disturbances. The power quality is an index to qualify of current and voltage available to industrial, commercial and household consumers of electricity. The problem regards both the utilities and customers. For the utilities, to provide adequate power quality is a moving objective because of changes in user equipment and requirements. For consumers, problems stemming from the sensitivity of electrical equipment to voltage quality have often very heavy consequences [1].

Power quality is a topic embracing a large field. On one side, several different events are involved in power quality: spikes or surges, sags, swells, outages, under and overvoltages, harmonics, flicker, frequency deviations, electrical noise. Accordingly, different measurements and analysis tools are required to investigate such phenomena, and different remedial actions can be adopted to compensate them or to reduce their effects.

On the other side, many electronic devices (such as computers, process controls, adjustable speed drives, solid-state-relays, optical devices, to name a few) are sensitive to a different extend to power quality.

Since a certain event may be not serious problem for a given customer class, but it may represent a big problem for another class, it has doubtful practical sense to rank

the above events in terms of importance without referring to a more specific context. As far as industrial and commercial customers are concerned, several recent studies agree on the statement that voltage sags must be regarded as one of the most important concerns in power quality. This statement is particularly true for industrial facilities, where even short duration voltage sags are often responsible for much more long-lasting production downtimes and consequent large lost revenue.

It is difficult to place a value on the impact of power quality problems, but it is safe to say that unscheduled shutdowns can cost tens of thousands of dollars. Along with the tangible cost of lost production time (and therefore sales), wasted raw materials and damaged equipment, there are also indirect costs, such as damaged to customer confidence caused by missed delivery schedules.

In many cases a custom power device can provide the most economic solution by establishing the proper power quality level that is required by the customer. Often such a device would negate the need for the utility to install additional feeders or substations or customer to install individual power conditioners at the load level.

IEEE Standard 1100-1992 (IEEE Emerald Book) defines a sag as "an rms reduction in the AC voltage, at the power frequency, for durations from a half-cycle to a few seconds". Note: The IEC terminology for a sag is dip. They may be accompanied with phase jumps. If the voltage is reduced to zero, the disturbance is said to be a momentary outage or microinterruption. The most obvious way to characterize a voltage sag is in terms of the reduced voltage rms, duration and probably accompanied phase jump.

The European Standard (EN50160-1994) defines very well about the sags and its indicative values [2];

Voltage dips (sags) are generally caused by faults occurring in the customers' installations on in the public distribution system. They are unpredictable, largely random events. The annular frequency varies greatly depending on the type of the

supply systems and on the point of observation. Moreover, the distribution over the year can be very irregular.

Voltage sags are often generated by starting of large loads, such as motors, transformer energizing, equipment faults, transmission and distribution system faults. Faults on the distribution and transmission systems can be caused by numerous sources such as lightning strikes, conductors blowing together in a storm, contact with objects (e.g. tree branches, animals, etc.) or vandalism. Most of these faults (70-80%) are temporary in nature; they are self-clearing within a few milliseconds. The fault that does not clear will cause a protective device/s (e.g. fuse, circuit breaker, or recloser) to operate to interrupt current to that part of the system in the affected area [3].



PCC, Point of Common Coupling

Figure 1.1 The voltage sag generation

Typical electronic equipment can operate at 80-85% of nominal voltage for several cycles. This operating characteristic is illustrated by the well known CBEMA curve that is shown in Figure 1.2 [10], which was established by the Computer Business Equipment Manufacturing Association (CBEMA). Most recently, CBEMA has changed its name to the Information Technology Industry Council (ITIC), and the existing curve has been changed as shown in Figure 1.3 [10]. Note: The ITIC curve is planned to be included in the next revision of the IEEE Emerald Book.



Figure 1.2 The CBEMA Curve

#### PERCENT CHANGE IN BUS VOLTAGE



Figure 1.3 The ITIC Curve

There are several solutions currently available that will provide ride-through capability to critical loads under voltage sag condition [4]:

- Motor-Generator Sets (M-G Sets)
- Uninterruptible Power Supplies (UPS's)
- Ferroresonant, Constant Voltage Transformers (CVT's)
- Magnetic Syntesizers
- Superconducting Storage Devices
- Dynamic Voltage Restorer (DVR)

Developed in the early 1990's, a Dynamic Voltage Restorer, with its excellent dynamic capabilities, when installed between the supply and a critical load feeder, can compensate for voltage sags, restoring line voltage to its nominal value within a few milliseconds and hence avoiding any power disruption to that load.

A typical DVR consist of the following major components [5]:

- Voltage Source Inverter/s (VSI)
- Injection Transformer/s
- Harmonic Filter
- Energy Storage Unit
- DC Link
- Control and Protection System

The DVR functions by injecting three single phase AC voltages in series with the three phase incoming network voltages during a dip, compensating the difference between faulty and nominal voltages. All three phases of the injected voltages are of controllable amplitude and phase. Voltage source inverter fed from the DC link supply the required active and reactive power.



Figure 1.4 The block diagram of the DVR

During undisturbed power supply condition, the DVR operates in a low loss standby mode. In the normal operation mode (no sag) the low voltage side of the booster transformer is shorted and it functions as a short-circuited current transformer.

At the heart of the DVR are three phase voltage source inverter/s: a solid state power electronics device which converts AC to DC and vice versa. By fast switching a DC source, the DVR is able to synthesize an AC waveform. The DVR constantly monitors incoming supply voltage and compares it with a reference voltage. In the event of a disturbance it injects three phase AC output voltages of compensatory amplitude, phase and harmonic content. This ensures that the voltage seen by the load is of the desired magnitude, preventing unnecessary process interruptions.

During sag event, DVR must supply real and reactive power to the line. The source of this energy is the DC link. This could be only charged capacitor bank or it can be fed either from a battery system or the line itself.

The primary side of the DVR injection transformer is sized to carry full line current. The primary voltage rating is the maximum voltage that the DVR can inject into the line for a given application. The secondary voltage is controlled by voltage source inverter connected to the DC link. The bridge outputs are filtered before being applied to the injection transformer by the harmonic filter and are independently controllable to allow each phase to be compensated individually.

In the literature, three control strategies are suggested to compensate for the voltage sags accompanied by phase jump, which is the usual case [6]:

- 1. Pre-sag compensation: The supply voltage is continuously tracked and the load voltage is compensated to the presage condition. The method gives a nearly undisturbed load voltage, but can often exhaust the rating of the DVR.
- 2. In-phase compensation: The generated DVR voltage is always in phase with the measured supply voltage regardless of the load current and the pre-sag voltage.
- 3. Energy optimal compensation: To fully utilize the energy storage, information about the load current is used to minimize the depletion of the energy storage.

The DVR need not be fully rated to the load requirements. Installing a DVR capable of injecting a fraction of total load requirement for a short period could effectively

screen a load from the majority of sags, while the remainder would be sufficiently reduced in severity that plant equipment would be able to tolerate them. For example, a 4MVA load capable of riding through sags of greater than 80% retained voltage could be protected by a 2MVA DVR from sags to as low as 30% retained voltage. The optimum economic solution for a given application depends on the ride through capability of the existing equipment, typical sag profile and costs of potential shutdowns.

In August 1996, Westinghouse Electric Corporation installed world's first DVR in Duke Power Company's 12.7kV substation in Anderson, South Carolina. This was installed to provide protection to an automated rug manufacturing plant. For a total load of 3.5MVA at a power factor of 0.8, a 2MVA DVR, with 660kJ of energy storage was installed and put into service on September 4, 1996. The next commissioning of a restorer was done by Westinghouse in February 1997 in Powercor's 22kV distribution system at Stanhope, Victoria, Australia to protect a diary milk processing plant. The total load was approximately 5.25MVA and a 2MVA DVR was installed. The saving that results from the installation of this installation is estimated at over \$100,000 per year. In the next phase of development, Westinghouse (now taken over by Siemens) installed world's first platform mounted DVR to protect Northern Lights Community College and several other smaller loads in Dawson Creek, British Colombia, Canada [7] [8]. ABB installed and commissioned the world's biggest dynamic voltage restorer in August 2000, in Israel. The two systems (each 22.5MVA) protect the production facility of a microprocessor manufacturer located in a desert environment.

Within the scope of this study, Super Film located in Gaziantep which is one of the SANKO subsidiary company will be handled as a practical case study from Turkish industry. It was recorded that the facility has a installed capacity of 39.550 MVA. It was also reported that since January 2004, for about 200 voltage sags have been experienced, 100 of which have caused serious process interruptions each of which costs \$500-1000.

In this study, a DVR with the load side connected converter topology for the Super Film case will be analyzed depending on the simulations carried on PSCAD/EMTDC software package.

The organization of the thesis is as follows:

- In Chapter 2, the operational basics of the DVR are discussed.
- In Chapter 3, the system design for the chosen case is described.
- In Chapter 4, the simulation results are given.
- In Chapter 5, the final conclusions on this study are made and the further work on this area is proposed.

#### CHAPTER2

#### **DVR BASICS**

A power electronic converter based series compensator that can protect critical loads from all supply side disturbances other than outages is called a dynamic voltage restorer. The restorer is capable of generating or absorbing independently controllable real and reactive power at its AC output terminal. This device employs solid-state power electronic switches in a pulse-width modulated (PWM) inverter structure. It injects a set of three-phase AC output voltages in series and synchronism with the distribution feeder voltages. The amplitude and phase angle of the injected voltages are variable thereby allowing control of the real and reactive power exchange between the device and the distribution system. The DC input terminal of the restorer is connected to an energy source or an energy storage device of appropriate capacity. The reactive power exchanged between the restorer and the distribution system is internally generated by the restorer output AC passive reactive components. The real power exchanged at the restorer output AC terminals is provided by the restorer input DC terminal from an external energy source or energy storage system [7].

#### 2.1 Basic DVR Operating Principles

The DVR functions by injecting three single phase AC voltages in series with the three phase incoming network voltages during a sag, compensating for the difference between faulty and nominal voltages. All three phases of the injected voltages are of

controllable amplitude and phase. Three pulse-width modulated (PWM) voltage source inverters (VSI) fed from a DC link supply the active and reactive power.

During undisturbed power supply condition, the DVR operates in a low loss standby mode. In the normal operation mode (no sag) the low voltage side of the booster transformer is shorted either by solid state bypass switch or by switching one of the inverter legs and it functions as a short-circuited current transformer. Since no VSI switching takes place, the DVR produces conduction losses only. These losses should be kept as low as possible so as not to cause steady state power loss.

Harmonics produced by the operation of VSI must be reduced to an acceptable limit defined by [11] by proper filtering scheme. Modulation scheme used on the VSI switches has also impact on the harmonics produced.

The required energy during sags has to be supplied by an energy source. The necessary amount of energy that must be delivered by the energy source depends on load MVA requirement, control strategy applied, deepest sag to be protected.

Under normal conditions, the short circuit impedance of the injection transformer determines the voltage drop across the DVR. This impedance must be low and has an impact on the fault current through the VSI on secondary side caused by a short-circuit at load side. The filter design is also affected by the impedance of the injection transformer.

In case of fault or over current exceeding the rating of DVR on the load side, solidstate bypass switches or electromechanical bypass switches must be added as a measure to protect DVR from getting damaged.

As an overview the following main design criteria influence the rating and the performance of the DVR [5]:

• Maximum MVA-load and power factor,

- Maximum 1 phase and 3 phase voltage sags to be compensated,
- Maximum duration of 3 phase voltage sag,
- Maximum allowed voltage drop across DVR under steady-state conditions,
- Short circuit impedance of the injection transformers,
- Short circuit impedance and connection of step down transformers at the input and output sides of the DVR as well as the short circuit power.

#### 2.2 DVR Components

A typical DVR consist of the following major components [5]:

- Voltage Source Inverter/s (VSI)
- Injection Transformer/s
- Harmonic Filter
- Energy Storage Unit
- DC Link
- Control and Protection System

#### 2.3 Location of DVR

The intention is only to protect one consumer or a group of consumers with value added power. Applying a DVR in the medium or low voltage distribution system would often be possible and a radial grid structure is the only type of system considered here. In Europe three wire systems are common in the medium voltage systems and four wires in low voltage systems. In both systems the main purpose is to inject synchronous voltages during symmetrical faults and in some cases inject an inverse voltage component during non-symmetrical faults [9].

A main difference between a Low Voltage (LV) connection and a Medium Voltage (MV) connection is the flow of zero sequence currents and the generation of zero

sequence voltages. In the four-wire system, the DVR must secure a low impedance for zero sequence currents and the zero sequence must either flow in the power converter or in a delta winding of the injection transformer.

#### 2.4 Converter Type

Pulse width modulated voltage source inverters are commonly used converters for this type of application. Applying a VSI to compensate for a missing voltage requires an injection transformer and a line filter to damp generated switching harmonics.

Additionally, losses should be minimized, because the DVR conducts the load current continuously and a fast response is important to avoid a deterioration of the load voltage. The critical factors when choosing a converter for a DVR application are [9]:

- Switching frequency
  - Generation of switching harmonics
  - Ripple current in the converter
  - Power losses caused by the switching and conduction
- Dynamic response
- DVR impedance

In general useful topologies are those where active power easily can be transferred from a simple DC voltage circuit to the DVR converter. A full bridge converter is also a good choice for DVR converters, by unipolar switching the first harmonic appear at the twice the switching frequency.

#### 2.5 Energy Source

Compensating effective for large voltage reductions requires active power, either from a storage system, the grid itself or from an auxiliary supply. The solutions can be summarized as follows [9]:

- Energy storage
- Auxiliary supply
- Line connected shunt converter
  - Load connected
  - Source connected

Operating with energy storage gives limitations in the performance to compensate for long duration sags and large energy storage is still costly, therefore most of the proposed DVR solutions have been realized with a shunt converter fed from the line itself or an auxiliary supply. Main advantage of load side connected shunt converter is that the shunt converter has a restored clean voltage to enable a stable charging to the common DC link. A drawback with the load side connected is the requirement of a higher current rating of the series converter[9].

The current rating of the DVR is critical. It should be scaled according to the existing load and a future load increase. If the load consists of large loads with transient currents, the DVR must be rated to handle these higher currents or bypass the current. During voltage sag, the voltage applied to the transformer changes abruptly and the transformer is magnetized according to the sag size. A transient DC current can be detected and the saturation effects in the transformer can even increase the inrush current. The DVR converter has to supply the inrush current and must be rated for this current [9].

#### 2.6 Injection Transformer

The injected voltages are introduced into the distribution system through an injection transformer connected in series with the distribution feeder. It is known that in order to guarantee the maximum reliability and effectiveness of this restoration scheme, clever selection of the injected transformer is a prerequisite. In order to carefully select a suitable injection transformer the following issues should carefully be addressed [17]:

- The MVA rating
- The primary winding voltage and current ratings
- The turn-ratio which, in turn, determines the secondary winding voltage and current rating
- The short-circuit impedance

Determination of the above parameters is dependent of the following system parameters[17]:

- The MVA rating of the sensitive load to be protected,
- The maximum allowable voltage drop across the transformer,
- The characteristics of the expected voltage sags to be compensated for,
- The design of the harmonic filter system
- The selection of the switching devices
- The energy storage capacity and the voltage restoration control strategy

One parameter influencing the specifications of a DVR is the maximum single-phase and three-phase voltage sags to be compensated for by the restorer. Given the finite energy storage capacity of the DVR system, it is clear that maximum single-phase voltage sag depth that is to be compensated for should be used to determine the primary-side voltage rating of the injection transformer. Depending on the voltage injection strategy, primary voltage rating of the transformer may vary greatly, reaching its maximum at minimum energy injection strategy.

The injection transformer is connected in series with the sensitive load which is to be protected by the DVR. Thus the current rating of the injection transformer is primarily determined by the rated capacity of the sensitive load. With the determination of primary voltage and current ratings of DVR, MVA rating of it also develops which is a fraction of the total MVA of the sensitive load to be protected.

The filtering system of the DVR can be placed either on the high-voltage or the lowvoltage side of the injection transformer and are referred to as line-side filter and the inverter-side filter respectively. When the inverter-side is used high-order harmonics from VSI is by-passed by the filtering scheme and thus its impact on the injection transformer current rating can be neglected. If the line-side filtering scheme is used, high-order harmonic currents penetrate through the injection transformer and it will carry the harmonic voltages, and will increase the rating of the transformer [17].

The selection of the transformer secondary voltage and current ratings and its turnsratio are interrelated. To determine the turns-ratio, first start with a given turns-ratio and as the primary ratings are known, the secondary voltage and current ratings can be determined. The current carrying capability and the blocking voltage of the switching devices can then be determined. If the rating of the calculated switches matches with commercially available switches, stop turns ratio calculation at that point, if not continue to get commercially available and economical switches.

The short-circuit impedance will affect the fault current through the injection transformer when a short-circuit occur on the load side. The impedance also affects the design of filtering schemes as discussed in the "Filtering Schemes" section. However, as the power system is usually operating under normal conditions, the primary concern when considering the specification of the short-circuit impedance of the transformer is the voltage drop across it during normal operations of the power system.

With the inverter-side filtering scheme applied to the DVR system, the equivalent circuit is as shown in Figure 2.1 [17].



Figure 2.1 Equivalent Circuit of DVR with Inverter-Side Filter

In Figure 2.1,  $R_1$  and  $L_1$  represents the primary-side resistance and leakage inductance of the transformer.  $R_2$  and  $L_2$  represent the secondary-side resistance and leakage inductance of the transformer referred to the primary-side.  $L_f$  and  $C_f$ constitute the filter elements and are also referred to the primary-side.  $R_v$  is a resistor to account for the total conduction voltage drop caused by the switches and diodes.  $Z_M$  represents the magnetizing impedance of the transformer. Figure 2.1 can be simplified to Figure 2.2 by considering the fact that  $Z_M$  is very large compared to  $R_2$ and  $L_2$ , while  $R_v$  is normally negligible [17].



Figure 2.2 Simplified Equivalent Circuit of DVR with Inverter-Side Filter

From Figure 2.2, let  $R_k$ +jwL<sub>k</sub> represents the short-circuit impedance of the injection transformer where  $R_k=R_1+R_2$ ,  $L_k=L_1+L_2$ . Suppose it is required that the voltage drop across the injection transformer during the normal operating conditions of the system be less than a specified value, say V<sub>d</sub>. To meet the requirement, the short-circuit impedance should therefore satisfy the following condition [17]:

$$\sqrt{R_k^2 + w^2 \left(L_k + L_f / \left(1 - w^2 L_f C_f\right)\right)^2} V_d / I_s$$
(2.1)

If the line-side filtering scheme is used, the equivalent circuit is as in Figure 2.3.



Figure 2.3 Equivalent Circuit of DVR with Line-Side Filter

Filter capacitance,  $C_f$ , is connected in shunt with the other structure of the DVR system, inclusion of it will not cause much voltage change of the power system. For simplicity, the effect of the capacitor can be neglected. Using the assumptions that  $Z_M$  and  $R_v$  are ignored, then to meet the voltage drop requirement, the short-circuit impedance should satisfy [17]:

$$\sqrt{R_k^2 + w^2 L_k^2} < V_d / I_s \tag{2.2}$$

#### 2.7 Filtering Schemes

In the design of DVR, special attentions must be paid to the filtering scheme as it is related with the system dynamic response. Two filtering schemes were seen from the recent literature, which are the inverter-side filter and line-side filter [12], [13]. Figure 2.4 shows the configuration of the inverter-side filter, and Figure 2.5 depicts that of the line-side filter. In the scheme of inverter-side filter, a series inductor  $L_f$  and a shunt capacitor  $C_f$  are inserted between the transformer and switching devices. From the view point of harmonic elimination, the inverter-side filter scheme may be a preferable one. Yet, as the insertion of the inductor may introduce an additional voltage-drop component across the series transformer, it is also found that the magnitude and phase difference between the fundamental components of voltage has appeared on both sides of the filter, implying that an inadvertent choice of the filter design would significantly downgrade the DVR control performance. As for the
DVR design of line-side filter, it can be implemented by placing the filtering scheme on the line-side of the series transformer as Figure 2.5 depicts. In such a line-side filter scheme, the leakage flux of series transformer is served as the filtering inductance, and the capacitor is placed across the transformer winding. By use of this design, the system will no longer require a physical inductor, avoiding the problem encountered in the inverter-side filter. However, similar to the inverter-side filter scheme, a transport delay is also encountered between the input and output of the filter network that may be attributed to the utilization of the line-side filter. Note that while the DVR along with the filtering scheme is devoted to cancel out the incoming nuisance, this resultant transport delay may instead offset the dynamic response in a significant manner, or even lead to a system compensation failure [14].



Figure 2.4 Inverter-Side Filter



Figure 2.5 Line-Side Filter

#### 2.7.1 Line-Side Filter

A typical DVR system can be analyzed using its equivalent circuit shown in Figure 2.6. All the variables in Figure 2.6 have been referred to the line side of injection transformer. In this figure  $R_i$  and  $L_i$  denote the resistance and the leakage inductance of the injection transformer. In the analysis, it will be assumed that  $R_i$  and  $L_i$  are known.  $C_f$  is the filter capacitor.  $V_{se}$  represents the equivalent source of the power system interfaced to the output of the filter with  $Z_e = R_e + jwL_e$  being the equivalent impedance (at the frequency w) external to the DVR.  $V_{si}$  represents the voltage on the inverter side of the filter. The functions of the other DVR components are not included in the analysis. Note that the capacitor  $C_f$  together with the equivalent impedance of the series injection transformer forms an LC filter which can be used to attenuate the harmonic contents appearing in the injection voltage [13].



Figure 2.6 Line-Side Filter Equivalent Circuit

The basic principle behind the selection of the capacitor is to provide a shunt path for the harmonic current and let the series transformer carry almost all the harmonic voltages. To achieve this goal, the capacitor should be chosen to satisfy

$$|Z_{e(m)}| = K_f |Z_{c(m)}|$$
  $K_f >> 1$  (2.3)

where  $Z_{e(m)} = R_e + jmw_0L_e$ ,  $Z_{C(m)} = -j/(mw_0C_f) w_0 = 2\pi f_0$ ,  $f_0$  represents the fundamental frequency and m is the lowest order of the harmonics to be attenuated.

Suppose that the supply source  $V_{se}$  is ideal and the rated voltage of the primary feeder is  $V_p$  (per phase). The THD limit considered acceptable at this voltage denoted as  $K_{THD}$ , can be obtained (for instance) from IEEE standard 519-1992. The permissible total harmonic voltage across the capacitor, denoted as  $V_T$ , can be readily be calculated and is given by

$$V_T = K_{THD} V_P \tag{2.4}$$

THD requirement on the injected DVR voltage can be satisfied, if the suitable filter capacitance is chosen according to the following criteria;

$$C_{f} \geq \frac{\left(1 + \sqrt{\sum_{n=m}^{M} \left\{ \left(\frac{m}{n}\right)^{2} V_{Si(n)} \right\}^{2}} \right)}{(mw_{0})^{2} L_{i}}$$
(2.5)

where  $V_{Si(n)}$  represents the nth order harmonic voltages (RMS) on the inverter side of the injection transformer, m is the lowest order of the harmonics to be attenuated and M is the higher order of the harmonics to be attenuated.

Once harmonic spectrum of the inverter output  $V_{Si(n)}$  is known and the voltage THD limit on the load side of the DVR is given filter capacitor can be selected using (2.5). Obviously (2.5) places a lower limit on the value of  $C_f$ . Thus it seems that a large value of  $C_f$  is preferable for harmonics attenuation. However, the selection of a large  $C_f$  may require the inverter rating to be increased.

If we consider the steady state operation of DVR power system load current is constant. Since the filter capacitor  $C_f$  is connected in parallel with the load, the difference between the inverter current  $I_s$  and the load current  $I_e$  appears as the capacitor current  $I_c$ . Obviously, the choice of  $C_f$  will have bearing on  $I_c$  and thus  $I_s$ .

In addition as the filter is located on the high voltage side of the series transformer, the high order harmonic currents will penetrate into the injected transformer, thus necessitates a higher rating on the transformer.

# 2.7.2 Inverter-Side Filter

The basic principle behind the design of the inverter-side filter is quite similar to that used in the design of the line-side filter. As shown in Figure 2.4, the selection of the capacitor should satisfy (2.3), with  $Z_{es(n)}$  and  $Z_{c(n)}$  given by [12];

$$Z_{es(n)} = (R_e + R_i) + jnw_0(L_e + L_i)$$
(2.6)

$$Z_{c(n)} = -j/(nw_0 C_f)$$
(2.7)



Figure 2.7 Inverter-Side Filter Equivalent Circuit

For the inverter-side filter design, both  $L_f$  and  $C_f$  are variables. Any combination of  $L_f$  and  $C_f$  which satisfies (2.8) and (2.9) will constitute a filter that will attenuate the higher order harmonics such that the voltage THD on the load side of the DVR will be below the specified level.

$$K_{(n)} = 1 / \left( (nw_0)^2 L_f C_f - 1 \right)$$
(2.8)

$$K_{(n)} \le V_T / \sqrt{\sum \left( V_{Si(n)} \right)^2}$$
(2.9)

where 
$$V_T = K_{THD} V_P / K_i$$
 (2.10)

For this case the difference of the calculation of  $V_T$  is due to the  $K_i$ , turn-ratio of the injection transformer.

Again the above conclusions, (2.8), (2.9) are reached based on the assumption that (2.3) is satisfied. Thus a bigger value of capacitor seems preferable. However, as in the case of the line-side filter, a larger  $C_f$  may also result in the inverter's being overrated [12].

The advantage of the inverter-side filter is that it is on the low voltage side of the injection transformer and is close to the harmonic source. Using this scheme, the higher order harmonic currents will be prevented from penetrating into the series transformer. However, when the DVR acts as a source, the introduction of the filter inductor  $L_f$  may cause voltage drop and phase-angle shift in the fundamental component of the inverter output. This may risk the control scheme of the DVR. Moreover, as the DVR is a series device, the inductor may also cause a drop in the distribution system supply voltage.

# 2.8 The Control of DVR

The control of a DVR is not straight forward because of the requirements of fast response, large variation in the type of sags to be compensated and variation in the type of connected load. The DVR must also be able to distinguish between background power problems and the voltage sags to be compensated. Sags are often nonsymmetrical and accompanied by a phase jump [15].

The possibility of compensation of voltage sags can be limited by a number of factors including finite DVR power rating, different load conditions, background power quality problems and different type of sags. If the DVR should be a successful

device, the control may be able to handle most sags and the performance must be maximized according to the equipment inserted. Otherwise, the DVR may not be able to avoid load tripping and even cause additional disturbance to load.

A control strategy for voltage sags with phase jump should be included, to be able to compensate this particular type of sag. The control strategy can depend on the type of the load connected. Some loads are very sensitive to phase jump and the load should be protected from them. Other types of loads are more tolerant to phase jump and the main task is to maintain the nominal voltage on all three phases. Three basic control strategies for a DVR can be stated as [15]:

- Method 1: Pre-sag compensation; the supply voltage is continuously monitored and the load voltage is compensated to the pre-sag condition. The method gives nearly undisturbed load voltage, but can often exhaust the rating of the DVR.
- Method 2: In-phase compensation; the generated DVR voltage is always in phase with the measured supply voltage regardless of the load current and presag voltage.
- Method 3: Energy optimal compensation; to fully utilize the energy storage, information about the load current is used to minimize the depletion of the energy storage.



Figure 2.8 Control Strategies for DVR

The discussed three methods are illustrated in Figure 2.8 and by studying Figure 2.8 it appears like the energy storage can be reduced applying the DVR voltage perpendicular to the load current, but the load current will change phase according to the new load voltage applied to it and energy will be drawn from DVR.



Figure 2.9 The Flow of Active and Reactive Power with DVR Inserted

The Figure 2.9 illustrates how power flows in the system [15]. The voltage generated which is perpendicular to the load current can be used to bring the current in-phase with the supply voltage or make the DVR and load appears as a capacitive load. A capacitive load current tends to raise the supply voltage and by raising the supply voltage, more power can be drawn from the grid and hence saved from the energy storage.

Before selecting a control method to be used further issues have to be addressed, which are closely linked to the chosen control strategy. A DVR has limited capabilities and the DVR will most likely face a sag outside the range of full compensation. Three important limitations for a DVR are:

• Voltage Limit: The design of the DVR is limited in the injection capability to keep the cost down and reduce the voltage drop across the device in normal operation.

- Power Limit: Power stored in the DC-link, but the bulk power is often converted from the supply itself or from a larger DC storage. An additional converter is used to maintain a constant DC-link voltage and the rating of the converter introduce a power limit to the DVR.
- Energy Limit: Energy is used to maintain the load voltage fixed and it is normally sized as low as possible in order to reduce cost. Some sags will deplete the storage fast and the control can reduce the risk of load tripping caused by insufficient energy storage.

All the limits should be included in the control to fully utilize the investment of a DVR. Figure 2.10 illustrates a single-phase phasor diagram for one load case. The phasor of the pre-sag voltage is shown with a lagging load current. The phase jump is negative with a reduced during-sag voltage [15].



Figure 2.10 Power, Voltage Limits on a Deep Voltage Sag with a Phase Jump

The voltage and power limits are indicated and the hatched region illustrates the region within the DVR can operate. The pre-sag voltage can not be maintained in the case illustrated in Figure 2.10. In-phase control to nominal voltage is also not obtainable if the current phasor stays, because of the power limit.

A phase jump could be initiated by certain voltage sags with phase jump, or by the DVR itself to reduce the power drain or maximize the load voltage at severe sags. In

both cases a phase jump may be undesirable for the load and may initiate transient currents in capacitors, transformers and motors, etc. The operation of line commutated converters may also be disturbed by a sudden change in the phasor of the load voltage.

# 2.8.1 Energy Optimal Compensation

For the loads which are not sensitive to phase changes, it is not necessary for the load voltage to be in phase with the pre-sag voltage. Load voltage vector can lie anywhere on the periphery of a circle, the radius of which equals to the amplitude of the pre-sag voltage, Figure 2.11 [16].

The function of the DVR shown in Figure 2.12 is to ensure that any load voltage disturbance can be compensated for effectively and the disturbance is therefore transparent to the load. The corresponding phasor diagram describing the electrical conditions during a voltage sag is depicted in Figure 2.11, where only the affected phase is shown for clarity [16]. V<sub>S</sub> is the source voltage, V<sub>1</sub> is the incoming supply voltage before compensation, V<sub>2</sub> is the load voltage after compensation, V<sub>dvr</sub> is the series injected voltage of the DVR, and I is the line/load current.  $\varphi$ ,  $\delta$  and  $\alpha$  represent load power factor angle, supply voltage phase angle, and load voltage advance angle, respectively. Energy optimal compensation is realized by the adjustment of  $\alpha$ . One distinct advantage of the scheme is that less real power needs to be injected from the DVR energy storage unit into the distribution system, which permits the DVR to help the load rides through more severe voltage sags, if the real power requirement of the DVR is provided by the energy storage device in the form of a battery, a capacitor bank, or a fly-wheel. The reactive power requirement is generated by the inverter.



Figure 2.11 Phasor Diagram of Power Distribution System During a Sag

Consider the power flow contributions of the DVR under the energy optimal compensation scheme. If  $P_{in}$  and  $P_{out}$  are the input power from the source and the load power respectively, then [16];

$$P_{in} = \sum_{\forall j} V_{1j} I_j \cos(\phi - \alpha + \delta_j)$$
(2.11)

$$P_{out} = \sum_{\forall j} V_{2j} I_j \cos(\phi)$$
(2.12)

the subscript j represents the jth phase and j=1, 2, 3.

With the correction introduced by the DVR, assume a balanced load  $(I_j = I)$  and a balanced output voltage  $(V_{2j} = V_2)$ 

$$P_{out} = 3V_2 I \cos(\phi) \tag{2.13}$$



Figure 2.12 Typical Schematic of a Power Distribution System Compensated By a DVR

Let  $P_{dvr}$  be the real power supplied by the DVR, then from (2.11) and (2.13)

$$P_{dvr} = P_{out} - P_{in} \tag{2.14}$$

$$P_{dvr} = 3V_2 I \cos(\phi) - \sum_{\forall j} V_{1j} I \cos(\phi - \alpha + \delta_j)$$
(2.15)

Similarly, let  $Q_{in}$  and  $Q_{out}$  are be the input reactive power from the source and load reactive power, respectively, then;

$$Q_{in} = \sum_{\forall j} V_{1j} I_j \sin(\phi - \alpha + \delta_j)$$
(2.16)

$$Q_{out} = \sum_{\forall j} V_{2j} I_j \sin(\phi) = 3V_2 I \sin(\phi)$$
(2.17)

Denote the reactive power supplied by the DVR as  $Q_{\mbox{\scriptsize dvr}},$  then;

$$Q_{dvr} = Q_{out} - Q_{in} \tag{2.18}$$

$$Q_{dvr} = 3V_2 I \sin(\phi) - \sum_{\forall j} V_{1j} I \sin(\phi - \alpha + \delta_j)$$
(2.19)

From (2.15) and (2.197), it is apparent that the control of real and reactive power exchange between the DVR and distribution system is possible with the adjustment of the phase angle  $\alpha$  for given  $\varphi$ ,  $\delta$ , V<sub>1</sub> and V<sub>2</sub>.

# 2.8.1.1 Minimum Power Operation

The real and reactive powers supplied by the DVR depend on the type of voltage disturbance experienced as well as the direction o the DVR injected voltage component with reference to presage voltage.  $P_{dvr}$  depends on the advance angle  $\alpha$ , for a given  $\delta$  and  $V_1$ , as shown in Figure 2.11. Indeed, depending on the particular values of  $\alpha$  used, the minimum value of  $P_{dvr}$  can be negative. When this occurs, it means that real power is being absorbed by the DVR. However, there is no technical and economical advantage by operating this way; during the sag period, the DVR should be exporting energy to support the load instead of drawing more power from the source. A negative  $P_{dvr}$  may even worsen the sag situation. A larger energy storage facility will be required to deliver for the absorbed power for no obvious technical advantage [16].

The possibility of operating at  $P_{dvr}=0$  during sag is an interesting proposition. The following analysis is therefore carried out to explore this possibility by determining the corresponding value of  $\alpha$  for such an operation.

Case 1: Operation at  $P_{dvr} = 0$ : From (2.15);

$$3V_2 I \cos(\phi) - \sum_{\forall j} V_{1j} I \cos(\phi - \alpha + \delta_j) = 0$$
(2.20)

Let  $X = \sum V_{1j} \cos(\delta_j)$ ,  $Y = \sum V_{1j} \sin(\delta_j)$ , then the phase advance angle  $\alpha$  that corresponds to  $P_{dvr} = 0$  is given by;

$$\alpha_{opt} = \phi + \beta - \arccos\left(\frac{3V_2\cos(\phi)}{\sqrt{X^2 + Y^2}}\right)$$
(2.21)

where  $\beta = \arctan(Y/X)$ . It can be seen from the expressions already shown that for balanced sags,  $\beta = \delta$ .

A necessary condition for the existence of  $\alpha_{opt}$  is such that

$$\sqrt{X^2 + Y^2} \ge 3V_2 \cos(\phi)$$
 (2.22)

Thus, DVR voltage correction with zero power injection is possible only if the condition imposed by (2.22) is satisfied. Indeed, if one were to consider a balanced  $sag\sqrt{X^2 + Y^2}$  equals  $3V_1$  for which it can be seen that (2.22) will be satisfied if and only if the per unit value of the sustained sag voltage is greater than the load power factor, assuming  $V_2$  is normalized to remain at 1 p.u. Of course, if it is not necessary to maintain  $V_2$  at 1p.u., then the effect of the particular disturbance can still be mitigated using zero power injection.

If the voltage sag is so severe that (2.22) can not be satisfied, then the optimum value of  $\alpha$  can still be calculated by setting  $dP_{dvr}/d\alpha = 0$ . At this operating point, the DVR is supplying minimum real power to the external system to keep V<sub>2</sub>=1 p.u. This is considered next.

Case 2: Optimal Operation When  $P_{dvr} > 0$ : As  $I_j \neq 0$ , use (2.13) and set  $dP_{dvr}/d\alpha = 0$ . This means that;

$$\sum_{\forall j} V_{1j} \sin(\phi - \alpha + \delta_j) = 0, \text{ i.e. } \alpha_{opt} = \phi + \beta$$
(2.23)

Therefore, the results of cases 1 and 2 can be combined to determine an optimum  $\alpha$  adjustment strategy for any given disturbance as follows:

If

$$\left[\left(\sum_{\forall j} V_{1j} \cos(\delta_j)\right)^2 + \left(\sum_{\forall j} V_{1j} \sin(\delta_j)\right)^2\right]^{1/2} \ge 3V_2 \cos(\phi)$$
(2.24)

then

$$\alpha_{opt} = \phi + \beta - \arccos\left(\frac{3V_2\cos(\phi)}{\sqrt{\left(\sum V_{1j}\cos\delta_j\right)^2 + \left(\sum V_{1j}\sin\delta_j\right)^2}}\right)$$
(2.25)

else

$$\alpha_{opt} = \phi + \beta \tag{2.26}$$

The corresponding DVR injection voltage and real power requirement under  $\alpha_{opt}$  control strategy are;

$$V_{dvr}^{j} = \sqrt{V_{2}^{2} + V_{1j}^{2} - 2V_{2}V_{1j}\cos(\alpha_{opt} - \delta_{j})}$$
(2.27)

$$P_{dvr}^{opt} = 3V_2 I \cos(\phi) - \sum_{\forall j} V_{1j} I \cos(\phi - \alpha_{opt} + \delta_j)$$
(2.28)

# 2.8.2 Presag Compensation

By carrying similar derivations, the injected voltage of DVR and power applied during sag for DVR under presag injection control are given as [16];

$$V_{dvr,presag}^{j} = \sqrt{V_{2}^{2} + V_{1j}^{2} - 2V_{2}V_{1j}\cos(\delta_{j})}$$
(2.29)

$$P_{dvr}^{presag} = 3V_2 I \cos(\phi) - \sum_{\forall j} V_{1j} I \cos(\phi + \delta_j)$$
(2.30)



Figure 2.13 Phasor Diagram of Presag Compensation.

# 2.8.3 In-Phase Compensation

For completeness, the corresponding equations for DVR under in-phase injection control are given as;

$$V_{dvr,inphase}^{j} = V_2 - V_1 \tag{2.31}$$

$$P_{dvr}^{inphase} = 3V_2 I \cos(\phi) - \sum_{\forall j} V_{1j} I \cos\phi$$
(2.32)



Figure 2.14 Phasor Diagram of In-Phase Compensation.

# 2.9 Short Circuit Operation and Protection of DVR

If the voltage drop caused by the DVR does not affect the load requirements, the secondary of the injection transformer may be short circuited during steady-state operation in two ways. One method is triggering the individual converter legs such as to establish a short-circuit path for the transformer low voltage leg. Note that no switching of semiconductors occurs in this type of operation. Therefore, only the comparatively low conduction losses of the semiconductors in this current loop contribute to losses. The switching of semiconductors may be seen in Figure 2.15 during short circuit operation (SCO) [10].



Figure 2.15 Short Circuit Operation of DVR with DVR Semiconductors

Another method to short circuit the transformer secondary is achieved by introducing a solid state bypass switch between the inverter and the transformer secondary. Furthermore since the Dynamic Voltage Restorer is connected in series, it will see the full load current as well as any currents due to downstream faults. In case of any temporary abnormal condition (i.e. load current overloads, etc.) the DVR will go into bypass until the load current returns normal conditions. Thyristors may be applied for the short-circuit device in order to protect the semiconductors to be thermally destroyed in case a downstream fault. Figure 2.16 illustrates the location of the short circuit device [10].



Figure 2.16 Short circuit operation with Thyristors

Measures implemented for the short-circuit operation of DVR can be used as protection scheme of DVR against short-circuit on the load current or large inrush current that may on the line DVR operates.

# CHAPTER3

#### SANKO SYSTEM MODELING AND DVR DESIGN

Within the scope of this study, Super Film located in Gaziantep which is one of the SANKO subsidiary company will be handled as a practical case study from Turkish industry. Super Film manufactures film products that are to be used for packaging of various industrial outcomes ranging from food to tobacco, cassette, serviette, soap, etc. Within its production process very critical processes such as tension, thickness and gloss control are involved.

# 3.1 Sanko System Description and Modeling

SANKO Super Film facility has an installed capacity of 39.550 MVA, including two service transformers, 1.25MVA and 2.25MVA, Service TR1 and Service TR2 in Figure 3.1 It is fed from 154 kV feeder from Gaziantep Industry Region, Transformer Center #2. Its single line distribution diagram is given in Appendix A.1. As also seen from Figure 3.1 connection to the 154 kV feeder is through a 100 MVA power transformer. Within the facility there are 3 synchronous generators installed, each of which has a capacity of 8.396 MW. Synchronous generators are used to power the installed capacity of facility. When synchronous generators produce more power than needed at any instant, remaining power is sold to utility. If they are not enough to supply power, extra power is drawn from utility. Power is distributed within the facility in the medium voltage range, 31.5 kV.



Figure 3.1 The Block Diagram of SANKO Super Film

# 3.1.1 Synchronous Machine and Exciter Modeling

# 3.1.1.1 Synchronous Machine Modeling

Synchronous machines installed at facility are known to be 8.396 MW. Their rated terminal voltage is 11 kV and pf is 0.8. Since no more information could be gathered from Super Film electrical authorities, only  $X_d$ " is known to be 0.19. To be more realistic in simulation, a similar synchronous machine is found in the literature and its parameters are put in the modeling of the machines [18].

R <sub>a</sub>	0.00363
X <sub>d</sub>	1.0525
Xq	0.6478
X <sub>d</sub> '	0.3806
X <sub>d</sub> "	0.2609
X <sub>q</sub> "	0.261
T <sub>d0</sub> '	9.21
T <sub>d0</sub> "	0.030
T <sub>q0</sub> '	0.052

TABLE 3.1: Synchronous Machine Modeling Parameters

# **3.1.1.2 Exciter Modeling**

As suggested in [18], IEEE DC1A type exciter is chosen to be modeled in the simulation. Its block diagram is given in Figure 3.2 and parameters in Table 3.2.



Figure 3.2 The Block Diagram of IEEE DC1A Exciter

K <sub>A</sub>	90
T <sub>A</sub>	0.08
T <sub>c</sub>	0.0
T <sub>B</sub>	0.0
T <sub>E</sub>	0.85
K <sub>E</sub>	1
A <sub>E</sub>	0.0625
$\mathbf{B}_{\mathrm{E}}$	1.15
V <sub>rmax</sub>	-1.8
V <sub>rmin</sub>	-1.8
K <sub>F</sub>	0.052
T <sub>F</sub>	1.5
X <sub>c</sub>	0.06
R <sub>c</sub>	0.0
Tr	0.003

# TABLE 3.2: IEEE DC1A Exciter Modeling Parameters

# 3.1.2 Wire Modeling

Wire modeling is based on the reference [19] and according to Table 3.3.

Cabla Tura	DC Resistance at 20°C	Operating Inductance
Cable Type	(Ω/km)	(mH/km)
3(1x240/25) XLPE, 31.5 kV	0.0754	0.603
3(1x95/16) XLPE, 31.5 kV	0.193	0.686
3(1x120/16) XLPE, 31.5 kV	0.153	0.665
3x2(1x120/16) XLPE, 11 kV	0.153	0.647
(1x70) NYY, 400V	0.268	0.5x10 <sup>-4</sup>
(1x70) NYY, 31.5 kV	0.268	0.5x10 <sup>-4</sup>
3x477 MCM, 31.5 kV	0.1194	7.49x10 <sup>-4</sup>
3x1/0, 31.5 kV	0.5362	8.9x10 <sup>-4</sup>
3x3/0, 31.5 kV	0.3366	8.9x10 <sup>-4</sup>

 TABLE 3.3: Power Cable Equivalent Resistance and Inductance

#### 3.1.3 Transformer Modeling

Since only available data from Super Film for transformers are MVA rating ,  $U_k$  rating, terminal voltages and configuration, they were modeled as they are and the rest of the parameters are modeled to represent the typical values.

### 3.2 DVR Design

DVR design was implemented to protect a 3.2 MVA critical load from 40% 3-phase and 50% single phase line to ground faults, therefore total capacity of the DVR came out to be 1.6 MVA. To be realistic, all the component ratings are chosen to be practical, i.e. if this system is needed to be implemented, suitable components can be found from the market.

Compensation system, DVR is inserted into 31.5 kV, before the step-down transformer. Its performance against different single and three phase fault scenarios

has been evaluated. The simulated fault locations are shown in Appendix A.2 as marked on the Super Film single line distribution diagram.

# 3.2.1 DVR Topology

Load side connected shunt converter topology was chosen to be the suitable DVR topology, Figure 3.3.



Figure 3.3 Load Side Connected Shunt Converter

Shunt converter feeding the DC-link is feed from the regulated load voltage, so DClink is almost constant, which ease the control of DVR. Since no limit on the capacity of DC-link, duration of the deepest sag that can be compensated is only limited by the thermal constraints on the semiconductors.

Power equations governing the load side connected shunt-converter are as follows:

$$P_{shunt} = P_{series} \cong \frac{\left(1 - V_{sag} / V_{rated}\right)}{V_{sag} / V_{rated}} \times P_{load}$$
(3.1)

$$I_{series} = I_{\sup ply} \cong \frac{P_{load}}{3 \times V_{sag}}$$
(3.2)

$$I_{shunt} = \frac{\left(1 - V_{sag} / V_{rated}\right)}{V_{sag} / V_{rated}} \times I_{load}$$
(3.3)

The relationship shows the main drawback of the topology, that is the high current through the series converter. For example in case of a 50% voltage, the current through the series converter increases at a rate of 200% (required supply current doubles) and through the shunt converter, current equal to  $I_{load}$  is drawing. This topology not only provides a clean and controlled voltage input to the rectifier, but also results in improved overload rating for the inverter during non-sagged voltage conditions [10].

#### 3.2.2 The Control of DVR

The control of DVR is chosen to be a combination of closed-loop PI control and feed-forward control. This combination combines the fast response of feed-forward control and the closely tracking of the load voltage during sag. Closely tracking of load voltage is especially important when there occurs single-phase or to-phase line-to-ground faults. If the close tracking of load voltage can not be obtained, some voltages may be over compensated while some other may stay under compensated.



Figure 3.4 Block Diagram of the Control of DVR

In Figure 3.4  $V_{ref}$  is the reference for the load voltages,  $V_{load}$  is the load side voltage and  $V_{source}$  is the source side voltage.  $K_i$  represent the gain of the inverter,  $V_{inv}$  is the inverter control signal, n is the turns ratio of the injection transformer. In the control strategy, magnitude of source and load side voltages is tracked by applying Fast Fourier Transform (FFT) and comparing them with reference voltage magnitudes. Two error voltages derived from load voltage error and source voltage error are combined to get a single voltage error which is fed to the inverter.

The phase difference between the reference signal and the source voltage and between the reference signal and the load voltage is continuously tracked and the phase of the reference signal for the inverter is calculated according to the in-phase voltage injection strategy. One disadvantage of the control strategy is the delay in the detection of sag voltage due to delay in the FFT block, it takes about 20ms for FFT block to reach steady-state, i.e. a sag can fully be detected after 20ms.

# **3.2.2.1 Voltage Injection Strategy**

In-phase compensation scheme is chosen to be applied to DVR since it is the strategy that results in the lowest of the injected voltage, thus lowest source side voltage rating of the injection strategy. Although power needed in this strategy is not minimal as in the case of energy optimal compensation, its power requirement is less than that of pre-sag compensation scheme.

#### 3.2.3 DVR Components Design

#### 3.2.3.1 Converter

Three single phase full bridge voltage source inverters are used to generate threephase voltages needed by the DVR which is a very common topology for DVR converters. In the generation of gate signals from reference signal from the control block unipolar pulse width modulation scheme is used. This scheme has the advantage of effectively doubling the switching frequency as far as the output harmonics are concerned, compared to the bipolar voltage switching scheme, i.e. when the inverter semiconductors switch at 500Hz first harmonic frequency will be 1kHz, which ease the filtering of produced harmonics.

### 3.2.3.2 Filter

An effective filtering scheme in DVR implementation is critical, since it affects both transient and steady state performance during sag and steady state performance during non-sag condition.

When advantages of line-side and inverter-side filter are compared, line-side filtering seems more preferable if at 50% sag voltage suitable capacitor can be found from the market. From the view point of harmonic elimination, the inverter-side filter scheme may be a preferable, since no harmonic voltage is passed to injection transformer reducing transformer rating, but the addition of filter inductance in series with the load causes in evitable voltage drop during sag compensation and non-sag condition. Also, the phase difference caused by the filter may downgrade the DVR control performance. In the light of this knowledge line-side filter is chosen to be applied in the DVR.

#### 3.2.3.3 Injection Transformer

Since three single phase full bridge inverter is used to generate DVR voltages, three single phase transformer is needed to inject the generated voltages to the line. The MVA rating of the injection transformer will be half the critical load MVA rating, since the deepest sag to be compensated will be 50%. And 50% voltage sag also determines the primary voltage rating as 50% of the rated voltage in the line. Turns ratio of the transformer is determined by the available semiconductor switches and the DC-link capacitor on the market. It has been reduced to the point where components can be found for feasible price, since this DVR should be practically implementable. Primary current rating is determined by the load current rating and

the harmonic currents penetrating to the transformer due to the inverter switches. For good short-circuit performance of the transformer, it is needed to have small leakage inductance and resistance, but when the leakage reactance of the transformer is used as the inductance of the filter it is desirable to have high leakage which reduces the cost of the transformer.

#### 3.2.3.4 DC-Link

In the load-side connected shunt converter topology there is continuous source of power, then the value of the capacitance can be significantly lower than that of DVR with sole capacitor in the DC-link. The value of the capacitor will be decided according to the simulation results.

# 3.2.3.5 Shunt Converter

The shunt converter of the DVR is implemented with three phase bridge rectifier. But it can not be directly connected to the distribution line, since then the DC-link voltage will be charged to the peak of load voltage. For the purpose of connecting three phase bridge rectifier to the line, three phase step-down transformer is utilized. Its rating will be the half critical load rating to be protected. According to the DClink voltage diodes for the shunt converter will be selected.

# 3.2.4 Protection and Short Circuit Operation of DVR

The protection and short circuit operation of DVR is implemented by properly switching the semiconductors of the VSIs. By this way additional thyristors needed during short circuit operation are eliminated. Since DVR is rated to compensate for 50% voltage sags, the current rating of the semiconductor switches must be enough to handle full load current which makes them suitable for continuous operation during non-sag condition.

# **CHAPTER4**

#### **DVR SIMULATION AND RESULTS ON SUPER FILM FACILITY**

For the modeling of power distribution system of Super Film facility and proposed DVR components PSCAD/EMTDC simulation tool was used. It is a time domain simulation tool, which is customized for high voltage system modeling and simulation with its available library of models ranging from machines to semiconductors and from control block functions to transmission line models.

The performance criteria of proposed DVR operation is compensation of load voltages with a fast dynamic response according to the voltage injection strategy with harmonic content within the limits defined by [11].

To observe the effects of the possible faults within the distribution system and the performance of DVR against these faults, three fault locations was defined. Simulated fault cases are given in Table 4.1. To be typical voltage sag, the duration of the sag was set to be 200ms, which starts at 0.52ms and lasts till 0.72ms.

In the simulated cases, voltage sag was generated by applying a fault through a controllable resistance between phases and ground. In fault cases #1, #2 and #3 in Table 4.1, indicated fault depths as 40%, 50% were achieved by playing with the fault resistance at the specified location. But in fault cases #4 and #5, one or three phase was totally shorted to ground through a zero ohm resistor.

Case	Fault Location	Fault Description
Case #1	Fault#3	40%, Three-Phase-to-Ground Fault, 154kV line
Case #2	Fault#3	50%, Single-Phase Line-to-Ground Fault, 154kV line
Case #3	Fault#2	40%, Three-Phase-to-Ground Fault, 31.5kV line
Case #4	Fault#1	Solid, Three-Phase-to-Ground Fault, 0.4kV line
Case #5	Fault#1	Solid, Single-Phase Line-to-Ground Fault, 0.4kV line

TABLE 4.1: Simulated Fault Cases

Illustrations of the simulated fault types are in Figure 4.1.



Figure 4.1 Simulated Fault Types

One of the loads within facility was chosen to be the critical load with capacity of 2x1.6MVA.

The modeled power system and all the modeled modules are given Appendix B.

The load angles of the synchronous generators were adjusted such that all the required power by the system is generated by the generators when the system is loaded to the 80% percent of the full load at power factor of 0.8.

In the modeled power system, load flow analysis has been done and the results in Table 4.2 have been obtained, where  $P_{in}$  is the input active power from the feeder,  $Q_{in}$  is the input reactive power from the feeder,  $P_{load}$  is the total active power delivered to load,  $Q_{load}$  is the total reactive power delivered to load,  $P_{gen}$  is the total active power from generators,  $Q_{gen}$  is the total reactive power from generators:

P <sub>in</sub> (MW)	0.38
Q <sub>in</sub> (MVAR)	8.5
P <sub>load</sub> (MW)	13.10
Q <sub>load</sub> (MVAR)	11.64
P <sub>gen</sub> (MW)	12.42
Q <sub>gen</sub> (MVAR)	4.92

TABLE 4.2: Load Flow Analysis of Modeled Power System

Table 4.2 indicates that load balance is satisfied in the simulated system, i.e. active and reactive power required by the load is equal to the supplied active and reactive power from input feeder and synchronous generators.

# 4.1 Voltage Data for Critical Load

As an input to DVR design, on the modeled power system, at the three fault locations, the defined faults at the previous paragraphs was applied and voltage at the terminals of the critical load were recorded with and without the synchronous generators integrated to the power system. The results taken are given in Table 4.3 indicating the readings at the 150ms of the total sag period, which are phase voltage rms values.

		Without Generator (kV)	With Generator (kV)
Normal	Ph-A	19.02	19.05
Conditions	Ph-B	18.98	19.00
	Ph-C	19.07	19.02
	Ph-A	11.5	11.72
Case #1	Ph-B	11.56	11.81
	Ph-C	11.4	11.59
	Ph-A	9.98	10.21
Case #2	Ph-B	18.25	18.39
	Ph-C	18.9	19.07
	Ph-A	11.518	11.72
Case #3	Ph-B	11.55	11.73
	Ph-C	11.53	11.75
	Ph-A	18.6	18.74
Case #4	Ph-B	18.5	18.66
	Ph-C	18.54	18.71
	Ph-A	18.98	19.1
Case #5	Ph-B	18.99	19.07
	Ph-C	19	19.12

TABLE 4.3: The Load Voltage with/without Synchronous Generators

As seen from the results of Table 4.3, synchronous generators can not respond fast enough to the voltage changes at their terminals. At 150ms from the beginning of the sag, only approximately 0.2kV change can be obtained due to presence of generators.

# 4.2 Parameters of Simulated DVR

In view of Chapter 3 and the optimization technique given in [10], for fault simulation DVR parameters were chosen to be as shown in Table 4.4.

	Parameters
DVR	
Rated Capacity	1.6MVA
Max. Injection Capacity-Single Phase	50%
Max. Injection Capacity-Three Phase	40%
Voltage Injection Duration	-
Injection Transformer	
Rated Capacity	1.6MVA
Leakage Impedance	0.05 p.u.
Primary Voltage Rating (rms)	12.6kV
Secondary Voltage Rating (rms)	1.60kV
No Load Losses	0.02 p.u.
Magnetizing Current	0.4%
Inverter	
Semiconductor Voltage	2200V DC
Semiconductor Current (peak)	1.95kA
Switching Frequency	500Hz
DC-Link Capacitor	
Voltage	2200V DC
Current (rms)	4 kA
Size	80mF
Filter Capacitor	
Voltage (rms)	12.6kV
Size	35µF
Current (rms)	400A
Shunt Transformer	
Rating	2MVA
Primary Voltage	31.5kV
Secondary Voltage	1.60kV
Leakage Inductance	0.06 p.u.
No load losses	0.1 p.u.
Magnetizing Current	2%
Rectifier Diodes	
Voltage (peak)	2.2kV
Current (peak)	10kA
Current (rms)	3.2kA

# 4.3 Performance of DVR Against Different Fault Cases

# 4.3.1 DVR Performance Against Faults at 154kV

Case#1 and Case#2 faults are generated at the power entry to the facility with proper fault resistance. The instance at which fault applied is 0.52ms and fault lasts till 0.72ms, between  $t_i$  and  $t_f$ .

# 4.3.1.1 154kV,Case#1 Fault

Firstly, three-phase, 40%, line-to-ground fault will be considered, since it will be the most powerful fault that will be faced by the DVR.



Figure 4.2 The Source, Injected and Load Line-to-Neutral Voltages (Case#1)



Figure 4.3 Three-Phase Source, Load Line-to-Line RMS Voltages (Case#1)

DVR performance can be observed from Figure 4.2 and Figure 4.3, in these figures 40% sag on the incoming there phase voltages is compensated to the pre-sag value by applying the DVR voltage.

In Figure 4.3 a steady-state voltage difference between source and load voltage is observed, this is due to the inevitable voltage drop on the transformer due to the leakage reactance and resistance present.



Figure 4.4 Phase-A Source, Injected and Load Line-to-Neutral Voltages (Case#1)

When source, injected and load voltages of phase-A is examined, Figure 4.4, it is clearly seen that in-phase injection scheme has been achieved.



Figure 4.5 Phase-A, Output Line-to-Neutral Voltage of Inverter and DVR (Case#1)



Figure 4.6 Phase-A, Output Line-to-Neutral Voltage of Inverter and DVR (Case#1)

Unipolar PWM switching scheme can be observed from Figure 4.5 and Figure 4.6. Pulsating voltage at the output of the inverter is filtered out of its high frequency harmonics and injected to the line. THD calculation according to Appendix C indicates that at this maximum sag depth THD of the load side voltage is 4.212, which is well below the limit indicated by [11]

The voltage stress on the semiconductor, current through it and its antiparallel diode is given in Figure 4.7. When these current and voltage stresses are considered together with the switching frequency, it is thought to that IGBT is a good candidate for the switch of the VSIs. The upper leg switches of the inverters carry the whole load current during the short circuit operation of DVR.



Figure 4.7 IGBT Voltage, IGBT Current and Antiparallel Diode Current (Case#1)


Figure 4.8 IGBT Voltage, IGBT Current and Antiparallel Diode Current (Case#1)

The current on the load side of DVR, source side of DVR and current through the shunt converter is as given Figure 4.9. As seen from the figure source side current is the sum of load side and shunt converter currents and due to the distorted current drawn from the shunt converter. Shunt converter draws current during sag at the points where the incoming line voltage exceeds the DC-link voltage, which clearly indicates that it will increase with low DC-link capacitance, since then voltage drop on the DC-link will be high.



Figure 4.9 Load Side, Source and Shunt Converter Currents (Case#1)

When the current through the filter capacitor and injection transformer is examined, it is seen that their currents are the combination of load current plus the harmonic current coming from the inverter as stated in Chapter 3, so their rating should chosen accordingly Figure 4.10, Figure 4.11.



Figure 4.10 Injection Transformer and Filter Capacitor Currents-Large Scale (Case#1)



Figure 4.11 Injection Transformer and Filter Capacitor Currents-Small Scale (Case#1)



Figure 4.12 DC-Link Capacitor Line-to-Neutral Voltage (Case#1)

During sag since large current porportional to sag depth is drawn from DC-link, its voltage reduces according to the installed capacitance on the DC-link. Due to the fed switching converters large switching currents are drawn from the capacitance, so the capacitor should be capable of producing that large currents, Figure .4.13 and Figure 4.14.



Figure 4.13 DC-Link Capacitor Current-Large Scale (Case#1)



Figure 4.14 DC-Link Capacitor Current-Small Scale (Case#1)

The above simulation results will be the input to the selection of DVR components since in this case the lost power due to sag, thus the power that will be injected by DVR is the highest.



Figure 4.15 Generator Line-to-Line rms and Line-to-Neutral Voltages (Case#1)

If the voltage on generator terminals is investigated, it is seen that generator has no contribution on the recovery of lost voltage due to the sag, Figure 4.15.

## 4.3.1.2 154kV,Case#2 Fault

Secondly, single-phase, 50%, line-to-ground fault will be considered. As seen from Figure 4.16, only phase-A has a sag depth of 50%. But again DVR is capable of restoring load voltage. It is obvious that in this case three-phase rms voltage drop is less than the previous case, Figure 4.17. In this case, the injected voltage on phase-A is higher due to the higher drop on phase-A.



Figure 4.16 Phase-A, Source, Injected and Line-to-Neutral Load Voltages (Case#2)



Figure 4.17 Three-Phase Source, Load Line-to-Line RMS Voltages (Case#2)



Figure 4.18 Phase-A Source, Injected and Load Line-to-Neutral Voltages (Case#2)

Again when source, injected and load voltages of phase-A is examined, it is clearly seen that in-phase injection scheme has been achieved, Figure 4.18.



Figure 4.19 Phase-A, Output Line-to-Neutral Voltage of Inverter and DVR (Case#2)

THD calculation according to Appendix C indicates that at this case THD of the load side voltage is 3.2741, which is well below the limit indicated by [11].

In this case the current through the semiconductor and its antiparallel diode is less in proportion to the lost power due to sag, Figure 4.20, but small increase in the voltage on semiconductors during sag, since in this case voltage drop on the DC-link is smaller. The situation is also true for source and diode rectifier current, Figure 4.21 and also for injection transformer and filter capacitor currents, Figure 4.22.



Figure 4.20 IGBT Voltage, IGBT Current and Antiparallel Diode Current (Case#2)



Figure 4.21 Load Side, Source and Shunt Converter Currents (Case#2)



Figure 4.22 Injection Transformer and Filter Capacitor Currents (Case#2)

Compared to the 40% three-phase fault, this fault results in small drop on DC-link voltage, Figure 4.23, and lower capacitor current, Figure 4.24.



Figure 4.23 DC-Link Capacitor Line-to-Neutral Voltage (Case#2)



Figure 4.24 DC-Link Capacitor Current (Case#2)

# 4.3.2 DVR Performance Against Faults at 31.5kV

## 4.3.2.1 31.5kV,Case#3 Fault

For 31.5kV line, three-phase, 40%, line-to-ground fault will be considered. This case is the same as 154kV line, three-phase, 40%, line-to-ground fault case from power lost, and the response of the DVR point of view. But in this case there is a phase-shift between the pre-sag and post-sag voltages. This is because fault appears on the adjacent 31.5kV line which is parallel to the 31.5kV line feeding the critical load,

large current drawn due to fault causes a phase shift. The overall response of the system is shown in Figure 4.25.



Figure 4.25 The Source, Injected and Load Line-to-Neutral Voltages (Case#3)

The performance of the DVR is same as 154kV fault case, by injecting proper voltages load voltage is recovered to the pre-sag level. Application of in-phase injection scheme is successfully achieved with a load voltage THD of 4.03, Figure 4.26, and Figure 4.27.



Figure 4.26 Phase-A Source, Injected and Load Line-to-Neutral Voltages-Large Scale (Case#3)



Figure 4.27 Phase-A Source, Injected and Load Line-to-Neutral Voltages-Small Scale (Case#3)

## 4.3.3 DVR Performance Against Faults at 0.4kV

In this fault case on one of the parallel loads to the critical load a three-phase and single-phase solid line-to-ground faults are applied. By this way at the load end all three phases or one of the phases reduced to zero during sag. as shown in Figure 2.28, and Figure 4.32.

#### 4.3.3.1 0.4kV,Case#4 Fault

Three-phase, solid line-to-ground fault was applied to the load end, which reduces all the three-phases to zero at the 0.4kV side as shown in Figure 2.28. But at the 31.5kV side only a little drop occurs. At his case, DVR source side, load side and injected

voltages are shown in Figure 2.29. Actually DVR injects negligible voltage as shown in Figure 2.30.



Figure 4.28 LV and HV Side Line-to-Neutral Fault Voltages (Case#4)



Figure 4.29 The Source, Injected and Load Line-to-Neutral Voltages (Case#4)



Figure 4.30 Phase-A Source, Injected and Load Line-to-Neutral Voltages (Case#4)

In this case inverter output pulses a very small, Figure 4.31. Load THD achieved in this fault is 1.2659.



Figure 4.31 Phase-A, Output Line-to-Neutral Voltage of Inverter and DVR (Case#4)

#### 4.3.3.2 0.4kV, Case#5 Fault

Single-phase, solid line-to-ground fault was applied to the load end, which reduces phase-A to zero at the 0.4kV side as shown in Figure 4.32. But at the 31.5kV side, the voltage sag is negligible, even less than the previous three-phase case. But to be complete DVR source side, load side and injected voltages have been put for reference, Figure 4.33, but all the other waveforms are omitted. Load voltage THD for this case has been measured as 1.1647.



Figure 4.32 LV and HV Side Line-to-Neutral Fault Voltages (Case#5)



Figure 4.33 The Source, Injected and Load Line-to-Neutral Voltages (Case#5)

## 4.4 Performance of DVR Against Parameter Variation

In this section with 40%, three-phase line-to-ground condition on 154kV line, various parameters in the DVR changed and the performance change has been observed.

#### 4.4.1 Performance of DVR with Inverter Side Filter

In this stage every thing with the DVR has been kept the same but line side filter has been changed with inverter side filter, for Case#1 fault. In the inverter side filter  $L_f$ , filtering inductance was chosen to be 1mH and filter capacitor  $C_f$  was chosen to be 100µH with the switching frequency of 1kHz. Load side, source side and DVR injected voltages for this case is shown in Figure 4.34. As seen from the figure and as stated in Chapter 2 and 3, the combined effect of leakage reactance of the injection transformer and filter inductor result in high voltage drop during steady state, for this case 1.73kV drop occurred on rms line-to-line voltage. When this filtering scheme is used, DVR secondary side voltage contains no harmonic voltages therefore these are not involved in the current of the series injection transformer.

The remaining performance graphics are the same as line-side filtering scheme, so only DC-link voltage and current is shown for reference in Figure 4.35. Load voltage THD obtained in this case appeared to be 3.8984.



Figure 4.34 The Source, Injected and Load Line-to-Neutral Voltages (Inverter-Side Filter)



Figure 4.35 DC-Link Capacitor Line-to-Neutral Voltage and Current (Inverter-Side Filter)

# 4.4.2 Performance of DVR Against Switching Frequency Variation

DVR switching frequency was changed to 1.5kHz from 500Hz while keeping other parts unchanged under Case#1 fault condition. The waveforms in Figure 4.36 were obtained. The increase in the switching frequency can be visualized in Figure 4.36. With the same line-side filter parameters used in the previous simulations, obtained load voltage THD level, 3.4251 is better than the previous one.



Figure 4.36 The Source, Injected and Load Line-to-Neutral Voltages (1.5kHz)



Figure 4.37 Phase-A, Output Line-to-Neutral Voltage of Inverter and DVR (1.5kHz)

## 4.4.3 Performance of DVR Against DC-Link Capacitance Variation

As in the previous cases 80mF DC-link capacitor was used, in this case DVR performance will be observed for 60mF, 40 mF, 20 mF and 10 mF DC-link capacitance cases keeping the other parameters unchanged. The load side, source side and DVR injected voltages for each case is given in Figure 4.38, Figure 4.39, Figure 4.40, and Figure 4.41.



Figure 4.38 The Source, Injected and Load Line-to-Neutral Voltages (60mFcapacitance)



Figure 4.39 The Source, Injected and Load Line-to-Neutral Voltages (40mFcapacitance)



Figure 4.40 The Source, Injected and Load Line-to-Neutral Voltages (20mFcapacitance)



Figure 4.41 The Source, Injected and Load Line-to-Neutral Voltages (10mFcapacitance)

The effect of DC-link capacitance variation on THD of final load voltage is given in Table 4.5. The results indicates that the higher the capacitance, the lower the THD. But considering the limit on the THD is 5, at the DVR implementation to be cost effective 10mF capacitance can be used.

Capacitance (mF)	THD
60	3.3957
40	3.3965
20	3.45
10	3.5150

TABLE 4.5: Load Voltage THD Variation Against DC-Link Capacitance

The resultant DC-link capacitance voltage and current waveforms are given in Figure 4.42, Figure 4.43, Figure 4.44, and Figure 4.45.



Figure 4.42 DC-Link Line-to-Neutral Voltage and Current Waveforms (60mFcapacitance)



Figure 4.43 DC-Link Line-to-Neutral Voltage and Current Waveforms (40mFcapacitance)



Figure 4.44 DC-Link Line-to-Neutral Voltage and Current Waveforms (20mFcapacitance)



Figure 4.45 DC-Link Line-to-Neutral Voltage and Current Waveforms (10mFcapacitance)

Figure 4.42, Figure 4.43, Figure 4.44, and Figure 4.45 indicates that decreasing the DC-link capacitance increases the voltage drop on the DC-link during sag, and but there is not significant effect on the current drawn from the capacitance, a little increase in current with decreasing capacitance may be mentioned.

## 4.4.4 Performance of DVR Against Line-Side Filter Parameter Variation

It is known that filtering performance of the DVR is very important to be able to get an acceptable load voltage. In this section filter parameters of the line-side filter, filter capacitance and injection transformer leakage reactance has been varied and the performance was examined.

# TABLE 4.6: Load Voltage THD Variation Against Line-Side Filter Parameter Variation

Leakage Reactance (p.u.)	Capacitance (µF)	THD
0.1	17.5	4.0195
0.07	25	3.7691
0.05	35	4.2122

For the above two cases load-side, source-side and DVR injected voltages are given in Figure 4.46 and Figure 4.47.



Figure 4.46 The Source, Injected and Load Line-to-Neutral Voltages (0.1pu Leakage Reactance, 17.5µH Filter Capacitance)



Figure 4.47 The Source, Injected and Load Line-to-Neutral Voltages (0.07pu Leakage Reactance, 25µH Filter Capacitance)

Injection transformer and filter capacitor variation are given in Figure 4.48 and Figure 4.49.



Figure 4.48 Injection Transformer and Filter Capacitor Currents (0.07pu Leakage Reactance, 25µH Filter Capacitance)



Figure 4.49 Injection Transformer and Filter Capacitor Currents (0.1pu Leakage Reactance, 17.5µH Filter Capacitance)

Although the leakage reactance, filter capacitance product remains the same, with the increase in leakage reactance steady-state voltage drop of DVR increases. Increasing the leakage reactance of the injection transformer increase the portion of the harmonic current flows in the transformer. The same is also true for filter capacitance.

The higher the leakage reactance the easier the manufacturing of the transformer, so it is preferable. On the other hand we want to use as small capacitance as possible due to the cost.

The known fact that leakage reactance of the transformer causes steady-state voltage drop on the transformer is proven by the data in Table 4.7. For reference the voltage drop of inverter-side filter has also been added, it is very large compared to line-side filtering scheme voltage drop.

Leakage Reactance (p.u.)	Source Side Line-to-	Load Side Line-to-
	Neutral Voltage (kV)	Neutral Voltage (kV)
0.05	31.09	30.64
0.07	31.09	30.47
0.1	31.07	30.19
0.05 + 1mH filter inductor		
for line side filter	31.1	29.37

TABLE 4.7: Steady-State Line Voltage Drop Due to Transformer Leakage Reactance

The decision of filter parameters will be an optimization between the filtering performance and cost of the filter.

# 4.5 Suitable Components from the Market

When a material search is done from the market, all components can be fouund. If we list:

• IGBT :

5SNA 1200E250100 from ABB (2500V, 1200A)
5SNR 10H2500 from ABB (2500V, 1000A)
5SNX 10H2500 from ABB (2500V, 1000A)
CM1200HA-50H from Mitsubishi (2500V, 1200A)
CM1200HB-50H from Mitsubishi (2500V, 1200A)
CM1200HC-50H from Mitsubishi (2500V, 1200A)

• IGBT-Antiparallel Diode:

5SKF20H2500 from ABB (2500V, 2000A)

5SLF20H2500 from ABB(2500V, 2000A)

• Shunt Rectifier Diode:

DZ540N from EUPEC (2600V, 1150A)

• DC-Link Capacitor

DKTFM2K405507 from AVX (5.5mF, 2500V), at least 2 parallel units needed.

MKP, DC Filter Capacitors from VISHAY (4.4mF, 2600V) at least 3 parallel units needed.

• Filter Capacitor

MKP, Filter Capacitors from VISHAY (128.6 $\mu$ F, 12000V) single unit enough.

## CHAPTER5

#### CONCLUSIONS

In this study, a custom power device, DVR has been modeled and applied on the model of an industrial facility, SANKO-Super Film.

With the development of more complicated process control equipment in the industry, more sensitive devices to the changes on the incoming supply voltage takes place on the market. This increase the severity of the power quality problems caused by non-ideal bus voltages. These non-idealities can be under-voltage, over-voltage, harmonics, shortages or sags. Although it does not seem so severe, every year large cost of lost production is paid by different manufacturers in the industry due to voltage sag, short periods of under-voltage, up to a few hundreds of milliseconds.

Precautions to voltage sags differ from location point of view, measure can be taken just at critical load terminals or at the terminals of the facility that contain the critical load or at the distribution system level, the also indicates the order of application cost from lowest to highest. Since there is not regulation for the distribution authority for such an improvement so for the moment each customer has to implement its own solution.

Basic operation of DVR, its critical components and design criteria was given as a reference. Within DVR components, filter, Voltage Source Inverter, injection transformer, DC-link, shunt rectifier has been examined. Also DVR injection strategies introduced, minimal energy control, in-phase injection and pre-sag injection strategies have been discussed.

Till now, various different applications of DVR have been recorded in the literature in different sizes. 2MVA DVR by Duke Power, in South Carolina, again 2MVA DVR by Westinghouse, in Australia, first platform mounted DVR by Westinghouse, in Canada, the world's largest DVR 2x22.5MVA by ABB, in Israel have been put in service.

In the Turkish industry, Super Film manufacturing film products has been chosen to be a practical application of DVR. Film production process is known to be very sensitive to voltage sags. It was recorded from the facility that temporary reduction of voltages causes considerable production loss. So this industry is a good candidate for DVR applications.

For the operation of DVR load-side connected shunt converter has been chosen to be the suitable topology, since no energy storage is necessary there is no limit on the duration of voltage sag except from the thermal stress on the semiconductors and ease of control due to constant DC-link voltage. DC-link is fed from shunt converter, which is a three-phase diode bridge rectifier. Three single-phase VSI and thus three single-phase injection transformers have been used to inject voltages to the incoming line. Since there occurs steady-state voltage drop due to inverter-side filter inductance, line-side filtering scheme was adopted in the DVR realization. On the VSI, unipolar switching strategy was used and effective frequency at the output of DVR appeared to be twice of the actual switching frequency.

Within the study the effect of frequency has been examined and increase in the frequency led to ease of filtering and reduction of load voltage THD.

When DC-link capacitance effect was investigated it was observed that even at the lower capacitance values DVR worked well enough to produce the required load voltage with THD well below the limit values.

Inverter-side filter was compared with the line-side filter scheme in Section 4.4.1 and as the theory suggests large voltage drop on the load voltage during steady-state

recorded. But it is also seen that inverter-side filter reduces the size of the injection transformer, since in this case no harmonic voltage penetrates to the transformer.

In the investigation of line-side filter parameters, it was seen that high leakage reactance increases the voltage drop on DVR, but eases the manufacturing of transformer. And also the increase in the leakage reactance results in increase in harmonics currents on the transformer, the same is true for filter capacitor value.

In the SANKO-Super Film facility modeling and simulations, 80% of full load is assumed and the entire load is fed from three synchronous generators. But in the case of fault condition the synchronous generators could not respond fast enough to compensate for the sag.

In the light of theory and the results of simulations, suitable components from the market have been proposed for the DVR realization. And this has shown that this custom power device can be implementable.

Single phase line to ground faults are the most common types of faults in the medium voltage distribution systems such as 31.5kV lines within the SANKO-Super Film facility [20]. When the waveforms of such a case are examined, it can be seen that a solid single-phase line-to-ground fault generated on phase-A causes other phase voltages (phase-B and phase-C) to rise up significantly as shown in Figure 5.1. The simulated DVR is capable of compensating for the missing voltage on phase-A, but it takes no action for the rise of voltage on phase-B and phase-C. This is another aspect of voltage sag compensation; some type of voltage sags can give rise to voltage swells on the non-faulted phases, especially when the distribution transformers in the system are not solidly grounded, rather grounded through an impedance. If this insufficiency of simulated DVR can be improved, it can be a complete solution for all types of voltage sags. In Figure 5.1,  $t_i$  and  $t_f$  are the instants that represent the beginning and the end of fault respectively.


Figure 5.1 The Source, Injected and Load Line-to-Neutral Voltages, 31.5kV Solid Single-Phase Line-to-Ground Fault

Within the scope of this thesis simulation of one practical case from the Turkish industry was made. This simulation can be improved to realize the actual situation, load requirements can be get from the facility and put into the design and with the recording of typical sags DVR performance can be optimized. Inclusion of compensation schemes for voltage swells accompanying voltage sags should be a must for the future study. After improving the simulation a scaled laboratory prototype can be develop before actually developing the full rated DVR.

#### REFERENCES

- [1] A. Boscolo, S. Quaia, F. Tosato "No Energy Stored Power Conditioners for Voltage Sag Compensation", Electrotechnical Conference, pp. 1194-1198, 1998
- [2] "Voltage Characteristics of Electricity Supplied by Public Distribution Systems", Dansk Standard DS/EN50160, January 31, 1995.
- [3] Michael D. Stump, Gerald J. Keane, Frederick K. S. Leaong, "The Role of Custom Power Products in Enhancing Power Quality at Industrial Facilities", Energy Management and Power Delivery, pp. 508-517, 1998.
- [4] Jeff Lamoree, Dave Mueller, Paul Vinett, William Jones, Marek Samotyj "Voltage Sag Analysis Case Studies", IEEE Transactions on Industry Applications, Vol. 30, Number 4, pp. 1083-1089, July/August 1994.
- [5] Toni Wunderlin, Peter Dahler, David Amhof, Horst Grüning, "Power Supply Quality Improvement with a Dynamic Voltage Restorer", Energy Management and Power Delivery, pp. 518-525, 1998.
- [6] John Godsk Nielsen, Frede Blaabjerg, Ned Mohan, "Control Strategies for Dynamic Voltage Restorer Compensating Voltage Sags with Phase Jump", Applied Power Electronics Conference and Exposition, pp. 1267-1273, 2001

- [7] Arindam Ghosh, Gerard Ledwich, "Structures and Control of a Dynamic Voltage Regulator", Power Engineering Society Winter Meeting, pp. 1027-1032, 2001.
- [8] Russel Buxton, "Protection from Voltage Dips with the Dynamic Voltage Restorer", Dynamic Power Ltd. Review, pp. 3/1-3/6, 1998.
- [9] John Godsk Nielsen, "Analysis of Topologies for Dynamic Voltage Restorer", pp. 1027-1032, 2001.
- [10] Çağrı ACAR, "The Analysis of a Dynamic Voltage Restorer Based on Load Side Connected Shunt Converter Topology", METU, 2002.
- [11] "Bozucu Etki Yaratan Müşterilerin Uymak Zorunda Olduğu Koşullar", TEAŞ, Haziran 1992.
- [12] S. S. Choi, B. H. Li , D. M. Vilathgamuwa, "Design and Analysis of the Inverter-Side Filter Used in the Dynamic Voltage Restorer", IEEE Transactions on Power Delivery, Vol.17, No.3, pp. 857-864, July 2002.
- [13] S. S. Choi, B. H. Li , D. M. Vilathgamuwa, "Design Considerations on the Line-Side Filter Used in the Dynamic Voltage Restorer", IEE Proc.-Gener. Distrib, Vol.148, No.1, pp. 1-7, January 2001.
- [14] Chi-Jen Huang, Shyh-Jier Huang, Fu-Sheng Pai, "Design of Dynamic Voltage Restorer With Disturbance-Filtering Enhancement", IEEE Transactions on Power Electronics, Vol.18, No.5, pp. 1202-1210, September 2003.
- [15] John Godsk Nielsen, Frede Blaabjerg, "Control Strategies for Dynamic Voltage Restorer Compensating Voltage Sags with Phase Jump", IEEE, pp. 1267-1273, 2001.

- [16] D. .Mahinda Vilathgamuwa, A. A. D. Ranjith Perera, S. S. Choi, "Voltage Sag Compensation With Energy Optimized Dynamic Voltage Restorer", IEEE Transactions on Power Delivery, Vol.18, No.3, pp. 928-936, July 2003.
- [17] S. S. Choi, B .H. Li , D.M.Vilathgamuwa, "On the Injection Transformer Used in the Dynamic Voltage Restorer", Power System Technology, pp. 941-946, 2000.
- [18] Meng Shen, Vaithiananthan Venkatasubramanian, Nicholas Abi-Samra, Dejan Sobajic, "A New Framework for Estimation of Generator Dynamic Parameters", IEEE Transactions on Power Systems, Vol.15, No.2, pp. 756-761, May 2000.
- [19] "Insulated Wires and Power Cables Catalog", September 2000.
- [20] A. Elnady, M. M. A. Salama, M. Kazerani, "An Efficient Compensator for The Voltage Related Power Quality Problems in Distribution Systems", Power Electronics Specialist, 2003, PESC'03, IEEE 34<sup>th</sup> Annual Conference on, Vol: 3, pp. 1235-1241, June 2003.

## APPENDIX A

#### SANKO-SUPER FILM DIAGRAM

## A.1 Sanko-Super Film Single Line Diagram

Sanko-Super Film Single Line Diagram is given at the next page.









# A.2 Sanko Super Film Single Line Diagram-Fault Locations

Fault locations on Sanko-Super Film Single Line Diagram is given at the next page.









### **APPENDIX B**

#### **PSCAD SIMULATIONS**

# B.1 Super Film and DVR Power Diagram

The implemented Super Film power diagram and the model of DVR is given at the next page.





# Figure B.1 Sanko-Super Film and DVR Power Diagram

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#### **B.2 PSCAD Modules**

Power circuit of Super Film and DVR was given in Appendix B.2. Below is the control module block diagram, Figure B.2.



Figure B.2 PSCAD Control Diagram

In the control block load side and source side voltages are compared with the reference signals and error signal magnitudes are generated. With the phase tracking of reference voltage with the source voltage, phase input to the inverter reference signal is obtained. The magnitudes of source, load and reference voltages are obtained through default FFT block of PSCAD/EMTDC.



Figure B.3 Gate Signal Generation

Gate signals for the inverter swtiches are generated by comparing the reference signal with the triangular carrier according to the unipolar switching scheme.



Figure B.4 Short Circuit Operation

Since no short-circuit device for the DVR has been incorporated, the short-circuit operation of DVR has been implementing by closing the upper leg switches of the inverter.



Figure B.5 Phase Difference Calculator

Since it is needed to track the difference between the source and the reference voltage for in-phase injection scheme, phase difference calculator has been implemented as shown in Figure B.5.

### **APPENDIX C**

### **THD Calculator**

%Waveform is named as x.	
x_rms=sqrt(mean(x.^2)); %Total rms	
Fs=2e4;	
Fn=Fs/2;	
NFFT=2.^(ceil(log(length(x))/log(2)));	% Next highest power of 2
	% greater than length(x).
NFFT=20000;	
FFTX=fft(x,NFFT);	% Take FFT, padding with zeros.
	% length(FFTX)==NFFT
NumUniquePts = ceil((NFFT+1)/2);	
FFTX=FFTX(1:NumUniquePts);	% FFT is symmetric, throw away
	% second half
MX=abs(FFTX);	% Take magnitude of X
MX=MX*2;	% Multiply by 2 to take into
	% account the fact that we
	% threw out second half of
	%FFTX above
MX(1)=MX(1)/2;	% Account for endpoint
	% uniqueness
MX(length(MX))=MX(length(MX))/2;	% We know NFFT is even
MX=MX/length(x);	% Scale the FFT so that it is

% not a function of the length

% of x.

x\_rms2=sqrt(sum(MX(60:10001).^2))/sqrt(2); % rms sum except fundamental

% component

IL=18.2; %this value should be modified wrt to the maximum load current

TDD=x\_rms2/IL\*100

% total demand distortion in percent of % IL

f=(0:NumUniquePts-1)\*2\*Fn/NFFT;

bar(f,MX)

% title('Harmonic Spectrum','FontSize',14)

% xlabel('Frequency (Hz)','FontSize',14)

% xlim([-40 5000])

% grid on;

% set(gca,'XTickLabel', {'0';'150';'450';'750';'1050';'1350';'1650'})

% % set(gca,'XTick',[0 160 440 760 1040 1360 1640]);

% ylabel('Magnitude (A, Peak)','FontSize',14)