ELECTRICAL TRANSPORT IN METAL-OXIDE-SEMICONDUCTOR CAPACITORS

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ABSTRACT

ELECTRICAL TRANSPORT IN METAL-OXIDE-SEMICONDUCTOR CAPACITORS

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The current transport mechanisms in metal-oxide-semiconductor (MOS) capacitors have been studied. The devices used in this study have characterized by current-voltage analyses. Physical parameter extractions and computer generated fit methods have been applied to experimental data. Two devices have been investigated: A relatively thick oxide (125 nm) and an ultra-thin oxide (3 nm) MOS structures. The voltage and temperature dependence of these devices have been explained by using present current transport models.

Keywords: Metal-Oxide-Semiconductor, ultra-thin oxide, Schottky emission, Fowler-Nordheim, Poole-Frenkel, trap.

ÖZ

METAL-OKSİT-YARI İLETKEN KONDANSATÖRLERDE ELEKTRİKSEL TAŞIMA

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Metal-Oksit-Yarı iletken (MOS) kondansatörlerdeki elektriksel taşıma mekanizmaları incelendi. Bu çalışmada kullanılan aygıtlar akım-gerilim yöntemleri kullanılarak karakterize edildi. Fiziksel katsayı çıkarımı ve bilgisayarla yaratılmış verilerin uyumu yöntemleri deneysel verilere uygulandı. İki aygıt incelendi: Göreceli kalın oksit (125 nm) ve aşırı ince oksit (3 nm) MOS yapıları. Bu aygıtların gerilim ve sıcaklık bağımlılıkları günümüzdeki akım-gerilim modelleri kullanılarak açıklandı.

Anahtar kelimeler: Metal-Oksit-Yarı iletken, aşırı ince oksit, Schottky salımı, Fowler-Nordheim, Poole-Frenkel, kapan..

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CHAPTER 1

METAL-OXIDE-SEMICONDUCTOR STRUCTURE AND CONDUCTION MECHANISMS

1.1 Introduction

In this introduction part of the thesis, mainly three books on semiconductor devices will be followed [1-4]. The information which is given as a summary of those books here can be found in those references and in many other books on semiconductor devices in a more detailed form.

There are a number of fundamental structures in today's microelectronics such as p-n junctions, metal-semiconductor contacts, MOS capacitors, MOSFETs, BJTs. Among them, the metal-oxide-semiconductor capacitors or MOS-Cs are very important because that the MOS capacitor is central to understanding the operation of MOSFETs since it uses an MOS capacitor structure as its control, or gate. Control of the electrical properties of the MOS system has been one of the major factors that have led to stable and high performance silicon integrated circuits. The MOS capacitors are also the most useful devices in semiconductor surface research. A MOS-C is also used as a basic device in many applications such as EEPROMs, DRAMs, optical sensors, solar cells etc. The simplicity of fabrication are among the main advantages of these structures.

The MOS structure was first proposed as a varactor in 1959 and its characteristics were then analyzed in 1961-62. The MOS diode was first employed in the study of a thermally oxidized silicon surface in 1962-63 [1, 2, and references therein].

1.2 MOS Capacitor

The MOS capacitor consists of a Metal-Oxide-Semiconductor structure as illustrated by Figure 1.1. Shown is the semiconductor substrate with a thin insulating layer and a top metal contact, the gate. A second metal layer forms an ohmic contact to the back of the semiconductor, also referred to as the bulk. The structure shown has a p-type substrate. We will refer to this as an n-type MOS capacitor since the inversion layer contains electrons. In this thesis, we use the convention that the voltage V is positive when the metal plate is positively biased with respect to the ohmic contact, and V is negative when the metal plate is negatively biased with respect to the ohmic contact.

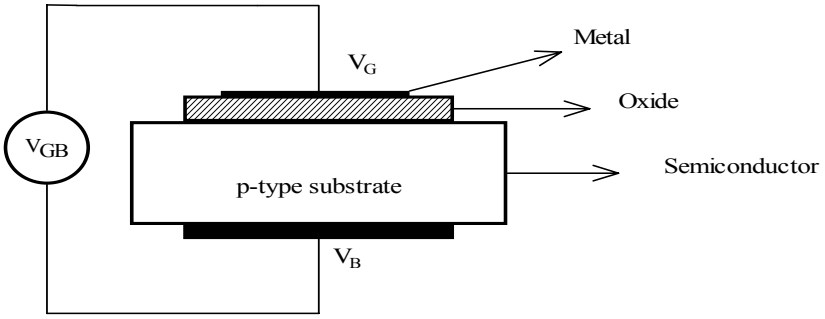

Fig.1.1 Metal-Oxide-Semiconductor capacitor [3].

1.2.1 Ideal MOS Capacitor

The Energy-band diagram of an ideal MOS diode for zero bias is shown in Fig.1.2:

In Sze [1], an ideal MOS diode is defined as follow;

i. In case of zero applied bias, metal (ϕ_m) and semiconductor (ϕ_s) work-function difference (ϕ_{ms}) is zero. The band is flat (flat-band condition) when there is no voltage applied Eq.1.1. :

$$\phi_{ms} \equiv \phi_m - \left(\chi + \frac{E_g}{2q} - \psi_B \right) = 0 \qquad (1.1)$$

ii. The only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those with the equal but opposite sign on the metal surface adjacent to the insulator.

iii. There is no carrier transport through the insulator under dc biasing conditions, or the resistivity of the insulator is infinite.

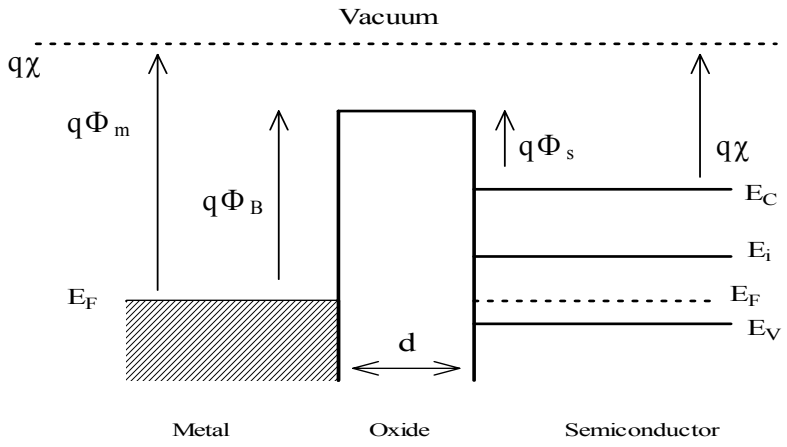

Fig.1.2 Ideal Metal-Oxide-Semiconductor capacitor band diagram [1].

1.2.2 Biasing the MOS Capacitor

Accumulation, Depletion and inversion cases may occur when a MOS-C is biased depending on the thype of the substrate and bias direction.. Here we review these modes of operation and the relationships between band-bending, charge, and electric field for a MOS capacitor on a p-type substrate.The analysis for an n-substrate MOS capacitor is similar, with obvious changes for different doping type, doping and fermi level etc.[3].

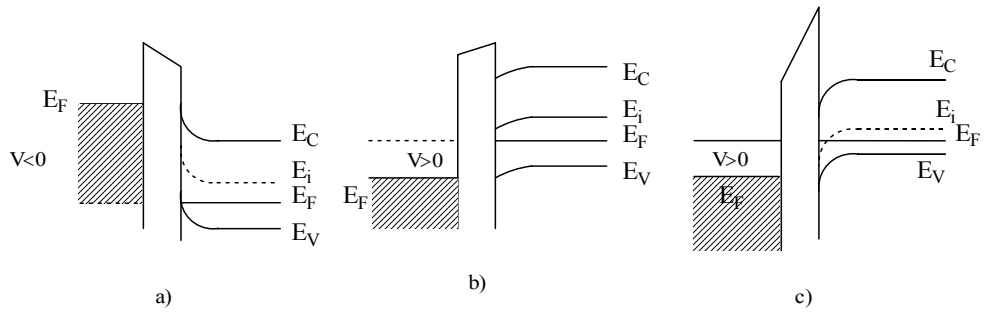

Fig.1.3 Biasing Metal-Oxide-Semiconductor diode with p-type substrate: (a) accumulation; (b) depletion; (c) inversion [1].

To understand the different bias modes of an MOS capacitor we now consider three different bias voltages. These bias regimes are called the accumulation, depletion and inversion mode of operation [3].

1.2.2.1 Accumulation

Accumulation occurs when one applies a voltage, which is less than the flatband voltage. The minority carriers on the gate attract majority carriers from the substrate to the oxide-semiconductor interface. Only a small amount of band bending is needed to build up the accumulation charge so that almost all of the potential variation is within the oxide.

1.2.2.2 Depletion

As a more positive voltage than the flatband voltage is applied, a negative charge builds up in the semiconductor. Initially this charge is due to the depletion of the semiconductor starting from the oxide-semiconductor interface. The depletion layer width further increases with increasing gate voltage.

1.2.2.3 Inversion

As the potential across the semiconductor increases beyond twice the bulk potential, another type of negative charge emerges at the oxide-semiconductor interface: this charge is due to minority carriers, which form a so-called inversion layer. As one further increases

the gate voltage, the depletion layer width barely increases further since the charge in the inversion layer increases exponentially with the surface potential.

1.2.3 Surface Space-Charge Region

In this subsection, the relations between the surface potential, space charge and the electric field are shown. These relations play important role in electrical characteristics of the ideal MOS structures.

Figure 1.4 shows a detailed band diagram at the surface of a p-type semiconductor. The potential ψ_s is defined as zero in the bulk of the semiconductor and is measured with respect to the intrinsic Fermi level E_i as shown. At the semiconductor surface, $\psi = \psi_s$ and ψ_s is called the surface potential. The electron and hole concentrations as a function of ψ are given by the following relations;

$$\begin{aligned} p_p &= p_{p_0} \exp(-q\psi / kT) = p_{p_0} \exp(-\beta\psi) \\ n_p &= n_{p_0} \exp(q\psi / kT) = n_{p_0} \exp(\beta\psi) \end{aligned} \tag{1.2}$$

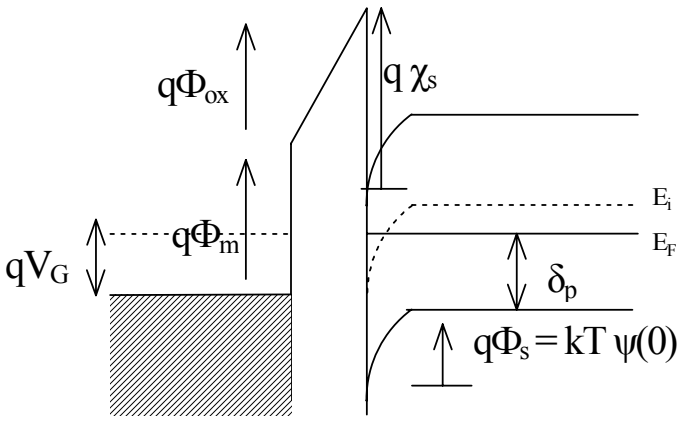

Fig.1.4 Energy-band diagram at the surface of a p-type semiconductor [1].

where ψ is positive when the band is bent downward (as shown in Fig.1.4), n_{p_0} and p_{p_0} are the equilibrium densities of electrons and holes, respectively, in the bulk of the semiconductor, k boltzmann constant, T temperature and $\beta = q/kT$. At the surface the densities are:

$$\begin{aligned} n_s &= n_{p_0} \exp(\beta\psi_s) \\ p_p &= p_{p_0} \exp(-\beta\psi_s) \end{aligned} \tag{1.3}$$

From previous discussions and with the help of Eq.1.3, the following regions of surface potential can be distinguished:

$\Psi_s < 0$	accumulation of holes (band bends downward)
$\Psi_s = 0$	flat-band condition
$\Psi_B > \Psi_s > 0$	depletion of holes (band bends downward)
$\Psi_B = \Psi_s$	midgap with $n_s = p_s = n_i$ (intrinsic concentration)
$\Psi_B < \Psi_s$	inversion (band bends downward, electron enhancement)

The potential Ψ as a function of distance can be obtained by using the one dimensional Poisson equation.

1.2.4. Work-Function Difference and Flat-band Voltage

For an ideal MOS diode, it is assumed that the work-function difference for an n-type semiconductor is zero. If the value of ϕ_{ms} is not zero and if oxide charges Q_0 exist in SiO_2, the experimental capacitance-voltage curve will be shifted from the ideal theoretical curve by an amount;

$$V_{FB} = \phi_{ms} - \frac{Q_o}{C_i} = \phi_{ms} - \frac{Q_o + Q_f + Q_m + Q_{it}}{C_i} \tag{1.4}$$

where V_{FB} is called the flat-band voltage shift, Q_f fixed charges, Q_m mobile charges and Q_{it} interface states. If negligible interface traps, mobile ionic charges and oxide trapped charges exist, equation reduces to;

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_i} \tag{1.5}$$

1.2.5 Ideal MOS Capacitor Analysis

We now give the MOS parameters with the aid of Figure 1.4

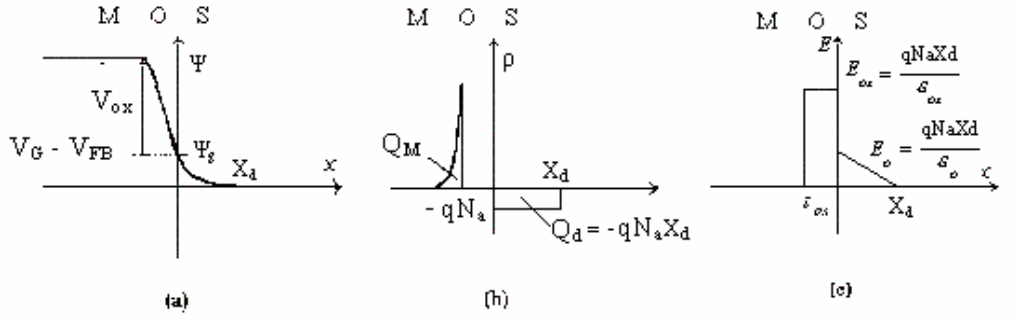

Fig.1.5 (a) Potential; (b) charge; (c) electric field diagram at the surface of a p-type semiconductor [3].

Two assumptions will be made to simplify the MOS analysis: i) the full depletion approximation can be used in a MOS-C and ii) inversion layer charge is zero below the threshold voltage. We also assume that inversion layer charge linearly changes with the gate voltage for voltages beyond the threshold. The derivation starts by examining the charge per unit area in the depletion layer, Q_d. As can be seen in Figure 1.5.b, this charge is given by:

$$Q_d = -qN_a X_d \tag{1.6}$$

Where X_d is the depletion layer width and N_a is the acceptor density in the substrate. The Electric field distribution which is obtained by integration of the charge density is shown in Fig. 1.5.c. The electric field in the semiconductor at the interface, E_s, and the field in the oxide E_{ox}, are equal:

$$E_s = \frac{qN_a X_d}{\varepsilon_s} \tag{1.7}$$

The difference in the dielectric constants of oxide and semiconductor causes an abrupt change in the electric field at the oxide-semiconductor interface. The dielectric constant for Silicon is $11.9\varepsilon_0$ and for SiO_2 is $3.9\varepsilon_0$. Therefore the electric field is about three times larger

in the oxide side at the semiconductor-oxide interface. The electric field in the semiconductor changes linearly due to the constant doping density and is zero at the edge of the depletion region. The potential shown in Figure 1.5.a is obtained by integrating the electric field. The potential at the surface, ψ_s, equals:

$$\psi_s = \frac{qN_a X_d^2}{2\varepsilon_s} \tag{1.8}$$

The calculated field and potential is only valid in depletion. In accumulation, there is no depletion region and the full depletion approximation does not apply. In inversion, there is an additional charge in the inversion layer, Q_{inv}. This charge increases gradually as the gate voltage is increased. However, this charge is only significant once the electron density at the surface exceeds the hole density in the substrate, N_a. We therefore define the threshold voltage as the gate voltage for which the electron density at the surface equals N_a. This corresponds to the situation where the total potential across the surface equals twice the bulk potential, ψ_B.

$$\psi_B = V_T \ln \frac{N_a}{n_i} \tag{1.9}$$

The depletion layer in depletion is therefore restricted to this potential range;

$$X_d = \sqrt{\frac{2\varepsilon_s \psi_s}{qN_a}} \quad \text{for} \quad 0 \le \psi_s \le 2\psi_B \tag{1.10}$$

For a surface potential larger than twice the bulk potential, the inversion layer charge change increases exponentially with the surface potential. Consequently, an increased gate voltage yields an increased voltage across the oxide while the surface potential remains almost constant. We will therefore assume that the surface potential and the depletion layer width at threshold equal those in inversion. The corresponding expressions for the depletion layer charge at threshold, $Q_{d,T}$, and the depletion layer width at threshold, $X_{d,T}$, are given as:

$$Q_{d,T} = -qN_a X_{d.T} \tag{1.11}$$

$$X_{d,T} = \sqrt{\frac{2\varepsilon_s(2\psi)}{qN_a}} \tag{1.12}$$

Beyond threshold, the total charge in the semiconductor has to balance the charge on the gate electrode, Q_M, or

$$Q_M = -(Q_d + Q_{inv}) \tag{1.13}$$

where we define the charge in the inversion layer as a quantity which needs to determined but should be consistent with our basic assumption. This leads to the following expression for the gate voltage, V_G:

$$V_G = V_{FB} + \psi_s + \frac{Q_M}{C_{ox}} = V_{FB} + \psi_s - \frac{Q_d + Q_{inv}}{C_{ox}} \tag{1.14}$$

where C_{ox} is the oxide capacitance.

In depletion, the inversion layer charge is zero so that the gate voltage becomes:

$$V_G = V_{FB} + \psi_s + \frac{\sqrt{2\varepsilon_s qN_a\psi_s}}{C_{ox}} \quad \text{for } 0 \le \psi_s \le 2\psi_B \tag{1.15}$$

while in inversion this expression becomes:

$$V_G = V_{FB} + \psi_B + \frac{\sqrt{4\varepsilon_s qN_a\psi_s}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} = \Delta V_T - \frac{Q_{inv}}{C_{ox}} \tag{1.16}$$

the third term in Eq.1.16 states our basic assumption, namely that any change in gate voltage beyond the threshold requires a change of the inversion layer charge

1.3 MOS Capacitor and Oxide Charges

This section can be found in B. Van Zeghbroeck`s book, "*Principles of Semiconductor Devices"* in a more detailed from [3]. The most important metal-insulator-semiconductor structure is metal-SiO_2-Si by far and in this subsection, SiO_2-Si system will be described briefly and the oxide and interface charges will be reviewed. A picture of the SiO_2-Si

interface is that the chemical composition of the interfacial region, as a consequence of thermal oxidation, is single-crystal silicon followed by a monolayer of SiO_x, that is, incompletely oxidized silicon, then a strained region of SiO_2 and the remainder stoichiometric, strain-free, amorphous SiO_2. For a practical MOS diode, interface traps and oxide charges exist that will, in one way or another, affect the ideal MOS characteristics. There are four general types charges associated with SiO_2-Si diodes :

i. Fixed Oxide Charge (Q_f , N_f); these are positive charges due primarily to structural defects (ionized silicon) in the oxide layer. The density of this charge, whose origin is related to the oxidation process, depends on the oxidation ambient and temperature, cooling conditions, and silicon orientation. Because that the fixed oxide charges cannot be determined unambiguously in the presence of moderate densities of interface trapped charges, these are only measured after a low-temperature hydrogen or forming gas anneal, which minimizes interface trapped charge.

ii. Oxide trapped charges (Q_{ot} , N_{ot}); these charges may be positive or negative due to holes or electrons trapped in the bulk of the oxide. Trapping may result from ionizing radiation, avalanche injection, tunneling or other mechanisms. Unlike fixed oxide charges, oxide trapped charges are sometimes annealed by low-temperature treatments, although neutral traps remain.

iii. Mobile oxide charges (Q_m, N_m); these are caused primarily by ionic impurities such as Na^+, Li^+, K^+, and possibly H^+. Negative ions and heavy metals may contribute to this type of charges.

iv. Interface trapped charge (Q_{it}, Q_{ss}, N_{it}, N_{ss} D_{it}); this type of charge is also called surface states, fast states, interface states, and so on. These are positive or negative charges, due to structural defects, oxidation-induced defects, metal impurities, or other defects caused by radiation or similar bond-breaking processes. These charges are located at the SiO_2-Si interface. Unlike fixed charges or trapped charges, they are in electrical communication with the underlying silicon. Interface traps can be charged or discharged, depending on the surface potential. Most of the interface states can be neutralized by low-temperature hydrogen or forming gas anneals. These localized states can affect the I-V characteristic of MOS capacitor. The effect of these states can be grouped into two categories: The first group is concerned with the electrostatic effects while the second with the dynamic effect [2]. The electrostatic effect can be xplained as follows; due to the charge storage in

the surface states, charge distrubition through and voltage drop over the oxide are affected strongly by interface state concentration D_{it}. There are two types of surface states; donor-like and acceptor-like states. The energy of donor states is less than the energy of surface state, which contributes a positive Q_{ss} when they are emptied while the energy of the latter is greater than E_{ss} which contributes a negative Qss, when they are occupied. The value of Qss and its sign can increase or decrease the band bending ψ_s. The dynamic effects of surface states are important at two points; first, they provide additional path for the carriers and secondly, they act as recombination centers.

1.4. Current Mechanisms in MOS Capacitors

In this section we present an extensive list of several proposed MIS current models and we give brief descriptons of those models.

1.4.1 Fowler-Nordheim Tunneling

Fowler-Nordheim emission is one of the most important mechanisms in MOS structures. It is the tunneling of electrons between the gate and the conduction band of the bulk through a triangular barrier. This mechanism was first proposed by Fowler and Nordheim [5] and then named after them. In the last three decades the FN tunnelng in the MOS capacitor structure has been intensively studied by many researchers [6-18]. The tunnel current component is computed as;

$$J_{FN} = a \mid E \mid^2 \exp(-b/|E|) \tag{1.17}$$

where a and b are fitting parameters and E is the electric field in the oxide. Lenzlinger and Snow [6] generalized the model and obtained a more explicit analytical result. Their current density is given as:

$$J_{FN} = \frac{q^3 m_0}{8 m_{ox} h \phi_b \pi} |E^2| \cdot \exp(-\frac{4\sqrt{2 m_{ox} \phi_b^3}}{3q\hbar|E|}) \tag{1.18}$$

where m_{ox} is the mass of the carriers in the oxide, m_0 is the free electron mass, h planck constant, q charge and φ is the potential barrier height that a carrier tunnels through. The oxide mass and the barrier height are used as physically-based fitting parameters. This

emission occurs under high electric field (more than 8-10 MeV/cm) since the theory assumes the barrier to be triangular. A brief derivation of Fowler-Nordheim current density for simple case ,that is no image force lowering or no finite temperature effects, is as follows (in this derivation we follow Depas et. al. [19]):

The tunneling current between tha gate and the semiconductor is given by

$$J_{FN} = \frac{4\pi q m_t}{h^3} \int_0^{E_F} dE \int_0^{E} T_t dE_t \tag{1.19}$$

where E_t is the transversal energy component, E the energy of the tunneling electron measured from the semiconductor conduction band edge at the SiO_2-Si interface and T_t the tunneling probability. T_t is given by WKB approximation as:

$$T_t = \exp(-2\int_0^{x_1} k_{ox}(x)dx) \tag{1.20}$$

where k_{ox} is the wave vector of the tunneling electron and x is the barrier length. After all the calculations performed, the tunneling probability is found as;

$$T_t = \exp(-\frac{4\sqrt{2m_{ox}}}{3qh} \frac{(\phi_b + E_F - E + \frac{m_t E_t}{m_{ox}})^{3/2}}{E_{ox}}) \tag{1.21}$$

A first order Taylor expansion on T around $E = E_F$ and $E_t = 0$ leads to the Eq.1.18. A plot of ln (J/E^2) vs. 1/E ,so called Fowler-Nordheim plot, should be straight line if the F-N mechanism is the dominant mechanism in conduction through the oxide. The intercept and the slope of this plot yield the oxide mass and the barrier height.

1.4.2 Direct Tunneling

An accurate modeling of tunneling current in today`s ultra-thin oxide MOS devices cannot be accomplished by widely used Lenzlinger-Snow FN model since it implies a metal as a gate and a triangular barrier. They are largely obsolete conditions for today`s devices where very high tunneling probability due to ultra-thin oxides (less than 4-5 nm), quantization effects of both electrons and holes in both inversion and accumulation regime, poly-silicon

depletion, several tunneling mechanisms besides conduction band electron tunneling and a trapezoidal barrier play fundamental role in conduction. For these reasons many authors have proposed new models to introduce these effects into current modeling [20-27]. In 1993, Schuegraf and Hu [28] introduced a tunneling model by taking the fact that the poly-silicon gate and interface states at SiO_2-Si cause a trapezoidal barrier rather than triangular barrier as in Fowler-Nordheim emission, into account. Their approach was the same as Snow and Lenzlinger`s but their tunneling probability was modified appropriety with respect to new barrier shape:

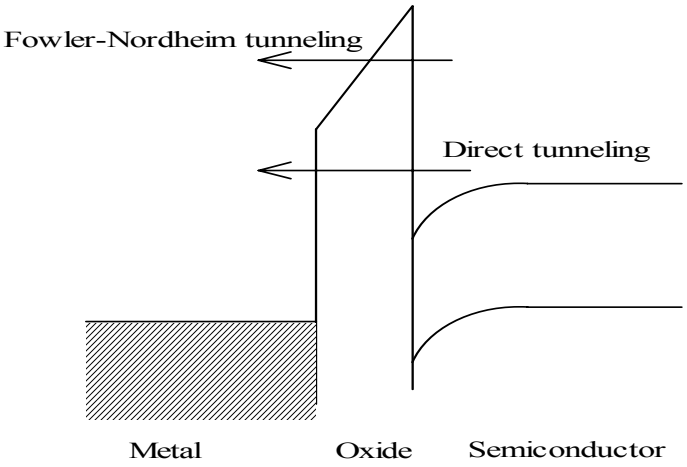

Fig. 1.6. Fowler-Nordheim and direct tunneling mechanisms.

The tunneling probability is given as:

$$T_t = \exp\left(-\frac{4\sqrt{2m_{ox}}}{3qh}\frac{(\phi_b + E_F - E + \frac{m_t E_t}{m_{ox}})^{3/2} - (\phi_b + E_F - E + \frac{m_t E_t}{m_{ox}} - qV_{ox})^{3/2}}{E_{ox}}\right) \quad (1.22)$$

They computed the current density as:

$$J_{DTt}=\frac{A\cdot\left|E^2\right|}{\left(1-\sqrt{1-qV_{ox}/\phi_b}\right)^2}\exp\left\{-\frac{B}{E_{ox}}\left[1-(1-qV_{ox}/\phi_b)^{3/2}\right]\right\}\cdot\left\{1-\exp\left[-\frac{3BE_F}{2E_{ox}\cdot\phi_b}(1-\sqrt{1-qV_{ox}/\phi_b})\right]\right\} \quad (1.23)$$

with A and B, defined as:

$$A=\frac{q^3(m_o/m_{ox})}{8\pi h\phi_b} \text{ and } B=\frac{8\pi\sqrt{2m_{ox}\phi_b^3}}{3qh} \quad (1.24)$$

For accumulation case, where

$$E_F > \frac{4\phi_b^3}{3qBt_{ox}} \quad (1.25)$$

the current density reduces to;

$$J_{DTt}=\frac{A\left|E^2\right|}{\left(1-\sqrt{1-qV_{ox}/\phi_b}\right)^2}\exp\left\{-\frac{B}{E_{ox}}\left[1-(1-qV_{ox}/\phi_b)^{3/2}\right]\right\}\cdot \quad (1.26)$$

In 2000, Lee and Hu [29], proposed a generalized direct tunneling model which is valid in both depletion and accumulation. The current density in their model is very similar to Schuegraf-Hu model except for the correction function;

$$J_{DTt}=\frac{q^3}{8\pi h\varepsilon_{ox}\phi_b}C(V_G,V_{ox},t_{ox},\phi_b)\cdot\exp\left\{-\frac{B}{E_{ox}}\left[1-(1-qV_{ox}/\phi_b)^{3/2}\right]\right\} \quad (1.27)$$

where $C(V_G, V_{ox}, t_{ox}, \phi_b)$ is the correction function;

$$C(V_G,V_{ox},t_{ox},\phi_b)=\exp\left[-\frac{20}{\phi_b}\left(\frac{|V_{ox}|-\phi_b}{\phi_{off}}+1\right)^{\alpha}\cdot\left(1-\frac{|V_{ox}|}{\phi_b}\right)\right]\cdot\frac{V_G}{t_{ox}}\cdot N \quad (1.28)$$

$$N=\frac{\varepsilon_{ox}}{t_{ox}}\cdot\left\{S\cdot\ln\left[1+\exp\left(\frac{V_{eff}-V_T}{n_{inv}V_T}\right)\right]+V_T\cdot\ln\left[1+\exp\left(-\frac{V_G-V_{FB}}{V_T}\right)\right]\right\} \quad (1.29)$$

where α is a fitting parameter, t_{ox} is the tickness of the oxide, S is subtreshold swing, V_T is the thermal velocity.

The main difference between this model and Schuegraf`s model is the correction factor. The exponential term accounts for secondary effects such as energy dependence of the densities of states at the electrode interface and effective masses in the dielectric, and that affects the curvature of the tunneling characteristic. N is an indicator of the density of either the tunneling carriers for electron conduction band tunneling (ECB) and hole valence band tunneling (HVB) or the receiving energy states for EVB. The rate of increase of the subtreshold carrier density with V_G is dictated by $n=S/V_T$ (S is the subtreshold swing in inversion or accumulation). These effects were neglected in Schuegraf`s approach altough that approach gives good results in accumulation and depletion modes.

There are also many other direct tunneling models proposed by different groups as brand new models or modification of Schuegraf-Hu model [29-48].

1.4.3 Band-to-Band Tunneling

This model describes the current due to carriers tunneling between the band of the semiconductor to the band of the gate and vice versa. It describes the same physicsal process with Fowler-Nordheim and Direct tunneling do. The difference between this model and Fowler-Nordheim or Direct Tunneling model is the temperarture dependency. The difference comes from the handling of the systems. This model follows the same steps while deriving the final current density function but it uses the thermal velocity. This approach causes a second order temperature factor in the final form of current density. The derivation can be summarized as follows and the details can be found in Card-Rhoderick [49, 50]or Kumar-Dahlke [51]:

Starting from the Eq.1.19 and substituting the tunneling probability into that equation and evaluation of the integration over the energy range yields;

$$J_{BTB} = A^* T^2 \cdot \exp(-\beta\phi_b) \cdot \exp(-q\phi_s / kT) \cdot \left[\exp(qV_G / kT) - 1\right] \qquad (1.30)$$

where A* is the Richardson constant, $\exp(-\beta\phi_b)$ the tunneling probability, φ_s the schottky barrier between the gate and the semiconductor. There is a significant similarity between this model and Schottky theory since the kinetic energy of the carriers is used in transport equations. In other words band-to-band tunneling can be approximated as Schottky model

with a transmission probability through the oxide and this mechanism can be important for especially MOS diodes with very thin (~ 5-10 Angstrom) oxide.

1.4.4 Trap Assisted Tunneling

There are many models related with traps such as pure trap assisted tunnelings or Poole-Frenkel emission or hopping conduction etc. In this subsection, hovewer, we only present the pure trap assisted tunneling models in the oxide. The other mechanisms mentioned above will be given in subsequent sections.

The existance of electron trap levels in the dielectric layer of a metal-oxide-semicondcutor device can result in a considerable leakage current at electric fields well blow those needed for Fowler-Nordheim or direct tunneling, in which electrons gain sufficient energy to tunnel directly from the gate electrode to the inulator or semiconductor conduction band and vice versa. Trap assisted conduction is a two-step process in which electrons first tunnel directly into a trap, and then are able to tunnel into the conduction band of the insulator or semicondcutor, incorporating energy loss by phonon relaxation.

The electrical conduction mechanisms of thin trapped oxides and nitrides have attracted much attention over many years [52-67]. The basic trap assisted current density is given as;

$$J_{TAT} = q\int_{o}^{t_{ox}} \frac{C_t N_t P_1 P_2}{P_1 + P_2} \quad \text{or} \quad J_{TAT} = \int_{0}^{t_{ox}} \frac{qN_t}{\tau_c + \tau_e} dx \quad \text{or} \quad J_{TAT} = \int_{0}^{t_{ox}} \sigma N_t \frac{J_{in} J_{out}}{J_{in} + J_{out}} dx \qquad (1.31)$$

or in similar forms. However the models employed in the form above work rely on the calculation and numeraical evaluation of integrals and hence are not readily applied to experimental data. There are also other TAT tunneling models that are ready to be applied to experimental data. We give a small description of those models in subsequent subsections.

Fleischer`s TAT Model;

In 1992 Fleischer, Lai, and Cheng [55] proposed a trap assisted tuneling model in MOS devices. Their model is based on two-step tunneling. The current density is given as in Eq.1.31. This equation reduces to

$$J_{TAT} = \frac{\frac{2qC_t N_t \phi_t}{3E} \cdot \exp(-\frac{A\phi^{3/2}}{E})}{3E} \tag{1.32}$$

This equation makes it possible to extract the trap energy from the slope of the plot of ln (JE) vs. 1/E without heavy calculations;

$$\phi_t = (-\frac{slope}{A})^{2/3} \tag{1.33}$$

The advantage of these appraoches is the easiness of data evaluation and reduced number of fit parameters. One doesn`t need to make simulations or heavy computational calculations. Instead, by plotting ln (JE) vs 1/E, it i easy to determine the trap energy from the slope. By deriving trap energy as a first step, the fitting procedure can be expected to be easier and more accurate. It is necessary to either use both φ_t and N_t as fitting parameters or to determine one of them by an independent method (such as C-V, avalanche injection, high-field injection or Poole-Frenkel evaluation etc.) when the numerical solution or simulation tools are used. Now both of these trap parameters can be extracted directly from the I-V measurements with respect to this theory.

Chang`s TAT Model;

This model [65] employs a general trapezoidal barrier rather than a triangular barrier which is oftenly used in conventional trap assisted models. The derivation of an explicit analytical current density is the same as in Fleischer`s model except the barrier function. The model predicts the current density as:

$$J_{TAT} \propto \exp(-\frac{4\sqrt{2qm_{ox}}\phi^{3/2}}{3\hbar E}) \tag{1.34}$$

By plotting ln(J) vs 1/E, it is easy to determine the trap energy from the slope.

1.4.5. Poole-Frenkel Tunneling

This mechanism is due to field-enhanced thermal excitation of trapped electrons into the conduction band of SiO_2. The structural defects cause additional energy states close to the band-edge called traps. These traps restrict the current flow because of a capture and emission process. The current is a simple drift current described by

$$J_{PF} = nq\mu E \tag{1.35}$$

where n is the carrier density and μ mobility [67]. While the carrier density depends exponentially on the depth of the trap which is corrected for the electric field

$$n = n_0 \exp\left[-\frac{q}{kT}\left(\phi_t - \sqrt{\frac{qE}{\pi\varepsilon_i}}\right)\right] \tag{1.36}$$

then current density becomes;

$$J_{PF} = qn_0\mu E \cdot \exp\left[-\frac{q}{kT}\left(\phi_t - \sqrt{\frac{qE}{\pi\varepsilon_i}}\right)\right] \tag{1.37}$$

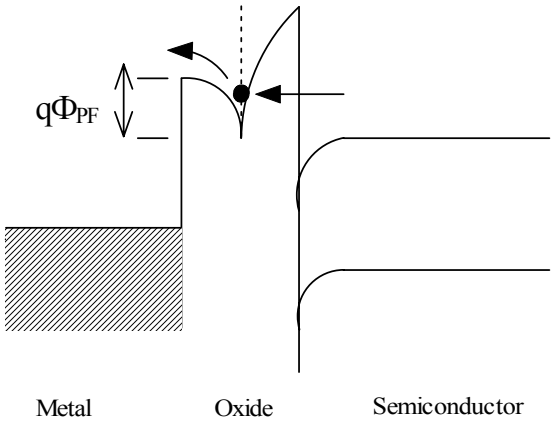

Fig. 1.7 Poole-Frenkel emission

1.4.6. Space-charge limited current

The space-charge limited current results from carrier injection into the insulator, where no compensating charge is present. For structures where carriers can readily enter the insulator and freely flow through the insulator one finds that the resulting current and carrier densities are much higher. The density of free carriers causes a field gradient, which limits the current density. This situation occurs in lowly doped semiconductors and vacuum tubes.

The well-known expression for space charge limited current, Eq. 1.38, is found by starting from an expression for the drift current and Gauss's law (it is assumed that the insulator contains no free carriers if no current flows). See for example [3] for details.

$$J = \frac{9\varepsilon \cdot \mu \cdot V^2}{8d^3} \tag{1.38}$$

where d is the thickness, ε is the permittivity and μ is the mobility of the insulator.

1.4.7. Hopping Conduction (Ohmic Conduction)

At very low voltages and high temperatures, current is expected to be carried by thermally excited electrons hopping from one isolated state to the next. This mechanism yield an ohmic characteristic exponentially dependent on temperature. The current density is given as [1]:

$$J \propto E \cdot \exp(-\Delta E_a / kT) \tag{1.39}$$

where ΔE_a is the activation energy.

1.4.8. Schottky-like Emission (Modified Poole-Frenkel Current)

This mechanism is similar to the thermionic emission in metal-semiconductor junctions. Thermal electrons which are emitted across the gate-oxide or semicondcutor-oxide interface are responsible for the carrier transport.

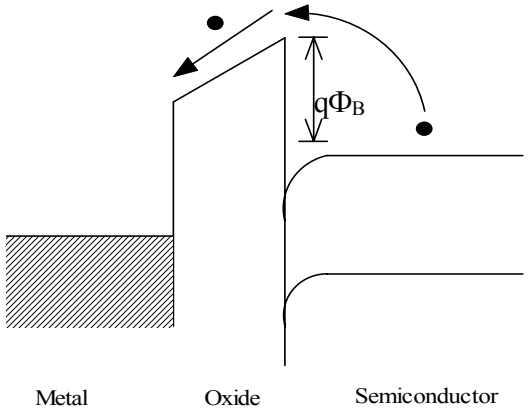

Fig. 1.8 Schottky emission

The thermionic emission theory by Bethe [68] is derived from the assumption that (i) the barrier height is much larger than kT and (ii) thermal equilibrium is established at the plane that determines emission, and (iii) the existance of net carrier flow does not affect this equilibrium. Because of these assumptions the shape of the barrier profile is immaterial and the current flow depends solely on the barrier height. The current density between the gate and the semiconductor is then given by the concentration of electrons with energies sufficient to overcome the potential barrier and traversing in the transport direction:

$$J = \int_{E_{F+q\phi_B}}^{\infty} qv_x dn \tag{1.40}$$

where $E_F + q\Phi_B$ is the minimum energy required for thermionic emisson into the oxide, and v_x is the carrier velocity in the direction of transport. The electron density in an incremental energy range is given by :

$$dn = N(E)F(E)dE = \frac{4\pi\left(2m^*\right)^{3/2}}{h^3}\sqrt{E-E_c}\,\exp\left[-\left(E-E_c+qV_n\right)/kT\right]dE \tag{1.41}$$

where N(E) and F(E) are the density of states and the distribution function respectively and qV_n is $(E_c\text{-}E_F)$. If we postulate that all the energy of electrons is kinetic energy, then

$$E - E_c = \frac{1}{2}m^* v^2 \tag{1.42}$$

If the speed is resolved into its component along the axes with th x axis parallel to the transport direction, we have

$$v^2 = v_x^2 + v_y^2 + v_z^2 \tag{1.43}$$

With the required transformations, we obtain the thermionic current as;

$$J = A^* T^2 \exp\left(-qV_n/kT\right)\exp\left(-\frac{m^* v_{ox}^2}{2kT}\right) \tag{1.44}$$

where v_{ox} is the minimum velocity required in the x direction to surmount the barrier and is given by

$$\frac{1}{2}m^* v_{ox}^2 = q(V_{bi} - V) \tag{1.45}$$

where V_{bi} is the built-in potential at zero bias. Substituting Eq.1.45 into Eq.1.44 yields

$$J = A^* T^2 \exp\left(-q\phi_B / kT\right)\exp\left(\frac{qV}{kT}\right) \tag{1.46}$$

Since the barrier height for electrons moving into the oxide remains the same, the current flowing into the oxide is thus unaffected by the applied voltage. It must therefore be equal to the current flowing from the semiconductor into the metal when thermal equilibrium prevails (i.e. when V=0). The corresponding current density is obtained from Eq.1.46 by setting V=0 as;

$$J = A^* T^2 \exp\left(-q\phi_B / kT\right) \tag{1.47}$$

However, when the electron enters the oxide, charge is redistributed on the electrode to maintain the equipotential surfaces. The result is to produce a so-called image field that adds to the applied field and helps to round and lower the potential barrier. The image lowering is given as [1] :

$$\sqrt{\frac{qE}{4\pi\varepsilon}} \tag{1.48}$$

and the thermionic current for MOS devices becomes

$$J = A^* T^2 \exp\left[q\left(\phi_b - \sqrt{\frac{qE}{4\pi\varepsilon}}\right) / kT\right] \tag{1.49}$$

A plot of $\ln(J/T^2)$ vs. 1/T yields a straight line with a slope determined by the permittivity of the oxide.

1.4.9. Surface-State Tunneling

Following the approach of Freeman and Dahlke [69, 70], the electron current, J_{ns}, from the conduction band of the semiconductor to the surface states is given by:

$$J_{ns} = qD_{it}v_{th}\sigma_n[(1-f_t)n_s - f_t n_1) \tag{1.50}$$

where ν_{th} is the thermal velocity, D_{it} density of surface states, σ capturre cross-section area for electrons, f_t surface state occupation probability with tunneling current through the surface states, n_s (p_s) electron (hole) concentration at the semiconductor surface, n_1 (p_1) electron (hole) concentration if the electron (hole) Fermi level is at the trap energy level. The hole current, J_{ps}, from the valence band to the surface states can be written as:

$$J_{ps} = qD_{it}v_{th}\sigma_p[f_t p_s - (1-f_t)p_1] \tag{1.51}$$

and the total current through the surface states, J_{ss} ,is

$$J_{ss} = J_{ns} - J_{ps} = \frac{qD_{it}}{\tau_t}(f_t - f_m) \tag{1.52}$$

where f_m is the occupation probability of an energy level in the metal. By substituting the Eqn.1.50 and Eq.1.51 into Eq.1.52 one obtains the surface state tunneling density. See [45] for details. Surface states provide additional path for carriers and they act as recombination centers at the surface.

1.4.10. Diffusion Current

Diffusion current can be calculated by following Hovel`s approach [71] by solving the continuity equation and applying the appropriate boundary conditions. Diffusion current can behave a limiting current when all the carriers supplied to the substrate are able to pass to the gate. This mechanism can especially be important in thin oxides where the transmission probability through the oxide is very high and the current in the device will be governed by the substrate. Mathematical details can be found in many papers [70].

1.4.11. Recombination-Generation Current

The generation-recombination mechanism plays an important role in MOS devices due to oxide-semiconductor interface. The surface states can behave as a recombination centers. If the surface state density is high then recombination-generation current might be significant and descriptive for a MOS device. The recombination-generation current is given as:

$$J_{rg} = \frac{qn_i w}{\tau_n}(e^{\beta\phi_s/2} - 1) \tag{1.53}$$

The derivation of this formula can be found in many books [1].

CHAPTER 2

EXPERIMENTAL PROCEDURES

We will briefly describe the basic fabrication steps of MOS capacitors. This chapter does not aim to explain all the process methods and details of a MOS capacitor but only main steps of fabrication of our samples. We will also give a short description of our measurement setup for current-voltage measurements.

One of the samples (Aliminum gate MOS) was prepared at our laboratory, and the other sample (PolySi gate MOS) was prepared at Physical Electronics & Photonics Laboratory at Chalmers, Sweden.

2.1 Al-SiO_2-Si MOS

The first sample we worked on was a relatively thick oxide MOS capacitor (1250 Angstroms) with Al/SiO_2/n-Si structure. To produce this sample we basically followed the steps shown in the figure 2.1 below:

Our wafer was n-type Si (100) with a doping of $1x10^{16}$. We applied a cleaning procedure to this wafer to reduce the contamination on the wafer (Fig.2.1.a). Then we used thermal oxidation (dry) method under N_2 atmosphere to coat the Si with SiO_2 (Fig.2.1.b). The oxidation was performed in a furnace at 1050 ^{0}C for 80 minutes. In this phase of the process, top and bottom surface of the Si-wafer was coated with SiO_2. Then, the bottom oxide was etched with Hydrofluoric acid (HF, 10%) to be able to deposit metal (Al) onto Si for back contact (Fig.2.1.c). After etching, we formed the gate of our MOS-C by Aluminum deposition with the help of a shadow mask in a deposition chamber. Finally, we deposited Aluminum onto the back side of the Si-wafer to have the back contact (Fig.2.1.d).

We will present the Si-wafer cleaning procedure in detail and abrief summary of oxidation in In subsection 2.1.1. and 2.1.2.

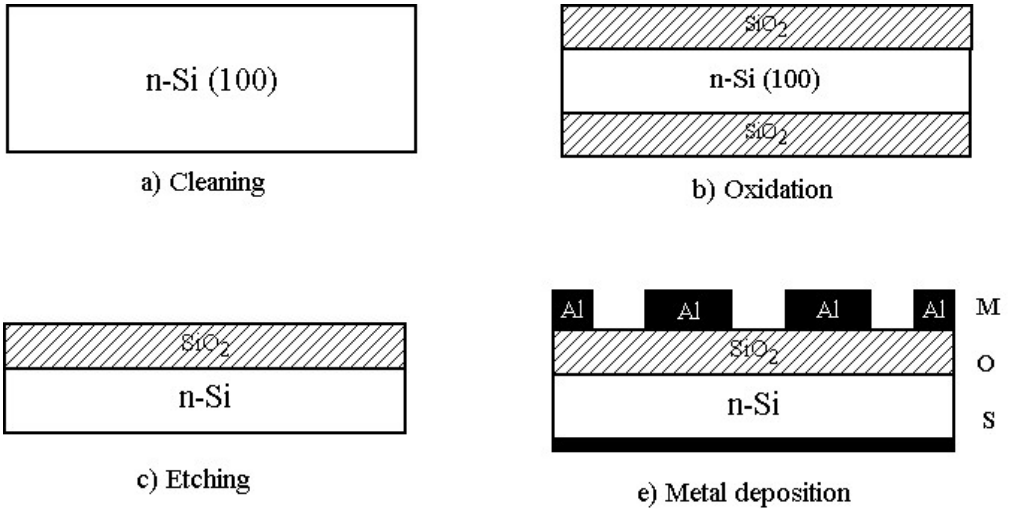

Figure.2.1. Fabrication of a MOS capacitor: a) Wafer cleaning; b) dry oxidation, c) etching; d) Metal formation.

2.1.1 Wafer Cleaning

Wafer cleaning has a central role in semiconductor device production. Due to the fact that existing organic (dust, oil etc.) and inorganic (native oxide, metallic ions etc.) contaminations on the wafer can effect the characteristics of the devices, wafers must be cleaned before any processing.

The first sample we used in this study was cleaned before oxidation with the following chemical processes:

1. Boiling in trichloroethylene: Removes organic contaminants,
2. Ultrasonically agitation first in deionized water and later in acetone,
3. Boiling in the mixture of HCl : H_2O_2 : H_2O : Removes metallic impurities and prevents their displacement plating back onto the silicon,
4. Washing in deionized water for a few minutes: Cleans up the traces of the chemicals from the preceding treatment,

5. Boiling in the mixture of H_2SO_4 : H_2O_2 : H_2O : Removes both organic and metallic films,
6. Washing in deionized water : Removes the remnants coming from the previous step,
7. Dipping a solution of HF: H_2O: Strips the thin native oxide layer on the sample (silicon atoms bond with the hydrogen atoms after the removing of oxide on the surface and this prevents the wafer from new oxidation for a while).
8. Washing in deionized water,
9. Drying by using N_2.

2.1.2 Oxidation

An oxide layer is rapidly formed when silicon wafer is exposed to an oxidizing ambient since silicon surface has a high affinity for oxygen. Two techniques are commonly used for oxidation: Thermal oxidation and chemical vapor deposition (CVD).

The deposition of SiO_2 using a CVD process is one where two gases, silane and oxygen, react to form silicon dioxide, which then sublimes onto any solid surface. The wafers are heated to 200 - 400°C yielding high quality oxides.

The thermal oxidation of silicon is obtained by heating the wafer in an oxygen or water vapor ambient. Typical temperatures range from 800 to 1200°C. The oxidation of a silicon surface also occurs at room temperature but the resulting 3 nm layer of oxide limits any further oxidation. At high temperatures, oxygen or water molecules can diffuse through the oxide so that further oxidation takes place. The oxidation in oxygen ambient is called a dry oxidation. The one in water vapor is a wet oxidation. The thermal oxidation provides a high quality interface and oxide. It is used less these days because of the high process temperatures [3].

Finally Aluminum deposition process was performed for front and back contacts. Fig. 2.3 below shows our metallization setup.

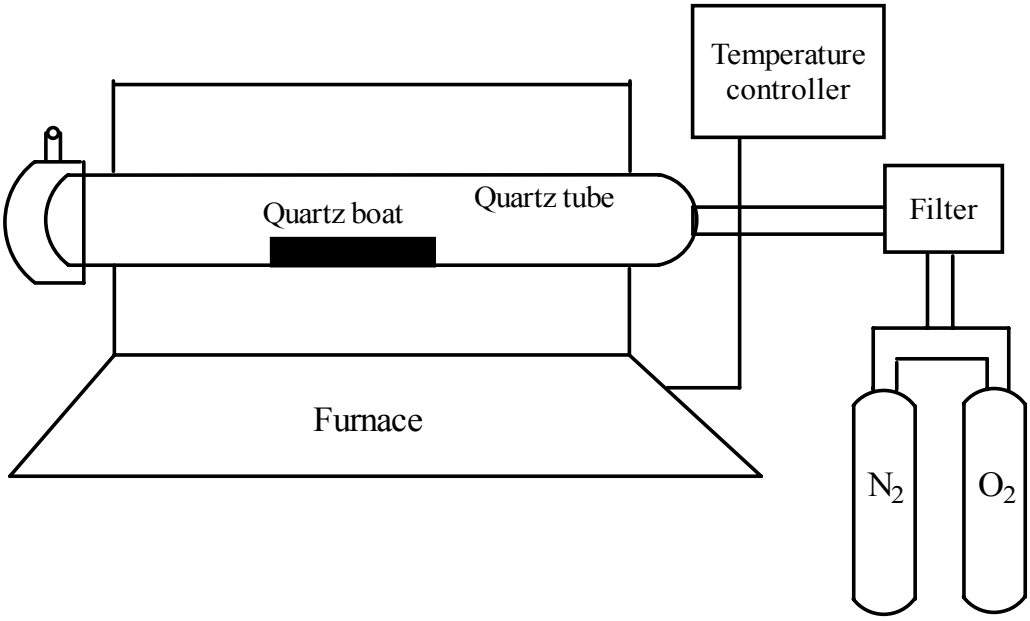

Fig. 2.2 Furnace system for oxidation

2.2. PolySi-SiO_2-Si MOS

This sample was prepared at Physical Electronics and Photonics Laboratory of Chalmers University of Technology, Gothenburg, Sweden. The structure is p-polysilicon/SiO_2/n-Si. The details are as follows:

The capacitor (PMOS) was fabricated on (100) n-type Silicon wafers from Wacker Silctronic. Ultrathin nitrided gate dielectric structure was grown at 750-800 ^{0}C by using an ASM A400 vertical furnace. The gate electrode p+-poly-Si (p-type, Boron doped greater than $1x10^{20}$ cm^{-3} and its thickness is 200 nm) was deposited in a low pressure chemical vapor deposition (LPCVD) ASM chamber using SiH_4 at a pressure of $5.3x10^3$ pa and temperature of 615 ^{0}C. In order to facilitate nucleation of poly-Si on the SiO_2 an undoped Si seed layer with a nominal thickness of 1 nm was deposited at 615 ^{0}C prior to poly-Si layer deposition [3].

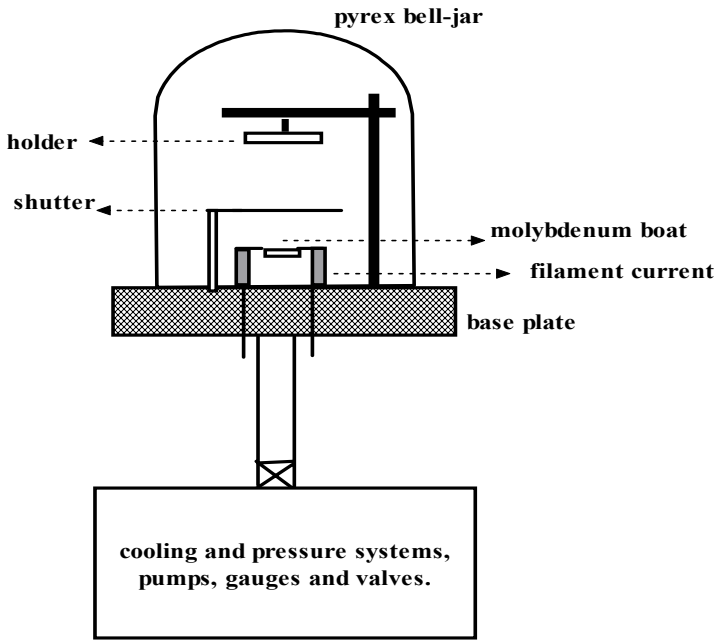

Fig. 2.3 Metal deposition system

2.3. Electrical Characterization Setup

In this thesis two different electrical measurements were performed; current-voltage (I-V) and capacitance-voltage (C-V). The aim of this thesis is to investigate the electrical transport in MOS structures based on I-V methods. Therefore C-V investigation is out of the scope of this thesis and will not be discussed in detail in this thesis, but we will give the basic C-V curves of our samples for the sake of completeness of electrical characterization. Only I-V measurements were performed as temperature dependent due to the same reason and C-V measurements were performed at 300 ^{0}K.

We used Hewlett- Packard (HP) 4140B pA meter / DC voltage source for I-V measurement and HP 4192 LF impedance analyzer for C-V measurements. Basic schematics of these setups are as follows:

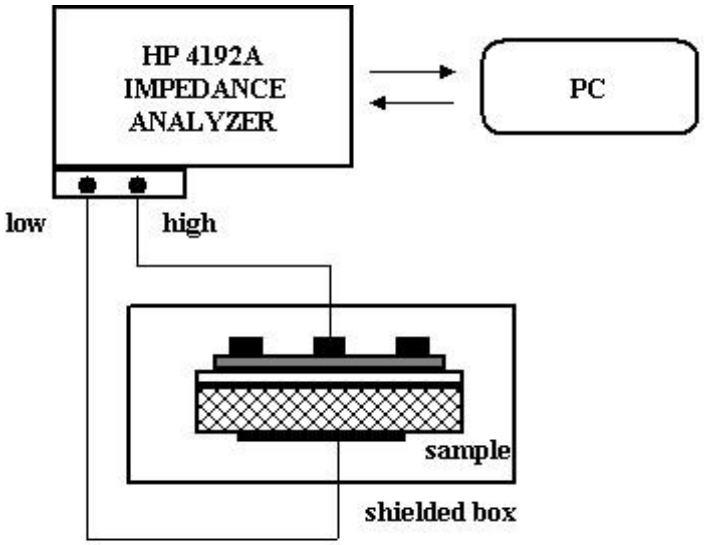

Fig.2.4 C-V measurement system.

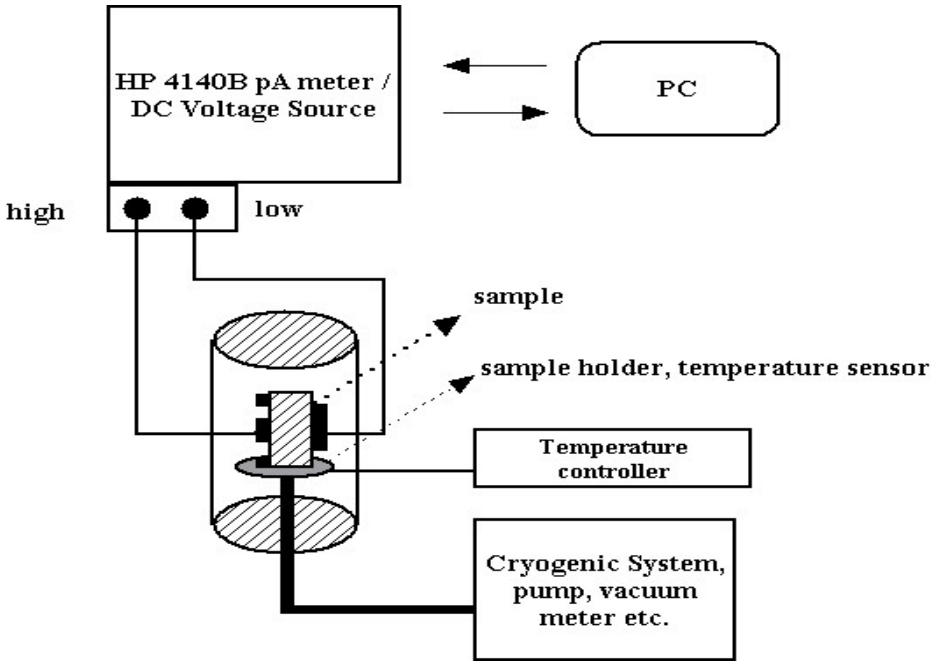

Figure 2.5 Temperature dependent I-V measurement system.

CHAPTER 3

ELECTRICAL TRANSPORT IN THICK SIO_2 FILM

3.1. Al-SiO_2-Si Capacitor

In this part of the thesis, we present our work on MOS capacitor fabricated on a thick SiO_2 layer. The oxide thickness is 1250 ±10 Angstroms. The gate material is Aluminum and the substrate is n-type Silicon (100). Fabrication processes were described in the previous chapter. The band diagram of this structure is as follows:

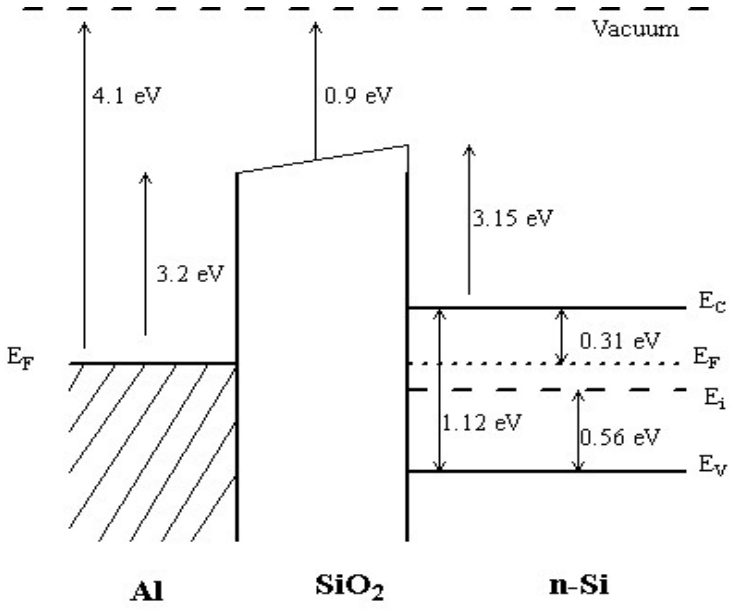

Fig. 3.1 Band structure of Al-SiO_2-Si

3.2. Electrical Characteristics:

3.2.1. C-V and G-V Curves:

The C-V curves of the sample are as follows:

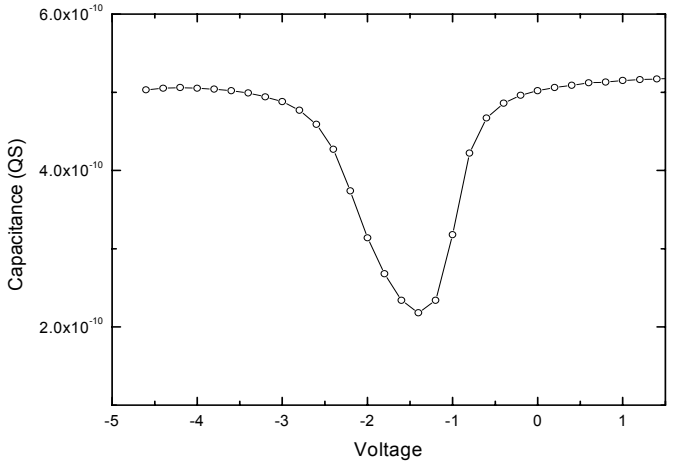

Fig. 3.2 Quasi-Static (QS) capacitance-voltage curve of sample-1

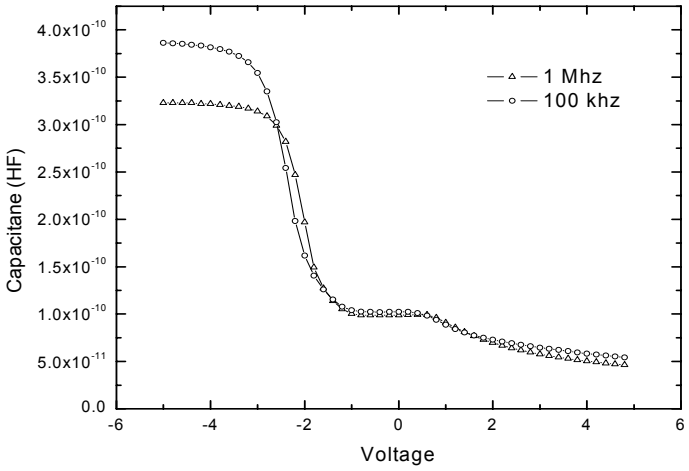

Fig.3.3 High-frequency capacitance at 1 MHz and 100 kHz.

Fig. 3.4 shows the conductance-voltage curves we measured at the same frequancies:

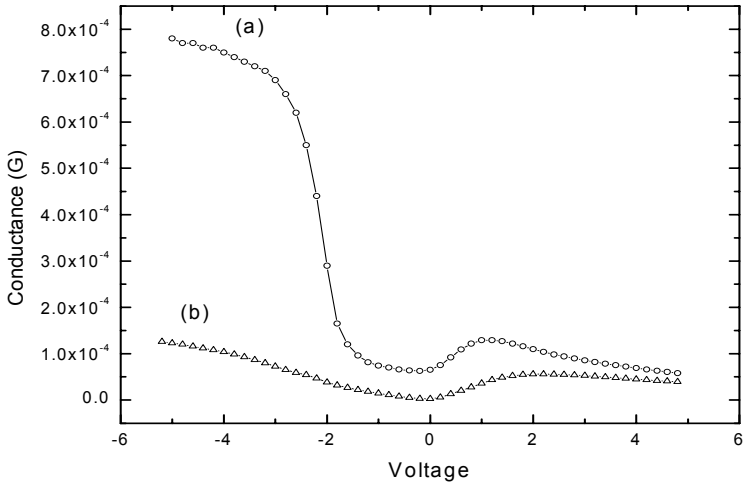

Fig.3.4 Conductance vs. voltage curves at (a) 1 MHz and (b) 100 kHz.

The quasi-static and high frequency curves indicate a certain MOS structure but they also show a leakage current in the oxide. The conductance-voltage curve shows a minimum at almost V=0. G-V curve also reveals that there is a leakage in the accumulation regime. This means that the carriers are able to pass through the oxide and the conductance increases due to these carriers. However, the saturation in the high frequency capacitance in accumulation indicates that the ratio of the leakage carriers is small compared to total carriers.

A thick oxide contains traps and these traps help carriers to leak in the oxide. Flat band voltage value (~-2.3 V) also supports these basic conclusions about our oxide.

3.2.2. I-V Curves

Current-Voltage measurements were performed in a broad temperature range from 20 K to 300 K. The I-V curves at selected temperatures are shown in figure 3.5:

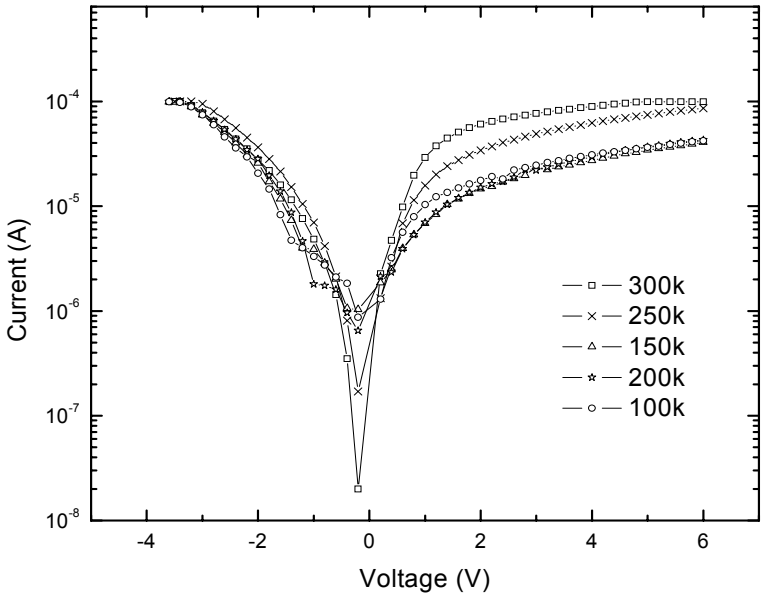

Fig. 3.5 Current-Voltage graphics at different temperatures.

In the accumulation regime, an explicit temperature dependence can easily be observed. Also a series resistance effect is seen in the figure 3.5, after about 1 volts at all temperatures. In the inversion, however, a weaker dependence on temperature is seen in the figure above. To find out which current mechanisms are responsible for this kind of behavior, we plotted the Arrhenius plots for both positive and negative voltage regimes.

3.3. Possible Current Transport Mechanisms:

We observed mainly two different characteristics in the Arrhenius plots for accumulation. As seen in Fig. 3.6, there is a strong temperature dependence at high temperatures. We observe a field activated process at medium and low temperatures. The same observation can easily be done by studying the I-V curve, shown in Fig. 3.5. One can easily realize that the current does not change significantly with the temperature (100 K and 200 K). At higher temperatures, an explicit increase in current is observed as the temperature increases (250 K and 300 K). The dependence on temperature also shows differences at different fields.

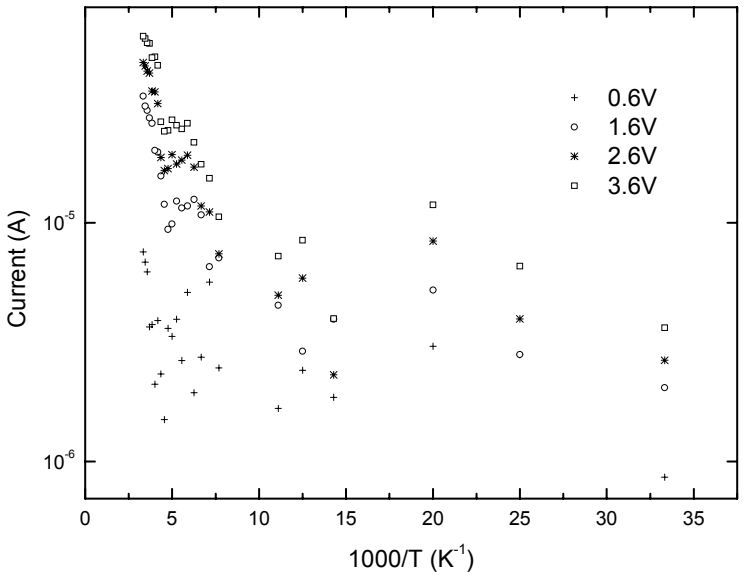

Fig. 3.6 Arrhenius plot for accumulation

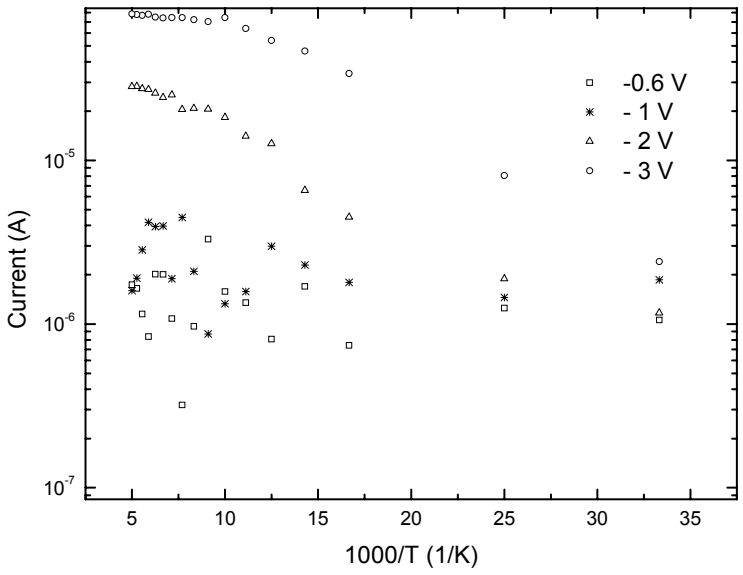

Fig. 3.7 Arrhenius plot for inversion

In the inversion regime, Arrhenius plot shows two different behaviors as a function of temperature and field, but in a different way than the Arrhenius plot for accumulation does. The temperature dependence is only seen at higher fields and at low fields we see a noisy data. At high fields, for example -3 V or -2 V, the current depends exponentially on temperature. The weak temperature dependence of the current at -1 V and temperature independence at lower fields suggest the existence of another mechanism.

As we presented in the first chapter, there are mainly four conduction mechanisms which are temperature dependent. These mechanisms are Schottky emission, band-to-band tunneling, Poole-Frenkel emission and ohmic conduction.

We plotted Poole-Frenkel curves at various temperatures and calculated the permittivity from those plots. We did this procedure for 270 K at first and then for all temperatures since we expect the Poole-Frenkel conduction to occur at higher temperatures: In the next section we will present the I-V and Poole-Frenkel plots [ln (J/E) vs. $E^{1/2}$] for accumulation and inversion at 270 K.

3.3.1. Thermally Activated Current

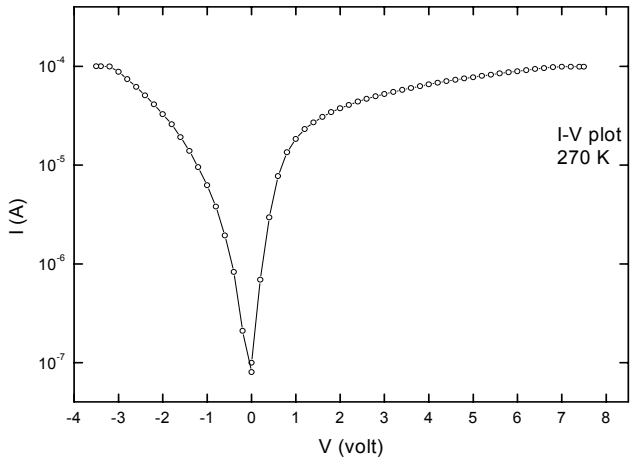

Fig. 3.8 Current-Voltage characteristics at 270 K.

In the Fig. 3.5 and Fig. 3.8, we can see that series resistance affects the current-voltage characteristics of the device at voltages higher than approximately 1.5 V in accumulation regime. For this reason, we expect Poole-Frenkel curves to give good results below this threshold.

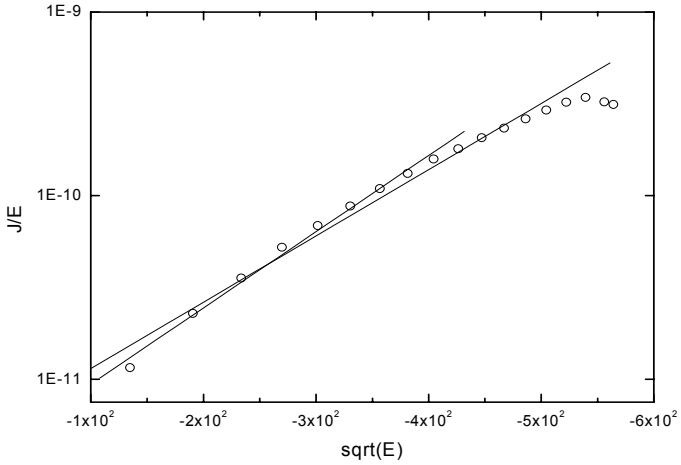

Fig. 3.9 Poole-Frenkel plot at 270 K for inversion.

In Fig. 3.9, Poole-Frenkel curve obtained from the experimental data at 270 K (circles) and two linear fits (black lines) to the curve are shown. Since the slope of Poole-Frenkel plot gives a function of temperature and permittivity, extracting the value of the permittivity from the slope is a simple algebraic procedure.

The Poole-Frenkel current density expression is given as:

$$J_{PF} = qn_0 \mu E \cdot \exp\left[-\frac{q}{kT}\left(\phi_t - \sqrt{\frac{qE}{\pi \varepsilon_i}} \right) \right] \tag{1.37}$$

And the slope of the Poole-Frenkel curve is:

$$slope = -\frac{q}{kT}\sqrt{\frac{q}{\pi \varepsilon_i}} \tag{3.1}$$

where q is the electron charge, k is Boltzmann constant, T is temperature and ε_i is the permittivity of the oxide.

One of the slopes (the upper one) in the Fig. 3.9 produced the permittivity as 0.85 ε_0 where ε_0 is the vacuum permittivity. The permittivity was found as 9.8 ε_0 for the other fit to the slope. It is clear that a better fit, which might give a permittivity value close to the commonly accepted 3.9 ε_0 value, can be found by making a fit between these two lines. The trap depth changes between 0.69 eV and 0.75 eV with respect to these permittivity values.

These two results when they are considered with the discussion above lead to the conclusion that the transport mechanism of the device is dominated by the Poole-Frenkel conduction at 270 K for inversion. Actually one does not have to extract perfect permittivity values from Poole-Frenkel plots since oxides include a lot of deficiencies such as oxide traps, mobile ions, localizations in the matrix an so on. These imperfections cause permittivity deflect from 3.9 ε_0. Therefore values found in the above analysis are good signs to assure us about the dominance of the Poole-Frenkel emission.

Therefore our conclusion for the conductivity in the device for inversion regime is Poole-Frenkel type trap assisted conduction. In order to be sure of this conclusion we plotted Poole-Frenkel curves at other temperatures. The results and the fits to the slopes of those curves are shown in figure 3.10 below:

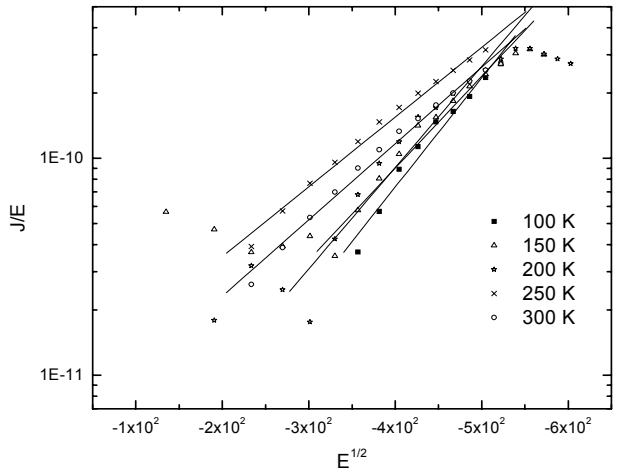

Fig. 3.10 Inversion regime Poole-Frenkel graphics at various temperatures.

The permittivity values extracted from these slopes are acceptable for high temperatures. For example at 300 K, the permittivity was found as 6.8 ε_0 and this value goes away from 3.9 ε_0 as the temperature decreases. This increase in permittivity values indicates that the second conduction mechanism, which was mentioned during the Arrhenius plot discussion above, becomes more effective at lower temperatures. The trap depths change from 0.56 eV to 0.60 eV. Trap depth decreases as the temperature increases. This is expected since as the temperature increases carriers will have more average energy and therefore they will be able to jump to higher trap states.

The Poole-Frenkel curve yielded a 6.49 ε_0 value for the accumulation regime. The Poole-Frenkel curve and the fit to the linear region of the curve are shown in Fig.3.11:

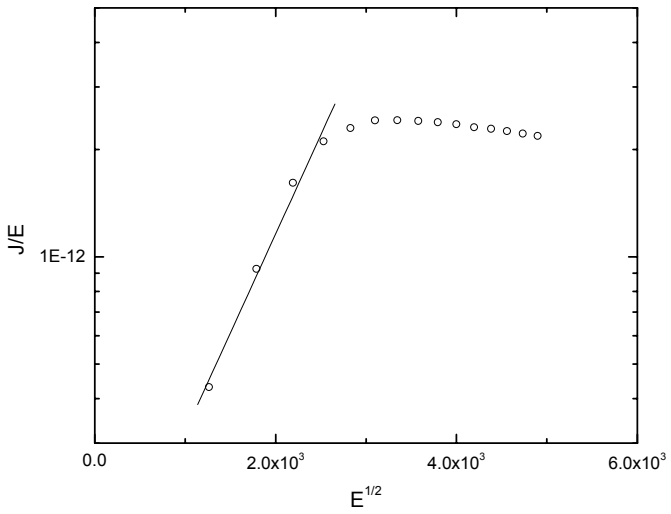

Fig. 3.11 Poole-Frenkel plot at 270 K for accumulation.

The permittivity value was found to be 6.49 ε_0 from the slope of the fit. This value is convincing enough to reach to the conclusion that Poole-Frenkel conduction governs the device at 270 K. The trap depth of 0.67 eV corresponds to 6.49 ε_0.

The Poole-Frenkel plots for other temperatures are shown in Fig. 3.12 below. From the slopes of the fits seen in the figure 3.12, we extracted different permittivity values as 5.5 ε_0

for 300 K, 13.2 ε_0 for 200 K and 262.5 ε_0 for 100 K. It is seen that the permittivity values become less and less acceptable as the temperature decreases. This behavior again indicates the two-component conduction we described before. As the temperature decreases Poole-Frenkel conduction loses its dominance and the other mechanism starts to show up more. The trap depth for 250 K was found as 0.51 eV. The trap depth decreases as the temperature increases again. Unlike the inversion regime in which traps show minor differences in depth (0.56 eV to 0.60 eV), the trap depth changes more significantly in accumulation. It is 0.51 eV for 250 K and 0.67 eV for 270 K. This drastic change in accumulation is understandable since a change in the conduction mechanism occurs at these temperatures. Current becomes dominated by Poole-Frenkel emission rather than the field activation.

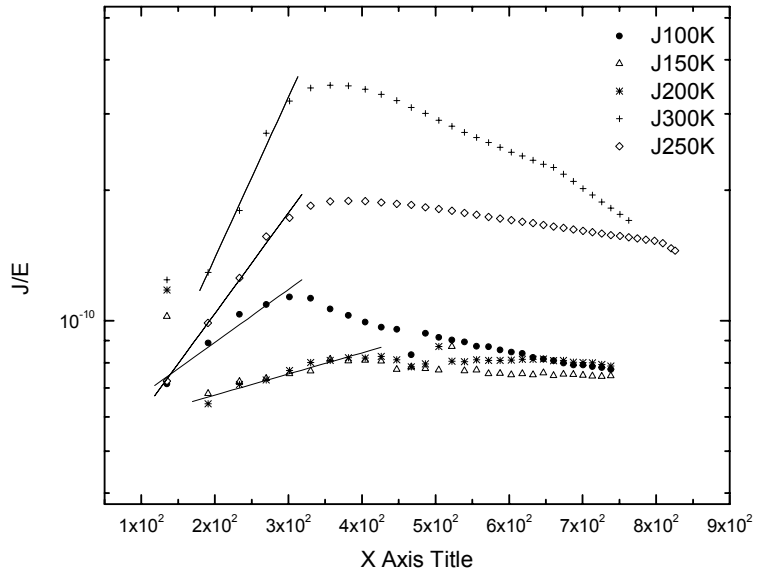

Fig. 3.12 Accumulation regime Poole-Frenkel graphics at various temperatures.

Up to now temperature dependent component of the total current has been discussed in detail and the field activated component was mentioned several times. We will discuss the

field activated constituent of the total device current in the next section.

3.3.2. Field Activated Current:

There are different current models related to field activation. For example Fowler-Nordheim emission, direct tunneling, trap assisted tunneling, space-charge limited current, diffusion current, recombination generation current and surface state tunneling. However most of these models are not applicable to our device since it contains a relatively thick oxide about 1250 Angstroms. This oxide is very thick for substrate currents to limit the total current in the device. Such a thing only happens when all the carriers injected to substrate pass to the gate. And the device must be ready for new more carriers. It is obvious that our oxide is too thick by far for such a thing. Surface state tunneling and recombination-generation models do not work due to the same reason. It is also commonly accepted that direct tunneling occurs in 4-5 nm oxides and Fowler-Nordheim tunneling is not expected to be seen before 9-10 MV/cm fields. The field we applied is much less than this value. The most appropriate model seems to be trap assisted tunneling in this case.
There are mainly two approaches to trap assisted tunneling: Numerical models and analytical solutions. The trap assisted tunneling is given as:

$$J_{TAT} = q\int_{o}^{t_{ox}} \frac{C_t N_t P_1 P_2}{P_1 + P_2} \tag{1.31}$$

or

$$J_{TAT} = \int_{0}^{t_{ox}} \frac{qN_t}{\tau_c + \tau_e} dx \tag{1.31}$$

where t_{ox} is the oxide thickness, C_t is a slowly varying function of electron energy, N_t is the trap density, P_1 and P_2 are the electron tunneling probabilities and τ_c and τ_e are the caption and emission times of the traps.

One needs several physical quantities such as life times, trap depths or trap distributions to evaluate these integrals. However, these parameters can be found by other characterization methods than current-voltage analysis. This is however outside the scope of this thesis.

The analytical approaches have been developed to investigate the pure trap assisted conduction by using the I-V data by different researchers. There are mainly two methods by Fleisher-Lai and Chang et. al. [55, 65].

These two methods are very similar to each other although Chang's method is more generalized. Fleischer-Lai (4.5) and Chang (4.6) models are formulated as:

$$J_{TAT} = \frac{\frac{2qC_t N_t \phi_t}{3E} \cdot \exp(-\frac{A\phi^{3/2}}{E})}{3E} \tag{1.32}$$

$$J_{TAT} \propto \exp(-\frac{4\sqrt{2qm_{ox}}\phi^{3/2}}{3\hbar E}) \tag{1.34}$$

where Φ_t is the trap depth.

One has to plot ln (J•E) vs. 1/E in Fleischer-Lai model and ln J vs. 1/E in Chang`s model. Both plots give a slope of $(-A\Phi_t^{3/2})$ where $A=4(2qm^*)^{1/2}/3\hbar$.

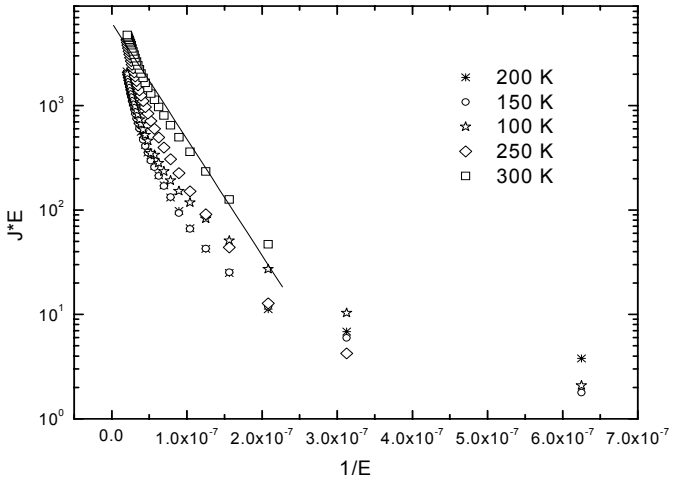

Fig. 3.13 Fleischer-Lai trap assisted tunneling model plots for accumulation at various temperatures.

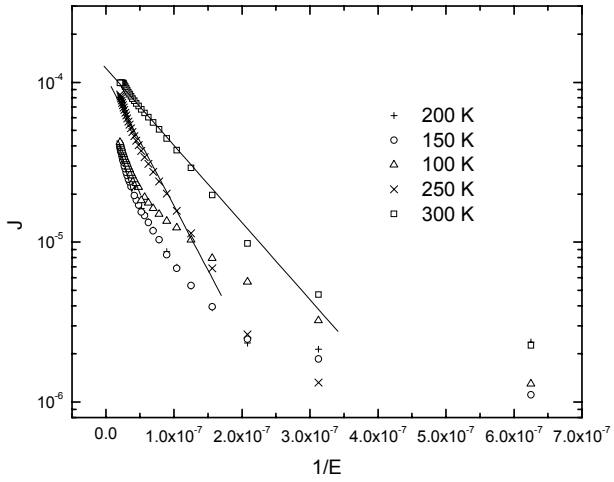

Fig. 3.14 Chang trap assisted tunneling model plots for accumulation at various temperatures.

In Fig. 3.13, Fig. 3.14, Fig. 3.15 and 3.16, the current vs. electric field characteristics are plotted according to both models. The results by these models are very alike and comparable. Both models indicate that trap assisted tunneling exists in the device for both accumulation and inversion regimes.

The trap depths we extracted from the slopes of fit lines (black lines in the Fig. 3.13 and Fig. 3.14) show variations with respect to temperature.

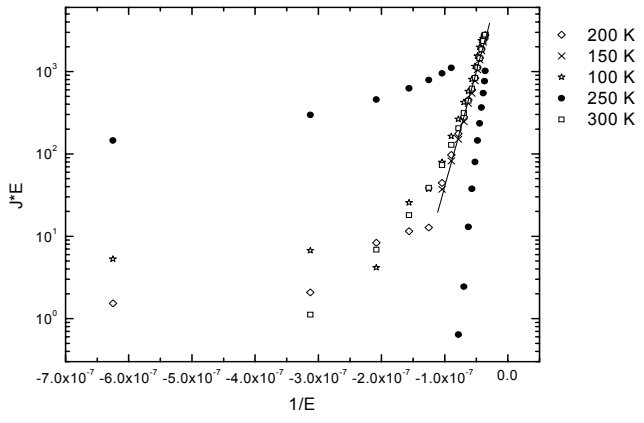

Fig. 3.15 Fleischer-Lai trap assisted tunneling model plots for inversion at various temperatures.

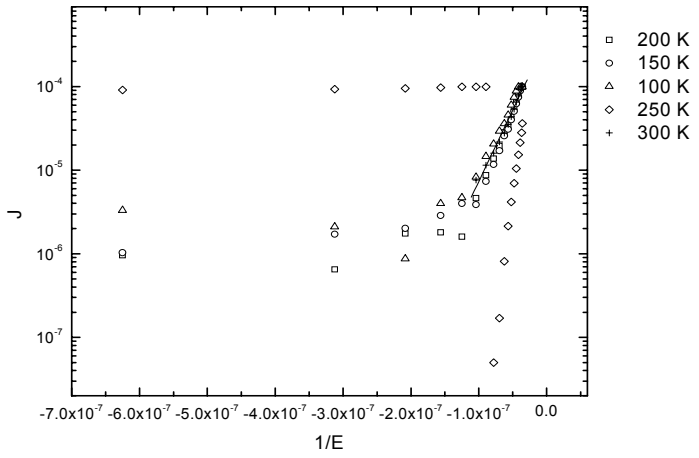

Fig. 3.16 Chang trap assisted tunneling model plots for inversion at various temperatures.

These plots indicate that trap assisted tunneling occurs in the device at all temperatures. This actually is expected for a thick oxide since it contains different type of defects. As it was explained in sec.3.2.2, the oxide is too thick to let most of the transport mechanisms occur at low and medium fields. Trap assisted tunneling however can occur at these fields.

The trap depths were extracted as 0.23 eV (Chang's model) and 0.32 eV (Fleisher's model) for inversion, 0.1 – 0.21 eV (Chang) and 0.17 – 0.26 eV (Fleischer) for accumulation.

3.4. Conclusion:

A more detailed analysis of the TAT plots presented above indicates that in the inversion regime, trap assisted tunneling current density doesn't change so much and the trap depths are almost the same at different temperatures. We found trap depths as 0.23 eV for 300 K and 0.26 eV for 50 K with respect to Chang's model and 0.32 eV for almost all temperatures with respect to Fleischer-Lai model. When

we combine these results and the conclusion which we reached for thermally activated current, we realize that the trap assisted current and Poole-Frenkel current are competing with each other to dominate the total device current for inversion regime at all the temperatures and the total current is the sum of these two components. The total current increases with the temperature due to the increase in Poole-Frenkel current with temperature. This increase is more significant at higher voltages since Poole-Frenkel emission is not a function of only temperature but also field. Therefore our conclusion for inversion regime current is that the current is divided into two components as base and active components. Base component is the pure trap assisted current occuring due to the traps in the oxide. These traps behave as centers for conduction in the oxide. Carriers jump into the trap by field activation and they leave the trap for the substrate when they are excited. The excitation might be due to field activation or collision with a free carrier in the SiO_2 or etc. The other component which we call active one is the Poole-Frenkel emission and we conclude that Poole-Frenkel emission is the main constituent of the total current since the Poole-Frenkel curves give acceptable permittivity values at all the temperatures. The trap assisted tunneling mechanism participates in the total current with Poole-Frenkel emission but it never becomes the dominant contributor.

The situation in the accumulation regime is similar to the situation in the inversion case with minor differences. In accumulation, the current is constituted by two different mechanisms again but this time both of these mechanisms become dominant at different temperatures. At higher temperatures the Poole-Frenkel emission becomes the first mechanism with a contribution of trap assisted tunneling to total current. Poole-Frenkel emission fades out at lower temperatures and trap assisted tunneling becomes more effective in determination of device characteristics.

Another interesting and confusing point to be noted is the trap depth values. We expect Poole-Frenkel emission to occur at higher trap states than the traps which assists TAT mechanisms since electrons gain more energy at high temperatures. More energetic carriers should be able to higher trap states more easily with respect to the carriers with lower energies. However, this is not the case with respect to the

parameters extracted from our plots. The traps which are active in Poole-Frenkel emission are deeper than the traps active in trap assisted tunneling for both accumulation and inversion. We believe that this might be resulted from the existence of more and complex conduction mechanisms in the oxide such as hopping conduction or vertical excitation between two oxide gap states in addition to pure trap assisted tunneling. Another possibility could be that carriers might use more traps rather than conventional two-step trapping. The models we used have been constructed by using the two-step process. Carrier first jump to the trap in the oxide from the gate (substrate) as the first step and then it reaches to the substrate (gate) by excitation somehow as the second step. In this case however, the trapping might include more steps than two due to thickness and impurity of our oxide. The other possible explanation of this inconsistency is the lateral inhomogeneity of the oxide due to for example fabrication conditions or metal penetration into oxide. At some region oxide might be thinner or surface states might be less and this could affect the conduction somehow.

CHAPTER 4

ELECTRICAL TRANSPORT IN AN ULTRA-THIN SIO_2 FILM

4.1. Introduction

The second sample is an ultra-thin oxide MOS capacitor. Such oxides are used in the production of high density memory elements recently. Understanding the electrical transport in these ultra thin oxides is crucially important for reliable operation of these memory devices. The oxide thickness is 30 (±2) Angstroms. The gate material is p type polysilicon and the substrate is n-type Silicon (100). The poly-Si is (in-situ) doped with Boron greater than $1x10^{20}$. Band diagram of this structure is as follows:

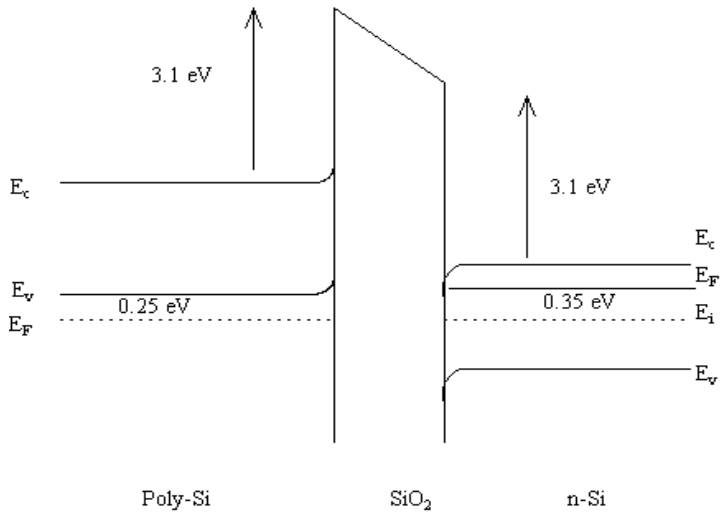

Fig. 4.1 Band structure of Poly-Si/SiO_2/n-Si MOS capacitor.

4.2. C-V and G-V Characteristics :

The C-V and conductance curves of the sample are as follows:

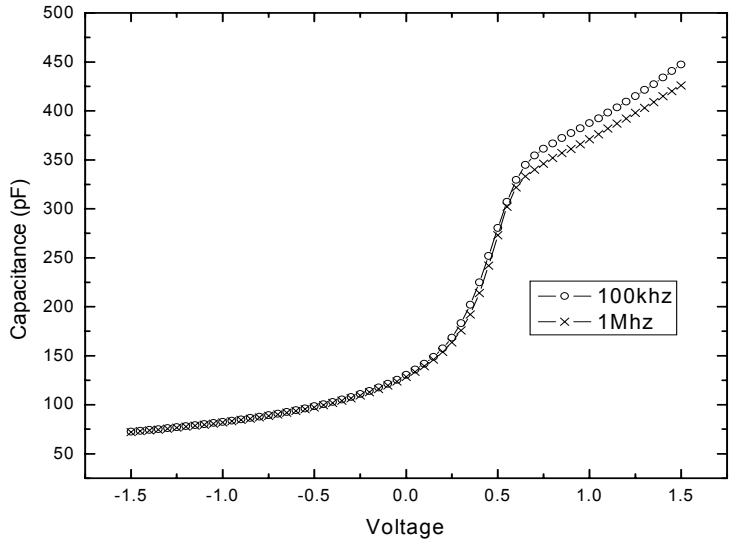

Fig.4.2 High-frequency capacitance at 1 MHz and 100 kHz.

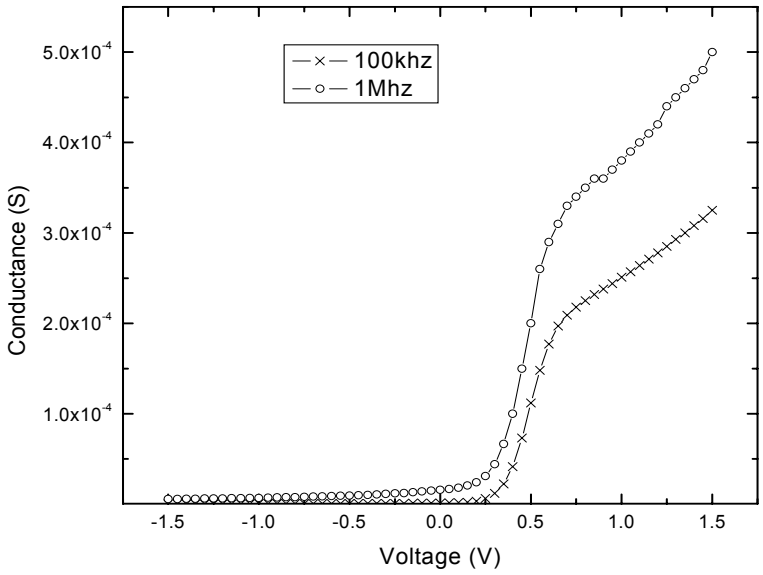

Fig.4.3. The conductance curves at 1MHz and 100 kHz.

Even though it is outside the scope of this work, we have performed C-V measurements for the sake of completeness. Fig. 4.2 and Fig. 4.3 show the C-V and G-V curves measured at two different frequencies (100 kHz and 1 MHz). We were not be able to measure a quasi-static C-V curve. This is no surprise due to oxide thickness. The static charge measurement is not expected at such thin oxides since there is a significant amount of leakage current even at very low fields. Having as little gate oxide leakage current as possible is very important in C-V measurements, because gate oxide current adds or subtracts from the displacement current. This leads an erroneous capacitance, because the current is no longer proportional to the capacitance in that case.

The leakage current in the inversion side gets smaller as we can see from the conductance data. The capacitance values approach true values in this regime. However, they do not saturate as one usually expect from an ordinary MOS capacitor. The decrease in inversion capacitance with voltage might be related to gate material. Poly-Si can be depleted and perhaps inverted with respect to the gate voltage, an effect which is not assumed for metals [73]. In this case the capacitance configuration will contain an additional gate capacitance in addition to oxide capacitance in series with substrate capacitance.

The high frequency curves in accumulation region do not reach a saturation level. The additional carriers to the substrate due to leakage might cause constant increase in total charge. The conductance curves also indicate this point at positive voltages. The conductance increases with the temperature which is an indication of additional flow of carriers.

There are also other factors one has to take into account while analyzing C-V and G-V curves for such thin oxides. In ultra-thin oxides Fermi-Dirac statistics is valid rather than Maxwell-Boltzmann statistics. Also inversion layer quantization must be taken into account. Both of these factors must be considered in an attempt to explain the C-V. In these degenerate conditions, free carriers can occupy higher energy states and this leads to an increase in band bending and surface potential and a decrease in substrate capacitance. These effects are discussed in many works in the scientific literature [74, 75].

4.3. I-V Characteristics :

The temperature dependent current-voltage characteristics are shown in the figure below:

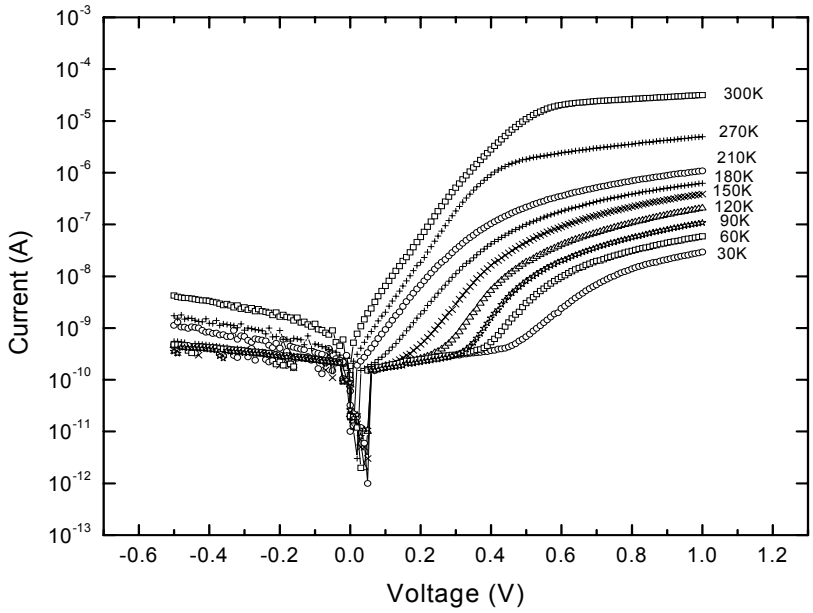

Fig. 4.4 Current-Voltage graphics at different temperatures

The measurements were performed in a range between 14 K and 300 K. I-V curves at chosen temperatures show a strong temperature dependency in the accumulation regime and weak temperature dependency in the inversion regime.

4.4. Possible Current Transport Mechanisms:

In the inversion region, the current doesn't show a strong dependency on temperature. Especially at low and medium temperatures (up to 200 K), the current shows no temperature dependency at all. As the temperature increases, an increase in the order of a decade is seen in the total current. It is clear that the device current is driven by voltage dependent or weakly temperature dependent mechanisms. The suggested model for this regime is the direct tunneling model formulated by Hu [29]. The expression describing the direct tunneling current was given by the formula (Eq.1.12). The weak temperature dependency in inversion is related to subtreshold swing in that expression.

In the accumulation part, it can easily be seen that two different mechanisms are competing to dominate the total current in the device. One of these mechanisms depends strongly on temperature. This mechanism plays an important role especially at high temperatures. It also becomes dominant at low temperatures as the field in the oxide increases. The second mechanism seems to be independent of temperature and dominant at low temperatures and low fields. This field activated current doesn't change with the temperature but it loses its dominance as the temperature increases due to increase in temperature dependent current.

One should plot the Arrhenius plot to find out more about the temperature dependency of the current. Semi-logarithmic plot of I vs. 1000/T plot for accumulation is seen in the Fig.4.5:

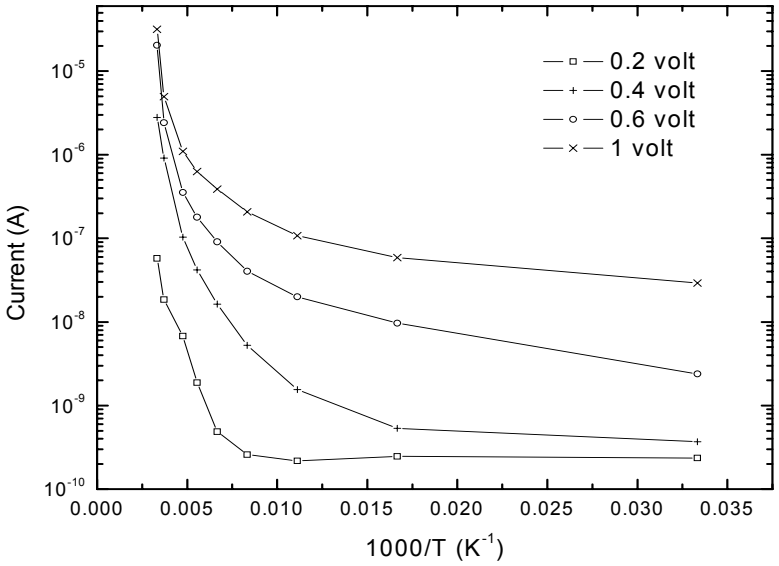

Fig.4.5. Arrhenius plot at different gate voltages

As seen in the figure, the current depends exponentially on temperature. This is the case especially for high temperatures. At lower temperatures, the Arrhenius curve exhibits little dependence on temperature since field activated mechanism starts to contribute to total current in more significantly. This effect is seen more clearly at 0.2 volt. Temperature dependence is seen only at high temperatures. At medium and low temperatures, Arrhenius

curve is almost horizontal which means that current at those temperatures is due to field activated carriers. Same conclusion can be obtained from Fig.4.5. At 0.2 V, field enhanced current dominates until 120 Kelvin and from that point on, the current turns out to be a temperature enhanced mechanism.

In addition to those two current regimes we explained above another current mechanism can be identified in the results displayed in Fig.4.4. For higher voltages than 0.6 volt, current-voltage curve shows a different behavior and becomes flatter. This can be seen for higher temperatures more explicitly such as 300 K or 270 K. This behavior is due to series resistance effect. We will get back to this point at the end of this chapter.

The suggested models for field activated current are Fowler-Nordheim and Schuegraf-Hu direct tunneling model. Fowler-Nordheim model should be eliminated since it is widely accepted that Fowler-Nordheim emission dominates at higher fields (more than 9-10 MeV/cm) and no higher field than 3-4 MeV/cm was applied in our measurements. The direct tunneling model is more suitable than the Fowler-Nordheim model in our case. We plotted ln (I/E^2) vs. 1/E plots, so called Fowler-Nordheim plot, to make sure that the tunneling type is direct rather than Fowler-Nordheim. There were two main regions in those plots; a linear region with a negative slope at high fields and an almost linear region with a positive slope at low fields. Also as the temperature decreases, qualitatively satisfactory parts (high-field) produce steeper curves but the quantitative analyses reveal that this field activated current is more likely to be direct tunneling from the substrate to the gate rather than Fowler-Nordheim type tunneling. We derived the barrier height for tunneling from the slopes of linear regions of Fowler-Nordheim plots. The barrier height values vary between 0.15 eV and 0.34 eV (higher barrier for lower temperature) with $m^*=0.42m_0$. These variations are expected since as the temperature increases, the ratio of thermally excited electrons gets higher and the effective barrier height decreases. The quantitative results for $Si\text{-}SiO_2$ system however are far from the commonly accepted values that vary between 3.0 eV or 3.15 eV. The shape of the Fowler-Nordheim plots and the extracted barrier heights from those plots reveal that although Fowler-Nordheim tunneling might be occuring in our system, it is not a dominant mechanism and the field activated component of the device current should be direct tunneling from Silicon substrate to poly-Silicon gate for accumulation.

The expression of direct tunneling formula for accumulation is [29];

$$J_{DTt} = \frac{A\left|E^2\right|}{\left(1-\sqrt{1-qV_{ox}/\phi_b}\right)^2}\exp\left\{-\frac{B}{E_{ox}}\left[1-(1-qV_{ox}/\phi_b)^{3/2}\right]\right\} \tag{1.26}$$

where

$$A = \frac{q^3(m_o/m_{ox})}{8\pi h\phi_b};\ B = \frac{8\pi\sqrt{2m_{ox}\phi_b^3}}{3qh} \tag{1.24}$$

As was mentioned above, the gate current depends exponentially on 1/T. There are basically four conduction processes in insulators which have exponential dependence on temperature [1]:

Schottky emission:

$$J = A^*T^2\exp\left[-\frac{q}{kT}\left(\phi_b-\sqrt{\frac{qE}{4\pi\varepsilon}}\right)\right] \tag{1.49}$$

Poole-Frenkel emission;

$$J_{PF} = qn_0\mu\cdot E\cdot\exp\left[-\frac{q}{kT}\left(\phi_t-\sqrt{\frac{qE}{\pi\varepsilon_i}}\right)\right] \tag{1.37}$$

Band-to-band tunneling:

$$J_{BTB} = A^*T^2\cdot\exp(-\beta\phi_b)\cdot\exp(-q\phi_s/kT)\cdot\left[\exp(qV_G/kT)-1\right] \tag{1.30}$$

Ohmic emission:

$$J = C\cdot E\cdot\exp(-\Delta E_a/kT) \tag{1.39}$$

We studied Poole-Frenkel plots, ln (J/E) vs. $E^{1/2}$, to determine which process is responsible for the increase of current with temperature. The plots didn't produce any significant evidence of existence of Poole-Frenkel conduction. Curves were the type of second order polynomials (i.e. parabolas) and deconvolution of oxide permittivity values from those rare

and narrow linear regions resulted in 10.1 ε_0 to 24 ε_0. It is obvious that these values are not realistic when one takes the fact that Silicon dioxide permittivity is 3.8-3.9 ε_0. Therefore our conclusion was that Poole-Frenkel model is not an appropriate explanation for our sample.

The last model we examined in search for thermal component of the device current was band-to-band tunneling. This model is based on the Schottky diode theory. It describes the tunneling thermal electrons in a MOS diode. Eq. 4.5 is identical to the standard thermionic emission equation for Schottky barriers except a tunneling probability term. We were be able to obtain very good results in our fit attempts by this model but the Schottky barrier height (work-functions difference between the gate and the substrate) ,which is one of the fit parameters, reduced mass in the oxide and the ideality factor, took unrealistic values for our diode. The Schottky barrier height values were about 0.15 and 0.20 eV for successful fits but in our structure this value has to be around 0.9 eV. When we used barrier height values close to 0.90 eV, we couldn't generate proper match between the experimental data and the model. Therefore band-to-band tunneling model for the thermal current was eliminated.

After all we concluded that thermal current is dominated by Schottky-like (thermionic) emission. To be sure of our conclusion, we, for the last, studied two more plots and compare them: one was J vs. $E^{1/2}$ and the other was J/E vs. $E^{1/2}$ at various temperatures. We did this step to ensure that the thermal current mechanism is Schottky emission and not the Poole-Frenkel. The existence of linearity in the first plot and variations in linearity in the second plot are another proof that thermally activated current results from Schottky emission.

4.5 Description of I-V curves:

Up to now, we used mostly qualitative methods to determine the current transport method in our MOS capacitors. We also used more quantitative techniques to examine our results further. We performed many fit attempts by using direct tunneling and thermionic emission models both separately and together. During these attempts, we defined and used many fit parameters and checked their physical meanings. All the details will be given in the following sections.

At first, we used only the direct tunneling model for tunneling part in our fits and the thermionic emission model for the thermally enhanced current. After then, we defined the total current in the device as the summation of two currents and tried to fit the theoretical results to experimental data by using the values of fit parameters we obtained from separate fits:

$$J = J_{DT} + J_{th} \tag{4.1}$$

$$J = A^{*}T^{2}\exp\left[-\frac{q}{kT}\left(\phi_b - \sqrt{\frac{qE}{4\pi\varepsilon}}\right)\right] + \frac{A\left|E^{2}\right|}{\left(1-\sqrt{1-qV_{ox}/\phi_b}\right)^{2}}\exp\left\{-\frac{B}{E_{ox}}\left[1-(1-qV_{ox}/\phi_b)^{3/2}\right]\right\} \tag{4.2}$$

Direct tunneling model worked very well for the field activated part of I-V curves but thermionic emission fit didn't` give any quantitative success although its qualitative results were acceptable:

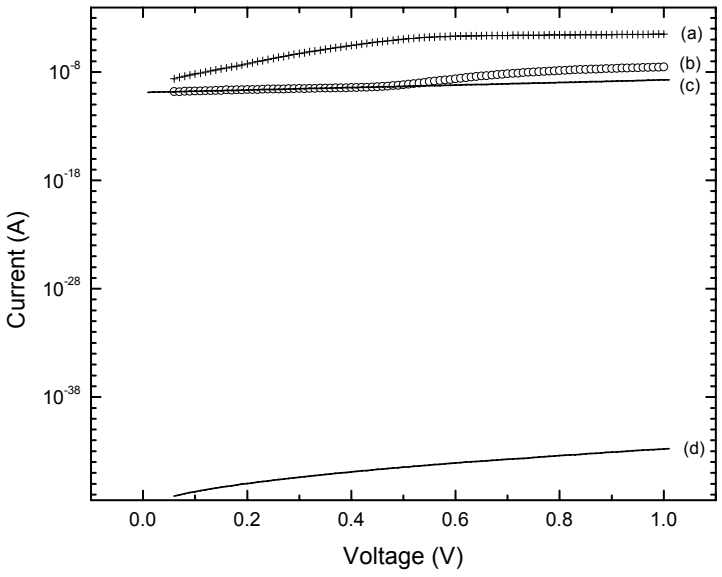

Fig. 4.6 (a) Experimental data at 30 K; (b) experimental data at 300 K; (c) theoretical tunneling curve; (d) theoretical Schottky curve.

In Fig.4.6 and in Fig. 4.7, the pure Schottky theory curve without α, seems to be more suitable to the region we described as series resistance effect rather than to the region we try to fit. However this is not the case and the high voltage region becomes flat due to series resistance. This topic will be discussed in section 4.5.

We made modifications on thermionic emission expression and introduced a fit parameter, n while the total current was still the sum of two components: and J_{th} became;

$$J_{th} = A^* T^2 \exp\left[-\frac{q}{nkT}\left(\phi_b - \sqrt{\frac{qE}{4\pi\varepsilon}}\right)\right] \tag{4.3}$$

The results were more successful with respect to previous ones but still far from satisfaction. In Fig.4.7 below, the fits with respect to different n values are shown:

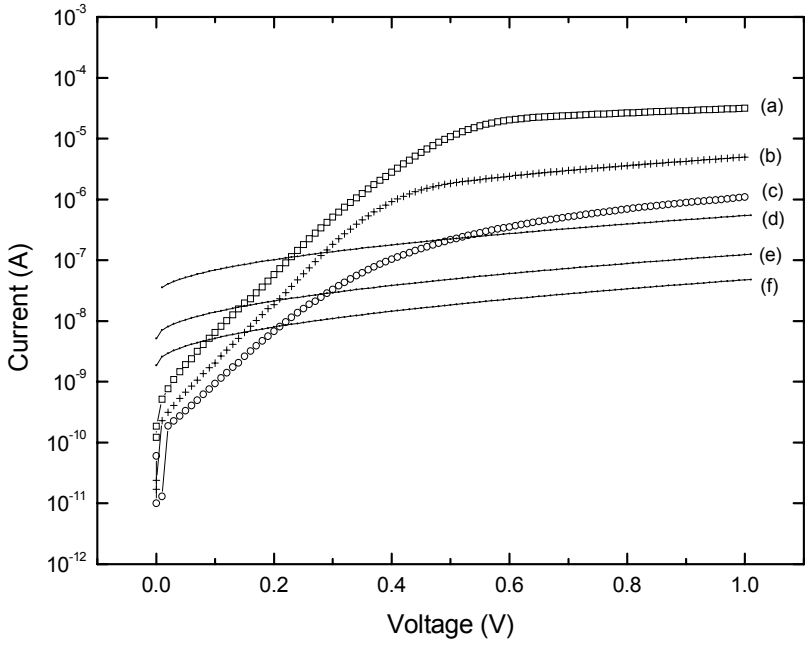

Fig. 4.7 Experimental data at (a) 300 K; (b) 270 K; (c) 210 K; and computer generated fits (d) 300 K; (e) 270 K; (f) 210 K.

After these results we decided to introduce another fit parameter to match the experimental data and computer generated fits. The electric field factor due to image force lowering is proportional to square root of electric field. We changed that power of ½ to a variable and labeled it as alpha, α. We made new fit attempts using the new expression of current and the results, this time, were much more better and satisfactory. The total current, therefore, we used in our fits became;

$$J = A\cdot R^{*}\cdot T^{2}\exp\left[-\frac{q}{nkT}\left(\phi_b-\sqrt{\frac{q}{4\pi\varepsilon}E^{\alpha}}\right)\right]+\frac{A\cdot R^{*}\cdot\left|E^{2}\right|}{\left(1-\sqrt{1-qV_{ox}/\phi_b}\right)^{2}}\exp\left\{-\frac{B}{E_{ox}}\left[1-(1-qV_{ox}/\phi_b)^{3/2}\right]\right\} \qquad (4.4)$$

Where A is the device area and R^{*} is Richardson constant;

$$R=\frac{q^{3}(m_o/m_{ox})}{8\pi h\phi_b};\ B=\frac{8\pi\sqrt{2m_{ox}\phi_b^{3}}}{3qh} \qquad (4.5)$$

In this expression there are two active fit parameters; n and α; and four passive fit parameters: carrier mass in the oxide, barrier height, oxide permittivity and device area. We chose the passive fit parameters at the beginning of each fit attempt and kept them constant during that fit session. We changed only the temperature and active parameters during the fit process.

Among many attempts, we found three different sets presentable. In these fits, we used different values for both active and passive parameters and tried to obtain the best match between the theory and the experimental data. The details of these fits and the values of the parameters are as follows;

Set 1:

Table 4.1 Passive fit parameters for set-1

Permittivity	ε	3.9 ε_0 (ε_0 = 8.85x10^{12} C^2/N•m^2)
Oxide thickness	d	30 Angstrom
Reduced mass	m	0.47 m_0 (m_0 = 9.1x10^{-31} kg)
Barrier height	Φ_b	3.05 eV
Area	A	550x550 μm^2

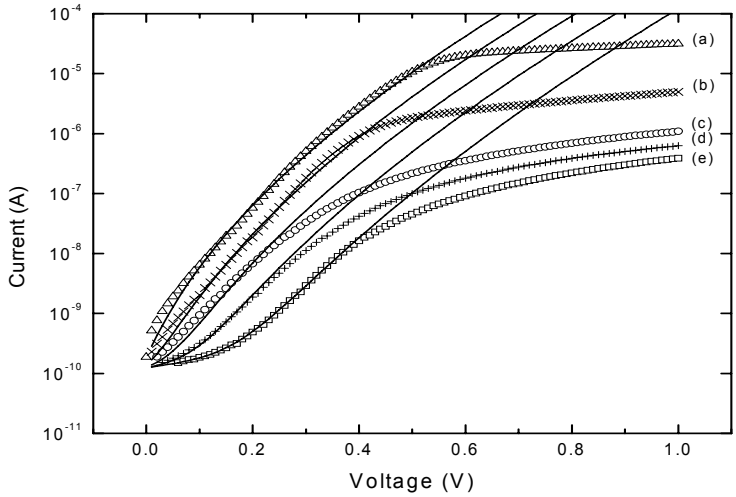

Fig. 4.8 Fits at (a) 300 K; (b) 270 K; (c) 210 K; (d) 180 K; (e) 150 K with parameters of set1.

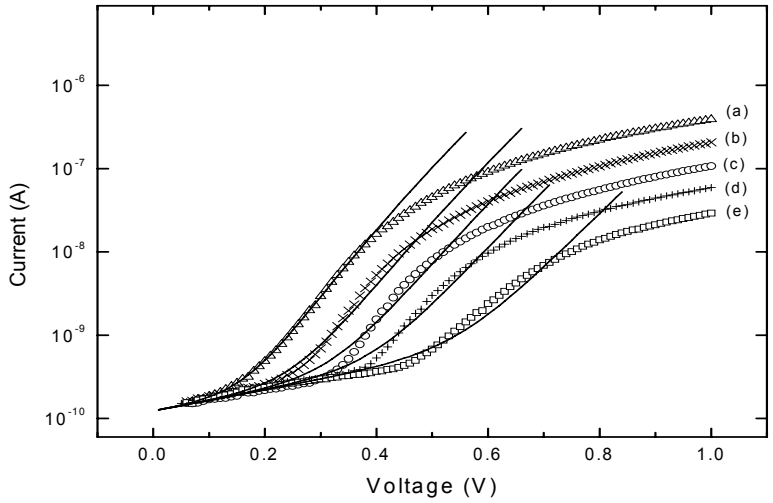

Fig. 4.9 Fits at (a) 150 K; (b) 120 K; (c) 90 K; (d) 60 K; (e) 30 K with parameters of set1.

The active parameters in this set are: Temperature (in Kelvin), n and α:

Table 4.2 The active fit parameters for Set-1

T	300	270	210	180	150	120	90	60	30
n	3.52	3.78	4.75	5.35	6.10	7.30	9.50	14.0	27.0
α	0.58	0.58	0.58	0.58	0.58	0.58	0.58	0.58	0.58

The observed characteristics of our MOS capacitor are separated into two parts as we mentioned above; thermionic characteristics with temperature and tunneling characteristics. These two transport processes are seemed to be competing mechanisms. The tunneling component can be accepted as a base current for the device. It follows only the changes in the field in the oxide and it is not affected by the variations in the temperature since its dependence on temperature is very weak. As the temperature increases thermionic current becomes dominant process and I-V curve looks like more and more pure Schottky emission curve. However Schottky mechanism is not just a temperature dependent mechanism but it also depends on voltage. As the voltage exceeds a threshold value the thermionic current becomes greater than the tunneling current and it overtakes the tunneling current. The threshold value should decrease as the temperature increases.

The tunneling current dominates the device characteristics at low temperatures up to 90 Kelvin. However, at medium temperatures from 120 Kelvin to 210 Kelvin, we see a transition from tunneling to thermionic current and the total current in the device is determined by the two components almost at the same amount. Under the light of these observations, we employed our defined total current with modifications to Schuegraf-Hu direct tunneling and Schottky emission models. At high temperatures such as 300 K or 210 K, there was an exact match between the experimental data and the generated data up to 0.6 volts. After this voltage series resistance effect becomes important. Since the device current is deeply affected by this phenomenon, we see big differences between the experimental data and model calculations. At very low temperatures, fits gave very good results for the tunneling and acceptable results for thermionic current. It was also observed that the voltage at which thermionic process starts to dominate decreases as the temperature increases. For example this threshold value is about 0.5 volts for 30 K and it decreases up to 0.2 volts at 120 K. The series resistance effect again dominates the high voltage regimes and it doesn't allow thermionic current to last long and it causes the thermionic current to rule the total current for a very short voltage interval. This interval is about, for example,

0.2 volts (0.5 to 0.7) for 30 K, 0.2 volts (0.3 to 0.5) for 60 K and 0.25 volts (0.15 to 0.4) for 150 K. This change from thermionic characteristics to series resistance effect in the observed current makes it difficult to make perfect fits to thermionic current component part of the total current for especially low temperatures.

The medium temperatures are the most important ones for our approach since we can see the transition between tunneling and thermionic currents for a, relatively, long voltage interval. We see from Fig.4.10 and Fig.4.12 that the fit results are very satisfactory at 120 K, 150 K and 180 K. The calculated total current shows a smooth transition from base tunneling region to up thermionic region very successfully.

The values of passive fit parameters are given in table 4.1 and table 4.2 above. The permittivity is chosen as 3.9 ε_0 which is universally accepted for SiO_2, and the device area (or the gate area) was measured as 550x550 (μm^2). These two parameters were kept constant for all the fits we did. The other three parameters were decided at the beginning of each fit. There is no consensus on some constant carrier mass value. The oxide mass values show great differences in different works in scientific literature. The values vary from 0.32 m_0 to 0.55 m_0 for electron mass and from 0.25 to 0.32 m_0 for hole mass. In this work we used three different mass values as fit parameters. In this set the carrier mass was 0.47 m_0 (electron). And the barrier height at the interface of Si/SiO_2 was chosen to be 3.05 eV. This is a suitable value as the commonly used values range from 2.95 eV to 3.15 eV for $Si\text{-}SiO_2$ system. This value was chosen for both the tunneling barrier height which electrons feel while they tunnel from Si substrate to poly-Si gate and the thermionic barrier height that the electrons must overcome thermally to pass to the conduction band of SiO_2.

The active parameters are n, a factor some groups call it as barrier lowering coefficient [76], and α, the image force lowering factor. The meanings of these factors will be discussed at the end of this section and therefore only the numerical values of them will be mentioned here. Alpha, α, was kept constant at a value of 0.58 while n changes from 3.52 to 27.0. At high temperatures n values were lower and n becomes greater as the temperature decreases. At high temperatures, n changes adiabatically but this change turns to be abrupt as the temperature decreases. For example, from 300 K to 270 K, change in n is 0.26 and 0.6 for 210 K to 180 K, and 1.2 for 150 to 120 K. For very low temperatures n values reach very high values (especially for 30 K). This is probably due to the fact that the thermionic component is negligible at these temperatures and a fit attempt by using this model is not meaningful.

SET 2

The details are as below for this fit attempt:

Table 4.3 The passive fit parameters.

Permittivity	ε	3.9 ε_0 ($\varepsilon_0 = 8.85 \times 10^{12}$ $C^2/N \cdot m^2$)
Oxide thickness	d	30 Angstrom
Reduced mass	m	0.467 m_0 ($m_0 = 9.1 \times 10^{-31}$ kg)
Barrier height	Φ_b	3.1 eV
Area	A	550x550 μm^2

Table 4.4 The active fit parameters.

T	300	270	210	180	150	120	90	60	30
n	3.60	3.87	5.05	5.42	6.25	6.85	8.75	12.7	24.2
α	0.58	0.58	0.57	0.58	0.58	0.59	0.59	0.59	0.59

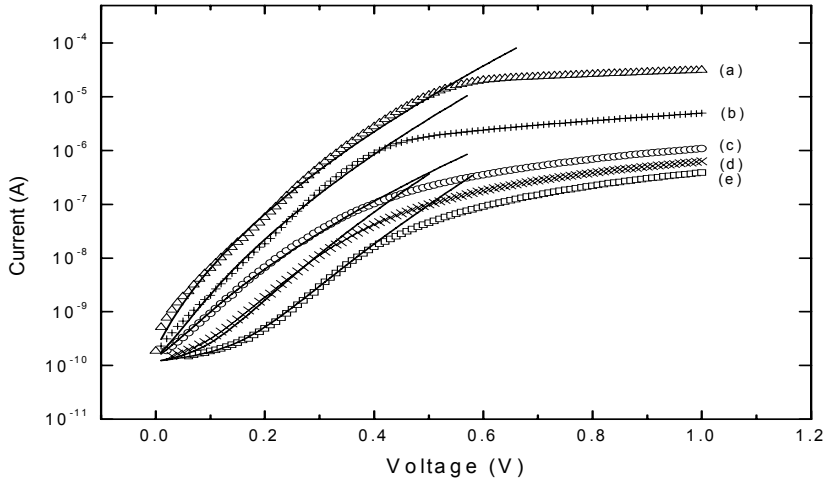

Fig.4.10 Fit plots at (a) 300 K; (b) 270 K; (c) 210 K; (d) 180 K; (e) 150 K with parameters of set2.

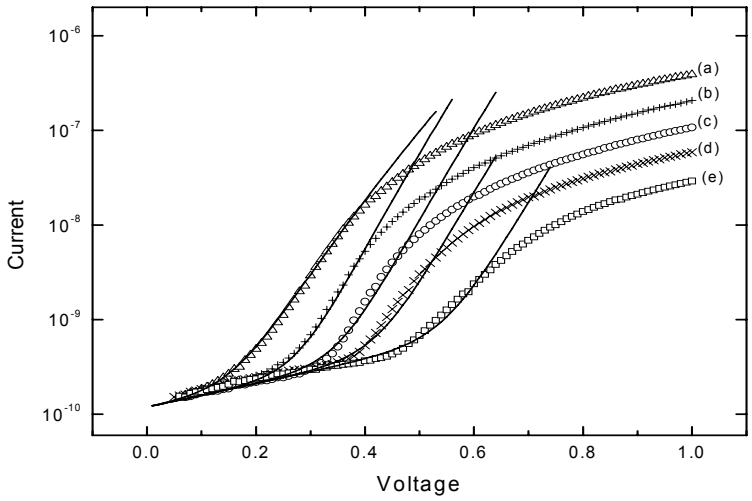

Fig.4.11 Fits at (a) 150 K; (b) 120 K; (c) 90 K; (d) 60 K; (e) 30 K with parameters of set2.

In the second set of fit, we set the barrier height as 3.1 eV and m^* as 0.467 m_0. The most notably difference in this try with respect to previous one is that α was not kept constant. It was allowed to change. By doing so we aimed to have better fits to the experimental data. The result was not much different from the previous fit set. Almost the same characteristics were obtained. The details are below:

SET 3

In the last fit attempt we present, we used the oxide thickness as 28 Angstrom rather than 30 ± 2 Angstroms. We modified almost all the parameters except the permittivity. Image force lowering parameter α was chosen to be variable as it was in the second fit set. The active and passive fit parameters are:

Table 4.5 The active fit parameters for set-3.

T	300	270	210	180	150	120	90	60	30
n	3.4	3.62	4.75	5.38	5.80	7.0	8.0	11.5	25.5
α	0.58	0.58	0.57	0.57	0.58	0.58	0.59	0.59	0.58

Table 4.6 The passive fit parameters for set-3

Permittivity	ε	3.9 ε_0 (ε_0 = 8.85x10^{12} C^2/N•m^2)
Oxide thickness	d	28 Angstrom
Reduced mass	m	0.55 m_0 (m_0 = 9.1x10^{-31} kg)
Barrier height	Φ_b	3.0 eV
Area	A	550x550 μm^2

And the fit results are for these parameters are:

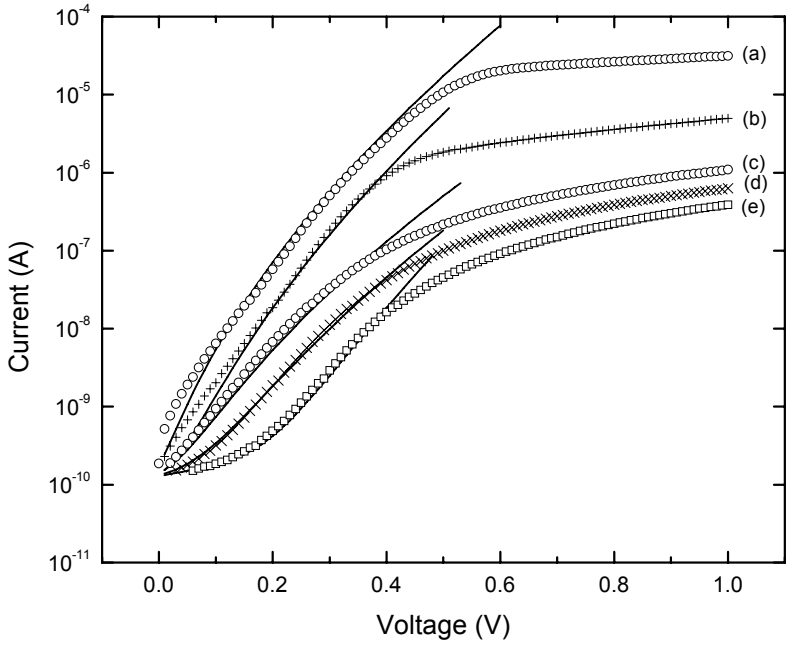

Fig.4.12 Fit plots at (a) 300 K; (b) 270 K; (c) 210 K; (d) 180 K; (e) 150 K with parameters of set3.

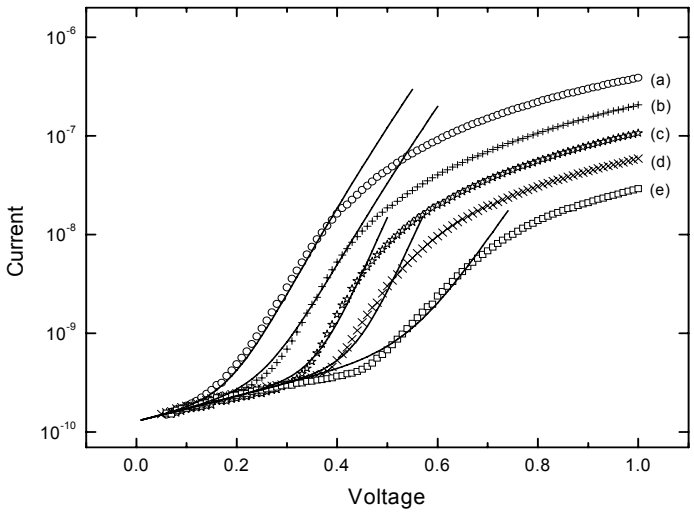

Fig.4.13 Fits at (a) 150 K; (b) 120 K; (c) 90 K; (d) 60 K; (e) 30 K with parameters of set3.

This set was little bit more successful than the other two ones but there was no significant change from the previous two ones. The main difference in this set was in the match at low-medium temperatures, 120 K and 90 K. The fits produced better results but in this region.

At the end of these three results, it can be said that all of them produce similar results with some minor differences. All the three sets were very successful at high and medium temperatures and they also gave good and acceptable results at low temperatures. Therefore none of them is preferable in this manner.

Also all the fits turned out to be successful with almost the same fit parameter values. For the passive fit parameters, all the values are in acceptable ranges, for example barrier height change between 3.0 eV and 3.15 eV or oxide mass between 0.47 to 0.55 m_0. And for the active parameters, image force lowering power α is centered on 0.58 for all the three fits. Although in other fit attempts we set this parameter up to different values from 0.54 to 0.61, the best fits were obtained by using 0.57, 0.58 and 0.59. The situation is also similar for the barrier height lowering parameter, n. This value starts from 3.52 in set1, 3.60 in set2, 3.4 in set3 and go up to 27.0 in set1, 24.2 in set2, and 25.0 in set3. Also, the increase in n between

two temperature increases at lower temperatures in all three sets. Set3 is little bit better in terms of n since it keeps n at 11.7 at 60 K.

4.6. Conclusion

The current-voltage characteristics of ultra-thin oxide capacitor was found to be temperature dependent in accumulation and tunneling in inversion. This case has also been observed by many other groups [76-88] and there is a growing interest in temperature dependent measurements in both cryogenics and high temperatures due to new advances in superconducting circuits and high temperature applications. The main questions about our modification on Schottky emission theory and our fit procedure at this point are the physical meaning of those fit parameters and their numerical values. What do these parameters imply and are they meaningful with these values?

This is a common method in I-V analysis that one changes the main parameters in a suitable conduction mechanism and set some parameters adjustable if one thinks that that mechanism occurs in the device but does not exactly match with the experimental data. Although some authors do this step without giving valid physical explanations and they approach to the problem from a purely mathematical point of view, we believe that all these parameters have to carry some physical meanings. In this work we introduced two basic parameters; n and α.

The barrier height parameter n decreases the weight of thermionic current as the temperature decreases just like as the ideality factor does in Schottky junctions. At low temperatures n goes higher and it reduces the thermionic current and allows the base tunneling current to show up more. Therefore n, in this manner, is very much like an ideality factor but the main difference between n and an ideality factor is that ideality factor is related with the voltage in the device. The ideality factor approaches unity if the applied voltage in a device is completely taken by the oxide. If some of the applied voltage falls on out of oxide then the ideality factor increases. However in our case, n is applied to barrier height and it somehow defines a new effective barrier value for the thermionic emission. The interesting point here is the effective barrier height decreases as the temperature decreases. It is expected that the barrier height decreases and hence the thermionic current increases as the temperature increases. However, if one considers the carrier distribution in the conduction band of the substrate and takes n as an implication of the carriers that can overcome the barrier, then as the temperature decreases the number of the carriers which

can get over the barrier and pass through the SiO_2 conduction band decreases which corresponds to the increase in n with decreasing temperature

Another explanation for the barrier lowering factor can be done from the view point of tunneling current. The factor n can behave the way it reduces the tunneling barrier and causes more carriers to be able to tunnel through the oxide.

Another conclusion can be made about inhomogeneous barriers. The temperature dependency of n can be attributed to lateral inhomogeneous barrier distribution over the device area. It means that not all the points in the device have the physical structure. Some of the regions contain small patches so that the barrier height in these regions is slightly different than the accepted barrier heights. This difference however should be small and the distribution can be described by a Gaussian curve centered on the accepted values, which are in our fits 3.0 eV, 3.05 eV and 3.15 eV.

The values which n took in our fits are reasonable and compatible with other works [76]. Yassine and Hijab found n as 3.7 in their paper. This is very close to our n which takes ~3.5 at 300 K in our fits.

The second fit parameter is α. In many reference books it can be found about image force lowering of barrier due to carriers injected to oxide conduction band. In these theories, the interaction between the injected carriers and the oxide matrix is assumed to be Coulombic. However in reality, the oxide is not perfect as it was assumed and the interactions are much more complex due to inhomogeneity of the oxide. There are oxide charges as well as surface states which destroy the presupposed homogeneity and make the interactions complex. We believe that the change in α from 0.50 to 0.58 and so on corresponds to this complexity.

Another idea about α could be that the oxide might not be uniform for all the interface region of Si/SiO_2. Some points might be much more thinner than 30 Angstroms and it could lead a device behavior like a pn junction rather than MOS structure.

The final words about the I-V characteristics will be on the series resistance. At high voltages at all temperatures series resistance effect plays important role in our I-V results as seen in Fig.4.4. At high temperatures such as 300 K or 270 K, this effect is seen after 0.5-0.6 volts and at lower temperatures (i.e. 30 K) it starts to be active from about 0.7 volts. I-V curves start to become parallel after these points at the mentioned temperatures and device

is driven to an ohmic characteristics. At this point we should avoid confusion; one might think of the Fig.4.5 and get confused since the original thermionic theory curve qualitatively looks like to the curve we label as series resistance as we mentioned in section 4.3 To make this point clear one should plot another type of Arrhenius curve: J/T^2 vs. 1/T assuming Schottky emission described by Eq.4.3. This plot gives such results as in Fig. 4.14:

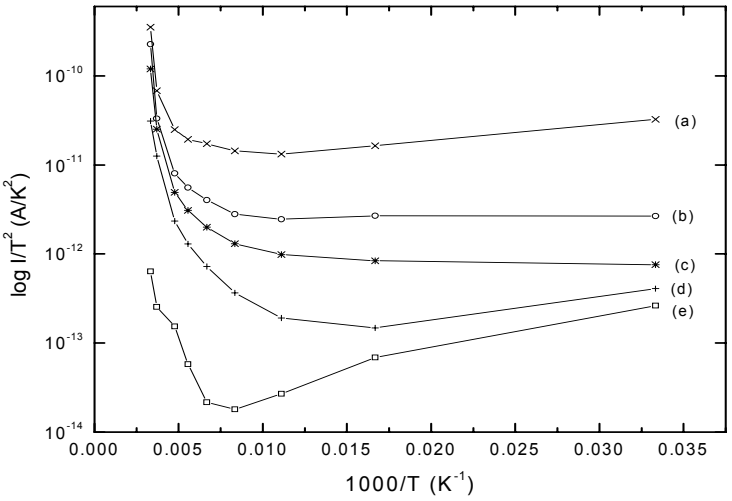

Fig.4.14 The second type Arrhenius plots at (a) 1 v; (b) 0.6 v; (c) 0.5 v; (d) 0.4 v; (e) 0.2 v.

When we compare Fig.4.5 and Fig.4.14 we see there are basic differences in all the plots at different voltages. In the Fig.4.5 it was observed that two different temperature dependency regions exist for high voltages (0.6 and 1 volts). At high temperatures the Arrhenius curve is steeper and for low temperatures this curve becomes smoother but still exists. After reading this information from the Fig.4.5, one can easily say that the dominant mechanism is certainly the thermionic emission for medium and high temperatures. And for low voltages such as 0.2 or 0.4 volts, two different behaviors can be identified; one part of the curve shows a strong temperature dependency and the other shows almost no temperature dependency. This indicates that at high voltages, a temperature dependent mechanism is dominant, for example thermionic emission at 300 K, but at low voltages the current is contributed by a field activated mechanism, i.e. 30 K.

Another interesting note about this point is that we tried to make a suitable fit to high field I-V curve at 300 K by using the thermionic emission. The successful result was obtained by letting α be 0.48. We believe that although α can be greater than 0.5 and this can be explained as we did above, it shouldn't be less than 0.48. Therefore, under the light of these discussions we believe that our first conclusion is correct and the high fields I-V characteristics are contributed by series resistance affect at all the temperatures. Also as it is expected, series resistance is seen at lower fields at higher temperatures with respect to lower temperatures.

REFERENCES

[1] S. M. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons, 2nd ed., 1981.

[2] Nicollian E.H. and Brews J.H., *MOS (Metal Oxide Semiconductor) Physics and Technology*, 1982.

[3] B. Van Zeghbroeck, *Principles of Semiconductor Devices*, 2004.

[4] Fonstad C. G., *Microelectronic Devices and Circuits*, McGraw-Hill, 1994.

[5] R. Fowler and L. Nordheim, "Electron emission in intense electric fields", Proc. Roy. Soc. A, vol. 119, pp. 173-181, 1928.

[6] Lenzlinger F.M. and Snow E.H., "Fowler-Nordheim tunneling into thermally grown SiO_2", J. Appl. Phys., 1969, 40, 278.

[7] Osburn C.M. and Weitzman E.J., "Electrical construction and dielectric breakdown in silicon dioxide films on silicon", J. Elec. Soc., 1972, 119, 603.

[8] Maserjian J., "Tunneling in thin MOS structures", J. Vac. Sci., 1974, 11(6), 996.

[9] Shatzkes M. and Av-Ron M., "Impact ionization and positive charge in thin SiO_2 films", J. Appl. Phys., 1976, 43, 3191.

[10] Weinberg Z.A., "Tunneling of electron from Si into thermally grown SiO_2", Solid-State Electronics, 1977, 20, 11.

[11] Av-Ron M., Shatzkes M., Distefano T.J., Gdula R.A., "Electron tunneling at Al-SiO_2 interface", J. Appl. Phys., 1984, 52(4), 2897.

[12] Krieger G., Swansson R.M., "Fowler-Nordheim electron tunneling in thin Si-SiO_2-Al structures", J. Appl. Phys. 1981, 52, 5710.

[13] Weinberg Z.A., "On the tunneling in metal-oxide-silicon structure", J. Appl. Phys. 1982, 53, 5052.

[14] Chang C. Brodersen R.W., Hu C., "Insulating films in semiconductors", Amsterdam, North Holland, 1983, p.717.

[15] Nissan-Cohen Y., Shappir J. Frohman-Bentchkowsky D., "Measurement of Fowler-Nordheim tunneling currents in MOS structures under charge trapping conditions", Solid-State Electronics, 1985, 28, 717.

[16] Kong S.O., Kwok C.Y., "Fowler-Nordheim tunneling current in a Mg/Polycrystallin Si oxide/n^- polycrystalline Si metal-oxide-silicon structure", Appl. Phys. Lett. 1993, 63(19), 2667.

[17] Olivo P. Sune J. Ricco B., "Determination of the Si-SiO_2 barrier height from the Fowler-Nordheim plot. IEEE Electron Dev. Lett. 1991, 12, 620.

[18] Chiou Y.L., Gambino J.P., Mohammad M., "Determination of the Fowler-Nordheim tunneling parameters from the Fowler-Nordheim plot", Solid-State Electronics, 2001, 45, 1787.

[19] Depas M., Vermeire B., Mertens P.W., Van Meirhaeghe R.L., Heyns M.M., "Determination of the tunneling parameters in ultra-thin oxide layer Poly-Si/SiO_2/Si structures", Solid-State Electronics, 1995, 38, 1465.

[20] Lo S.L., Buchanan D., Taur Y., Wang W., "Quantum mechanical modeling of electron tunneling current from the inversion layer of ultra-thin oxide nMOSFETs", IEEE Electron Dev. Lett. 1997, 18, 209.

[21] Bowen C., Fernardo C., Klimeck G., Chatterjee A., Blanks D., Lake R., Hu J., Davis J., Kulkarni M., Hattangady S., Chen I., "Physical oxide thickness extraction and verification using quantum mechanical simulation", IEDM Technical Digest, 1997, p.869.

[22] Sune J., Olivo P. Ricco B., "Self-consistent solution of Poisson and Schrödinger equations in accumulated semiconductor-insulator interfaces", J. Appl. Phys. 1991, 70, 337.

[23] Rana F., Tirwari S., Buchanan D., "Self-consistent modeling of accumulation layers and tunneling currents through very thin oxides", Appl. Phys. Lett. 1996, 69(8), 1104.

[24] Yang. N., Henson W., Hauser J., Wortman J., "Modeling study of ultra-thin gate oxides using direct tunneling current and capacitance-voltage measurements in MOS devices", IEEE Trans. Electron Dev., 1999, 46(7), 1464.

[25] Register L., Rosenbaum E., Yang K., "Analytic model for direct tunneling in polycrystalline silicon gate metal-oxide-semiconductor devices", Appl. Phys. Lett., 1999, 74(3), 457.

[26] Yang K.N., Huang H.T., Chang M.C., Chu C.M., Chen Y.S. Chen M.J., Lin Y.M., Yu M.C., Jang S., Yu D., Liang M., "A physical model for hole direct tunneling current in P^+ poly-gate PMOSFETS with ultra-thin gate oxides", IEEE Trans. Electron Dev., 2000, 47(11), 2161.

[27] Ghetti A., "Characterization and modeling of the tunneling current in Si-SiO_2-Si structures with ultra-thin oxide layer", Microelectronic Engineering, 2001, 59, 127.

[28] Schuegraf K.F., King C.C., Hu C., Digest Symposium on VLSI, IEEE, New York, 1992, pp.18.

[29] Lee W.C. and Hu C., "Modeling gate and substrate currents due to conduction and valence band electron and hole tunneling", Digest Symposium on VLSI Technology Digest of Technical Papers, IEEE, New York, 2000, pp.198.

[30] Timp G. et al., "Process toward 10-nm CMOS devices," in IEDM Tech. Dig., 1998, pp. 615–618.

[31] Hou Y. T., Lia M. F., Jin Y., and Lai W. H., "Direct tunneling hole currents through ultra-thin gate oxides in metal-oxide-semiconductor devices", J. Appl. Phys. vol.91, No.1, 2002.

[32] Lo S. H., Buchanan D. A. and Taur Y., "Modeling and characterization of quantization, polysilicon depletion, and direct tunneling effects in MOSFETs with ultrathin oxides", IBM J. Res. Develop. vol.43 No.3, 1999.

[33] Clerc P., Sullivan P. O., McCarthy K. G., Ghibaudo G., Pananakis G., Mathewson A., "A physical compact model for direct tunneling from NMOS inversion layers", State Electronics, 2001, vol. 45, p.1705.

[34] Lee J., Bosman G., Green K. R., and Ladwig D., "Model and analysis of gate leakage current in ultra-thin nitrided oxide MOSFETs", IEEE Trans. Electron Dev., 2002, 49(7).

[35] Mao L., Tan C., and Xu M., "The effect of image potaential on electron transmission and electric current in the direct tunneling regime of ultra-thin MOS structures", Microelectronics Reliability, 2001, 41, p.927.

[36] Sheu C-Y., and Jang S-L., "A physics-based electron gate current model for fully depleted SOI MOSFETs", Solid-State Electronics, 2000, 44, p.1799.

[37] Bhattacharya S. S., Banarjee S. K., Nguyen B. Y, and Tobin P. J., "Temperature dependence of the anomalous leakage current in poly-silicon-on-insulator MOSFETs", IEEE Trans. Electron Dev., 2002, 41 (2).

[38] Sullivan P. O., Clerc P., McCarthy K.G., and Ghibaudo G., "Direct tunneling models for circuit simulation", Microelectronics Reliability, 2001, 41, p.951.

[39] Hsu B. C., Chen K. F., Lai C. C., Lee S. W., and Liu C. W., "Oxide roughness effect on tunneling current of MOS diodes", IEEE Trans. Electron Dev., 2002, 49 (12).

[40] Chen L., Ma Y., and Tian L., "Modeling on direct tunneling current in ultra-thin oxide NMOSFET considering quantum mechanics", Proc. 23rd International Conference on Microelectronics, vol.2, NIS, Yugoslavia, 2002.

[41] Ghetti A., Bude J., Silverman P., Hamad A., and Vaidya H., "Modeling and simulation of tunneling current in MOs devices including quantum mechanical effects", IEICE Trans. Electron., 2000, vol.E83-C, No.8, p.1175.

[42] Wettstein A., Schenk A., Scholze A., and Fichtner W., "The influence of localized states on gate tunnel currents: Modeling and simulation", SISPAD Tehc. Dig., 1997, p.101.

[43] Gupta A., Fang P., Song M., Lin M-R., Wollesen D., Chen K., and Hu C., "Accurate determination of ultra-thin gate oxide thickness and effective poly-silicon doping of CMOS devices", IEEE Trans. Electron Dev., 1997, 18(12).

[44] Miranda E., Redin G., and Faigon A., "Modeling of the I-V characteristics of high-field stressed MOS structures using a Fowler-Nordhei type tunneling expression", Microelectronics Reliability, 2002, 42, p.935.

[45] Choi C-H., Nam K-Y., Yu Z., and Dutton R. W., "Impact of gate direct tunneling current on circuit performance: A simulation study", IEEE Trans. Electron Dev., 1999, 48(12), 2823.

[46] Cova P., Singh A., and Masut R. A., "Simultaneous analysis of current-voltage and capacitance-voltage characteristics of metal-insulator-semiconductor diodes with a high mid-gap trap density", J. of Appl. Phys. vol.85, No.9, 1999.

[47] Magnus W., and Schoenmaker W., "Full quantum mechanical model for the charge distribution and the leakage currents in ultra-thin MOS capacitors", J. App. Phys., 88 (10), p.5833.

[48] Iwata H., Matsuda T., and Ohzone T., "Two-dimensional self-consistent calculation of gate direct tunneling current in metal-oxide-semiconductor transistors", Jap. J. of Appl. Phys. Part-1 Regular Papers Short Notes & Review Papers, 42(6A), p.3364.

[49] Card H.C. and Rhoderick E.H., "Studies of tunnel MOS diodes I. Interface effects on silicon Schottky diodes", J. Phys. D: Appl. Phys., 1971, vol.4, 1589.

[50] Card H.C. and Rhoderick E.H., "Studies of tunnel MOS diodes II.Thermal equilibrium considerations", J. Phys. D: Appl. Phys., 1971, vol.4, 1602.

[51] Kumar V. and Dahlke W.E., "Characteristics of Cr-SiO_2-nSi tunnel diodes", Solid-State Electronics, 1977, vol. 20, p.143.

[52] Wu J., Register L., Rosenbaum E., "Trap assisted tunneling current through ultra-thin oxide", Proc. IRPS Symposium, 1999, pp.389-395.

[53] Ghetti A., Alam M., Bude J., Sangiogi E., Timp G., Weber G., "Native and stress induced traps in SiO_2 films", Proc. Of the 4^{th} Symposium on the Physics and Chemistry of SiO2 and the Si-SiO_2 interface, Toronto, Canada; 2000, pp.419-428.

[54] Takagi S., Yasuda A., Torimu A.,"A new model for stress induced leakage current including inelastic tunneling", IEEE Trans. Electron Dev., 1999, 46(2), 348.

[55] Fleischer S., Lai P.T., Cheng Y.C., "A new method for extracting the trap energy in insulators", J. Appl. Phys., 1993, 73(1), 3348.

[56] Fleischer S., Lai P.T., Cheng Y.C., "Effects of nitridation temperature on the electron trap characteristics of nitrided-oxide metal-oxide-semicondcutor capacitors", J. Appl. Phys., 1993, 74(1), 740.

[57] Ricco B. and Azbel M. Y., "Physics of resonant tunneling: The one-dimensional double-barrier case", Phys. Rev. B, 1984, vol. 29, no. 4, p.1970

[58] J.P. Sorbier J.P., Croci S., Imbert B., and Plossu C., "Model of leakage current induced by dynamic stress in thin EEPROM tunnel oxides", J. of Non-Crystalline Solids, 2003, 322(1-3), p.122.

[59] Takagi S., Yasuda N., and Toriumi A., "A new I-V model for stress-induced leakage current including inelastic tunneling", IEEE Trans. Electron Dev., 1999, 46(2), p.348.

[60] Buttiker M., "Coherent and sequential tunneling in series barriers", IBM J. Res. Develop., 1988, vol. 32, p.63.

[61] Ricco B., Gozzi G., Lanzoni M., "Modeling and simulation of stress induced leakage current in SiO_2 films", IEEE Trans. Electron Dev., 1998, 45(7), 1554.

[62] Okada K. and Taniguchi K., "Electrical stress-induced variable range hopping conduction in ultrathin silicon dioxides", Appl. Phys. Lett. 1997, 70, 351.

[63] Suzuki E. and Schroeder D.K., J. Appl. Phys., 1986, 60, 3616.

[64] Cheng X.R., Cheng Y.C., Liu B.Y., J. Appl. Phys., 1992, 72, p.5711.

[65] Houng M.P., Yeong H.W., Chang W.J., "Current transport mechanism in trapped oxides: A generalized trap assisted tunneling model", J. Appl. Phys., 1999, vol.86 (3), 1488.

[66] Chou A.I., Lai K., Kumar K., Chowdhury P., and Lee J.C., "Modeling of stress-induced leakage current in ultrathin oxides with the trap-assisted tunneling mechanism", Appl. Phys. Lett., 1997, 70(25), p.3407.

[67] Ng K.K., Comlete Guide to Semiconductor Devices, 1995, McGraw-Hill Inc.

[68] Bethe H. A., "Theory of the Boundary Layer of Crystal Rectifiers" MIT, Radiat. Lab. Rep. 43-12, 1942.

[69] Freeman L.B. and Dahlke W.E., "Theory of tunneling into interface states", Solid-State Electronics, 1970, vol.13, 1483.

[70] Dogish M.Y. and Ho F.D., "A comprehensive analytical model for metal-insulator-semiconductor (MIS) devices", 1992, IEEE Trans. Electron Dev., vol.39, 2771.

[71] Hovel H.J., Semiconductors and Semimetals, vol.11: Solar Cells. NY Academic Press, 1975.

[72] Jacop A.P. et. al. Semiconductor Science and Technology, 2002, 17(9), 942.

[73] Schroder D.K., *Semiconductor Material and Device Characterization 2nd ed.*, 1998, John Wiley & Sons Inc.

[74] Krisch K.S., Bude J.D. and Manchanda L., "Gate Capacitance Attenuation in MOS devices With Thin Dielectrics", IEEE Electron Dev. Lett., 1996, 17, 521.

[75] Vasileska D., Schroder D.K. and Ferry D.K., "Scaled Silicon MOSFET's: Degradation of the Total Gate Capacitance", IEEE Trans. Electron Dev., 1997, 44, 584.

[76] Yassine A., and Hijab R., "Temperature dependence of gate current in ultra-thin SiO_2 in direct tunnelling regime", Integrated Reliability Workshop Final Rep., 1997, p.56.

[77] Lin C.H., Hsu B.C., Lee M.H., and Liu C.W., "A comprehensive study of inversion current in MOS tunnelling diodes", ", IEEE Trans. Electron Dev., 2001, 48(9).

[78] Jacob A. P., Mryberg T., Nur O., Willander M., Lundgren P., Sveinbjörnsson E. Ö., Ye L. L., Thölen A. and Caymax M., "Cryogenic performance of ultra-thin oxide MOS capacitors with in situ doped p+ poly-Si1-xGex and poly-Si gate materials", Semiconductor Science and Technology, 2002, 17, p.942.

[79] Houssa M., Aoulaiche M., Autran J. L., Parthasarathy C., Revil N., and Vincent E., "Modeling negative bias temperature instabilities in hole channel metal-oxide-semiconductor field effect transistors with ultrathin gate oxide layers", J. of Appl. Phys., 2004, 95(5), p.2786.

[80] Pananakakis G., Ghibaudo G., Kies R., Papadas C., "Temperature dependence of the Fowler-Nordheim current in metal-oxide-degenerate semiconductor structures", J Appl. Phys., 1995, 78(4), p.2635.

[81] Schroeder D., and Avellan A., "Physical explanation of the barrier height temperature dependence in metal-oxide-semiconductor leakage current models", Appl. Phys. Lett., 2003, 82 (25), p.4510.

[82] Hadjadj A., Simonetti O., Maurel T., Salace G., and Petit C., "Si-SiO2 barrier height and its temperature dependence in metal-oxide-semiconductor structures with ultrathin gate oxide", Appl. Phys. Lett., 2002, 80(18), p.3334.

[83] Hadjadj A., Salace G., and Petit C., "Fowler-Nordheim conduction in polysilicon (n(+))-oxide-silicon (p) structures: Limit of the classical treatment in the barrier height determination", J. of Appl. Phys. , 2001, 89 (12), p.7994.

[84] Larcher L., Paccagnella A., and Ghidini G., "Gate current in ultrathin MOS capacitors: A new model of tunnel current", IEEE Trans. Electron Dev., 2001, 48(2), p.271.

[85] Salace G., Hadjadj A., Petit C., and Ziane D., "The image force effect on the barrier height in MOS structures: correlation of the corrected barrier height with temperature and the oxide thickness", Microelectronics Reliability, 2000, 40(4-5), p.763..

[86] Waters R., and Van Zeghbroeck B., "Temperature-dependent tunneling through thermally grown SiO2 on n-type 4H-and 6H-SiC", Appl. Phys. Lett., 2000, 76 (8), p.1039.

[87] Salace G., Hadjadj A., Petit C., and Jourdain M., "Temperature dependence of the electron affinity difference between Si and SiO2 in polysilicon (n(+))-oxide-silicon (p) structures: Effect of the oxide thickness", J. of Appl. Phys., 2001, 85 (11), p.7768.

[88] Liu Y., Chen T.P., Ang C.H., and Fung S., "Power-law dependence of charge trapping on injected charge in very thin SiO2 films", Jap. J. of Appl. Phys. Part-2 Letters, 2002, 41 (4A), L384.