A NOVEL APPROACH FOR SYNTHESISING SINUS WAVEFORMS AT POWER LEVEL

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Approval of the Graduate School of Natural and Applied Sciences

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ABSTRACT

A NOVEL APPROACH FOR SYNTHESISING SINUS WAVEFORMS AT POWER LEVEL

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In variable speed motor drive and uninterruptible power supply (UPS) applications, taditional method is to employ some kind of a modulation technique at a high frequency typically 6 kHz to 20 kHz range. In these modulation techniques, the switches are hard switched. The result is application of a series of pulses to the load, and if the load is inductive, sine wave current flows into the load. Hard and rapid switching causes a voltage waveform with a very high dv/dt (rate of change in voltage) causing high EMI problems, reduced life expectancy of the motor and additional losses. So a power supply generating pure sinusoidal voltage waveform is very desirable. In industry some low pass filters called sinusoidal filters, are used at the output of the inverters but this comes with additional cost and bulky filter elements.

In this study, a novel approach for generating power level sinusoidal waveforms is proposed. The basic structure is a DC-DC converter that produces a

rectified DC-link at its output and an H-bridge inverter that inverts the rectified sinusoids to form a sinusoidal voltage. Main advantages of the circuit are that the H-bridge inverter switches have no switching stresses, they are switched at low frequency so the reliability is increased.

Throughout the study different circuit topologies have been investigated and the analysis of the chosen topologies is supported with computer simulations. The system is then set up in the laboratory. In order to prove of the concept, only a single phase inverter has been investigated at steady state conditions. Efficiency, distortion level, magnitude error and device stresses have been obtained. The results indicate that the proposed configuration is very promising.

Keywords: Pure Sinusoidal voltage waveform, complementary switching DC-DC buck converter, rectified DC-link.

ÖZ

GÜÇ SEVİYESİNDEKİ SİNÜS DALGA ŞEKİLLERİNİN SENTEZLENMESİNDE YENİ BİR YAKLAŞIM

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Değişken hızlı motor sürücüleri ve kesintisiz güç kaynakları, kısaca "yüksek frekanslı eviriciler", çıkış gerilimini oluşturmak için hızlı anahtarlama yapabilen transistörler (genellikle FET veya IGBT) kullanırlar. Bu anahtarlar çok ani açılıp kapanırlar ve bu işlem açık ve kapalı olmak üzere iki durumdan oluşur ve ara durumlar içermez. Bunun sonucu olarak bir dizi darbeden meydana gelen bir gerilim oluşur ve de eğer yük endüktif ise motora sinüs dalga şekilli bir akım akar. Voltaj geçişleri çok anidir. Bu ani anahtarlamalar çok yüksek dv/dt (gerilimdeki değişim oranı) ye sahip olan bir gerilim dalga şekli meydana getirir ki bu da yüksek elektromagnetik kirlilik, motor ömründe azalma ve ekstra kayıplara neden olur. Bunlardan kurtulmak için motor sürücüleri ve güç kaynaklarının çıkışlarında saf sinüs bir gerilim elde etmek gerekir.

Bu çalışmada sinüzoidal dalga şekilleri üretmek için yeni bir yaklaşım ortaya atıldı. çıkışı saf sinüzoidal dalga şekilleri olan ve böylece yüksek frekanslı elemanları

ve dv/dt problemlerini ortadan kaldıran bir üreteç fikri ortaya atıldı. Önerilen devre topolojisi iki bölümden oluşmaktadır. Giriş bölümü doğrultulmuş sinüs dalga şekilleri üretmekte, çıkış ise bunları evirip sinüsoidal bir dalga şekli üretmektedir. Bu tez çalışmasında değişik devre topolojileri araştırıldı ve seçilen topolojinin detaylı dizyn prosedürü ve bilgisayar simülasyonu sunuldu. Ayrıca sistem labaratuvarda kurularak çalıştırıldı ve teorik çalışmaların sonuçları deneylerle doğrulandı.

Anahtar Kelimeler: Saf sinüs dalga şekli, tamamlayıcı anhtarlayan DC-DC çevirici, Doğrultulmuş Doğru Akım Barası.

To My Family...

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TABLE OF CONTENTS

ABSTRACT.....iii
ÖZ.....v
ACKNOWLEDGMENTS.....vii
TABLE OF CONTENTS.....ix
LIST OF TABLES.....xiii
LIST OF FIGURES.....xiv
LIST OF SYMBOLS.....xviii

CHAPTER

1 INTRODUCTION..... 1
2 THEORETICAL STUDY.....6
2.1 General Overview of the Proposed System..... 6
2.2 Output Stage (Inverter Stage)..... 6
2.3 Input Stage 7
2.3.1 Determination of Suitable Topology for Input Stage..... 7
2.3.2 DC-DC Converter Basics..... 8
2.3.3 Step Down (Buck) Converter.....9
2.3.3.1 Continuous Conduction Mode..... 10
2.3.3.1.1 Mode 1: switch is on..... 10
2.3.3.1.2 Mode 1: switch is off..... 11
2.3.3.1.3 Steady-State Analysis and Volt-Second Balance on Inductor.....12
2.3.3.1.4 Output Voltage Ripple of Buck Converter for Continuous Conduction Mode (Approximate Analysis) 13

2.3.3.2 Boundary between Continuous and Discontinuous Conduction Modes..... 15
2.3.3.3 Discontinuous Conduction Mode..... 17
2.3.3.3.1 Subinterval 1: switch is on..... 18
2.3.3.3.2 Subinterval 2: switch is off..... 18
2.3.3.3.3 Subinterval 3: switch is off and inductor current is 0.....18
2.3.3.3.4 Steady-State Analysis and Volt-Second Balance on Inductor.....19
2.3.3.3.5 Output Voltage Ripple of the Buck Converter Operating in Discontinuous Conduction Mode.....20
2.4 Combination of Input and Output Stages..... 23
2.4.1 Analysis of the Basic Topology In Terms of Operating Conditions..... 24
2.4.2 Analysis of the Basic Topology In Terms of Load Types……..27
2.4.2.1 Feed Forward Control.....28
2.4.2.2 Closed Loop Control.....32
2.4.2.2.1 Determination of the Control Circuit Parameters Used for Closed loop Operation……...32
2.4.3 Modified Circuit Topology..... 39

3 DETERMINATION OF THE DC-DC CONVERTER PARAMETERS.....43
3.1 Introduction.....43
3.2 Inductance Design.....44
3.2.1 Inductance Design Software..... 46
3.2.2 Calculation of L_{max}, Possible With the Selected Core and Specifying the Inductance Value.....50
3.2.3 Calculation of Winding Loss..... 52
3.2.4 Calculation of Core Loss..... 52
3.2.5 Thermal Analysis..... 53
3.2.5.1 Thermal Resistance Due to Radiative Heat Transfer….. 54

3.2.5.2 Thermal Resistance Due To Convective Heat Transfer. 55
3.2.5.3 Temperature Rise in the Inductor..... 56
3.2.6 Specifying the Air gap Length..... 57
3.3. Determination of the Capacitance (Value and type)…….....60

4 HARDWARE AND SOFTWARE IMPLEMENTATION…….. 62
4.1 Introduction…….62
4.2 Hardware…….68
4.2.1 Power Stage of the Circuit…….. 69
4.2.2 Gate Driver and Protection Circuits……71
4.2.3 Voltage Sensing Circuit……. 74
4.2.4 The Controller ……..…… 75
4.3 Software…….. 77
4.4 Experimental Study and Verification of Theoretical Calculations……. 78
4.4.1 Experimental Results of Feed Forward Control Operation …….. 79
4.4.1.1 Experimental Results for No-Load Operation …..... 80
4.4.1.2 Experimental Results for Full load Operation ……..... 81
4.4.2 Experimental Results of Closed Loop Control Operation…….. 83
4.4.2.1 Experimental Results for No-Load Operation……. 84
4.4.2.2 Experimental Results for Full load Operation……. 85
4.4.3 Determination of the Level of the Minimum Achievable Voltage. 88
4.4.4 The Effect of Power Factor on Inverter Operation ……. ..89
4.4.5 Stresses on the Semiconductor Switch……92
4.4.6 Inductor Losses at 15000 Hz……...94
4.4.7 Sinusoidal Power Filters in the Market…….. 96
4.4.8 Conclusions…….96

5 CONCLUSION…….…… 98
5.1 General……...…….……98
5.2 Experimental Results…….. 100
5.3 Conclusion and Future Work…… 101

REFERENCES……103

APPENDIX A. DATA SHEETS OF THE COMPONENTS AND FULL PROGRAM CODES……..105

A.1 Flow Charts and Source Codes Written in C language.....106
A.2 Source Code of The Inductor Design Software.....114
A.3 Data Sheets of the Components.....115
A.4 Simulation model…….127
A.5 Determination of Suitable Topology for the Output Stage..... 128
A.5.1 Full Controlled Bridge Inverters..... 128
A.5.1.1 Topology One of the Full Controlled Bridge Inverter.. 129
A.5.1.2 Topology Two of the Full Controlled Bridge Inverter..129
A.5.1.3 Topology Three of the Full Controlled Bridge Inverter130
A.5.1.4 Topology Four of the Full Controlled Bridge Inverter..131
A.5.1.5 Topology Five of the Full Controlled Bridge Inverter..134
A.6 Sinusoidal Filters Available in the Market…….. 138

LIST OF TABLES

TABLE

3.1 Properties of Ferrite E shaped cores for medium power applications..... 44
3.2 Coefficients applied to core loss formula……..... 52
4.1 Performance Analysis for Feed Forward Control Operation……..83
4.2 Performance Analysis for Closed Control Operation…… 87
4.3 Performance Analysis at different Load power factor values…… 92
4.4 Expected and Measured Efficiency Values for Closed Loop Control Operation…..... 95
4.5 Physical Dimensions of the filter Inductors……96

LIST OF FIGURES

FIGURES

1.1 Full-rectified sinusoids…….....4
1.2 Sinusoidal waveform inverted from full-rectified sinusoids…….. 5
2.1 Full controlled H-Bridge inverter with back diodes (output stage)..…… 7
2.2 Output of the input stage…….. 7
2.3 Step Down (Buck) converter…… 9
2.4 Buck converter waveforms and circuit states…… 10
2.5 Equivalent circuit for switch is on…… 10
2.6 Equivalent circuit for switch is off…… 11
2.7 Inductor voltage..... 13
2.8 Actual Output Voltage Waveform of a Buck Converter..... 13
2.9 inductor current ripple(stored charge)..... 14
2.10 Inductor voltage and current waveforms at the boundary of continuous and discontinuous conduction..... 15
2.11 Converter characteristics with duty-cycle and load.....16
2.12 vL and iL waveforms with discontinuous conduction.....17
2.13 Switch is on (discontinuous conduction).....18
2.14 Switch is off (discontinuous conduction)..... 18
2.15 Switch is off, Inductor current is 0 (discontinuous conduction).....18
2.16 Converter characteristics with discontinuous conduction..... 20
2.17 Capacitor current waveform (stored charge)..... 20
2.18 Inductance current waveform for discontinuous conduction mode.....21
2.19 Basic circuit diagram of the overall system.....24
2.20 Circuit diagram for open loop analysis.....28
2.21 Output voltage for full resistive load with open loop control.....29

2.22 Harmonic Spectrum of the output voltage (open loop control, resistive load)..... 29
2.23 Output voltage for inductive load with open loop control.....30
2.24 Harmonic spectrum of the output voltage (open loop control, inductive load)..... 30
2.25 Buck converter inductor current for inductive load (open loop)..... 31
2.26 Buck converter inductor current for inductive load (open loop, magnified).....31
2.27 Circuit diagram for closed loop analysis…… 32
2.28 Type 2 compensated error amplifier (PI Controller)…..... 33
2.29 Frequency response of the uncompensated system…….. 34
2.30 Output voltage for full resistive load with closed loop control…… 35
2.31 Harmonic Spectrum of the output voltage (closed loop control, resistive load)…… 35
2.32 Output voltage for inductive load with closed loop control.....36
2.33 Output current for inductive load with closed loop control..... 36
2.34 Harmonic Spectrum of the output voltage and current (closed loop control, inductive load)…… 37
2.35 Output voltage and gate signal of the buck converter.....38
2.36 Modified Circuit Topology.....39
2.37 Output voltage and load current for inductive load with closed loop control..... 40
2.38 Harmonic Spectrum of output voltage and load current for inductive load with closed loop control..... 41
2.39 Inductance current (modified topology))..... 41
2.40 Inductance current (magnified version of Fig.2.60) (modified topology).42
3.1 Conventional Buck Converter.....43
3.2 Complementary Switching Buck Converter..... 44
3.3 Inductor current over one period.....47
3.4 Saturation flux density vs. temperature for P Material..... 48
3.5 Area Productand maximum inductance current vs.inductance.....49
3.6 Area Productand maximum inductance current vs.inductance (magnified)49

3.7 Area Product and I_{rms} versus Inductance……..... 50
3.8 Fringing fields in the air-gap of an inductor (a), effective cross-sectional area of the gap (b)……..... 57
3.9 Double E-core, its bobbin and an assembled inductor ……..... 58
3.10 Capacitance vs. Duty cycle for ΔV_o = 7V…… 61
4.1 Block diagram of the hardware setup..... 63
4.2 Input DC link and Filter Capacitors.....64
4.3.DC-DC Converter Power Stage (2MBI50N120 IGBT and Snubber Capacitance).....64
4.4 Output Inverter Power Stage (IRF 740 Mosfets).....65
4.5 DC-DC Converter IGBT Gate Drivers and Protection Circuit……...65
4.6 Output Inverter Mosfet Gate Driver Circuit..... 66
4.7 Voltage Sensing Circuit…….....66
4.8 TMS320LF2407A DSP Controller Circuit.....67
4.9 Experiment Setup.....67
4.10 Experiment Setup….....68
4.11 Power Stage of the Circuit.....69
4.12 Circuit schematic of the protection and gate driver circuit..... 73
4.13 Connection of the Voltage Sensing Circuit …….. 74
4.14 Schematic of the voltage Sensing Circuit …… 75
4.15 Basic flow-chart of the software for feed-forward control …….. 77
4.16 Basic flow-chart of the software for closed loop control …… 78
4.17 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 10 Hz. ……..80
4.18 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 50 Hz ……. 80
4.19 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 100 Hz…… 81
4.20 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 10 Hz …… 81
4.21 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 50 Hz……. 82

4.22 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 100 Hz ……82
4.23 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 10 Hz…….. 84
4.24 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 50 Hz …… …… 84
4.25 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 100 Hz ……85
4.26 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 10 Hz …… 85
4.27 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 50 Hz …….. 86
4.28 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 100 Hz ……..... 86
4.29 Input DC-Link capacitor current…….. 87
4.30 Constant V/f operation for 5 Hz. Upper waveform is load voltage and the lower one is rectified DC-link voltage …… 88
4.31 Constant V/f operation for 10 Hz.Upper waveform is load voltage and the lower one is rectified DC-link voltage ……. 88
4.32 Load Voltage and current at 1 kVA with pf = 0…… 90
4.33 Load Voltage and current at 1 kVA with pf = 0 …….. 90
4.34 Load Voltage and current at 1 kVA with pf = 0.8. ……. 91
4.35 Load Voltage and current at 1 kVA with pf = 1……..... .. 91
4.36 Voltage and Current on the DC-DC converter IGBT ……..92
4.37 IGBT Current for full load (1 kVA) at pf = 1……...93
4.38 IGBT Current for full load (1 kVA) at pf = 0.8……....93
4.39 Turn on and turn off characteristics of the DC-DC converter IGBT …… . 94
A.1 Flow Chart of the main program for open loop control……. 106
A.2 Flow Chart of the interrupt service routine for open loop control……..107
A.3 Flow Chart of the main program for closed loop control……... 108
A.4 Flow Chart of the interrupt service routine for closed loop control……109

A.5 Simulation Model.....127
A.6 First topology consists of four tyristors ……..129
A.7 Four anti-parallel diodes are added to topology one ……...129
A.8 Third topology consists of two tyristors and two transistors …….. 130
A.9 T1 and TR2 are turned on ……130
A.10 Load current closes its path through D2…….131
A.11 Fourth topology consists of four transistors…… 132
A.12 Anti-parallel diodes connected to topology shown in figure A.11…… 132
A.13 TR1 and TR4 are on……132
A.14 D2 and D3 are on…….. 133
A.15 TR2 and TR3 are on……133
A.16 D1 and D4 are on……134
A.17 Theoretical voltage and current waveforms indicating the operation modes for inductive load ……..134
A.18 Fifth topology consists of two transistors, two capacitors at the input 135
A.19 TR1 is on……135
A.20 D2 is on…… 136
A.21 TR2 is on……136
A.22 D1 is on…… 136
A.23 Theoretical voltage and current waveforms indicating the operation modes for inductive load……..137

LIST OF SYMBOLS

V_d	DC-DC Converter input voltage
V_o	DC-DC Converter output voltage
V_L	DC-DC Converter inductance voltage
i_L	DC-DC Converter inductance current
ton	Turn-on duration of the switch of the DC-DC Converter
toff	Turn-off duration of the switch of the DC-DC Converter
T_s	Switching period of the switch of the DC-DC Converter
f_s	Switching frequency
D	Duty cycle
ΔV	DC-DC Converter output voltage ripple
ΔQ	Stored charge on DC-DC Converter output capacitor
f_c	Cut-off frequency
I_{LB}	Average inductor current at boundry
I_{oB}	DC-DC converter output current at boundry
L	DC-DC Converter filter inductance
C	DC-DC Converter
$\hat{I}$	Maximum inductance current
N	Number of turns
$\hat{\Phi}$	Peak flux in the inductor
k_{cu}	Winding factor
A_w	effective winding area
A_{cu}	Conductor area.
A_{core}	effective core area
$\hat{B}$	Maximum flux density

I_{rms}	rms value of the inductor current
J_{rms}	rms current density
Z_o	DC-DC converter output impedance
AP	Area Product
B_{sat}	Saturation flux density
P_{Cu}	Copper loss
P_{core}	Core loss
V_{core}	core volume
$R_{\theta sa}$	Surface-to-ambient thermal resistance
$R_{\theta,rad}$	Radiative thermal resistance
$R_{\theta,conv}$	Convective thermal resistance
P_{rad}	Radiated power
P_{conv}	Heat power lost via convection
l_c	Magnetic flux path length in the core material
R_m	Total reluctance of the magnetic flux path

CHAPTER 1

INTRODUCTION

In variable-speed ac drives which utilize voltage-fed inverters, control of the voltage and frequency output of the inverter feeding the ac motor is essential for torque and speed control of the motor. Similarly in ac power supplies which utilize uninterruptible power supplies, again control of the output voltage and frequency of the supply feeding the load is essential for supplying regulated voltage to the load without any distortion. The early approach has been to use a voltage-fed square wave inverter fed by a variable DC voltage source. Variable DC voltage is required since the only way to change the fundamental voltage of a square-wave inverter is to change its amplitude. The variable DC-link voltage is obtained from a phase-controlled rectifier. This system has a big drawback. The output of a square-wave inverter contains high-amplitude low frequency harmonics. Therefore, the losses of a motor (in the case of a motor drive application) due to the resulting harmonic currents tend to be high.

With the recent developments in power electronic devices and controller circuits, different techniques have been developed called Pulse-Width Modulation (PWM) techniques, which carry the harmonics of the output voltage to higher frequency levels eliminating lower order harmonics. Also these techniques make possible both voltage and frequency control within the inverter itself. There are some advantages of these techniques. First, a variable DC-link is not essential. A PWM

inverter is usually fed by an uncontrolled diode bridge rectifier. Secondly, high amplitude low frequency harmonics are eliminated.

Various PWM strategies have been introduced for controlling inverters. The common principle in all these strategies is to introduce notches in the basic square-wave pole voltage, such that the resulting periodic waveform has the desired fundamental frequency and amplitude. [1]

PWM techniques can be classified into the following categories:

- Square-wave modulation
- The sampling method
- Optimized PWM
- Selected Harmonic Elimination
- Delta Modulation
- Space-vector based PWM

Beside the advantages of the PWM techniques, some drawbacks occur with the increasing frequency levels. The switches in the inverter are rapidly switched and are either turned hard ON or OFF with no in between state. The result is that the sine wave current is generated if the load is inductive by using pulse width modulated switching. However as discussed before the voltage wave form is a series of pulses in the output of the inverter, and the voltage transitions are very rapid. This rapid switching causes a voltage waveform with a very high dv/dt (rate of change in voltage).

In recent studies it has been proven that these pulses introduce some additional drawbacks to the system. First, the losses especially copper and core losses are increased. Secondly, in motor drive applications motors have parasitic capacitances of the electrically conducting components with respect to the ground potential. If the available DC voltage is chopped in the inverter, then, during the potential jumps of the voltage, considerable pulse currents flow across the parasitic capacitance's to the earth. If the grounding of the motor is inadequate, the potentials

at the parasitic capacitances increase sharply. The values of the bearing currents also increase massively, and flow fully through the bearings to the earth. In that case, the life expectancy of the ball bearings, and hence of the entire motor is reduced. Also the insulation of the motor is affected by these pulses. Thirdly, even the load current is sinusoidal, high dv/dt can cause high radiated energy causing EMC problems as well.

Under these circumstances, synthesizing a pure sinusoidal waveform at the output of the inverter seems to be an important concept and demand in order to further increase the performance of inverter-load systems.

With the developments in power electronic devices and magnetic materials a novel idea is proposed by the supervisor of this thesis in order to synthesize pure sinusoidal waveform. Basic idea is a DC-DC converter which can track a high frequency sinusoidal reference and create a DC bus of rectified sinusoids at desired frequency as shown in figure 1.1. By inverting the rectified sinusoids at the DC-DC converter's output, a pure sinusoidal output voltage can be obtained as shown in figure 1.2. An added advantage of this technique is that the input current can be also made sinusoidal without additional cost. Hence, injection of harmonic currents to the mains can be avoided.

Throughout this thesis study, proper topologies for DC-DC converter and the inverter part are analyzed in detail. Necessary basic theoretical information is given about the selected topologies. Some modifications made on topologies in order to improve the performance. Also detailed design procedures are given for the magnetic parts. Practical results are obtained in the laboratory environment.

Second chapter includes the choice of the best topologies necessary for the proposed idea. In this section some candidate topologies are examined and the chosen topologies are supplied with detailed theoretical background information. Also this chapter includes the integration of chosen topologies and computer

simulations. The modifications on the topologies and further computer simulations including different control approaches are given in chapter 2 as well.

In chapter 3, determination of DC-DC converter parameters are examined. This is followed by an evoluation of how the output filter parameters L, and C should be chosen.The inductance value and size minimization is specially emphasized, which has a vital role in our application. A computer program is developed in order to calculate the proper value of the inductor depending on the current and size parameters. Then thermal analysis of the inductor is given in order to guarantee the operation.

Chapter 4 includes the practical implementation of the proposed system. The hardware and control software are introduced in this chapter. Also detailed experimental results are given in this chapter.

Finally conclusions and proposals for future studies are given in chapter 5.

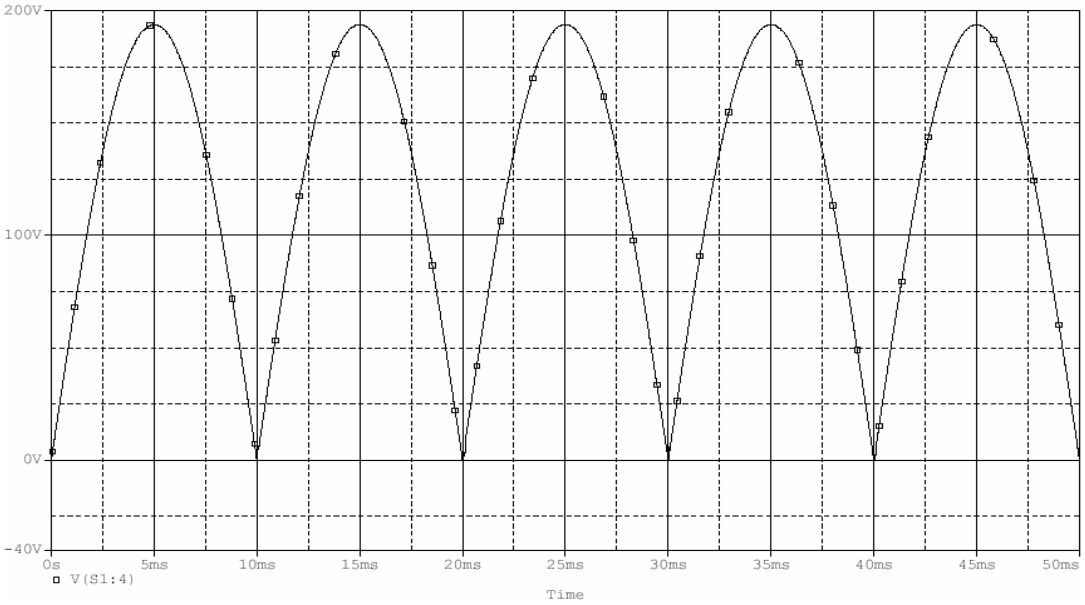

Fig.1.1 Full-rectified sinusoids

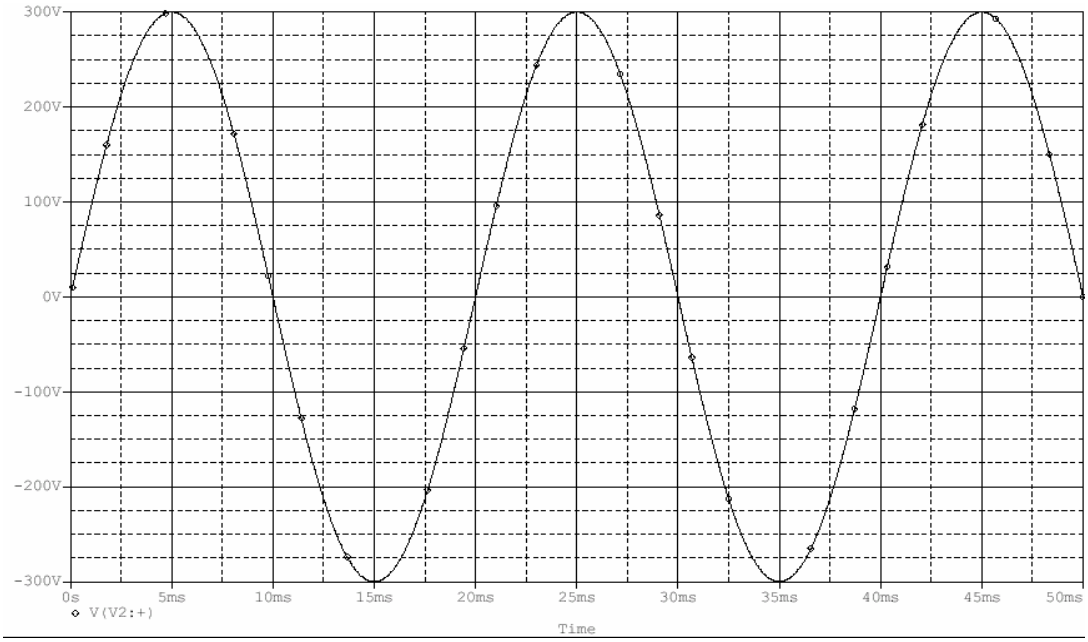

Figure.1.2 Sinusoidal waveform inverted from full-rectified sinusoids

CHAPTER 2

THEORETICAL STUDY

2.1 General Overview of the Proposed System

In chapter 1 the problem has been defined. As discussed in the introduction, the overall system is supposed to be composed of two discrete stages that are the input stage which generates rectified sinusoidal voltages in other words which produces a DC- link has a voltage waveform of rectified sinusoids that can be called as “Rectified DC-Link”. And the output stage that forms the sinusoidal output voltage from the rectified sinusoids in other words inverts the rectified sinusoids of the output of the first stage.

In this chapter, first of all the suitable circuit topologies for input and output stages are reviewed and analyzed.

Subsequently, integration of two discrete stages will be analyzed. At that section the drawbacks of the proposed basic circuit configuration will be given.

Consequently the modifications proposed on the circuit topology and their effects on the performance are investigated. Also detailed computer simulations of the resultant circuit will be examined.

2.2 Output Stage (Inverter Stage)

The inversion capabilities of different topologies, under two types of load

(purely resistive, inductive), are examined and detailed mode by mode analysis are given in Appendix A5. The chosen topology is given below

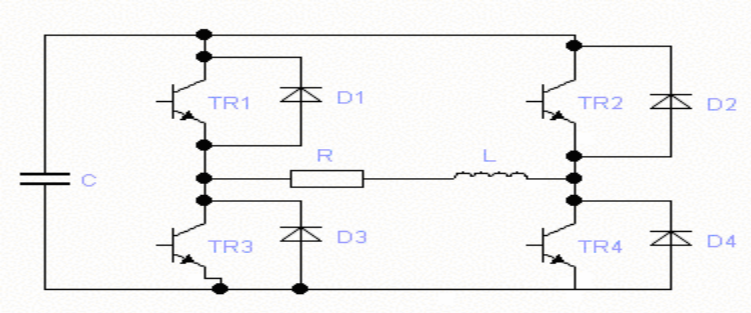

Figure 2.1 Full controlled H-Bridge inverter with back diodes (output stage)

2.3 Input Stage

In this section, the best and feasible topology for the input stage is determined and analyzed in detail.

2.3.1 Determination of Suitable Topology for the Input Stage

The input of the input stage is a constant DC bus voltage, and the output should be rectified sinusoidal voltage as shown in figure 2.2. Also the frequency and the magnitude of the output voltage should be variable. The output of this circuit is called as “Rectified DC-Link”

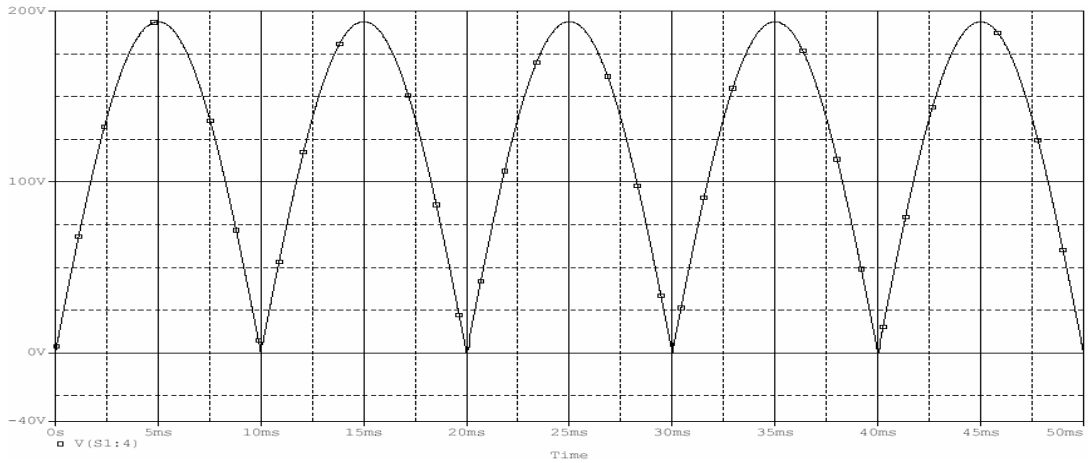

Figure 2.2 Output of the input stage (Rectified DC-Link voltage)

The waveform shown in figure 2.2 is a variable DC voltage waveform. So it can be said that both the input and the output of the circuit is DC quantities.

Consequently a DC-DC converter will be suitable for the application. But contrary to conventional operation of a DC-DC converter which operates in steady-state, the operation must be always in transient region for the proposed application. In another words, DC-DC converter should be operated to track a rectified sinusoidal reference voltage, but not a constant one as usual.

Due to its simplicity and linearity, in this thesis, a DC-DC step down (buck) converter is chosen as the input stage of the overall topology. It has the advantage of linear input output voltage relation and also has the ability of control the voltage down to 0 volts as well. Detailed information about DC-DC converters focusing on the step down (buck) type is given in the next section.

2.3.2 DC-DC Converter Basics

A DC-to-DC converter is a device that accepts a DC input voltage and produces a DC output voltage. Typically the output produced is at a different voltage level than the input.[2,3]

Two alternatives for delivery of electric power from a dc source to a load in a controllable manner are linear and switched mode power conversion.

Linear power conversion relies on the presence of a series linear element, especially a semiconductor device used in the linear region such that the total load current passes through the linear element. Therefore, the greater the difference between the input and the output voltages, the more power is lost in the element. So this type of conversion is very dissipative and inefficient.

In switched mode power conversion, the controlling device is a switch which is either closed or open. By controlling the duty cycle, the power flow to the load can be controlled in a very efficient way. The only losses may be the element losses(semiconductor, inductor and capacitor). However, the output voltage is not a pure dc

as in the linear case, and pulsed power is delivered to the load. The power flow to the load may be easily smoothed out by implementing a low-pass LC filter.

2.3.3 Step Down (Buck) Converter

The basics of the single quadrant buck converter is given in [2,3] in detail. In this section only brief information and necessary equations are given also some equations which are not available in the literature such as output voltage ripple equations for discontinuous conduction mode.

The simplest configuration of the converter is given in the figure 2.3 below.

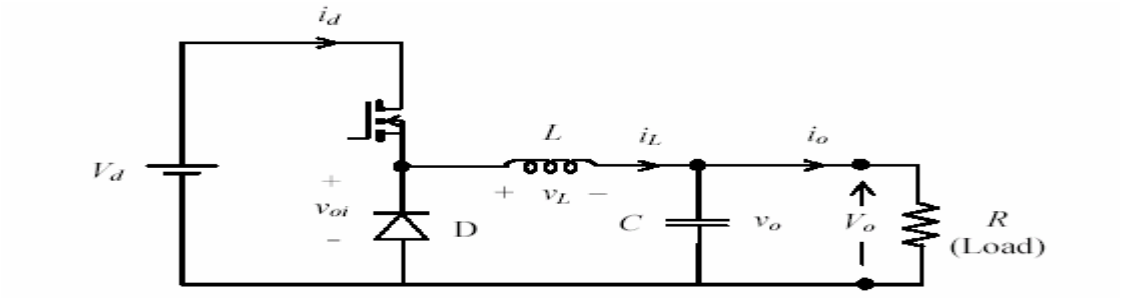

Figure2.3 Step Down (Buck) converter

During $0 < t < t_{on}$, voltage across the inductor L is $V_d - V_o$; i_L rises to I_{Lmax}. During $ton < t < T_s$, voltage across the inductor L is $-V_o$, and i_L falls to I_{Lmin}. In the steady state, the inductor current must return to I_{Lmin} at the end of the switching period T_s, and the integral of the inductor voltage (i.e., the dc voltage supported across the inductor) must be zero. In the following we assume that the output voltage ripple is negligible.

Depending on the inductor current waveform, the operation of the step down (buck) converter will be examined in 2 different modes. These are:

- Continuous Conduction Mode
- Discontinuous Conduction Mode

2.3.3.1 Continuous Conduction Mode

For continuous conduction mode of operation, there are two circuit states as shown in figure 2.4. The circuit is analyzed mode-by-mode for continuous conduction mode.

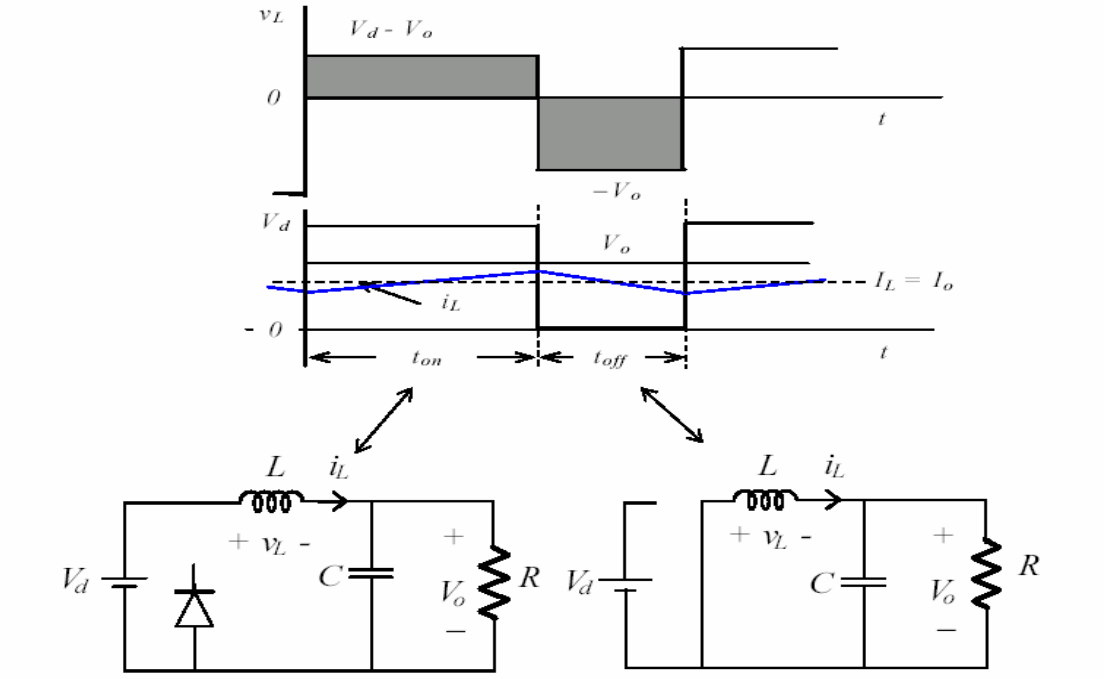

Figure 2.4. Buck converter waveforms and circuit states

2.3.3.1.1 Mode 1: switch is on

The equivalent circuit diagram is shown in Figure2.5

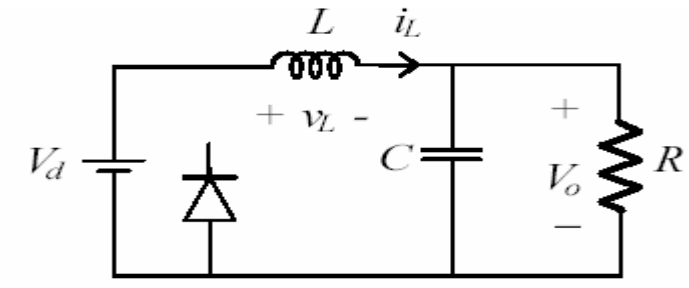

Figure 2.5 Equivalent circuit for switch is on

Inductor voltage

$$v_L(t) = V_d - v_o(t) \quad 2.1$$

Small ripple approximation

$$v_L(t) \approx V_d - V_o \quad 2.2$$

Knowing the inductor voltage, now the inductor current can be found via Faraday's Law

$$v_L(t) = L\frac{di_L(t)}{dt} \quad 2.3$$

Solve for the slope of the inductor current:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} \approx \frac{V_d - V_o}{L} \quad 2.4$$

2.3.3.1.2 Mode 2: switch is off

The equivalent circuit diagram is shown in Figure2.6

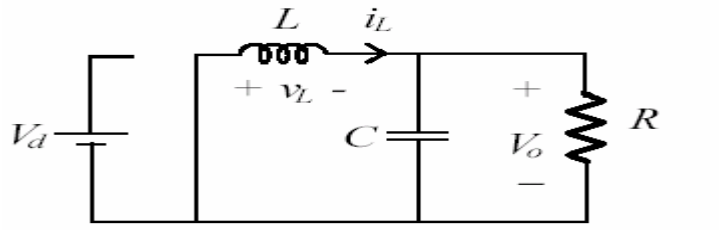

Figure 2.6.Equivalent circuit for switch is off

Inductor voltage

$$v_L(t) = -v_o(t) \quad 2.5$$

Small ripple approximation

$$v_L(t) \approx -V_o \quad 2.6$$

Knowing the inductor voltage, we can again find the inductor current via

$$v_L(t) = L\frac{di_L(t)}{dt} \Rightarrow \frac{di_L(t)}{dt} \approx -\frac{V_o}{L} \qquad 2.7$$

2.3.3.1.3 Steady-State Analysis and Volt-Second Balance on Inductor

From Faraday's law for the inductor voltage,

$$v_L(t) = L\frac{di_L(t)}{dt} \qquad 2.8$$

Integrating over one complete switching period:

$$i_L(T_s) - i_L(0) = \frac{1}{L}\int_0^{T_s} v_L(t)dt \qquad 2.9$$

In periodic steady state, the net change in inductor current is zero

$$0 = \int_0^{T_s} v_L(t)dt \qquad 2.10$$

Hence, the total area (or volt-seconds) under the inductor voltage waveform, shown in figure 2.7, is zero whenever the converter operates in steady state. An equivalent form

$$0 = \frac{1}{T_s}\int_0^{T_s} v_L(t)dt = \langle v_L \rangle \qquad 2.11$$

The average inductor voltage for one cycle is zero at steady state. Using this statement and figure 2.7

$$(V_d - V_o)\, D\, Ts = V_d\,(1\text{-}D)\, Ts \quad \Rightarrow \quad \frac{V_o}{V_d} = D \qquad 2.12$$

Eq 2.12 equation is called the conversion ratio equation for continuous conduction mode.

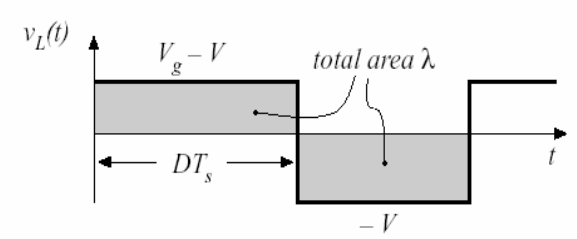

Figure 2.7. Inductor voltage

In ideal cases, voltage control range of a buck converter operating in continuous conduction mode, is from 0 V to V_d.

2.3.3.1.4 Output Voltage Ripple of Buck Converter for Continuous Conduction Mode (Approximate Analysis)

Actually the output of a buck converter is not a pure DC voltage. It has a small ripple on a DC component as shown in figure 2.8. In order to calculate the switching output voltage ripple ΔV, it is assumed that the inductor current ripple Δi_L flows into the output capacitor to generate the voltage ripple. The total voltage ripple ΔV is obtained from the stored charge ΔQ, which is the area under inductor current ripple as shown in figure 2.9

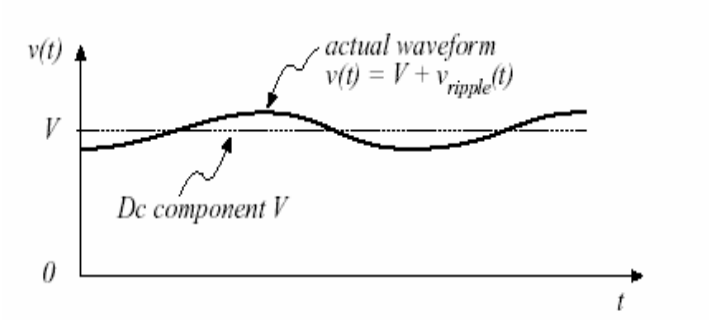

Figure 2.8. Actual Output Voltage Waveform of a Buck Converter

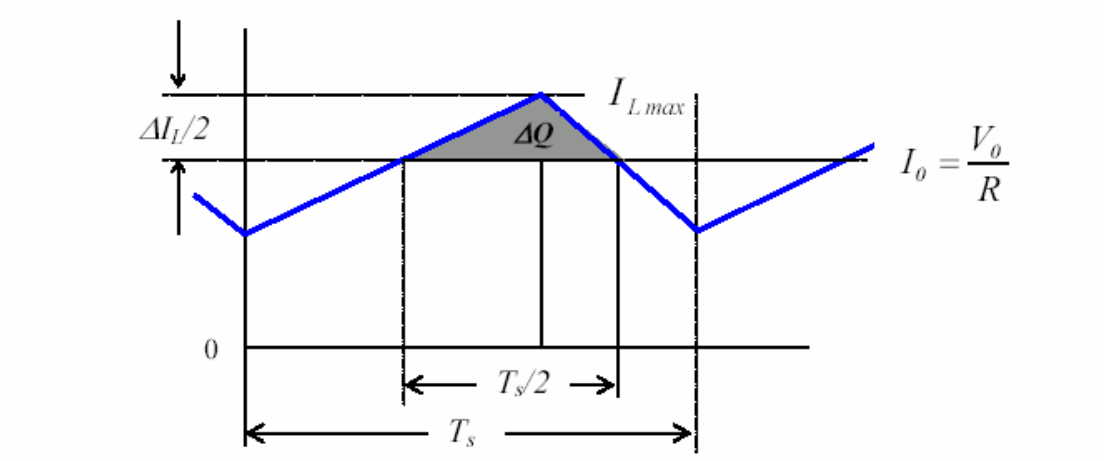

Figure 2.9. inductor current ripple(stored charge)

Hence,

$$\Delta Q = \frac{1}{2}\frac{Ts}{2}\frac{\Delta i_L}{2} = \frac{1}{8}Ts\Delta i_L, \qquad 2.13$$

$$\Delta V_O = \frac{\Delta Q}{C} = \frac{1}{C}\frac{1}{8}Ts\Delta i_L, \qquad 2.14$$

$$\Delta i_L = \frac{Vo}{L}(1-D)Ts \qquad 2.15$$

$$\Delta V_O = \frac{Ts}{8C}\frac{Vo}{L}(1-D)Ts \Rightarrow \frac{\Delta V_O}{Vo} = \frac{1}{8}\frac{Ts^2(1-D)}{LC} = \frac{1}{8}\frac{(1-D)}{LCf_s^{\,2}} \qquad 2.16$$

Eq. 2.16 can also be expressed in terms of switching and cut-off frequencies as,

$$\frac{\Delta V_O}{Vo} = \frac{\pi^2}{2}(1-D)\left(\frac{fc}{fs}\right)^2 \qquad 2.17$$

where fs = 1/Ts and

$$fc = \frac{1}{2\pi\sqrt{LC}} \qquad 2.18$$

The output voltage ripple can be minimized if fs >> fc. Also it is obviously seen that the output voltage ripple of a buck converter operating in continuous conduction mode, is independent from load. It is only a function of constant parameters such as L, C, f_s, and D.

2.3.3.2 Boundary between Continuous and Discontinuous Conduction Modes

In this section, the boundary condition for the inductor current is investigated. Figure 2.10 shows this condition for inductor current and voltage.

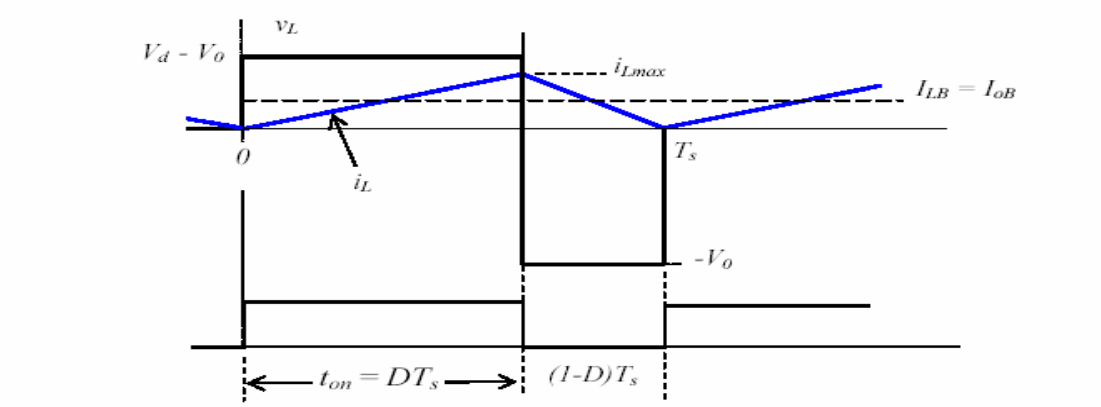

Figure 2.10. Inductor voltage and current waveforms at the boundary of continuous and discontinuous conduction.

From figure 2.10, average inductor current I_{LB}, where subscript B refers to the boundary, is found as a function of duty cycle as,

$$I_{LB} = \frac{1}{2} i_{L\max} = \frac{1}{2} \frac{V_d - V_O}{L} t_{on} = I_{oB} \qquad 2.19$$

$$= \frac{DT_s}{2L}(V_d - V_O) = \frac{DT_s}{2L}(V_d - DV_d) = \frac{T_s V_d D(1-D)}{2L} \qquad 2.20$$

I_{LB} becomes maximum when D = 0.5 (this is found by differentiating I_{LB} with respect to D and equating the derivative to zero). For D = 0.5,

$$I_{LB\max} = \frac{T_s V_d}{8L} \qquad 2.21$$

And,

$$I_{LB} = 4 I_{LB\max} D(1-D) \qquad 2.22$$

Using Eq. 2.21 and 2.22 I_{LB} loci for duty cycles between 0-1 can be plotted as shown in figure 2.11

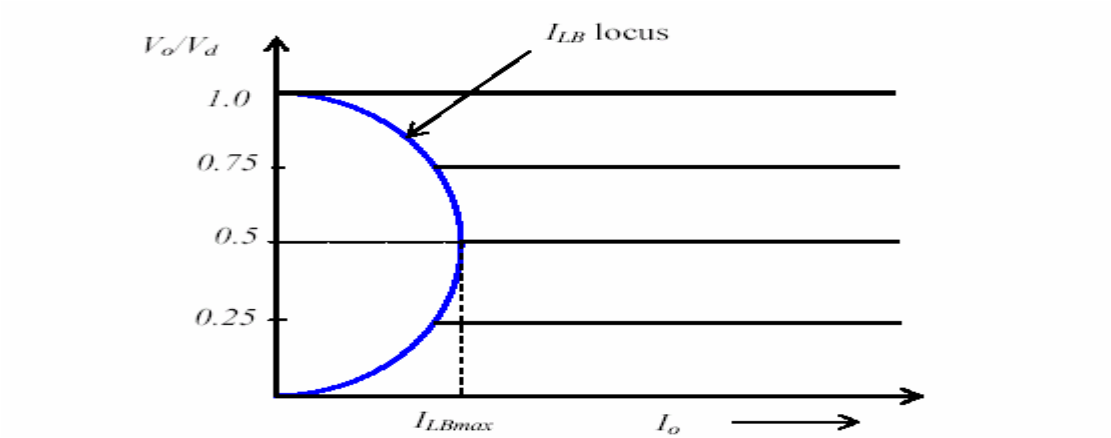

Figure 2.11.Converter characteristics with duty-cycle and load

During normal operation, I_{LB} should be smaller than the lowest load current, so that the converter operates in continuous conduction mode (i.e., in the linear mode with Vo = DVd). The minimum inductance L and the switching frequency f_s for this condition of operation are obtained from the following consideration. In periodic steady state, the net change in inductor current is zero

$$\int_0^{T_s} \frac{v_L}{L} dt = \int_{(0)}^{(T_s)} di = 0 \qquad 2.23$$

$$\frac{V_d - V_o}{L} DT_s - \frac{V_o}{L}(1-D)T_s = 0 \qquad 2.24$$

The first term in Eq.2.24 is $.i_L$ (rise) and the second term is $.i_L$ (fall). For a given load resistance R,

$$i_{L\max} = \frac{V_o}{R} + \frac{\Delta i_L}{2} = \frac{V_o}{R} + \frac{V_o}{2L}(1-D)T_s \qquad 2.25$$

$$i_{L\min} = \frac{V_o}{R} - \frac{\Delta i_L}{2} = \frac{V_o}{R} - \frac{V_o}{2L}(1-D)T_s \qquad 2.26$$

At the boundary of continuous-discontinuous conduction, $i_{Lmin} = 0$, so that

$$(Lf_s)_{\min} = \frac{(1-D)R}{2} \qquad 2.27$$

Hence, for continuous conduction,

$$Lf_s \geq \frac{(1-D)R}{2} \qquad 2.28$$

2.3.3.3 Discontinuous Conduction Mode

In practice load current may change over a wide range, from no load to full load. Increase of load resistance leads to a decrease of load current. Hence a new operation region is encountered, termed discontinuous conduction mode. The load current and consequently the inductor current cheases before the next cycle begins. Inductor current and voltage waveform is shown in figure 2.12.

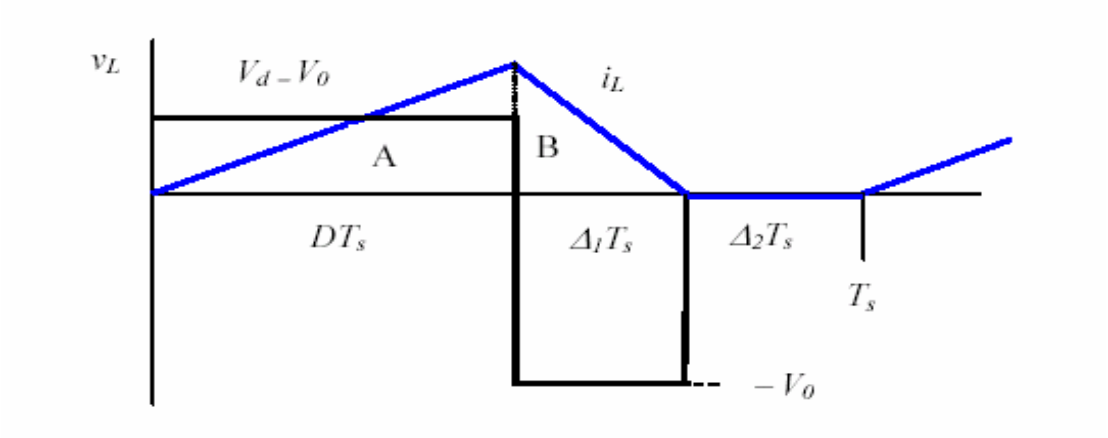

Figure 2.12 vL and iL waveforms with discontinuous conduction.

For discontinuous conduction mode of operation, there are three circuit states as shown in figure 2.13, 2.14, and 2.15.

2.3.3.3.1 Subinterval 1: switch is on

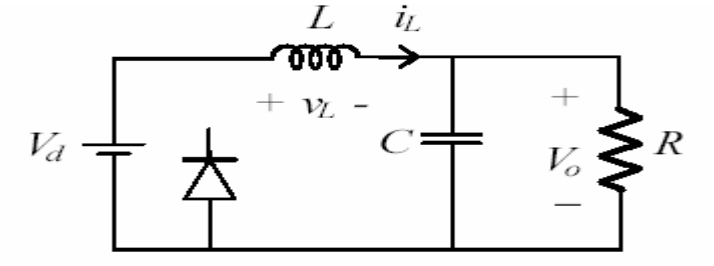

Figure 2.13 Switch is on (discontinuous conduction)

2.3.3.3.2 Subinterval 2: switch is off

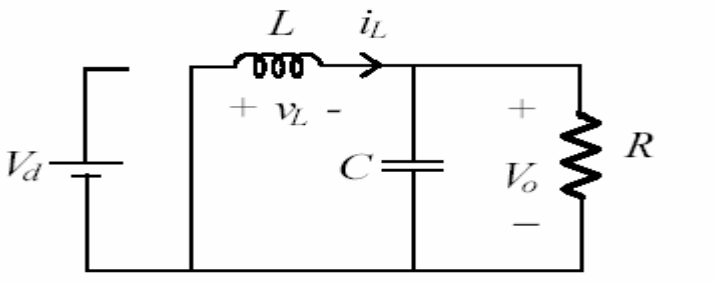

Figure 2.14 Switch is off (discontinuous conduction)

2.3.3.3.3 Subinterval 3: switch is off and inductor current is 0

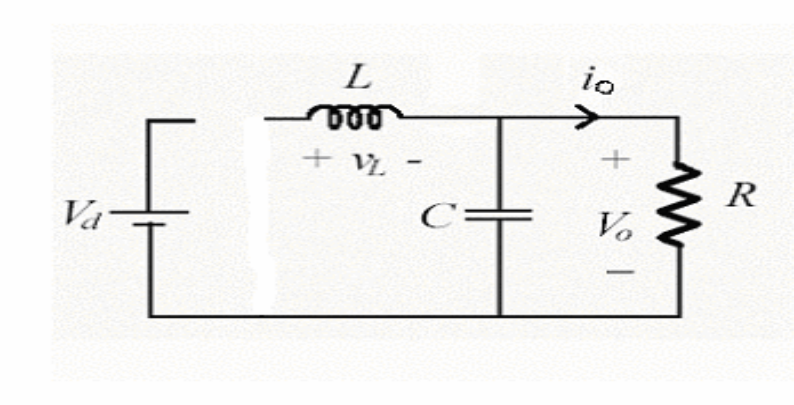

Figure 2.15 Switch is off, Inductor current is 0 (discontinuous conduction)

2.3.3.3.4 Steady-State Analysis and Volt-Second Balance on Inductor

The average inductor voltage for one cycle is zero at steady state. Using this statement and Fig 2.12

$$(V_d - V_o)DT_s - V_o\Delta_1 T_s = 0 \tag{2.29}$$

Thus input output voltage relationship becomes

$$\frac{V_o}{V_d} = \frac{D}{D+\Delta_1} \tag{2.30}$$

Where $D + \Delta_1 < 1$. Now

$$i_{L\max} = \frac{V_o}{L}\Delta_1 T_s \tag{2.31}$$

And,

$$I_o = \frac{\left\{ i_{L\max}\frac{DT_s}{2} + i_{L\max}\frac{\Delta_1 T_s}{2} \right\}}{T_s} = i_{L\max}\frac{(D+\Delta 1)}{2} \tag{2.32}$$

Using Eq.2.31

$$= \frac{V_o}{L}\Delta 1 T_s \frac{D+\Delta_1}{2} \tag{2.33}$$

Using Eq.2.30

$$= \frac{V_d}{L}\frac{D}{D+\Delta_1} \times \Delta_1 T_s \times \frac{D+\Delta_1}{2} \tag{2.34}$$

$$= \frac{V_d}{2L} T_s D\Delta_1 \tag{2.35}$$

Using Eq. 2.21

$$= 4I_{LB\max} D\Delta_1 \tag{2.36}$$

$$\Delta_1 = \frac{I_o}{4I_{LB\max} D} \tag{2.37}$$

Using Eq.2.30

$$\frac{V_o}{V_d} = \frac{D^2}{D^2 + \frac{1}{4}\left(I_o / I_{LB\max}\right)} \qquad 2.38$$

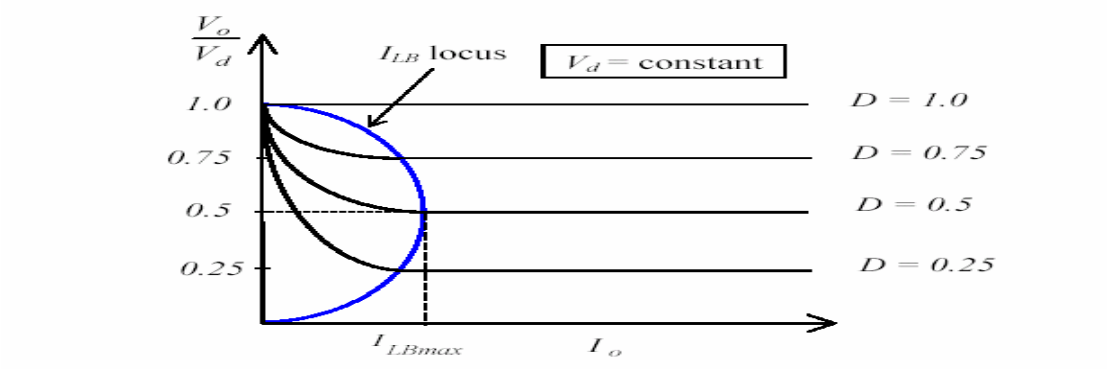

Figure 2.16 Converter characteristics with discontinuous conduction.

Note that V_o falls sharply with load when the inductor current is discontinuous. Note also that with discontinuous conduction, the V_o/V_d ratio becomes higher than D, implying loss of voltage gain of the converter.

2.3.3.3.5 Output Voltage Ripple of the Buck Converter Operating in Discontinuous Conduction Mode

The same approach followed for Continuous Conduction mode of operation is applicable for discontinuous conduction mode of operation. The total voltage ripple ΔV is obtained from the stored charge ΔQ, which is the area under inductor current ripple as shown in figure 2.17

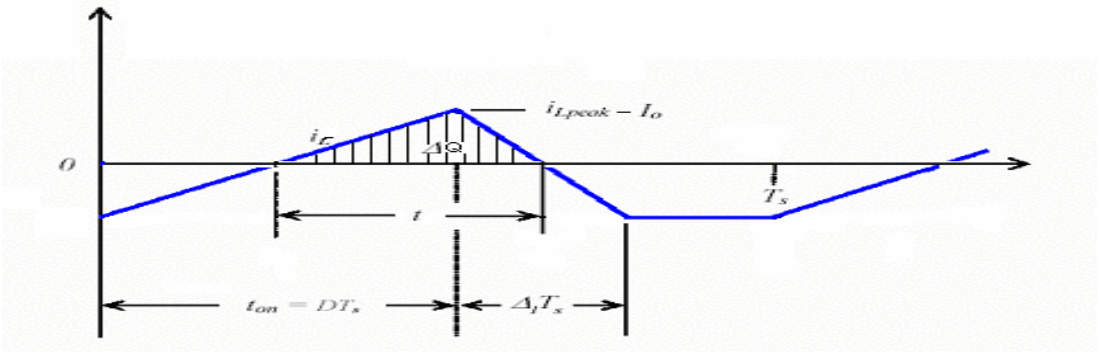

Figure 2.17. Capacitor current waveform (stored charge)

$$\Delta Q = C\,\Delta V_o = \frac{t(I_{peak} - I_O)}{2} \qquad 2.39$$

$$(I_{peak} - I_o) = \left(\frac{(V_s - V_O)DT}{L} - I_O\right) = \frac{(V_S - V_O)DT - I_O L}{L} \qquad 2.40$$

Time t can be calculated from inductance current waveform given in figure 2.18

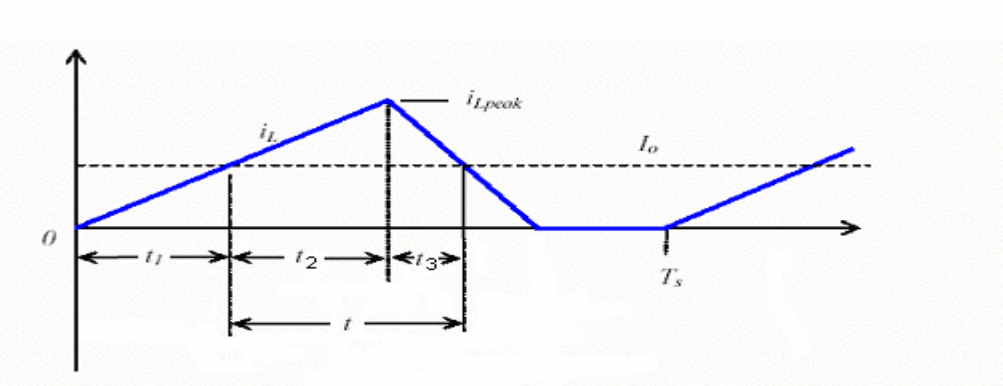

Figure 2.18 Inductance current waveform for discontinuous conduction mode

$$t = t_2 + t_3, \qquad 2.41$$

And

$$t_2 = DT - t_1 \qquad 2.42$$

By using the slope of the inductance current for $t < t_2$

$$\left(\frac{V_S - V_O}{L}\right) t_1 = I_O \qquad 2.43$$

Yields,

$$t_1 = \left(\frac{I_O L}{V_s - V_O}\right) \qquad 2.44$$

Thus using Eq. 2.42

$$t_2 = DT - \left(\frac{I_O}{V_S - V_O} \right) \tag{2.45}$$

On the other hand using the slope of the inductance current waveform for $t > t_3$,

$$I_{peak} - t_3 \frac{V_O}{L} = I_O \tag{2.46}$$

I_{peak} can be expressed as,

$$\left(\frac{V_S - V_O}{L} \right) DT - t_3 \frac{V_O}{L} = I_O \tag{2.47}$$

Therefore,

$$t_3 = \left(\frac{V_S - V_O}{V_O} \right) DT - \frac{LI_O}{V_O} \tag{2.48}$$

Using Eqs. 2.42, 2.44 and 2.48 in Eq. 2.41 yields,

$$t = DT - \left(\frac{I_O L}{V_S - V_O} \right) + \left(\frac{(V_S - V_O)}{V_O} \right) DT - \frac{LI_O}{V_O} \tag{2.49}$$

Finally using Eq.2.49 in Eq.2.39 gives

$$C\Delta V_O = \left[\frac{[DT(V_S - V_O) - LI_O][DT(V_S - V_O)V_O - LI_O V_O + [(V_S - V_O)(DT(V_S - V_O) - LI_O)]]}{2LV_O(V_S - V_O)} \right] \tag{2.50}$$

Thus the output voltage ripple is expressed as

$$\Delta V_O = \left[\frac{[DT(V_S - V_O) - LI_O][DT(V_S - V_O)V_O - LI_O V_O + [(V_S - V_O)(DT(V_S - V_O) - LI_O)]]}{2LCV_O(V_S - V_O)} \right] \tag{2.51}$$

It is obviously seen from equations 2.38 and 2.51 that both buck converter's input output voltage relationship and output voltage ripple functions are depending on load. This has some disadvantages in terms of both control of the converter output

voltage and also selection of the circuit parameters especially the output filter capacitor for specific applications.

2.4 Combination of Input and Output Stages

In this section, the two discrete circuits, which are the buck converter and the H-bridge inverter, are connected together to form a sinusoidal wave shape and the performance of the resultant circuit will be investigated.

As discussed in previous sections, input stage will generate rectified sinusoids and the output stage will invert this waveform. And also proper circuit topologies have been determined that can separately do necessary operations. This section of the study investigates the combinational operation of discrete stages and will analyze the effects of each stage on the other. If necessary, modifications will be proposed.

Performance of the combined circuit will be investigated in terms of

- Operating conditions of the DC-DC converter filter inductance (continuous and discontinuous conduction modes)

- Under load conditions (resistive and inductive load)

During the analysis of the DC-DC filter inductance operating conditions, minimum inductance values will be calculated which satisfy the continuous conduction mode of operation. With these values necessary comments will be done for the performance of the system.

For the load analysis, first of all feed forward control for DC-DC converter will be analyzed. Than if necessary closed loop control will be applied to the system. For all load analysis, system performance will be evaluated by output voltage FFT (Fast Fourier Transform) results and also THD (Total Harmonic Distortion) of the output voltage.

During the analysis, the parameters that is calculated for the filter elements (capacitor and inductor) in chapter 3, is used in foregoing analysis in this section. L = 950 μH and C = 10 μF.

The basic proposed topology of the circuit is shown in figure 2.19. The maximum output power and voltage of the system is desired to be 1kVA and 220 V_{rms} respectively. Full load current is approximately 4.5 A. So for full load, load impedance is approximately 50Ω.

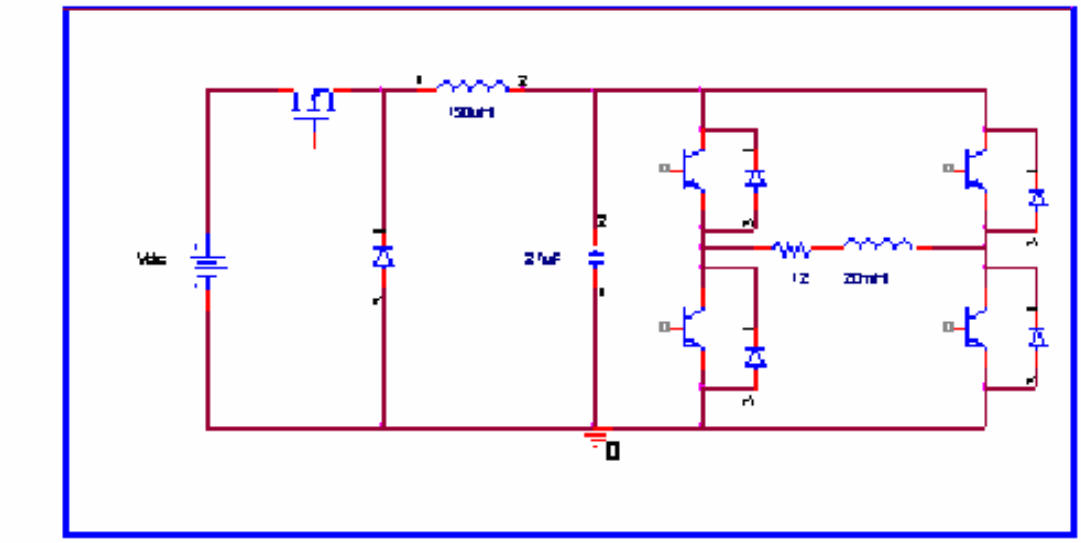

Figure 2.19 Basic circuit diagram of the overall system

2.4.1 Analysis of the Operating Conditions of the DC-DC Converter Filter Inductance

In this section the operating conditions of the buck converter used in our application will be examined. The circuit will be analyzed whether it operates in continuous conduction mode or in discontinuous conduction mode.

As discussed before the output voltage of the DC-DC Converter used in this thesis, is supposed to be rectified sinusoidal voltages. In other words, the amplitude of this voltage is changing between 0 and $V_{out,peak}$. Thus, duty cycle is changing between 0 and D_{max}.

Boundary operation condition (boundary condition between continuous and discontinuous inductor current) for a buck converter is given by equation 2.28

$$Lf_s \geq \frac{(1-D)R}{2}$$

Maximum output power of the circuit is desired to be in the range 750VA - 1 KVA. Maximum Output Voltage is 311 V_{peak}, 220V_{rms}. For an input voltage of 530 V_{dc}, Dmax ≅ 0.6, f_s = 15.000 Hz.

So the minimum inductance that satisfies continuous conduction mode for an output voltage of 310V_{peak} and for full load impedance (50Ω) is

$$L_{\min,fullload,D=0.6} \cong \frac{(1-0.6)50}{30000} \Rightarrow L_{\min} \cong 670\mu H$$

In our application, even if the circuit operates at full load, and at maximum operating voltage, the inductance value is just satisfies the necessary condition for continuous inductor current just for the higher instantaneous voltages of the sinus curve. Because as it is said before the actual inductance value is 950 μH (calculated in chapter 3).

As the output voltage is sinusoidal and in one cycle its magnitude already changes between 0 and 310 at rated conditions. That mean duty cycle gets a value of range 0-0.6.

For voltage values near 0, let's say D ≅ 0.1, then again for full load, the minimum inductance value necessary for continuous conduction operation is,

$$L_{\min,fullload,D=0.1} \cong \frac{(1-0.1)50}{30000} \Rightarrow L \cong 1.5mH$$

Consequently it is obvious that even if the output voltage is max (220 V_{rms}), and the circuit operates at full load, the inductor current is essentially both continuous and discontinuous in one period, in our application.

The equations for a buck converter show that, for discontinuous operation mode, the system is nonlinear in terms of input-output voltage relationship as shown in equation 2.30. As a result of this nonlinearity, two problems occur.

- Proper voltage regulation can not be achieved with linear control techniques such as PI control. Because, as it is discussed in DC-DC buck converter basics, for discontinuous conduction mode of operation, the circuit is out of control of the switches as the inductor current vanishes, as was shown in figure 2.36. There will be no switching in this period and the variation of the output voltage is directly proportional with the time constant of the output capacitor and the load. Thus the system is operates in this region uncontrollably with its own nature.

- Secondly, the output voltage ripple relation with the converter operating characteristics must be analyzed especially for determining the value of the output filter capacitance of the DC-DC buck converter.

For continuous conduction mode of operation, the output voltage ripple is given by Eq.2.16 as

$$\Delta V_O = \frac{(1-D)V_O}{8CLf_s^{\,2}}$$

Solving Eq.2.16 for C gives,

$$C = \frac{(1-D)V_O}{\Delta V_O 8Lf_s^{\,2}}$$

For constant values of DC-DC converter input voltage, inductance, switching frequency, and for a specified value of output voltage ripple, capacitance value can be determined as a function of duty cycle, independent of the load and if the highest possible value of the inductance is chosen, the desired low output voltage ripple level will be guarantied.

On the other hand, for continuous conduction mode of operation, the output voltage ripple is given by Eq.2.51 as

$$\Delta V_O = \left[\frac{[DT(V_S - V_O) - LI_O][DT(V_S - V_O)V_O - LI_O V_O + [(V_S - V_O)(DT(V_S - V_O) - LI_O)]]}{2LCV_O(V_S - V_O)} \right] \quad 2.51$$

Solving Eq.2.51 for C gives,

$$C = \left[\frac{[DT(V_S - V_O) - LI_O][DT(V_S - V_O)V_O - LI_O V_O + [(V_S - V_O)(DT(V_S - V_O) - LI_O)]]}{\Delta V_O 2LV_O(V_S - V_O)} \right] \quad 2.52$$

As it is seen in Eq.2.52, capacitance value is dependent to the load. As a result of this for specified circuit parameters it is impossible to obtain constant output voltage ripple for dynamic loads. Such as in the application in this thesis, output voltage is always varying to form rectified sinusoidal wave shape so it always operates in transient region. Therefore discontinuous conduction mode is undesirable.

2.4.2 Analysis of the Proposed Circuit under Load Conditions

The analysis is done with ORCAD's PSpice version 9.2 [5]. Throughout the simulations, non-ideal (actual) semiconductor switches and diodes are used for buck converter and H-bridge inverter. In closed loop control case, an analog PI controller is used composed of analog comparators. In order to prevent convergence problems of the analysis, small series resistances added to the passive elements as discussed in [5, 22]. Simulation model is given in appendix A.4

The system is first simulated using feed-forward control. A reference voltage that is rectified sinusoids is applied to the buck converter and then the signal at the output of the buck converter is inverted by the output stage.

Secondly the system is simulated using closed loop control by taking feedback from the output of the buck converter. The output voltage of the buck converter is compared with the reference and the error is applied to a PI controller. The output of the controller is applied to the buck converter.

Load analysis is done at rated output voltage and at full load (Load impedance = 50Ω) conditions.

2.4.2.1 Feed-Forward Control

The schematic of the simulated circuit with open loop control is shown in figure 2.20 below. Firstly the resistive load and then inductive load is used in the simulations.

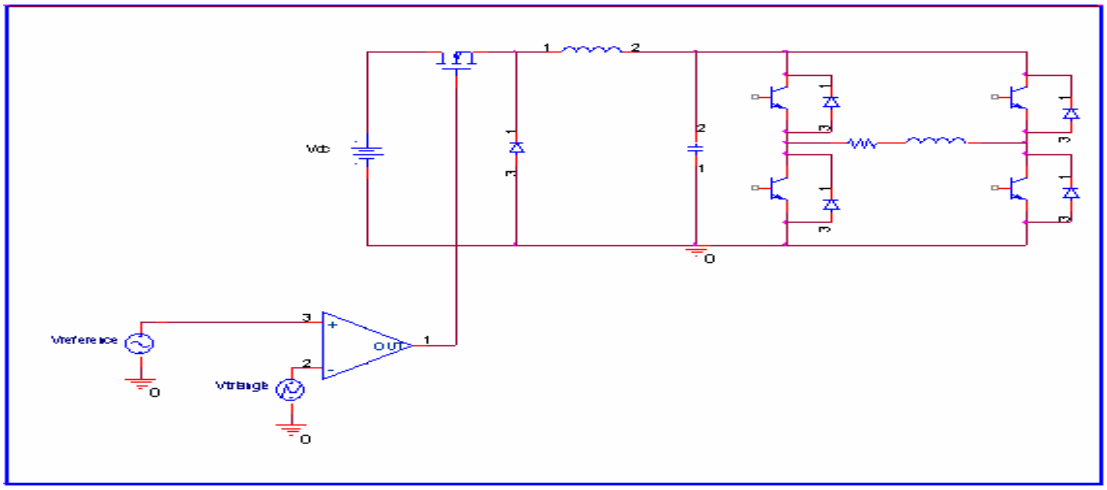

Figure 2.20 Circuit diagram for open loop analysis

The input of the circuit is rectified line voltage of 530V DC. Output is desired to be $220V_{rms}$, 50 Hz, sinusoidal voltage without any low or high frequency harmonics.

For a rectified sinusoidal reference voltage (feed-forward control) and for a purely resistive load of 50Ω, the output voltage of the system for one period is shown in figure 2.21

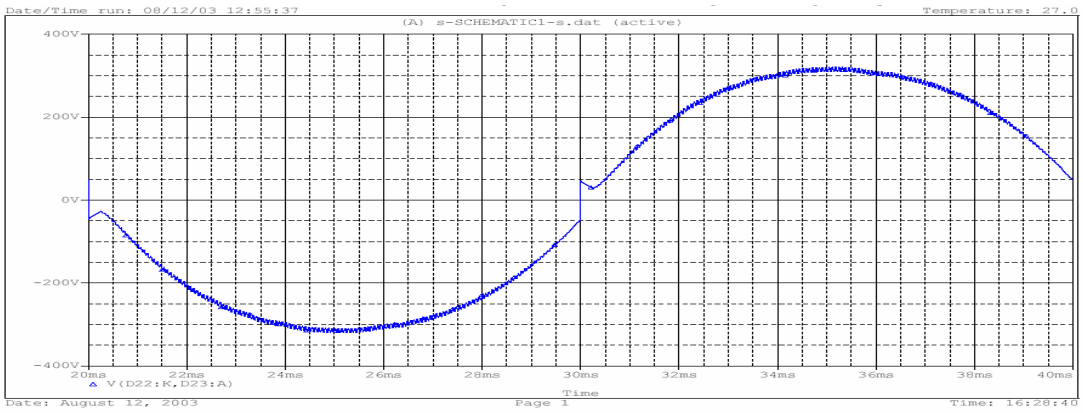

Figure 2.21 Output voltage for full resistive load with open loop control

It is seen from the figure that, for purely resistive load, the output voltage tends to follow the reference sinusoidal input voltage. But it is obvious that the response of the system is not very well at lower voltage regions depending on the circuit dynamics. The harmonic diagram is shown in the figure 2.22. The representation of FFT in PSpice 9.0 is in the form of triangles with only their peak values indicate the amplitude of related harmonics. THD of the waveform shown in figure 2.21 is calculated approximately 11.37%.

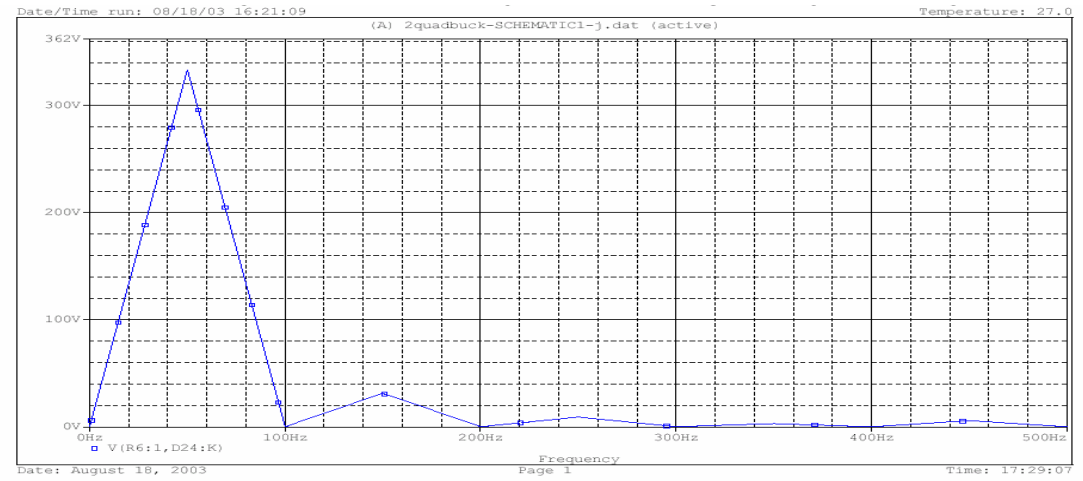

Figure 2.22 Harmonic Spectrum of the output voltage (open loop control, resistive load).

The system shown in figure 2.20 is now simulated for inductive load. The load is now a combination of resistance and an inductance and is specified as $50\angle 20^\circ$ during the simulations.

The simulation has been run for inductive load and results are obtained. Output voltage and harmonic spectrum of the system with open loop control and with inductive load, is shown in Figs.2.23 and 2.24 respectively.

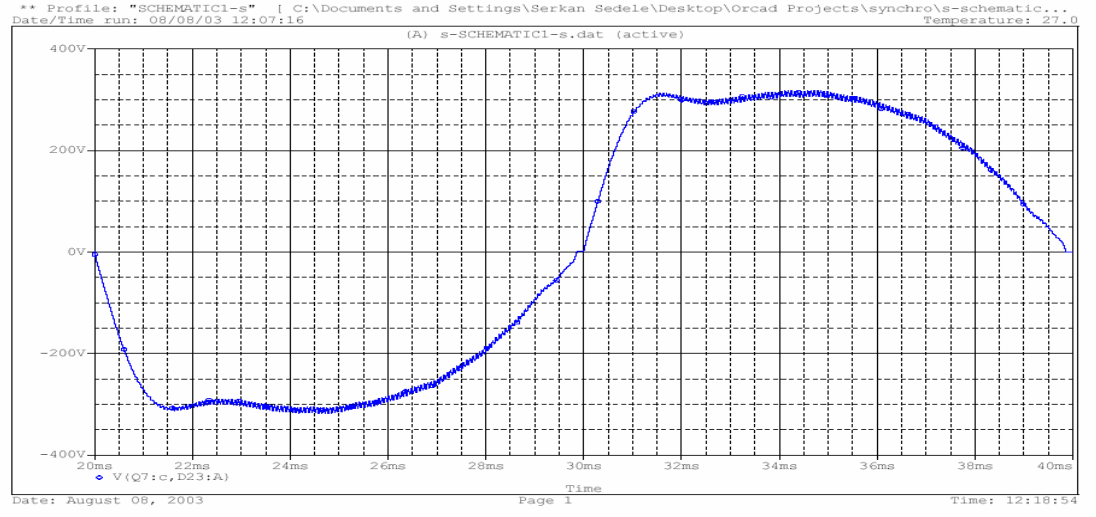

Figure 2.23 Output voltage for inductive load with open loop control

As it is seen in figure 2.23, the output voltage is far from being sinusoidal. As the load becomes inductive, a distortion occurs on the output voltage of the buck converter due to the inductive current flowing back to the capacitor. This phenomenon was discussed in section A.5.1.4 (choosing the best topology for output stage). Harmonic spectrum is shown in figure 2.24. THD of the waveform shown in figure 2.23 is calculated approximately 19.5%.

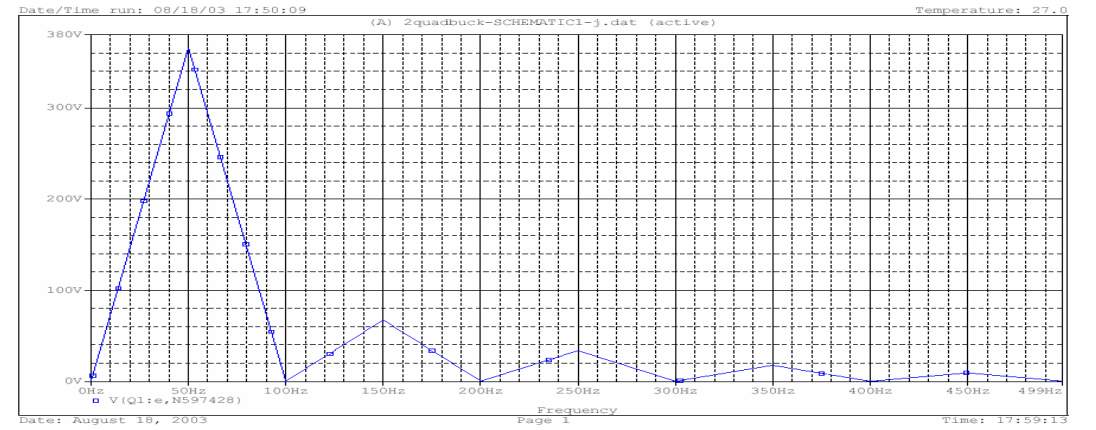

Figure 2.24 Harmonic Spectrum of the output voltage (open loop control, inductive load).

The inductor current for one period is shown in figure 2.25. Also a magnified version of figure 2.25 is given in figure 2.26. These waveforms show that the inductor current is both continuous and discontinuous in one period of operation.

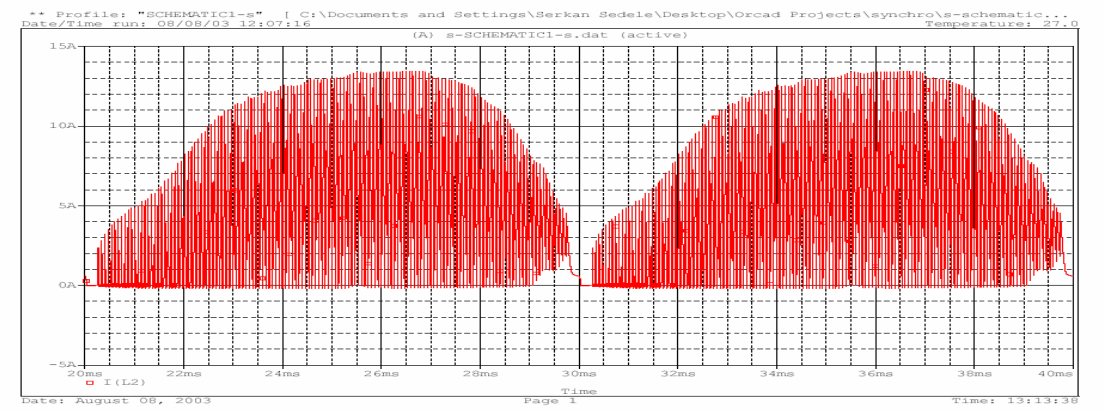

Figure 2.25 Buck Converter Inductor current for inductive load (open loop)

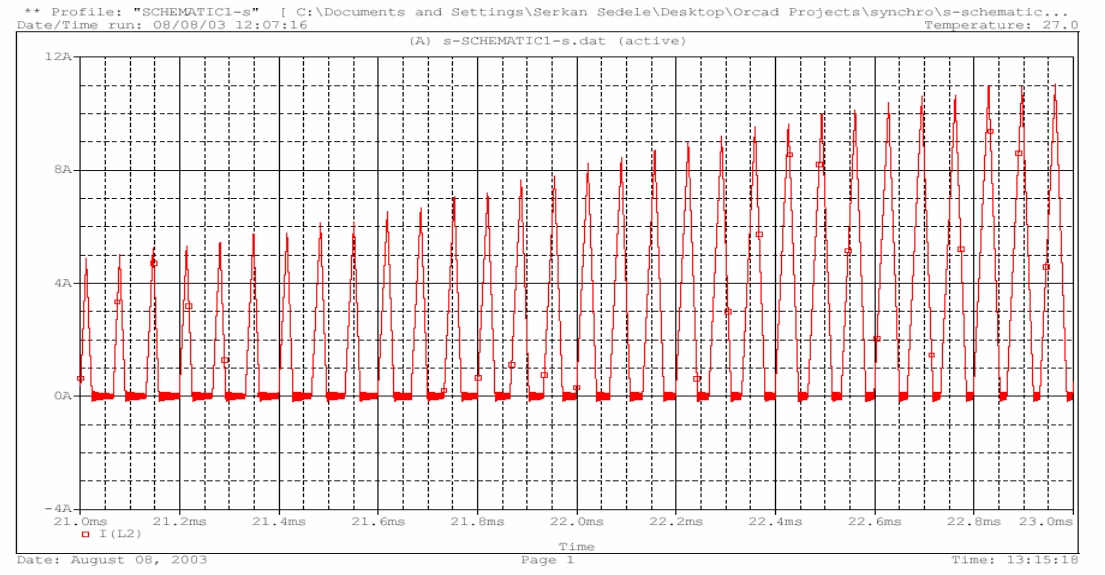

Figure 2.26 Buck Converter Inductor current for inductive load (open loop) Magnified.

Output voltages include lower order harmonics for both load types as seen in figures 2.22 and 2.24 resulting from inadequate dynamic response and in addition the distortion for inductive load case.

Another disadvantage of the open loop is poor voltage regulation capability resulting from the voltage drops of the semiconductor switches.

2.4.2.2 Closed Loop Control

As a result of the feed-forward control technique gave unsatisfactory results, closed loop control is decided to be used in order to regulate the output voltage. Voltage feed-back is taken from the output filter capacitance of the DC-DC converter. Circuit schematic is shown in figure 2.27. System is again first simulated for resistive load and than for inductive load.

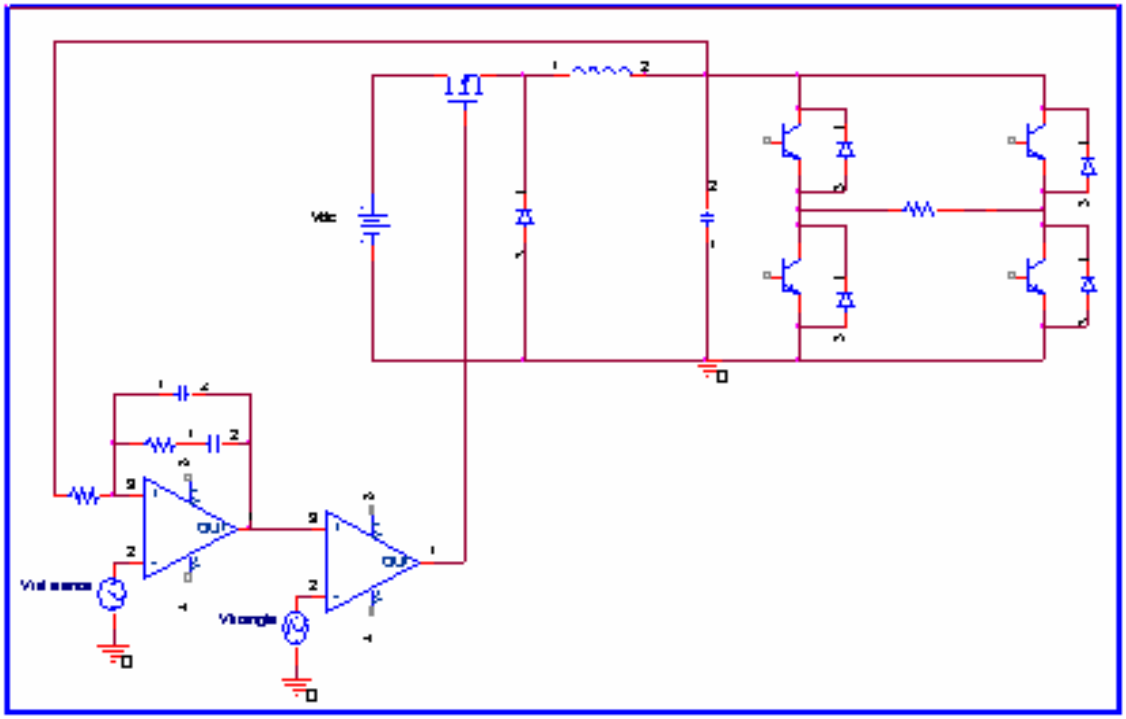

Figure 2.27 Circuit diagram for closed loop analysis

2.4.2.2.1 Determination of the Control Circuit Parameters Used for Closed loop Operation

The buck converter output capacitor voltage, should track the reference voltage which is full-rectified sinusoids. So the capacitor voltage and the reference voltage are compared. Then the error is compensated by PI controller. An amplifier circuit used as PI regulator is shown in figure 2.28. The control signal is then applied to a PWM generator and the resultant signals become the switching signals of the buck converter's controllable switch. Determination of control circuit parameters for

a buck converter is discussed in [21] in detail. The foregoing analysis for the control circuit design is taken from [21].

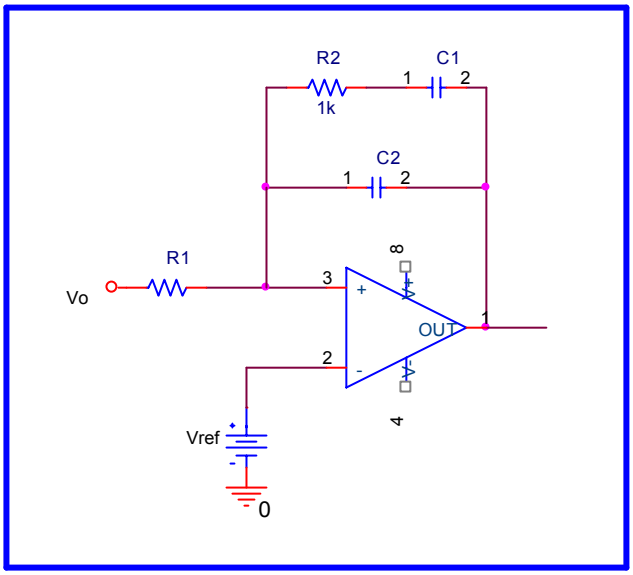

Figure 2.28 Type 2 compensated error amplifier (PI Controller)

In order to determine the controller parameters, transfer function of the overall system must be obtained from the small signal averaged circuit. The transfer function is given in [21, 2} by Eq.2.52

$$\frac{Vo(s)}{Vc(s)} = \frac{Vs}{Vp \times L \times C}\left[\frac{1 + sr_c C}{s^2 + s\left(\frac{1}{|X_L| \times C} + \frac{r_c + r_L}{L}\right) + \frac{1}{L \times C}}\right] \qquad 2.52$$

The crossover frequency can be calculated using the DC-DC converter inductance and the capacitance values in Eq.2.18 as

$$fc = \frac{1}{2\pi\sqrt{950 \times 10^{-6} \times 10 \times 10^{-6}}} = 1650Hz$$

The frequency characteristics of the system is obtained with MATLAB as

shown in figure 2.29

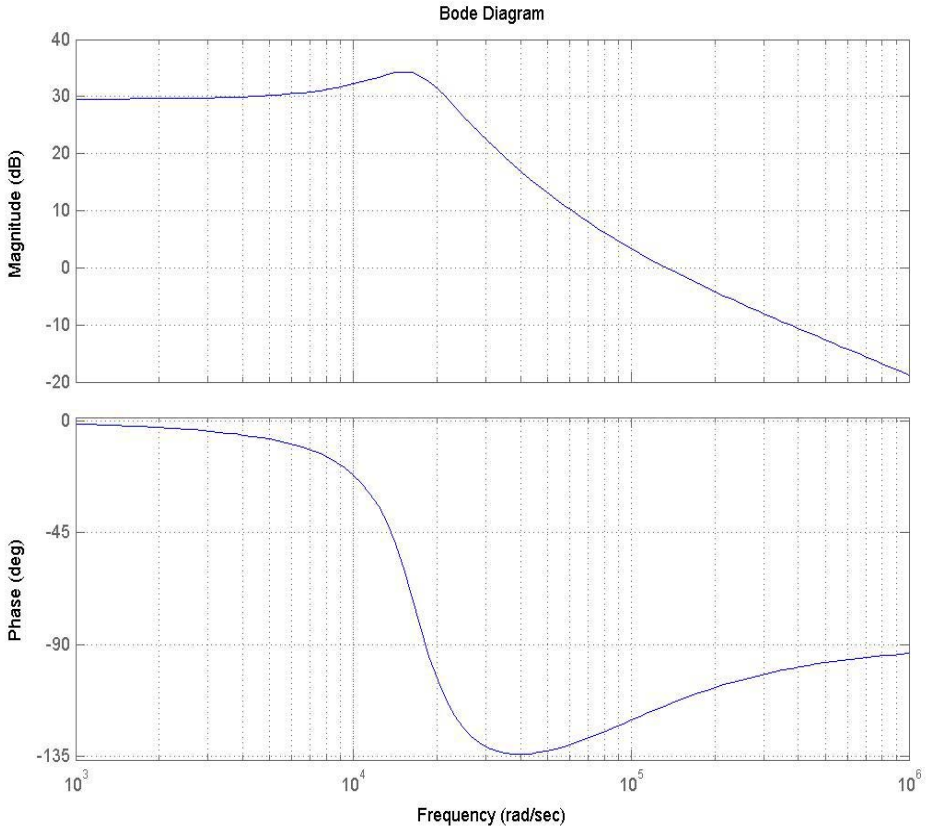

Figure 2.29 Frequency response of the uncompensated system.

From the bode diagram it is seen that, the system gain at 1.65 kHz (10367 rad/s) is 4 dB with a phase angle of -120°. The compensated error amplifier should have a gain of -4 dB at 1.65 kHz in order to make the loop gain 0 dB. Also phase margin is adjusted to be ≅ 46° in order to assure the stability [2, 21]

Therefore the resistance and the capacitance values of the compensated error amplifier shown in figure 2.28 are obtained as, R1= 1kΩ, R2= 6kΩ, C1=8nF, C2=1nF [21]

Using these parameters, the simulation has been run and results are obtained. Output voltage and harmonic spectrum of the system with closed loop control and purely resistive load is shown in Figs.2.30 and 2.31 respectively.

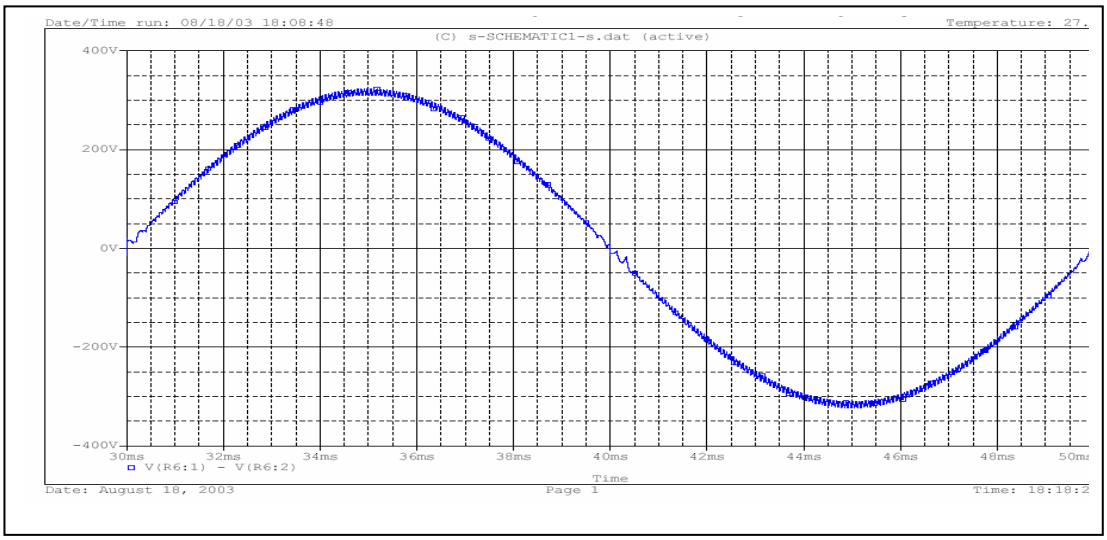

Figure 2.30. Output voltage for full resistive load with closed loop control

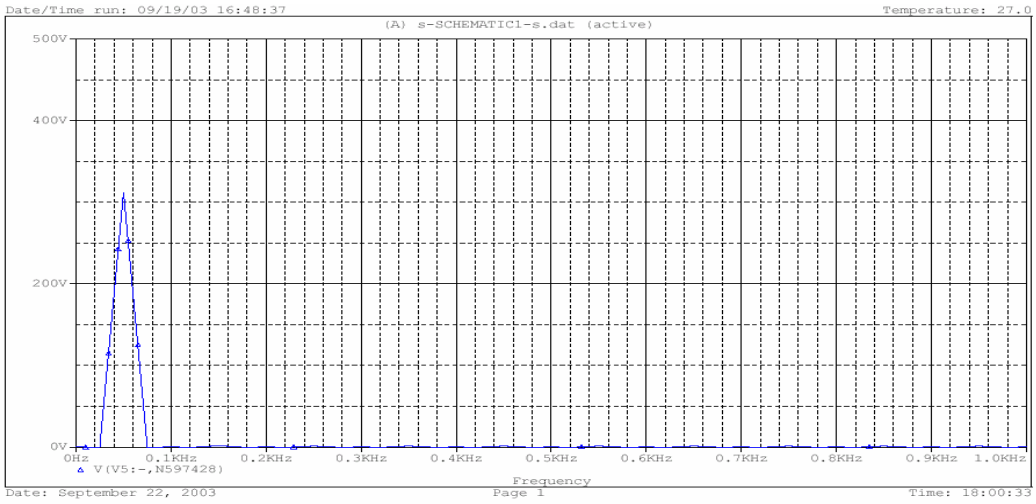

Figure 2.31 Harmonic Spectrum of the output voltage (closed loop control, resistive load).

For purely resistive load, THD of the waveform shown in figure 2.30 is calculated as 1.78%.

The system is now simulated for inductive load. The load is now a combination of resistance and an inductance and is specified as $50\angle 20^\circ$ during the simulations.

The simulation has been run and results are obtained. Output voltage, output current and harmonic spectrum of the system with closed loop control and with inductive load, is shown in Figs.2.32, 2.33 and 2.34 respectively.

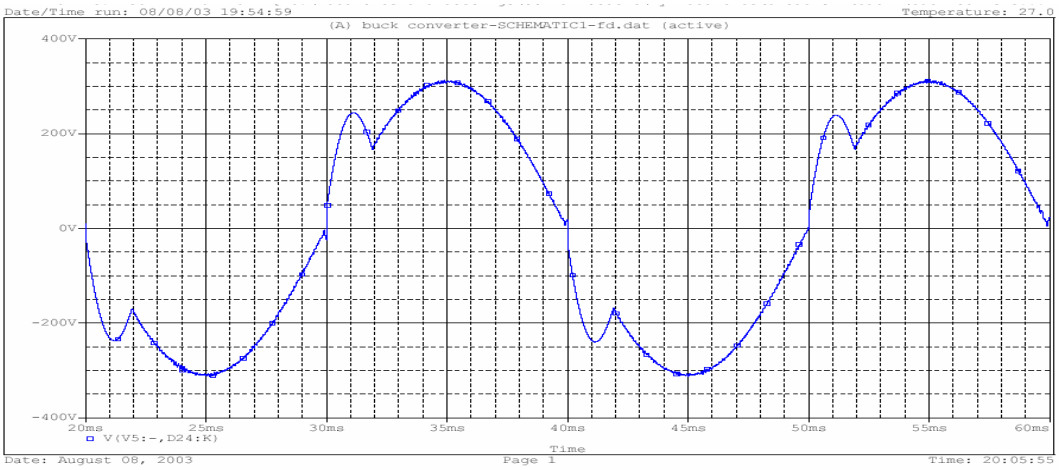

Figure 2.32 Output voltage for inductive load with closed loop control

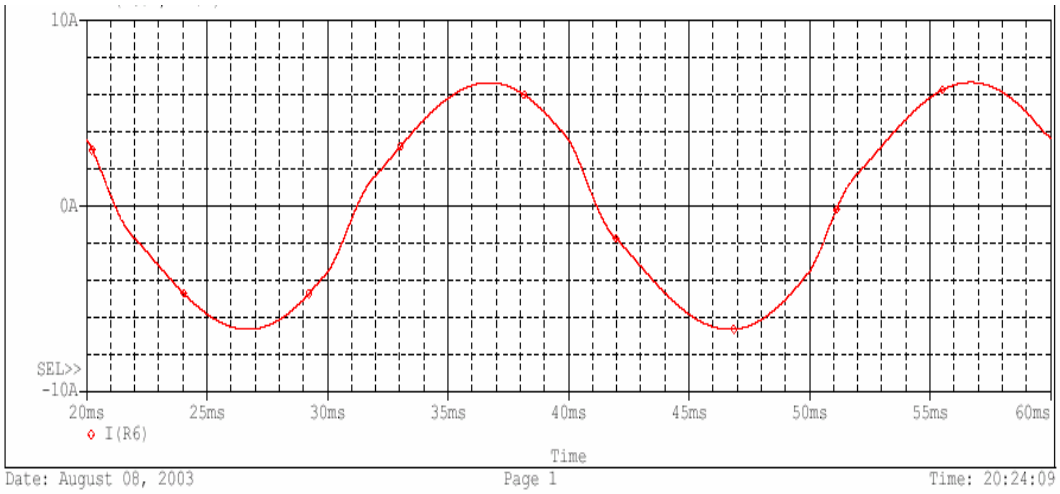

Figure 2.33 Output current for inductive load with closed loop control

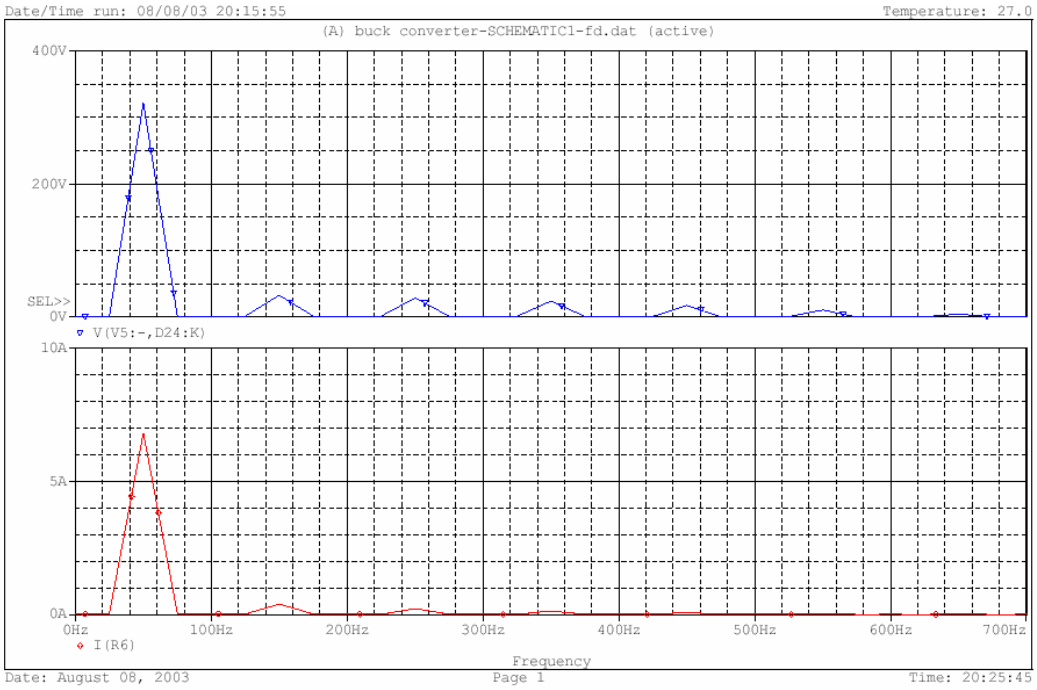

Figure 2.34 Harmonic Spectrum of the output voltage and current (closed loop control, inductive load).

The distortion of the voltage is reduced but still exists in serious levels. During reactive current flowing, the control circuit turns off the switch at the DC-DC converter as shown in figure 2.35 but this could not be sufficient to suppress the over voltage. In figure 2.35, upper waveform in blue is output voltage, and the lower waveform in red is gate signals of the switch of the DC-DC converter.

THD of the waveform shown in figure 2.32 (output voltage), is calculated as 10%.

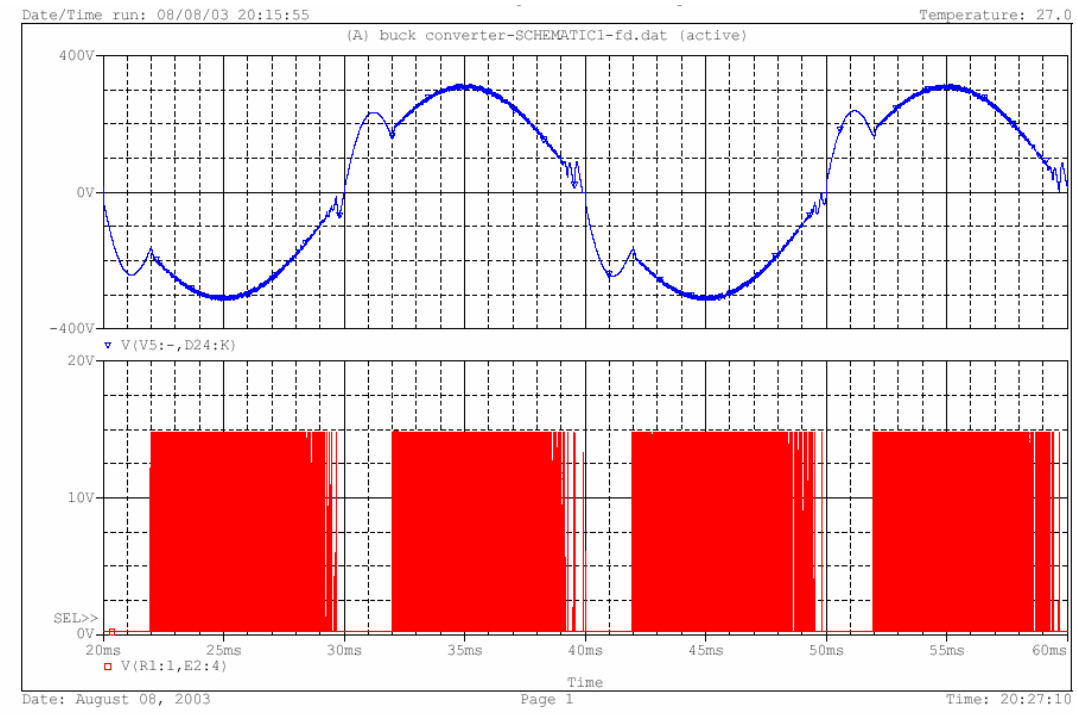

Figure 2.35 Output voltage and gate signal of the buck converter for closed loop control and inductive load.

To sum up, the simulations show that the reactive current distorts the sinusoidal shape of the output voltage. It was expected that, the closed loop control circuit would solve this problem. But even with the feed-back control, the overcharge could not be removed but decreased to a lower value than that obtained with open loop control, as shown in figure 2.32.

The problem is the nonlinear reactive current flowing through the capacitor, pumping up the capacitor voltage beyond the reference voltage.

The solution must be to provide an alternative path to the reactive current to prevent the over voltage on the capacitor. This can be done by some modifications on the conventional buck converter topology.

As conclusion, it is obvious that the proposed circuit topology is not sufficient especially for inductive loads and also for control point of view it is undesirable to operate the circuit in discontinuous conduction mode.

The inverter part works properly but DC-DC buck converter part fails. The next section is devoted to solving this problem and a modified circuit topology for the DC-DC converter is proposed.

2.4.3 Modified Circuit Topology

Two main drawbacks of the proposed system are defined in the previous section.

- The distortion of the "rectified DC-link" voltage.
- Control Complexity for discontinuous conduction mode.

The circuit called complementary switching Buck Converter or two quadrant Buck Converter or so-called Synchronous Buck Rectifier is supposed to solve these two problems. The circuit schematic is shown in figure 2.36

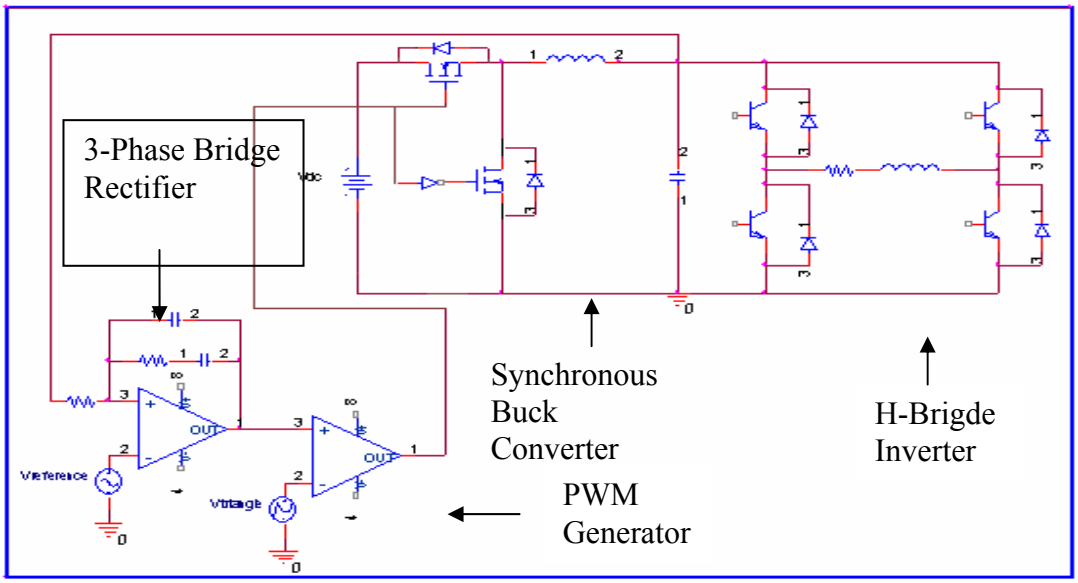

Figure 2.36. Modified Circuit Topology

The advantage of this circuit is the inductance current of the synchronous buck rectifier will flow in both directions. So the circuit always operates in continuous conduction region. If the voltage on the output capacitor of the input

stage tends to increase more then the reference voltage (as seen in previous sections) due to the inductive current flowing through it, the additional switch turns on and provides an alternative path for that current. So the distortion will be prevented

As a result of this, all conventional Buck Converter equations for continuous conduction mode of operation are valid for complementary switching Buck converter.

Since this circuit never operates in discontinuous region, the linear relationship between the input and output voltages of the input stage is guarantied for all type of loads.

Also the modified topology provides fast response to a load transient which is demanded by this application. [12]

The modified topology is simulated for inductive load and the results are given in the figures below. The output voltage and current waveforms are shown in figure 2.37. Upper waveform is voltage and the lower one is current.

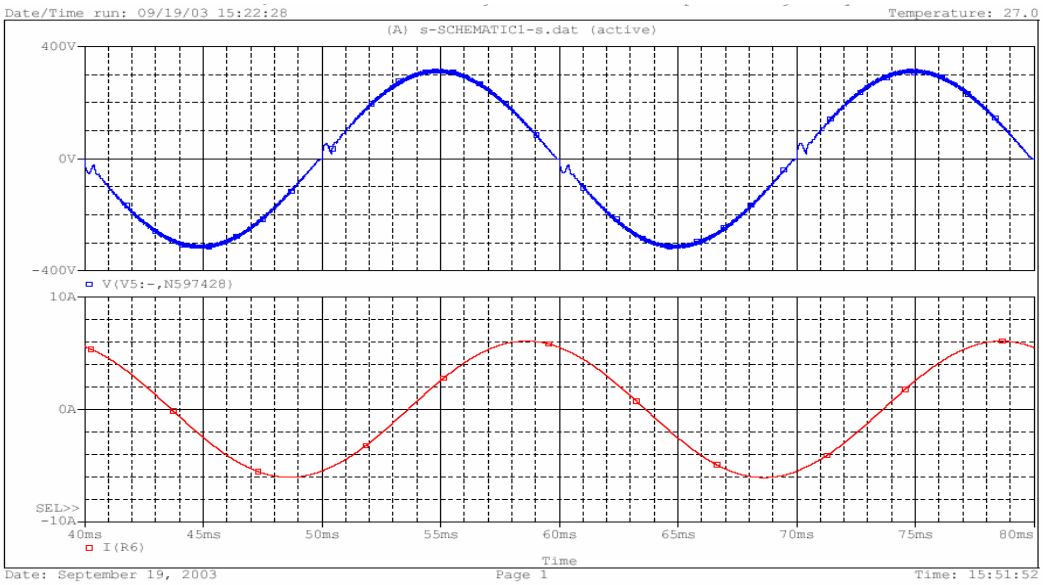

Figure 2.37 Output voltage and load current for inductive load with closed loop control. (Upper waveform is voltage and the lower one is the current).

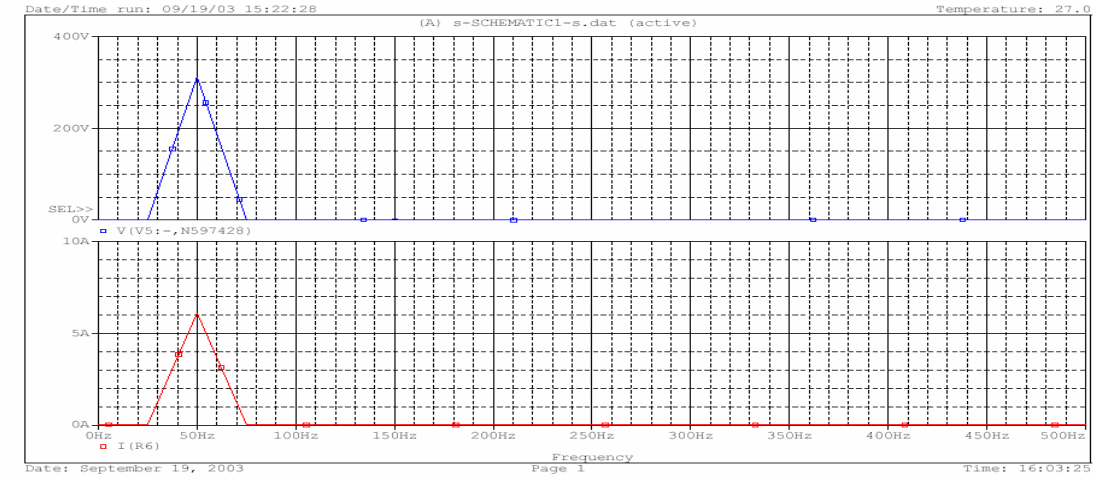

Figure 2.38 Harmonic Spectrum of output voltage and load current for inductive load with closed loop control. (Upper waveform is voltage and the lower one is the current).

The FFT results shown in figure 2.38 show that the fundamentals of both voltage and current are at 50 Hz, beside these there are significantly small (negligible) lower order harmonics. Also figure 2.37 proves that the modified topology has solved the control complexity problem and the undesirable distortion on the rectified DC-link is eliminated.

THD of the waveform shown in figure 2.32 (output voltage), is calculated as 10%.

Fig 2.39 shows the inductance current of the buck converter. Also a magnified version of figure 2.39 is shown in figure 2.40.

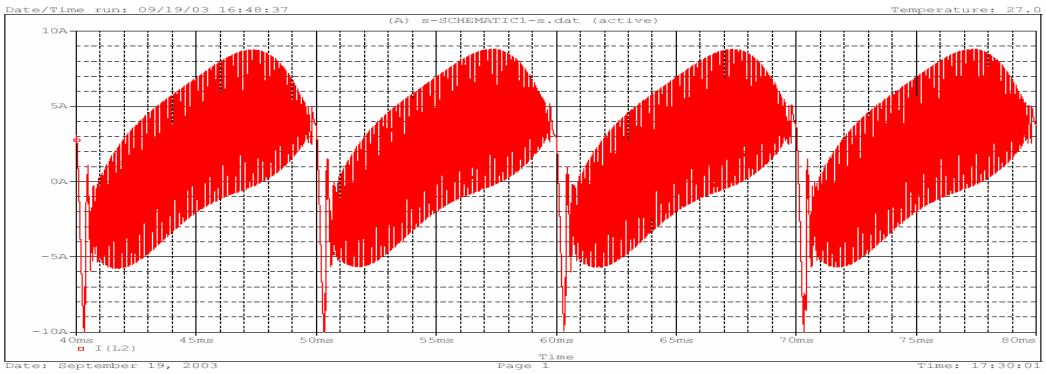

Figure 2.39 Inductance current (modified topology)

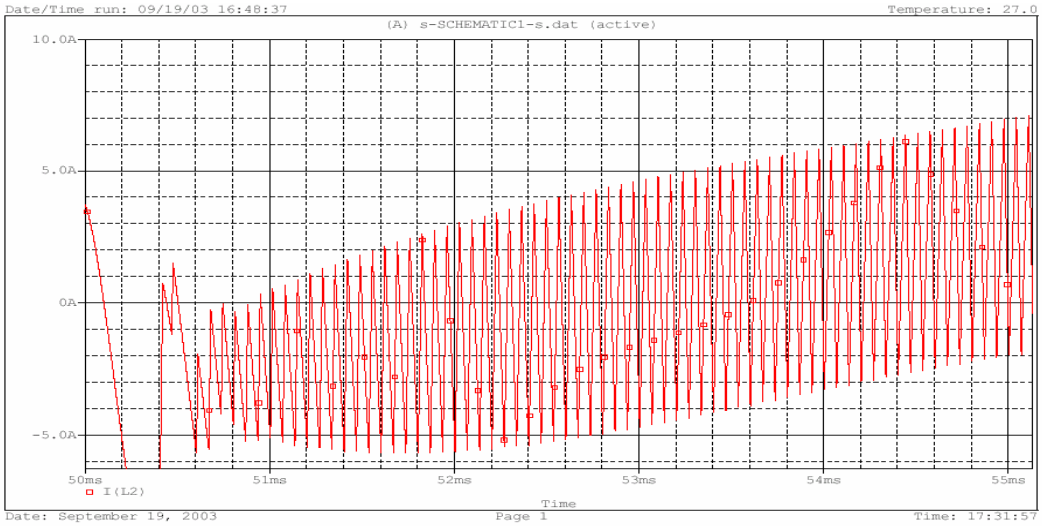

Figure 2.40 Inductance current (magnified version of figure 2.60) (modified topology)

The advantage of the new modified topology can be clearly seen from figures.2.39 and 2.40. The inductance current can be bidirectional due to the additional switch. As a result of this, the reverse inductive current pumped from the output stage to the in put stage can be directed through this switch to either ground or to the input DC-link instead of it flows into the DC-DC converter filter capacitance. Thus the distortion is avoided.

CHAPTER 3

DETERMINATION OF THE DC-DC CONVERTER PARAMETERS

3.1 Introduction

In conventional buck converter (figure 3.1) design procedures, except for special applications, the inductance value L is chosen such that the inductance current is continuous. A minimum value of the inductance that satisfies the continuous conduction mode of operation can be calculated and selected as the criteria for the design, as discussed in section 2.3.3.2 and given by the formula

$$Lf_s \geq \frac{(1-D)R}{2} \qquad 3.1$$

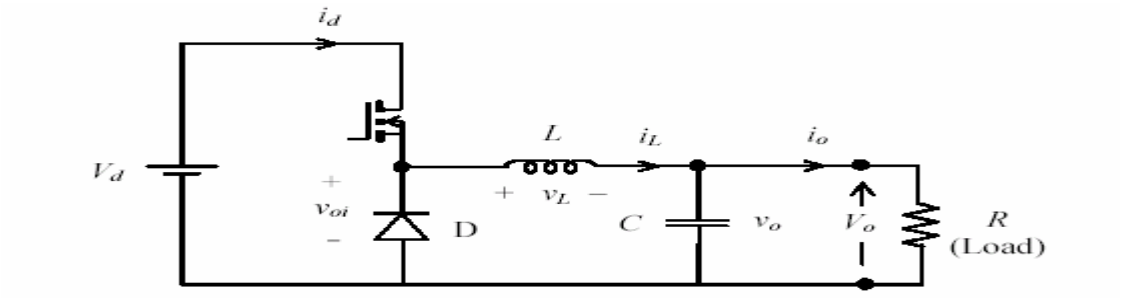

Figure 3.1 Conventional Buck Converter

However in our application the system always operates in continuous conduction mode as a result of the additional switch connected in parallel with diode D in figure 3.1, thus providing a path for the inductance current to flow in both directions as shown in figure 3.2 as discussed in section 2.4.3. So a “minimum

inductance value for continuous conduction mode" definition does not exist for the case. Another criterion should be defined for the inductance value.

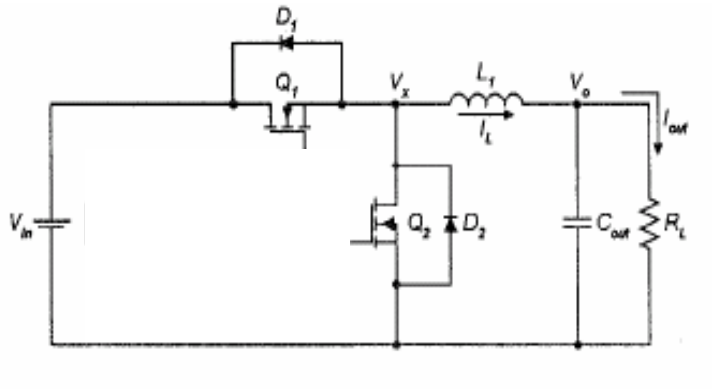

Figure 3.2 Complementary Switching Buck Converter

In this thesis study this criteria is defined as the physical volume of the inductor. After determining the inductance value, the capacitance value will be determined depending on the output voltage ripple specification.

3.2 Inductance Design

While starting the inductance design, the operating conditions of the circuit should be considered. The inductance used in this thesis is operating at high frequencies such as 15 kHz. In manufacturers application notes and data sheets [13, 14], ferrite E shaped cores are recommended for high frequency and medium power inductance and transformer design applications. The properties of some of E shaped ferrite cores that will be proper for our application are shown in table 3.1.

MAGNETIC DATA

TO ORDER SEE NOTE ↓		AL VALUES MH/1000 Turns										
PART NUMBER (Note 1)	COMBI-NATION	MATERIALS μ μ2300 R (min.)	μ μ2500 P (min.)	μ μ3000 F ±25%	μ μ5000 J (min.)	$\frac{\mu}{l_e}$ (cm)	A_e (cm²)	MINIMUM AREA (cm²)	V_e (cm³)	SET NOM. Wt. (gms)	BOBBIN WINDOW AREA (cm²)	WaAc (cm⁴) (Note 2)
45021-EC	E-E	4,600	5,000	8,000	8,010	9.29	2.25	2.13	20.9	108	1.78	4.00
45528-EC	E-E	4,720	5,130	8,220	9,375	12.3	3.50	3.46	43.1	212	2.83	9.91
45530-EC	E-E	5,640	6,130	9,800	11,190	12.3	4.17	4.13	51.4	255	2.83	11.8
46016-EC	E-E	4,300	4,680	6,590	7,445	11.0	2.48	2.40	27.2	135	2.89	7.16
47228-EC	E-E	4,470	4,860	7,780	8,885	13.7	3.68	3.63	50.3	264	4.02	14.8
48020-EC	E-E	3,505	3,810	6,000	6,940	18.5	3.89	3.82	72.1	357	7.91	30.8

Table 3.1 Properties of Ferrite E shaped cores for medium power applications

In the last column of the table 3.1 a term defined as WaAc (cm^4) is seen. This term is called Area Product and is the basis of the design procedure for selecting the proper core. In the foregoing analysis Wa is indicated as Aw and Ac is indicated as Acore in the formulations in order to prevent complexity.

Design procedure is discussed in detail in [2]. The starting point of the inductor design is the equation commonly termed stored energy relation defined as,

$$L I_{\max} = N \hat{\Phi} \tag{3.2}$$

where L is inductance, I_{max} is maximum inductance current, N number of turns, and $\hat{\Phi}$ is peak flux in the inductor. The number of turns N is given by,

$$N = \frac{k_{cu} A_w}{A_{cu}} \tag{3.3}$$

where k_{cu} is winding factor (0,3-0,6 depending on the insulation and the wire type), A_w is effective winding area and A_{cu} is conductor area. The flux in the inductor is,

$$\hat{\Phi} = A_{core} \hat{B} \tag{3.4}$$

where A_{core} is effective core area and $\hat{B}$ is maximum flux density in Tesla. Conductor area, A_{cu} , is given by

$$A_{cu} = \frac{I_{rms}}{J_{rms}} \tag{3.5}$$

where I_{rms} is the rms value of the inductor current and J_{rms} is the rms current density in A/mm^2. Using Equations. 3.3, 3.4 and 3.5 in equation 3.2 yields,

$$L I_{\max} = \frac{k_{cu} A_w}{A_{cu}} A_{core} \hat{B} \tag{3.6}$$

$$L I_{\max} = \frac{k_{cu} A_w}{\frac{I_{rms}}{J_{rms}}} A_{core} \hat{B}$$

$$L I_{\max} I_{rms} = J_{rms} k_{cu} A_w A_{core} \hat{B} \quad 3.7$$

A_wA_{core} is called AREA PRODUCT and given by

$$AP = A_w A_{core} = \frac{L I_{\max} I_{rms}}{J_{rms} k_{cu} \hat{B}} \quad 3.8$$

This equation is the basis for the inductor design procedure in this thesis. This equation relates design inputs (L,I_{max} and I_{rms}) to the material parameters (J_{rms} and $\hat{B}$) and geometric parameters (k_{cu}, A_w, *and* A_{core}) of the core and winding. [2]

Design software is developed in MATLAB in order to determine the proper inductance value depending on the Eq.3.8

3.2.1 Inductance Design Software

The software is developed particularly for a complementary switching buck converter. Program code is given in appendix A2. With this software, I_{max}, I_{min}, I_{rms}, and AP values are calculated for a defined range of inductance values, where I_{max} is maximum inductance current, I_{min} is minimum inductance current, I_{rms} is rms value of inductance current, and AP is Area Product of the core. I_{max} , and I_{min} are defined and formulated in section 2.3.3.2 and shown by equations 2.25 and 2.26 respctively also I_{rms} is the rms value of the inductance current shown in figure 3.3 and calculated simply by integrating the square of the waveform shown in figure 3.3 over one period and taking its square root. The derived expression of I_{rms} in terms of D, I_{max}, and I_{min} is given in equation 3.9.

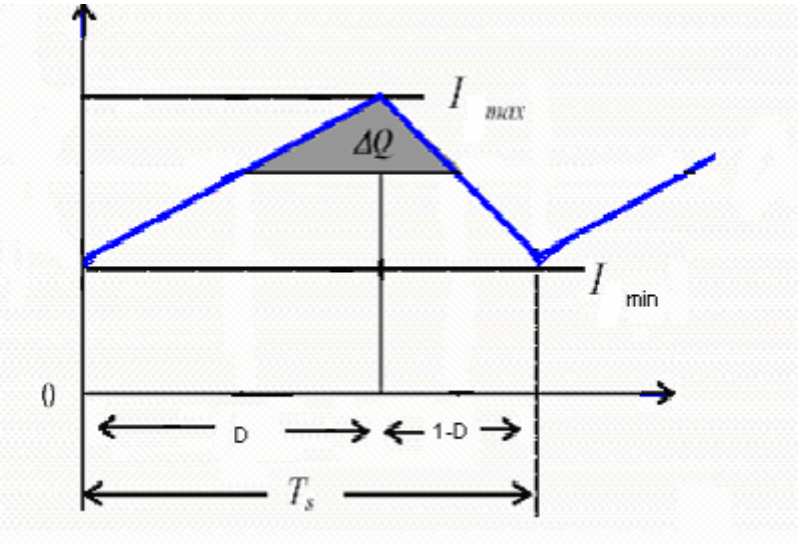

Figure 3.3 Inductor current over one period

$$I_{rms} = \sqrt{\left[\left[\frac{1}{(1-D)^2}\left[\frac{a^2}{3}(1-D^3) - ab(1-D^2) + b^2(1-D)\right]\right] + \frac{a^2}{3} + aI_{\min} + I_{\min}{}^2\right]} \quad 3.9$$

where,

$$a = I_{\max} - I_{\min} \quad 3.10$$

$$b = I_{\max} - DI_{\min} \quad 3.11$$

$$i_{L\max} = \frac{V_o}{R} + \frac{\Delta i_L}{2} = \frac{V_o}{R} + \frac{V_o}{2L}(1-D)T_s \quad 3.12$$

$$i_{L\min} = \frac{V_o}{R} - \frac{\Delta i_L}{2} = \frac{V_o}{R} - \frac{V_o}{2L}(1-D)T_s \quad 3.13$$

By using equations 3.9, 3.10, 3.11, 3.12, and 3.13 in equation 3.8, Area Product value is calculated in the software.

Program inputs are, k_{cu}, J_{rms}, $\hat{B}$, Z_o, V_o, f, V_s, where k_{cu} is winding factor, J_{rms} is RMS value of current density in A/mm^2, $\hat{B}$ is maximum flux density, Z_o is

load impedance, V_o is output voltage, f is switching frequency, V_s is input voltage.

For the given values of input parameters, AP and I_{max} values are calculated for inductance values between 25μH and 5mH in steps of 25μH. Load is assumed to be full load as discussed in section 2.4.1 as Maximum output power of 750VA - 1 KVA. Maximum Output Voltage is 311 V_{peak}, 220V_{rms}. f_s = 15.000 Hz.

The input parameters are determined as,

k_{cu} = 0.3, J_{rms} = 200 A/cm^2, Z_o = 50-70Ω, V_o = 220V_{rms}, f = 15000Hz, V_s = 530V.

$\hat{B}$ value is determined with the aid of manufacturer's data sheet. For our application the most proper material which has the highest saturation flux density is material P core of Magnetics Corporation.. For P type material, the saturation flux density versus temperature curve is shown in figure 3.4.

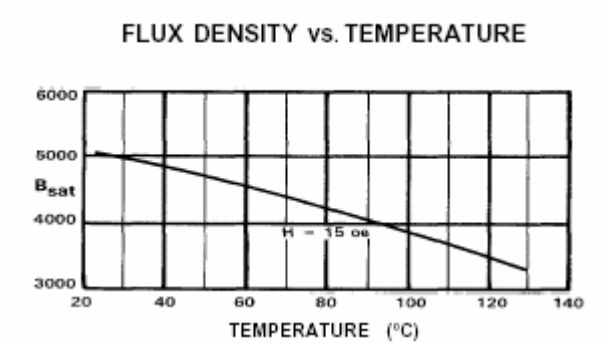

Figure 3.4 Saturation flux density vs. temperature for P Material

This material has B_{sat} of 500 mT at 30 °C and 400 T at 90 °C. $\hat{B}$ is determined as 0.35T in order to assure safe operation.

The outputs of the program, area product versus inductance value are shown in figures.3.5, 3.6

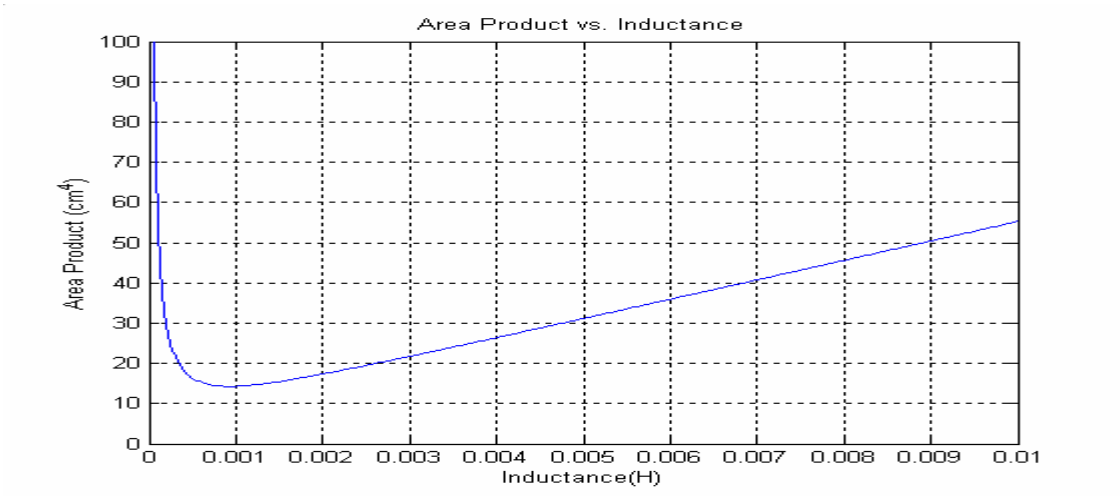

Figure 3.5 Area product vs. inductance

It is obviously seen that at the neighborhood of 1mH, area product has its minimum value as shown in figure 3.6. For greater values of inductance above 1mH, area product increases to the values that are not feasible with the cores given in table 3.1.

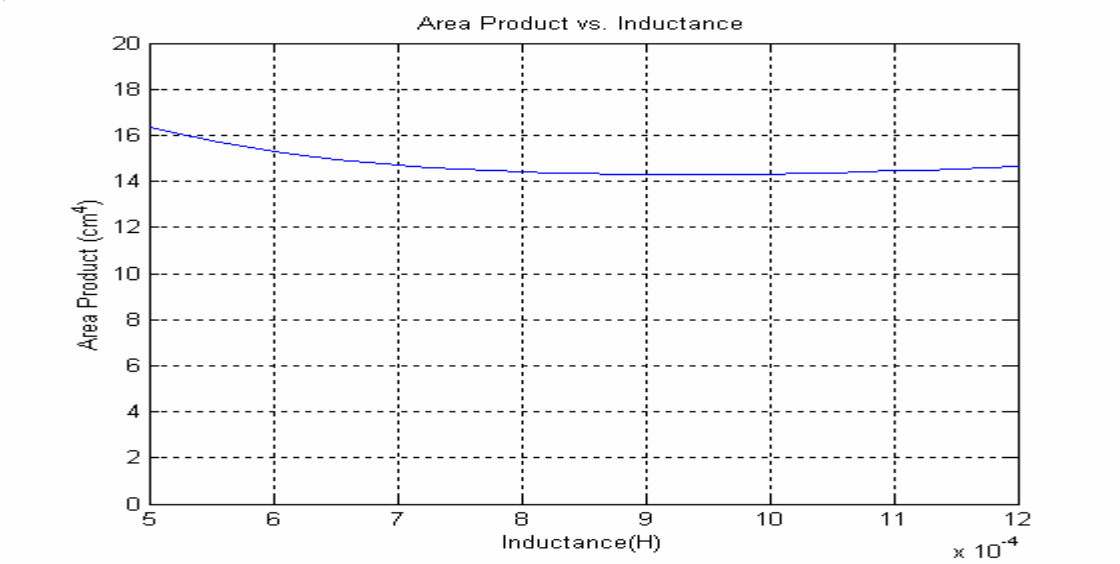

Figure 3.6 Area product vs. inductance (Magnified)

In this design procedure, the standard commercially available inductor cores are also taken into account while choosing the proper inductance value [13].

In figure 3.6 Area Product value for 900-1000 μH is approximately 14.2 – 14.3 cm^4. Depending on that, the most proper core for our application is selected to be 47228-EC material P core of Magnetics Corporation. This core has an Area Product of 14.8 cm^4 as shown in table 3.1. Also inductance value is determined to be 950 μH depending on figure 3.6. A number of samples of this core has been manufactured in USA and sent by the manufacturer.

3.2.2 Calculation of L_{max}, Possible With the Selected Core and Specifying the Inductance Value

For the selected core, the maximum inductance value possible with must be calculated in order to assure the selection of core. In the design, the winding material will be Litz wire because it has the lowest eddy current loss of any conductor type at high frequencies. For Litz wire $k_{cu} = 0.3$. J_{rms} is chosen as 200A/cm^2 in order to avoid over temperature problems.

I_{rms}, can also be calculated by the inductance design software. The result is shown in figure 3.7. I_{rms} for 950 μH is approximately 4.2 A.

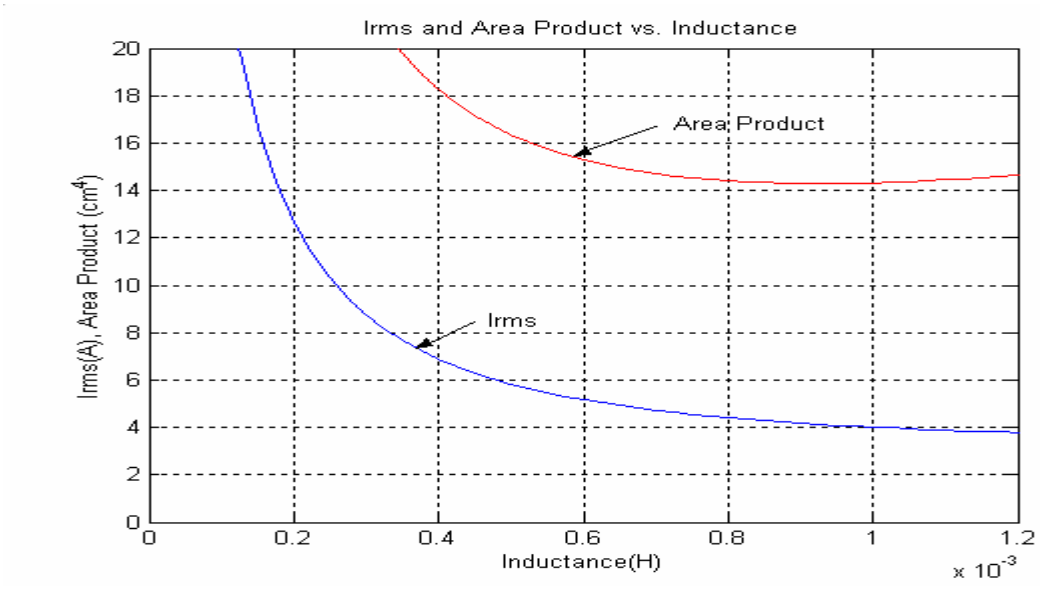

Figure 3.7 Area Product and I_{rms} versus Inductance

The required area of the copper conductor is given by Eq.3.4. Using Eq.3.4 and figure 3.3 required copper area is calculated as,

$$A_{cu} = \frac{4.2}{2} = 2.1mm^2$$

From data sheet of the core 47228-EC, A_w = 402 mm^2. So the maximum number of turns that is possible to wind to the selected core, with the conductor area obtained above and with k_{cu} = 0.3 is calculated using Eq.3.2 as,

$$N_{\max} = \frac{402 \times 0.3}{2.1} \cong 60 Turns$$

The maximum inductance achievable with the specified core could then be calculated. Combining Eqs.3.1 and 3.3 gives,

$$L_{\max} = \frac{N_{\max} A_{core} \hat{B}}{\hat{I}}$$

$$L_{\max} = \frac{60 \times 350mT \times 3.68 \times 10^{-4} m^2}{7.8} = 990\mu H$$

The possible inductance value will be an arbitrary value in the range of 900-990 μH. however if the maximum achievable inductance value is chosen, the minimum achievable inductance current values will be obtained. So inductance value is chosen as 950μH, leaving a safety margin for the assembling process.

Number of turns necessary for 950 μH, can be calculated using Eqs.3.1 and 3.3 assuming that $\hat{I}$ is constant within a small interval of inductance value as,

$$\frac{L_{\max}}{N_{\max}} = \frac{L}{N} \Rightarrow N = \frac{950 \times 10^{-6} \times 60}{990 \times 10^{-6}} \cong 57 \quad Turns$$

3.2.3 Calculation of Winding Loss

Specific power $P_{Cu,s}$ dissipated per unit of copper volume in a copper winding due to its resistance is given by

$$P_{w,s} = 22k_{Cu}(J_{rms})^2 \, mW/cm^3 \qquad 3.14$$

Winding volume is calculated approximately as V_w = 75 cm^3. Thus total power dissipated in the windings is

$$P_w = 22 \times 0.3(2)^2 \times 75 \cong 2W$$

3.2.4 Calculation of Core Loss

All magnetic cores exhibit some degree of hysteresis in their B-H characteristic. The area inside the B-H loop represents work done on the material by the applied field. The work (energy) is dissipated in the material, and heat caused by the dissipation raises the temperature of the material.

The hysteresis loss increases in all core materials with increases in ac flux density B_{ac}, and switching frequency f. The general form of the loss per unit volume (specific loss), is given by Eq.3.10.

$$P_s = af^c B_{ac}^{\ d} \qquad 3.15$$

where P is in mW/cm^3, B_{ac} is in kiloGauss, and f is in kHz. Coefficients are given by the manufacturer as shown in Table 3.1.

	a	c	d
f < 100 kHz	0.158	1.36	2.86
100 kHz ≤ f < 500 kHz	0.0434	1.63	2.62
f ≥ 500 kHz	$7.36\ 10^{-7}$	3.47	2.54

Table.3.2 Coefficients applied to core loss formula

AC core flux density B_{ac} is calculated in [2] and given as

$$B_{ac} = \hat{B}\frac{I_{\max} - I_{dc}}{\hat{I}}$$

I_{max}, and I_{dc} are calculated by the inductance design software by the given formulas in section 3.2.1 for 950 μH as I_{max} = 7.9 A and I_{dc} = 4.4 A

Thus B_{ac} = 0.155 T = 1.55 kilo Gauss and for f = 15 kHz.

$$P_s = 0.158 \times 15^{1.36} \times 0.155^{2.86} = 30.37\, mW/cm^3$$

Total core loss is given by Eq.3.11 as,

$$P_{core} = P_s V_{core} \qquad 3.16$$

where, V_{core} is core volume, in cm^3. Core volume of 47228-EC is 50.3 cm^3 (from data sheet given in appendix A3. Thus max core loss is

$$P_{core} = 24.1 \times 50.3 = 1.527W$$

3.2.5 Thermal Analysis

In this section, thermal verification of the inductance design will be given.

Increases in the temperature of the magnetic core and winding materials degrade the performance of these materials. The resistivity of the copper winding increases with temperature and so the winding loss increases with temperature, assuming a constant current density. In the magnetic materials, the core loss increases with increasing temperature, assuming the frequency and flux density

remain constant. However the value of the saturation flux density becomes smaller with increases in temperature. [2]

To keep the performance degradation within bounds, the temperature of the core and windings must be kept below some maximum value. This value is approximately 100°C for ferrite material [13, 14].

The internal temperature and surface temperature of the inductor is assumed to be nearly the same. This assumption is made because the power dissipation is approximately uniformly distributed throughout the volume of the core and the windings. This leads a large cross-sectional area for heat conduction to the surface and for relatively short path lengths. Moreover, the thermal conductivities of the materials are large. Hence the thermal resistance of importance in determining the temperature of the inductor is the surface-to-ambient resistance, $R_{\theta sa}$. The heat transfer from a body to its surroundings is composed of two parallel mechanisms which are heat transfer by radiation and heat transfer by convection. Thus surface-to-ambient thermal resistance $R_{\theta sa}$, has two components, that are radiative, $R_{\theta,rad}$, and convective, $R_{\theta,conv}$.

3.2.5.1. Thermal Resistance Due to Radiative Heat Transfer

Heat transfer via radiation is given by the Stefan-Boltzman law as,

$$P_{rad} = 5.7 \times 10^{-8} EA(T_s^4 - T_s^4) \qquad 3.17$$

where P_{rad} is the radiated power in watts, E is the emissivity of the surface, T_s is the surface temperature in K, T_a is the ambient temperature in K, and A is the outer surface area in m^2. For dark objects, E = 0.9.

For black ferrite material, Eq.3.17 can be rewritten as

$$P_{rad} = 5.1A\left[\left(\frac{T_s}{100}\right)^4 - \left(\frac{T_a}{100}\right)^4\right] \quad 3.18$$

The thermal resistance $R_{\theta,rad}$ is defined as

$$R_{\theta,rad} = \frac{\Delta T}{P_{rad}} \quad 3.19$$

Thus,

$$R_{\theta,rad} = \frac{\Delta T}{5.1A\left[\left(\frac{T_s}{100}\right)^4 - \left(\frac{T_a}{100}\right)^4\right]} \quad 3.20$$

The surface area of the inductor for the selected core and winding configuration is 0.0112 m^2. For an ambient temperature of T_a = 40°C and for maximum surface temperature of T_s = 100°C, the thermal resistance due to radiation is calculated using Eq.3.20 as

$$R_{\theta,rad,100°C} = 10.75°C/W$$

3.2.5.2 Thermal Resistance Due To Convective Heat Transfer

If a vertical surface has a vertical height d_{vert} less than about 1 m, it loses heat energy via convection to the surrounding air [2] at a rate given by

$$P_{conv} = 1.34A\frac{(\Delta T)^{1.25}}{(d_{vert})^{0.25}} \quad 3.21$$

where P_{conv} is the heat power lost via convection in watts, ΔT is the temperature difference between the surface and ambient, A is the total surface area of the body in m^2, and d_{vert} is the vertical height of the body in meters.

The thermal resistance $R_{\theta,rad}$ is defined as

$$R_{\theta,conv} = \frac{\Delta T}{P_{conv}} \tag{3.22}$$

Combining Eqs.3.21 and 3.22,

$$R_{\theta,conv} = \frac{1}{1.34A}\left(\frac{d_{vert}}{\Delta T}\right)^{0.25} \tag{3.23}$$

The surface area of the inductor for the selected core and winding configuration is 0.0112 m^2 and d_{vert} = 5.8 cm. For an ambient temperature of T_a = 40°C and for maximum temperature of T_s = 100°C, the thermal resistance due to convection is calculated using Eq.3.23 as

$$R_{\theta,conv,100°C} = 13.88°C/W$$

These two thermal resistances are in parallel, and the total thermal resistance of the inductor body to ambient when T_a = 40°C and T_s = 100 °C is

$$R_{\theta sa} = \frac{R_{\theta,rad}R_{\theta,conv}}{R_{\theta,rad} + R_{\theta,conv}} = 6.06\ ^{\circ}C/W$$

3.2.5.3 Temperature Rise in the Inductor

For a given total power dissipation of P_T (Core loss + copper loss), max surface temperature of the inductor is given by,

$$T_s = R_{\theta sa}P_T + T_a \tag{3.24}$$

$$P_T = P_w + P_{core} \tag{3.25}$$

For our application the max surface temperature, at an ambient temperature of 40 °C, is

$$T_s = 6.06 \times (1.527 + 2) + 40$$

$$T_s = 61\ ^\circ\text{C}$$

This result is in the safe operating region. Possibly, the current density will be increased a little bit in order to increase the power.

3.2.6 Specifying the Air gap Length

The air-gap length must be specified in such a way that the gap must be tailored to give the value of $\hat{B}$ when the inductor current is I_{max} . The total reluctance, R_m, of the magnetic flux path is given in [2] by

$$R_m = \frac{N I_{\max}}{A_{core} \hat{B}} = R_{m,core} + R_{m,gap} = \frac{l_c}{\mu A_c} + \frac{\sum g}{\mu_0 A_g} \qquad 3.26$$

where l_c is the magnetic flux path length in the core material. At every air-gap in the magnetic core, there will be fringing flux as shown in figure 3.8a. However the total flux in the air-gap must be the same as the total flux in the core, the flux density in the air-gap is much smaller than the flux density in the core. The effect of the air-gap is modeled as a rectangular block as shown in figure 3.8b having a gap length g and cross-sectional area A_g.

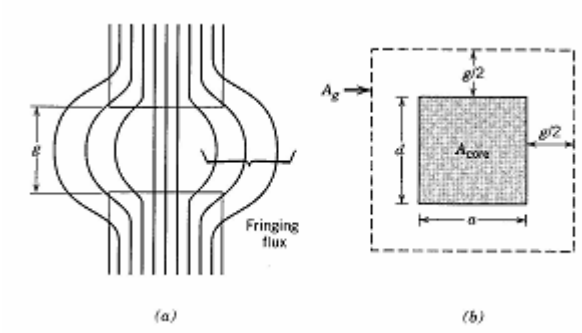

Figure 3.8 Fringing fields in the air-gap of an inductor (a), effective cross-sectional area of the gap (b)

Double E-core, its bobbin and an assembled inductor is shown in figure 3.9

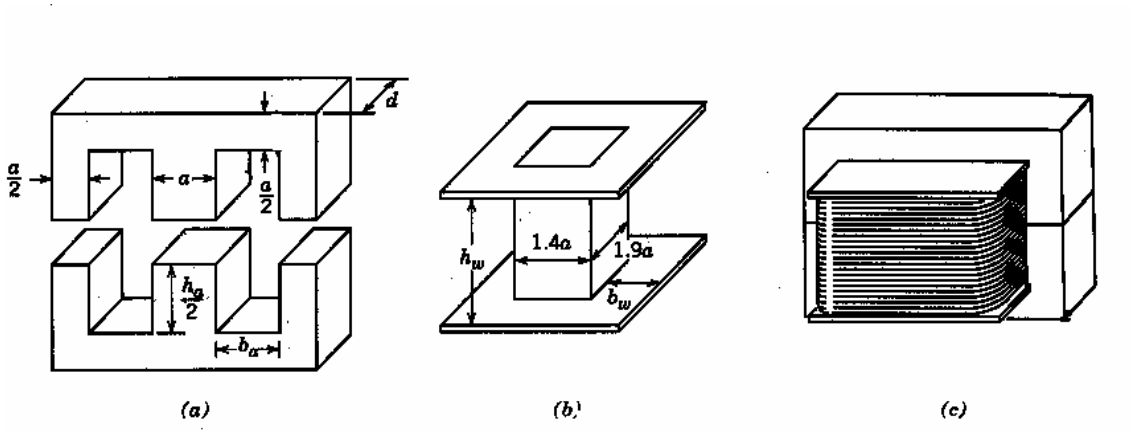

Figure 3.9 Double E-core, its bobbin and an assembled inductor

A_g is given for a double-E core by,

$$A_g = (a+g)(a+g) \tag{3.27}$$

Mostly,

$$R_{m,gap} = \frac{\sum g}{\mu_0 A_g} >> R_{m,core} = \frac{l_c}{\mu A_c}$$

So that the gap length $\sum g$ is given by

$$\sum g = \mu_0 A_g R_{m,gap} = \mu_0 A_g \frac{N I_{\max}}{A_{core} \hat{B}} \tag{3.28}$$

Eqs.3.27 and 3.28 give,

$$\sum g = \mu_0 \frac{N I_{\max}}{A_{core} \hat{B}} (a+g)(d+g) \tag{3.29}$$

Moreover, the double, E-shaped inductor does not have a single large air-gap as shown in figure 3.9. In stead of one, three air-gaps (distributed air-gaps) are used to keep the magnetic flux, which fringes into the copper windings to a minimum.

Thus the distributed air-gapped inductor has less eddy current loss than a single large air-gapped inductor. If there is N_g such distributed air gaps each having a length g then

$$\sum g = N_g g \tag{3.30}$$

As the air-gap at the center leg of the E-shaped inductor is twice in width of the gaps at the side legs, the center gap will be thought as two gaps. Thus in calculations it is assumed that the inductor has four air-gaps.

Substituting Eq.3.29 into Eq.3.30 yields

$$\sum g = \mu_0 \frac{N I_{\max}}{A_{core} \hat{B}} \left(a + \frac{\sum g}{N_g} \right) \left(d + \frac{\sum g}{N_g} \right) \tag{3.31}$$

Expansion of Eq.3.26 yields a quadratic equation in the desired parameter $\sum g$. In practical designs involving distributed air-gaps, the individual gap length g << a and d. Thus the quadratic terms in Eq.3.31 can be neglected in comparison to the linear terms in $\sum g$ to yield

$$\sum g \approx \frac{A_{core}}{\frac{A_{core} \hat{B}}{\mu_0 N I_{\max}} - \frac{(a+d)}{N_g}} \tag{3.32}$$

In our application, A_{core} = 3.68 cm^2 (from data sheet of 47228-EC core), $\hat{B}$ =0.35 T, $\mu_0 = 4\pi * 10^{-7}$ H/m, N = 57 (calculated and verified in section 3.2.4), $\hat{I}$ =7.9 A (calculated in section 3.2.1), a = d = 1.9 cm (from data sheet of core 47228-EC), N_g = 4 (for a double-E core, two in series in each leg). Then

$$\sum g \approx \frac{3.68\times10^{-4}}{\frac{\left(3.68\times10^{-4}\times0.35\right)}{4\pi\times10^{-7}\times60\times7.9}-\frac{\left(3.8\times10^{-2}\right)}{4}} = 1.78mm$$

The length of each of the four distributed air-gaps is

$$g = \frac{1.78}{4} = 0.445mm$$

3.3. Determination of the Capacitance (Value and type)

After specifying the inductance value, the capacitance value can be determined by the output voltage ripple equation (Eq.2.16) derived in section 2.3.3.1.

$$\Delta V_O = \frac{(1-D)V_O}{8CLf_s^{\,2}} \qquad 3.33$$

For the maximum possible output voltage V_o = 318 V, D = 0.6. f = 15000 Hz. L = 950 μH. Then solving Eq.3.28 for C, for a specified output voltage ripple be ΔV_o ≅ 2.5 % yields

$$C = \frac{(1-0.6)318}{8\times7\times950\times10^{-6}\times(15000)^2} = 10.62\times10^{-6}F$$

This will be corrected as 10μF in order to match the standards.

Now whether the capacitance value calculated for max output voltage assures reasonable output voltage ripple values for lower voltage levels is checked. In order to do this, output voltage ripple equation 3.33 is expressed as a function of duty cycle D and solved for ΔV_o as shown in Eq.3.27,

$$\Delta V_O = \frac{(D-D^2)V_g}{C8Lf_s^{\,2}} \qquad 3.34$$

where V_g = 530 V, L = 950 μH, f_s = 15000 Hz and C = 10 μF. Remembering that the linear input output voltage relationship $V_o = V_g D$, equation 3.34 is said to be a function of output voltage as well. Output voltage ripple values are calculated and plotted for duty cycle values D = 0 - 0.8 as shown in figure 3.10.

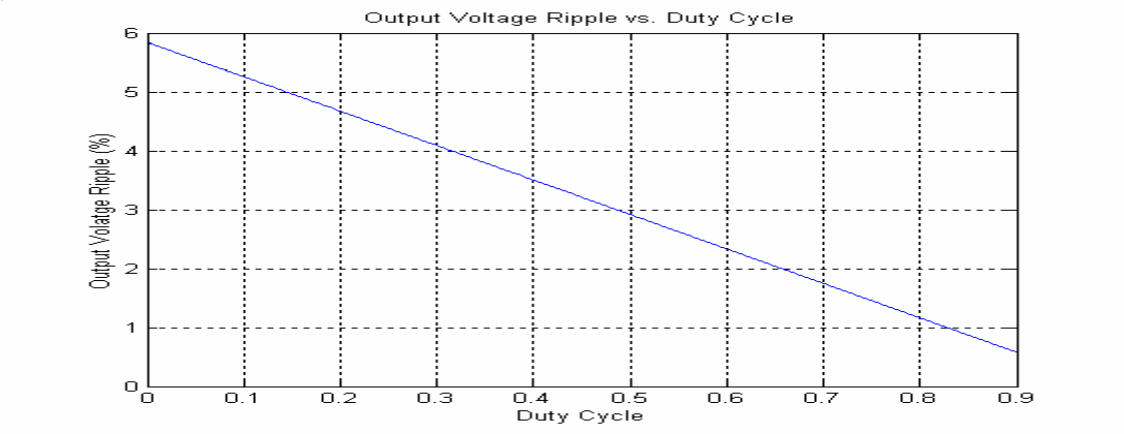

Figure 3.10 Capacitance vs. Duty cycle for ΔV_o = 7V.

It is obviously seen in figure 3.10 that the calculated capacitance value C = 10μF provides reasonable % output voltage ripple for all values of duty cycle, and output voltage values as well. Even if the output voltage value is minimum let's say D = 0.1 and V_o = 53V, output voltage ripple is calculated using figure 3.10 as

$$\Delta V_o = 0.052 \times 53 = 2.756V$$

At the frequency level of f = 15000 Hz, standard electrolytic capacitors may have higher equivalent series resistances. As a result, capacitor losses may be excessive. Instead of electrolytic, metalised poly-propylene film capacitors are preferred in this application in order to reduce capacitor losses.

Also the voltage rating of the capacitor is important. Since the output voltage of the synchronous buck converter is a DC quantity with a maximum value of $V_{o,peak}$ = 318 V_{dc}, at least two times of $V_{o,peak}$ should be chosen as the capacitor rating voltage.

CHAPTER 4

HARDWARE AND SOFTWARE IMPLEMENTATION

4.1 Introduction

The block diagram and pictures of the hardware setup used in this research is given in figure 4.1. Description of each block and brief information about software is given in the following sections. Also specifications of the components and the codes written in C and assembly languages are given in appendix A1. Experimental results obtained in laboratory are also given also in the following sections.

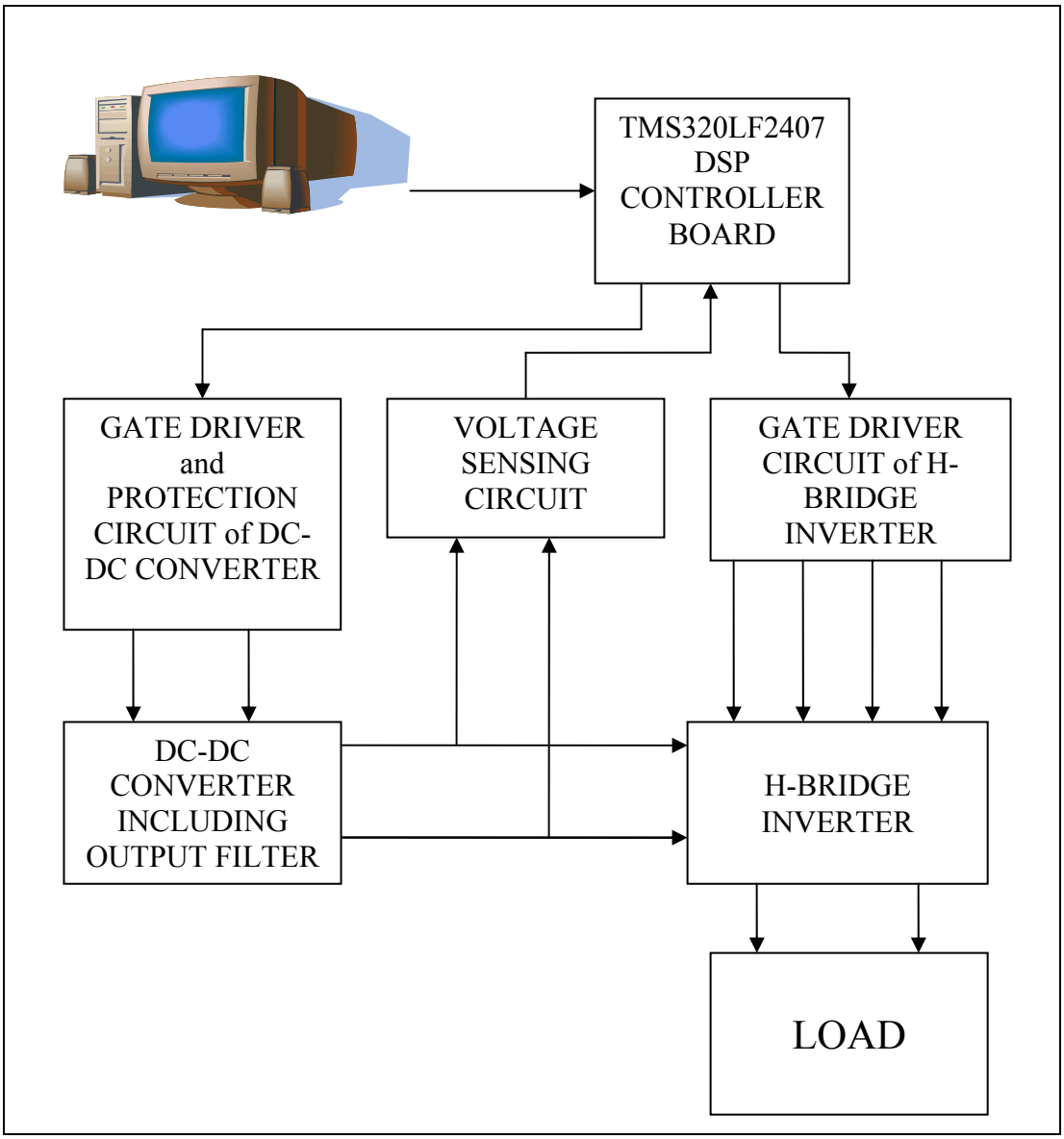

Figure 4.1 Block diagram of the hardware setup

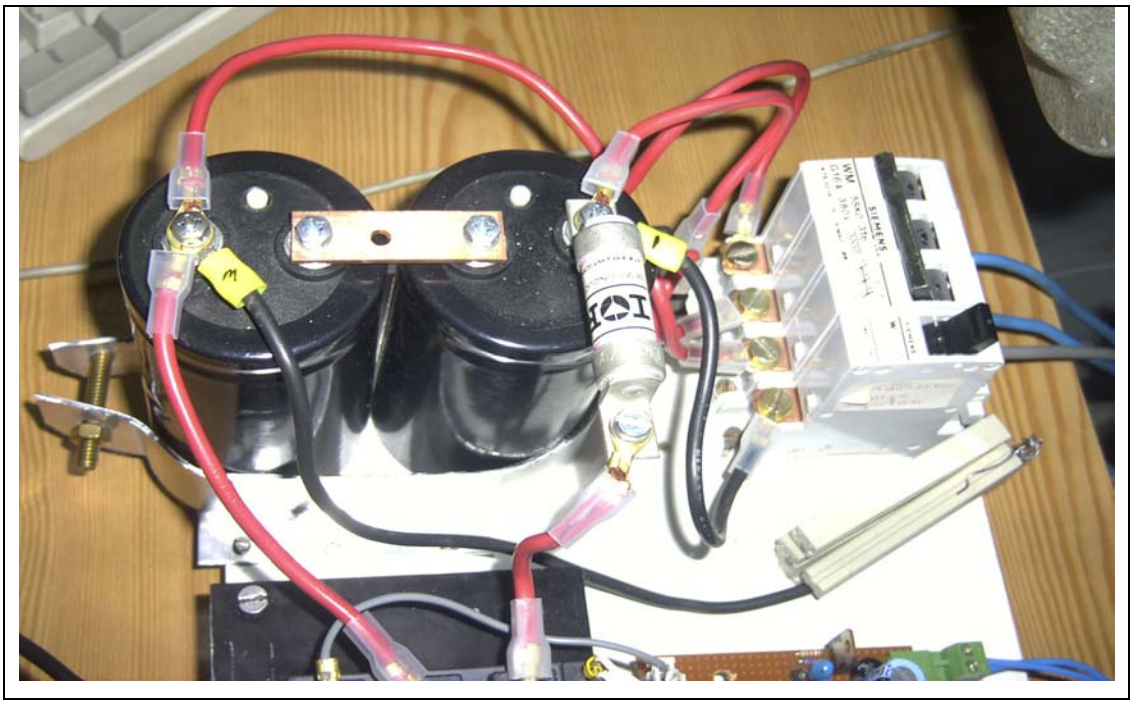

Figure 4.2 Input DC link and Filter Capacitors

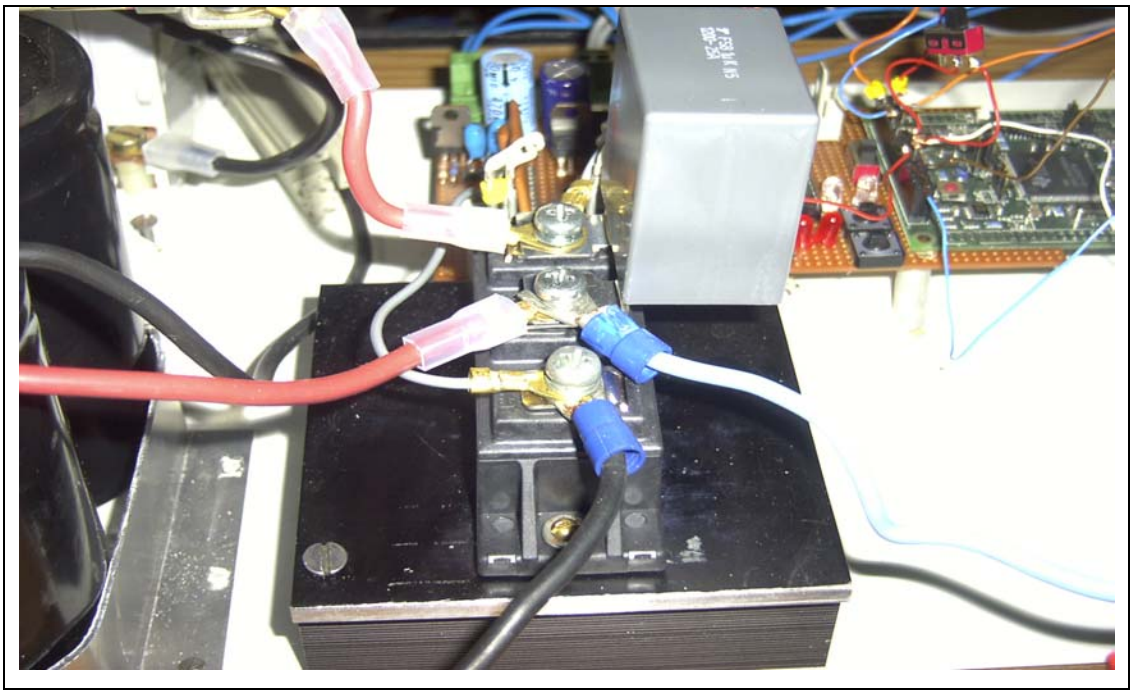

Figure 4.3 DC-DC Converter Power Stage (2MBI50N120 IGBT and Snubber Capacitance)

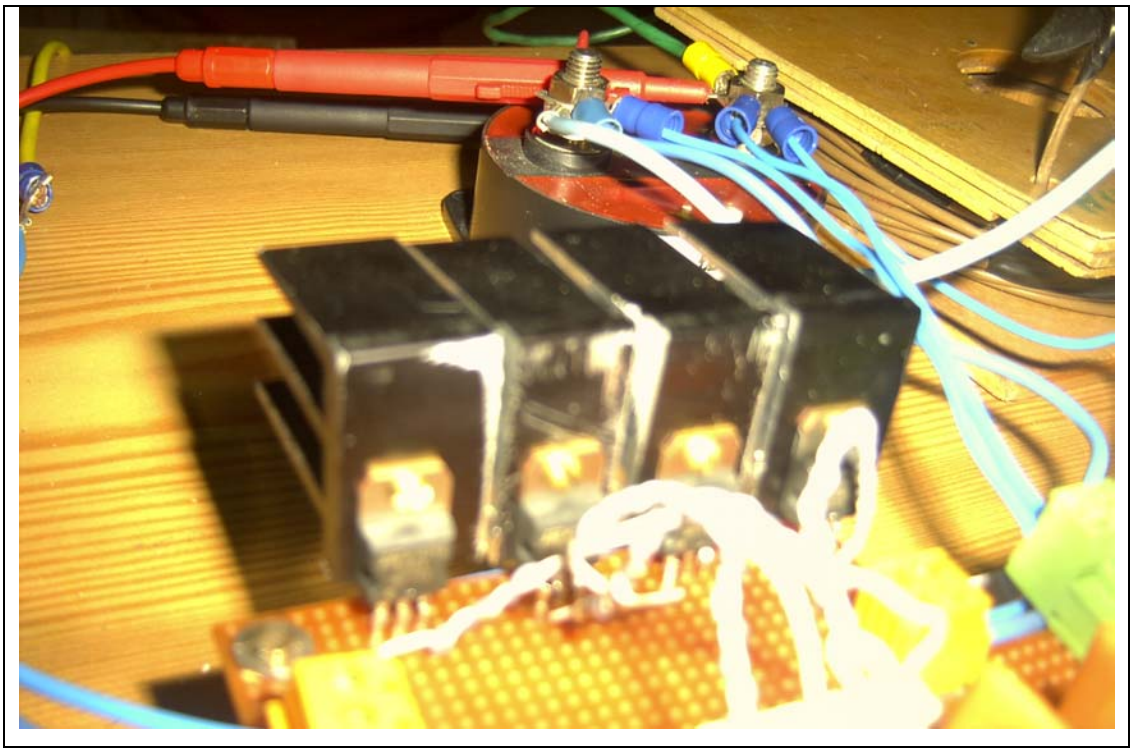

Figure 4.4 Output Inverter Power Stage (IRF 740 Mosfets)

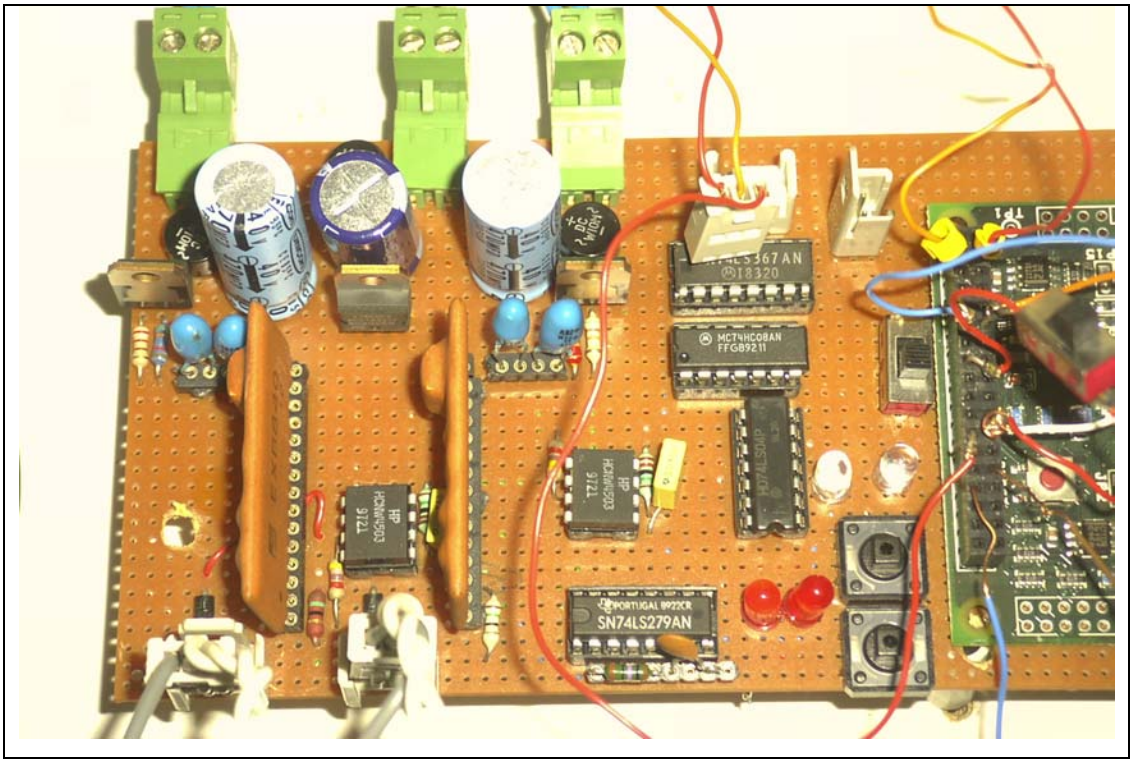

Figure 4.5 DC-DC Converter IGBT Gate Drivers and Protection Circuit

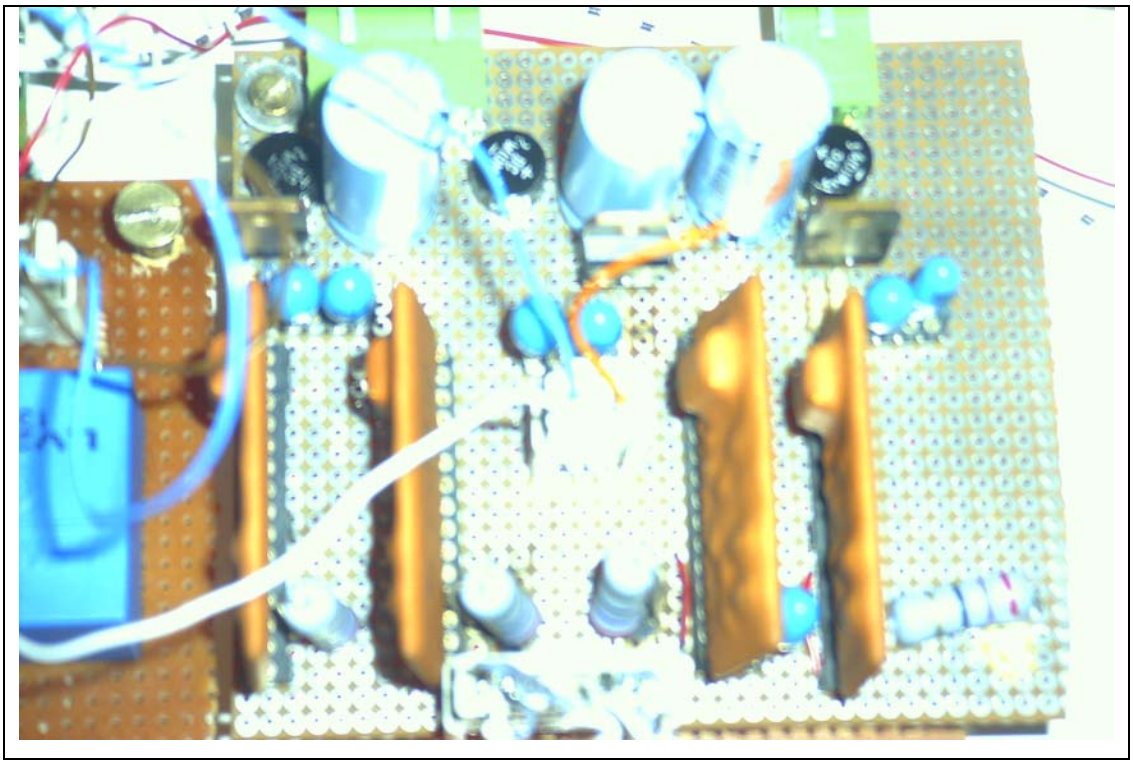

Figure 4.6 Output Inverter Mosfet Gate Driver Circuit

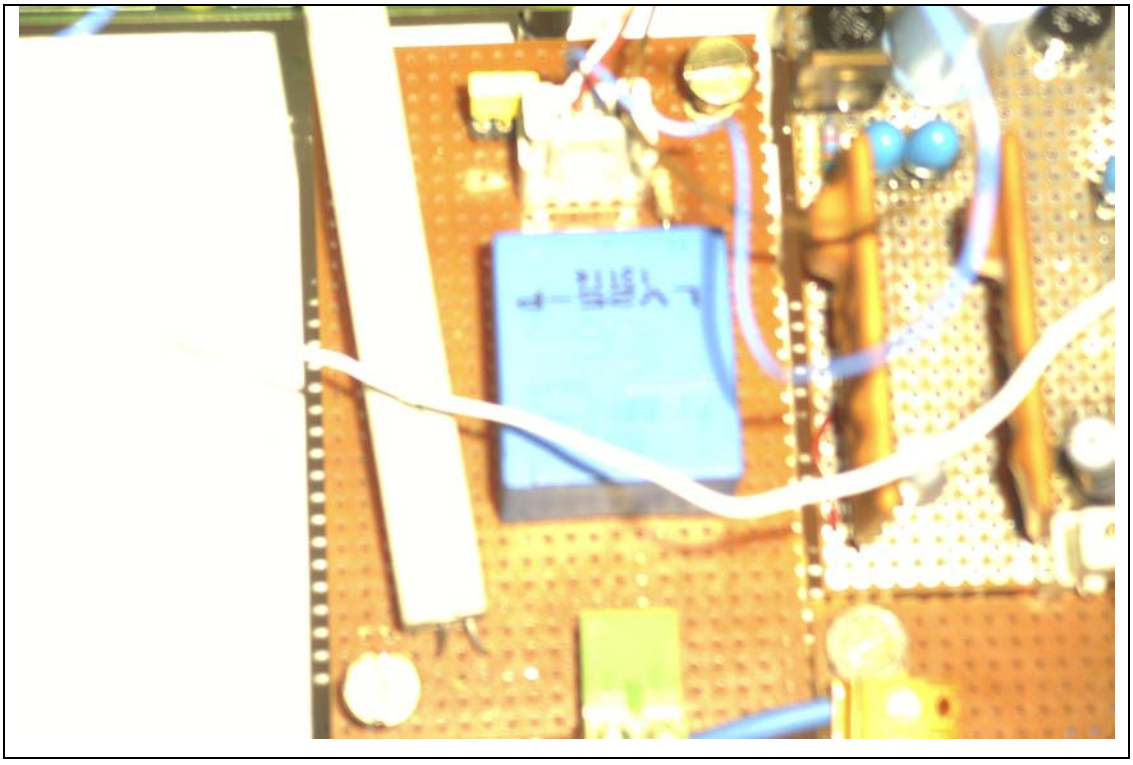

Figure 4.7 Voltage Sensing Circuit

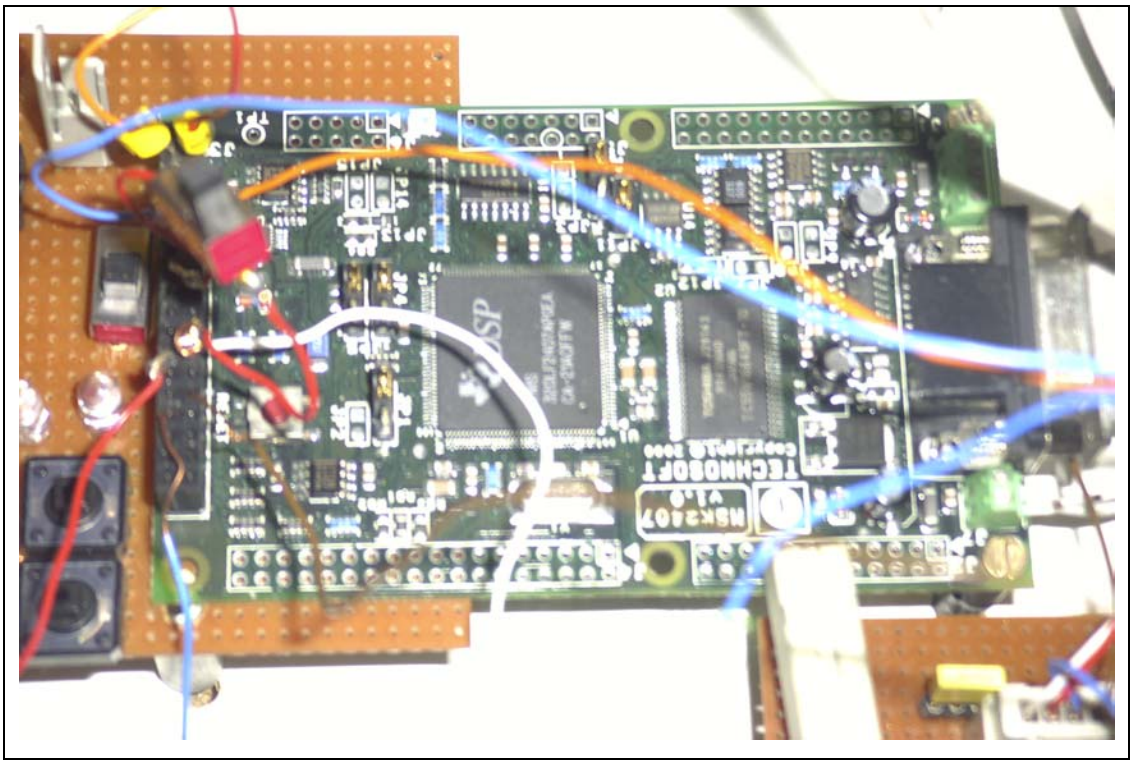

Figure 4.8 TMS320LF2407A DSP Controller Circuit

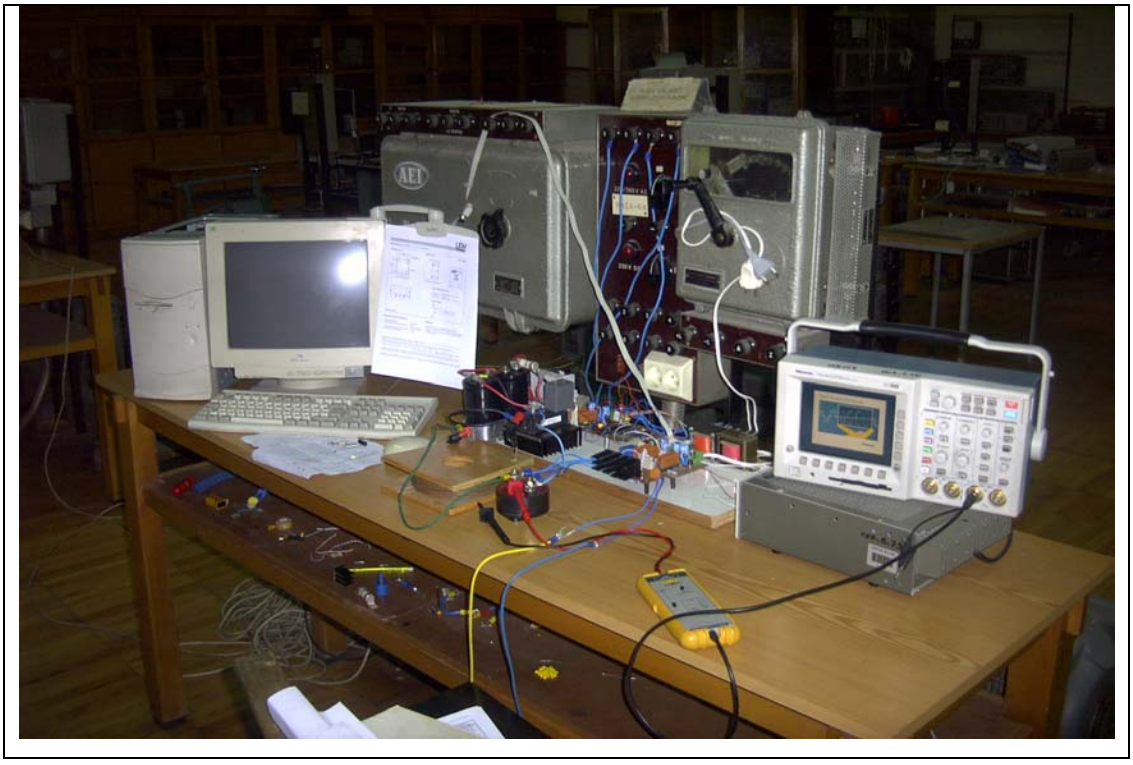

Figure 4.9 Experiment Setup

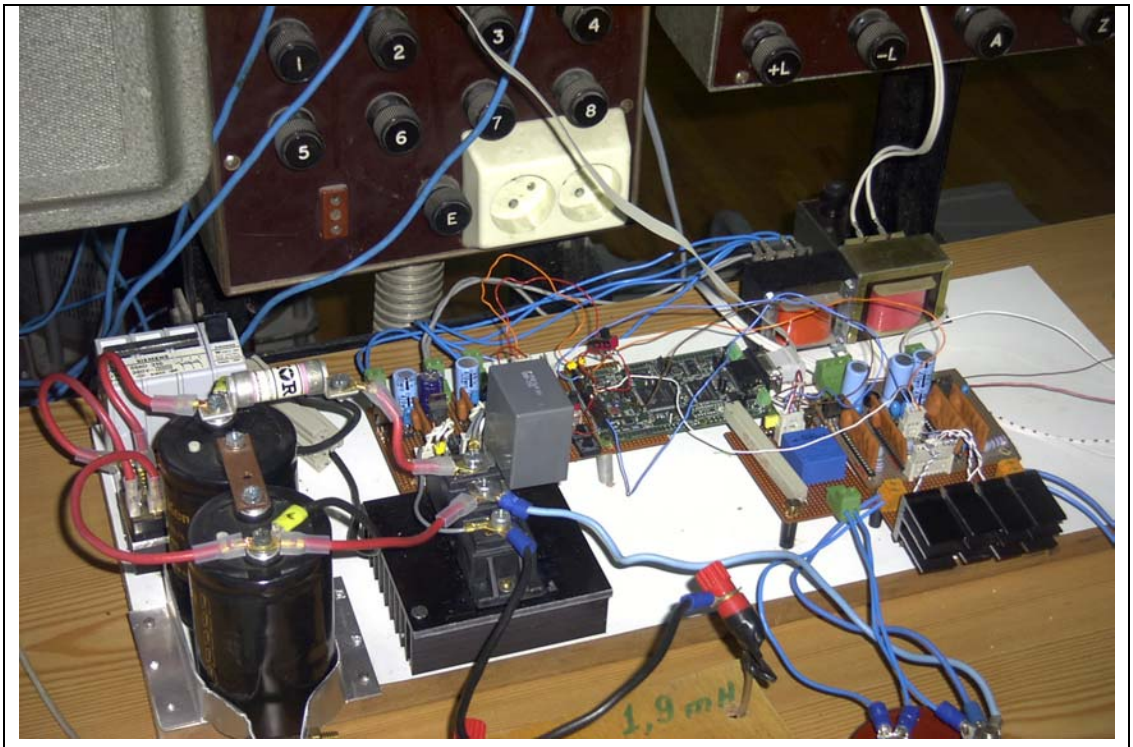

Figure 4.10 Experiment Setup

4.2 Hardware

In the implementation phase of the study, as the aim is to proof of the concept given in section 2, some critical components of the hardware are selected so that they have 3-4 times rating values above the demanded ratings. Also some devices are chosen so that they give perfect performance compromising the cost such as voltage sensing LEM module.

As discussed in previous chapters the overall system has two basic functional stages that are DC-DC converter and H-bridge inverter. The purpose of the DC-DC converter is generating a rectified DC-link, and the inverter is to invert the rectified DC-link to form a sinus waveform.

However experimental set up used may be investigated as having three parts. The separation into parts is based on the functions.

- Power Stage of the Circuit
- Gate Drive and Protection Circuits
- Control Circuit

4.2.1 Power Stage of the Circuit

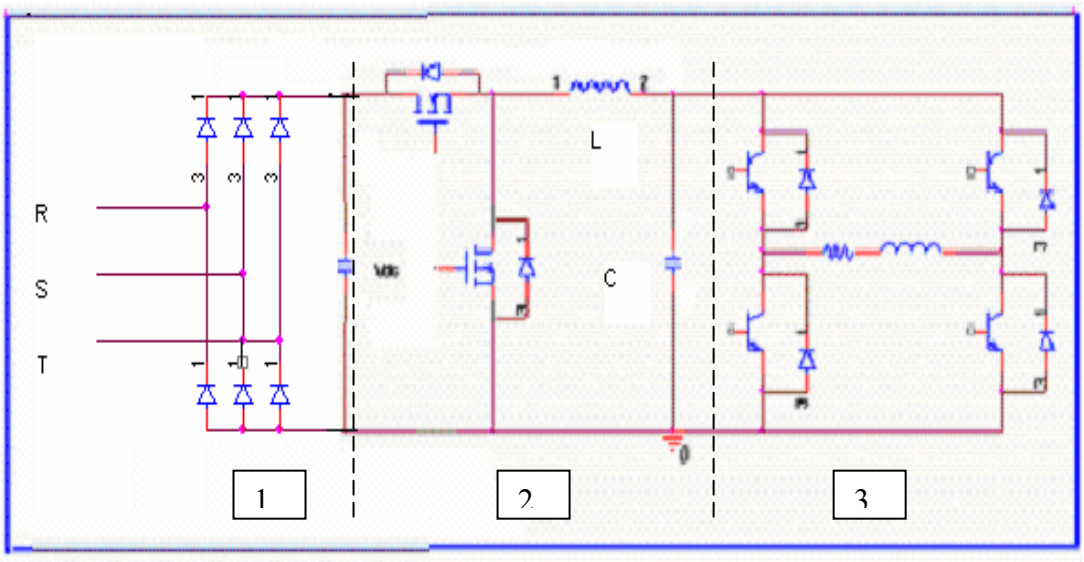

Figure 4.11 Power Stage of the Circuit

Power stage can be divided into three parts as shown in figure 4.2 Each part is indicated with numbers.

1. Input DC bus (including 3-phase bridge rectifier)
2. DC-DC converter (including 2 IGBT's and Filter inductor and capacitor)
3. Output Inverter (including 4 power mosfet's and load)

In order to obtain DC link of the power stage of the overall system shown by #1 in figure 4.11, line voltage V_{rms} = 380 V is converted into DC by using a standard 3-phase uncontrolled bridge diode rectifier and a filter capacitor is used to eliminate voltage ripples. The leads in the DC-link between the input filter capacitor and the power semiconductor devices have stray inductances. These inductances may cause voltage spikes on the power semiconductors. In order to reduce the effects of these

stray inductances the connection is kept as small as possible and filter capacitor of the bridge rectifier is connected to the DC-DC converter switches as close as possible.

In the DC-DC converter stage shown by #2 in figure 4.11, 2MBI50N-120 Dual IGBT module was used as the controlled switches as discussed in section 2.4.3 The basic specifications of the IGBT module are as follows

- 1200 V, 50 A
- Over current Limiting Function (4-5 Times Rated Current)
- Integrated Gate to Emitter protection zener diodes.

Detailed Information about the IGBT module is given in appendix A3.

In order to absorb the surge voltage on the DC link, a snubber capacitor is also used in the DC-DC converter stage.

At the output of the DC-DC converter, there is a low-pass filter consists of an inductor and capacitor as shown by #2 in figure 4.11. This filter inductor is designed for high frequency application and detailed information about the core material is given in the appendix A.3. The capacitor is polypropylene film type which is suitable for high frequency applications. Detailed information about this capacitor is given in appendix A3.

In the output inverter stage shown by #3 in figure 4.11, four IRF 740 power mosfets were used in order to invert the signal at the output of the DC-DC converter stage. This stage is operated at low frequencies and also the switching instants are at the zero voltage crosses of the rectified DC-link voltage thus eliminating the switching losses. Mosfets used here have rather higher turn on resistances. BJT's can be used to reduce the conduction losses of the output stage so the efficiency of the system will be improved. Discussion on this topology was made in section 2.2.1.2.4

and shown in figure 2.11. The basic specifications of the each mosfet are given in the following:

- 400V, 10A
- Typical $R_{DS}(on) = 0.46\Omega$
- Low gate charge

Detailed Information about the mosfet IRF 740 is given in the appendix A3.

4.2.2 Gate Driver and Protection Circuits

For proper operation of an IGBT, the gate signals are required to be +15V for high state, and -5V for low state. EXB-840 of Fuji Corp. gate driver hybrid integrated circuit is used in this application. Basic features of EXB-840 are given as:

- Up to 40 kHz operation
- Built-in photocoupler for high isolation voltage 2500V AC for 1 minute
- Single supply operation (requires +20V DC supply)
- Built-in over current protection circuit
- Over current detection output

Detailed Information about the gate driver hybrid EXB 840 is given in appendix A3.

The over current detection output generates a signal if a short circuit fault occurs on the IGBT. This signal of the EXB-840 must be processed to provide the necessary protection for the gate drivers and the IGBT's. A protection circuit is designed based upon the over current detection output of the gate driver the circuit diagram of the protection and gate drive circuit is shown in figure 4.12. the protection circuit consists of two R-S latches, two optocouplers, and necessary logic gates each for one IGBT. The operation of the circuit is discussed briefly below

In normal operation (no-fault), the output of the R-S latches are both high. Each of these signals is applied to distinct AND gates with the gate signals coming from the controller. Whenever a fault signal is generated by the gate driver hybrids, the SET input of the R-S latch goes low and the output of the R-S latch goes low and both gate signals are goes low immediately. Even if the fault situation cleared the gate signals are not applied to the IGBT's unless the RESET signal is applied to the R-S latch thus providing a complete protection for both IGBT's.

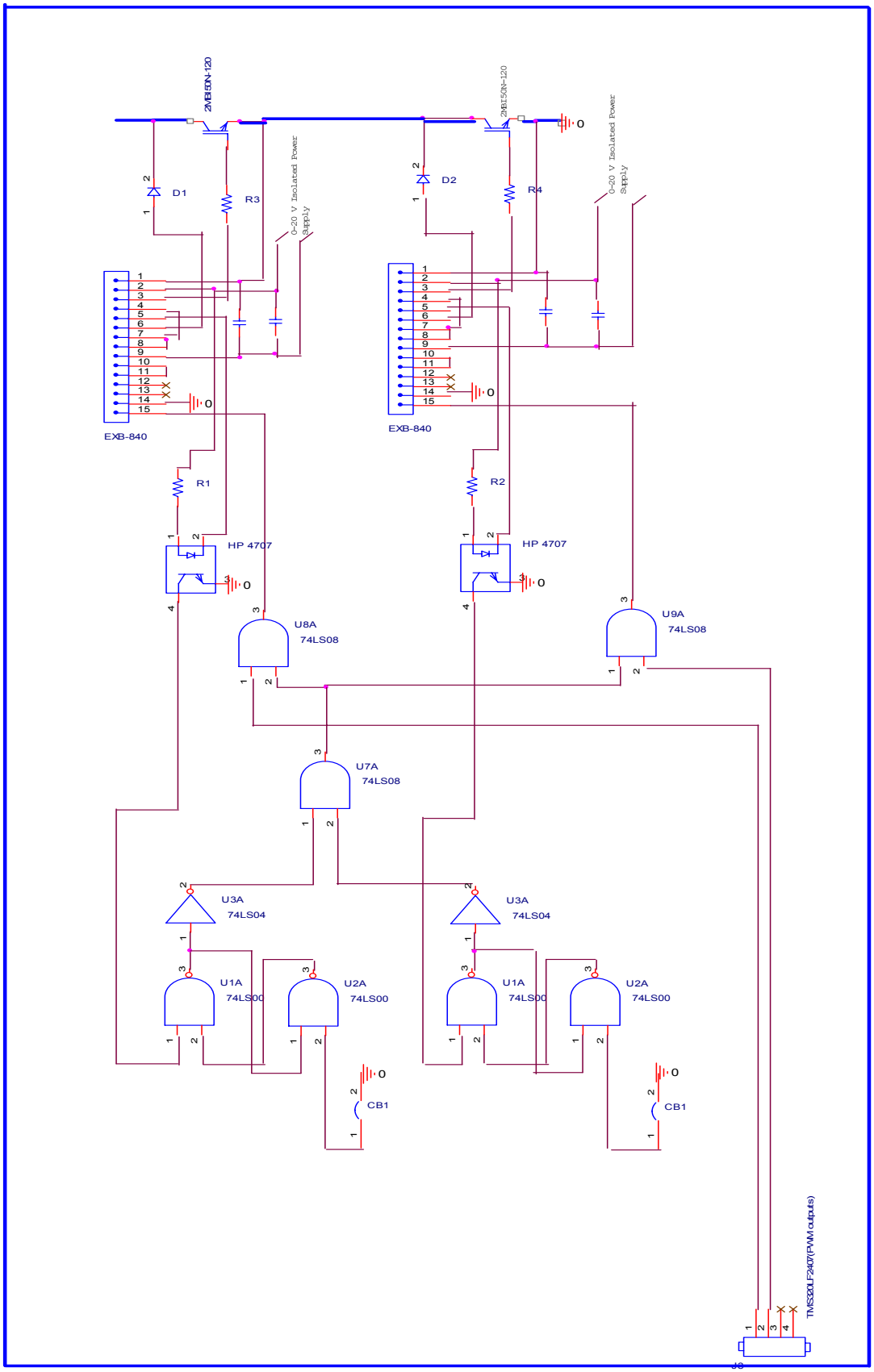

Figure 4.12 Circuit schematic of the protection and gate driver circuit

In the output inverter stage, the same gate driver circuit used in DC-DC converter stage is used to drive the mosfets.

4.2.3 Voltage Sensing Circuit

In order to obtain satisfactory operation of the system, the output voltage must be controlled by taking samples from it and regulate depending upon the error between the reference and the actual value as discussed in section 2.4.2.2. The output voltage can be measured with a simple voltage divider but its accuracy may not be satisfactory. In this thesis, a new circuit concept is analyzed so proving the concept is more important then struggling with details. For this reason in order to get reliable voltage measurement results (without any noise problems), a voltage transducer is used in stead of a voltage divider as the sensing device. LEM LV-25P voltage transducer is used in this project. Connection and schematic of the voltage sensing circuit is shown in figures 4.13 and 4.14 respectively.

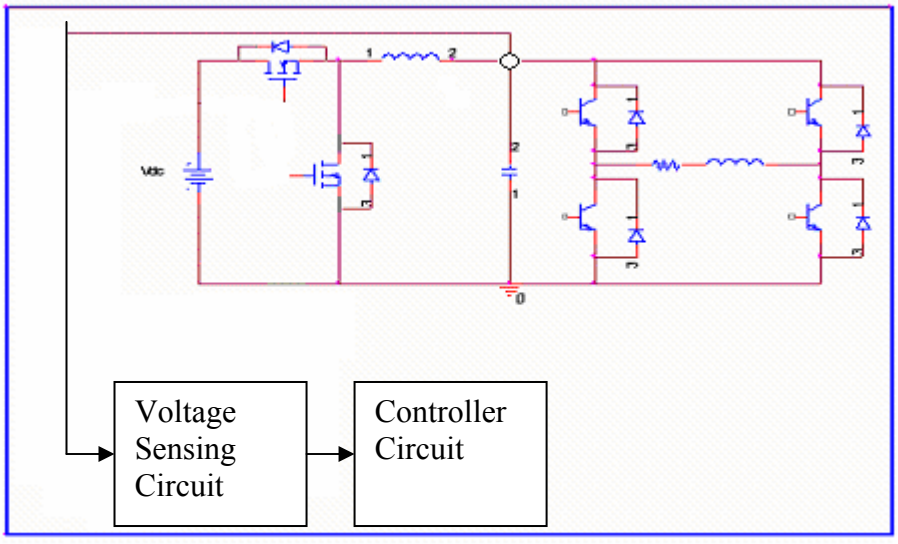

Figure 4.13 Connection of the Voltage Sensing Circuit

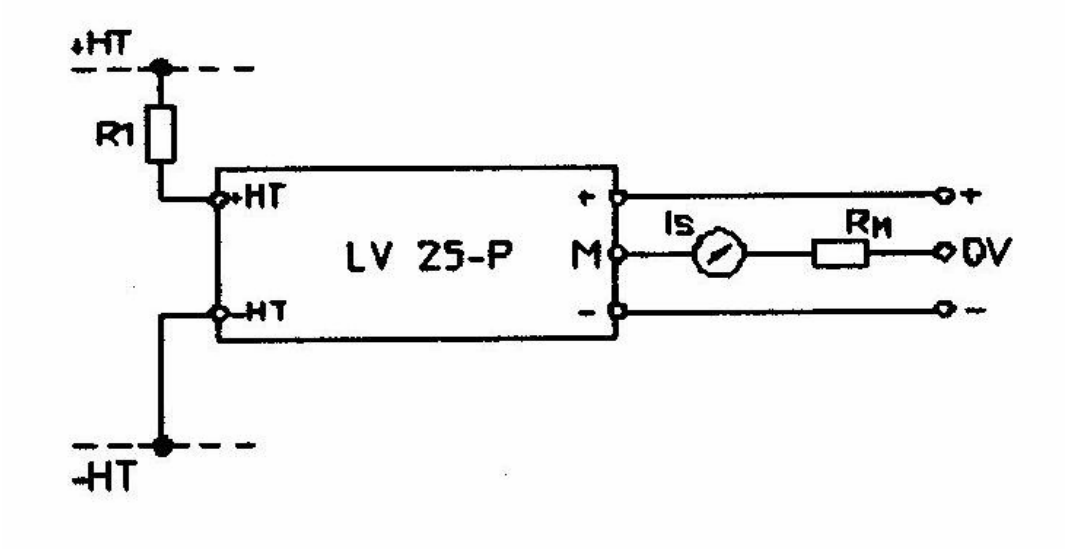

Figure 4.14 Schematic of the voltage Sensing Circuit

Basic features of LV-25P are given below

- Closed Loop (compensated) voltage transducer using the Hall-Effect principle.
- Ipn = 10mA, Vpn = 10..500V
- Galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit).

Detailed Information about the LV-25P LEM voltage transducer module is given in appendix A3.

4.2.4 The Controller

The controller used in this study is composed of a Digital Signal Processor. In power electronics laboratory an application software development kit with digital signal processor (DSP) of Texas Instruments TMS320LF2407A, of Technosoft Corp. was available. The software has a user interface called DMC Developer Pro, providing a code generation interface and built-in compiler, builder and debugging tools. This development kit is used throughout the experimental studies although far

less sophisticated microcontrollers could be sufficient to do this task. Basic features of the TMS320LF2407A are given in the following:

- TMS320LF2407 running at 30/40 MHz
- 64-kB 0-wait state external RAM
- 2x12-bit accuracy D/A outputs
- RS-232 and JTAG interfaces
- 16 channel,10 bit A/D converter. (400 ns conversion time)
- Six PWM outputs with internal dead-time generating register.

Detailed Information about the TMS320LF2407A DSP is given in appendix A3.

The controller circuit used in this study has three basic functions. First, it takes the analog voltage measurements of the voltage sensing circuit as shown in figure 4.13 and converts them to digital quantities, using its built-in Analog-Digital Converter. Second function is to generate necessary PWM signals for the gate drive circuit of the DC-DC converter semiconductor switches (IGBT's).. To do this the measurement from the ADC converter is compared with the reference and applied to a PI controller as mentioned in section 2.4.2.2.1. The third function of the controller circuit is to detect the zero voltage cross of these rectified sinusoids, and generate necessary gate signals for the semiconductor switches (mosfets) of the H-bridge inverter.

The input to the DSP is the analog voltage measurement coming from LEM module as discussed above and enters to the ADC pins. The output of the DSP is the gate signals for both DC-DC converter IGBT's and output stage mosfet's. The output signals are generated at the PWM pins of the DSP and goes to the related gate driver integrated circuit.

4.3 Software

The purpose of the software is to realize all the control algorithms that are mentioned in section 2.4.2.2.1. The reference voltage is defined in the software as a look-up table. By this software the voltage measurement is converted to digital with the DSP. The result is then compared with the reference and the error is processed by the software within a PI loop. The reference is defined in a look-up table and at each interrupt service routine the controller reads the necessary reference voltage from this table as shown in Appendix A.1 Then the necessary initializations of the PWM ports are done. Then the basic function of the software that is to generate the necessary gate signals for the controlled switches is generated at the related PWM ports of the DSP. The software is developed in DMC Developer Pro which is an interface program between DSP card and user. It has a built-in C compiler and runs in the Windows O.S. environment.

Two programs are developed during the course of this study, one is for open loop operation (without feed back from output voltage of the DC-DC converter), and the other for closed loop operation (taking feed back from the output voltage of the DC-DC converter). The basic flow chart of the programs for two control strategies is given in the next parts. The detailed flow charts and source codes written in C and assembly are given in appendix A2.

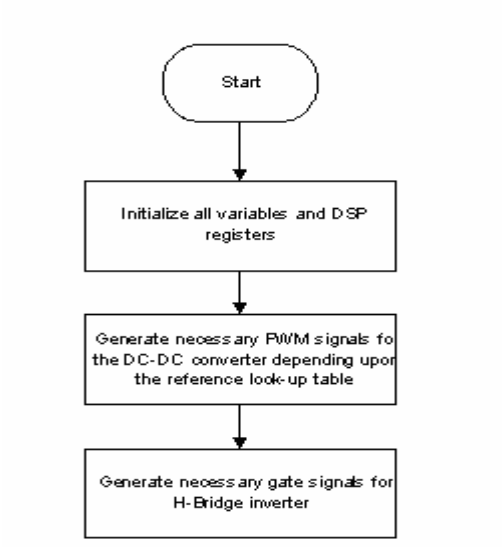

Figure 4.15 Basic flow-chart of the software for feed-forward control

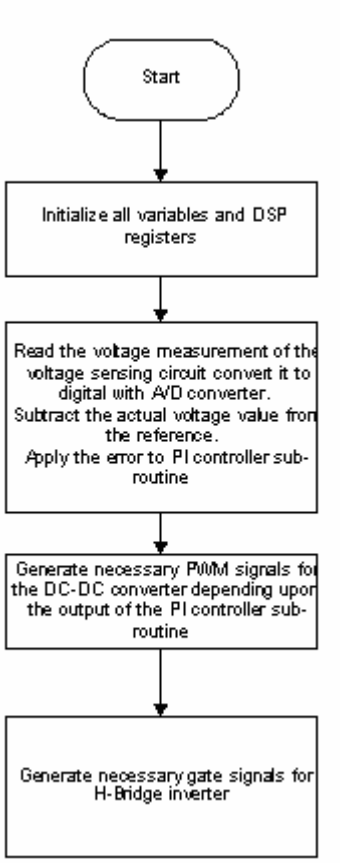

Figure 4.16 Basic flow-chart of the software for closed loop control

4.4 Experimental Study and Verification of Theoretical Calculations

In this section, results of the laboratory experiments are shown. As discussed many times in the previous sections, the purpose of this thesis is to generate a rectified DC-link and than invert the voltage at this link to generate pure sinusoidal voltage. So at each step of the experiments, the load and the rectified DC-link voltages are obtained under different conditions. A systematic experimental procedure is followed. The purpose is to identify the open loop (feed forward) and closed loop performance of the converter at steady state. In other words to determine

a) Whether the output follows the reference voltage, and the level of minimum voltage achievable
b) The magnitude error
c) Distortion level (THD) of the output voltage and possible causes

d) Identify device stresses
e) Identify efficiency of the system and causes of the losses
f) Determine the effect of load power factor variations on the capability of the converter to follow a specified reference voltage.

The experiments are carried out at 10 Hz, 50 Hz, and 100 Hz at no load and full load (1kVA) conditions. In order to determine the level of minimum voltage achievable, the voltage level of frequencies of 5 Hz and 10 Hz is adjusted to keep the V/f level at 50 Hz (220V/50Hz). The effect of the load power factor variation on the converter output is tested at 50 Hz.

All experiments are carried out at steady state conditions. In this work, input power factor correction algorithms are not employed. Note that to achieve this purpose only additional software is needed. Hardware modifications are minimal.

The results presented in the following sections are obtained with TEKTRONIX TDS3400 digital phosphor oscilloscope.

4.4.1 Experimental Results of Feed Forward Control Operation

In this section the experimental setup is operated for feed forward control. In feed forward control operation there is no feedback taken from the rectified DC-link as mentioned in section 4.2.3. The reference voltage waveform available as a look-up table in the controller software is directly applied to the IGBT's. The experiments for the feed forward control operation are done first for no-load case. Then a series combination of adjustable resistances and inductances available in the laboratory are connected as load. The system is then operated for full load case (1 kVA). Cos ϕ is adjusted to 0.8. The measurements are taken for 10 Hz, 50 Hz, and 100Hz. At each frequency level the rectified DC-link and load voltages are obtained with differential voltage probes. For all steps, magnitude error between actual waveform and the reference is obtained with the scope. Also THD levels of the waveforms are calculated approximately by using the FFT property of the scope. Also input and

output powers of the system are measured and the efficiency of the system is calculated. These quantities are given in tables at the end of the section.

4.4.1.1 Experimental Results for No-Load Operation

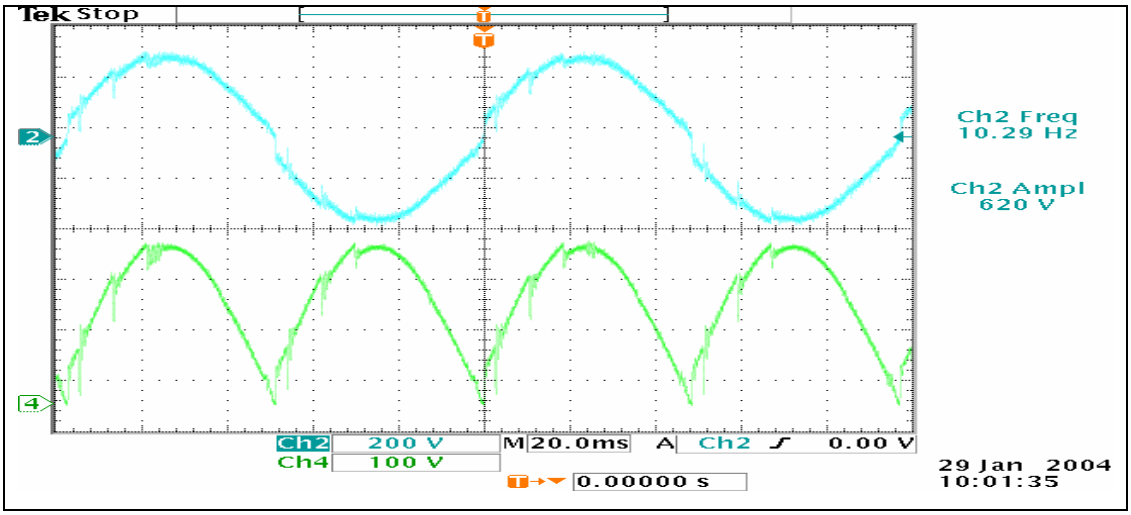

Figure 4.17 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 10 Hz.

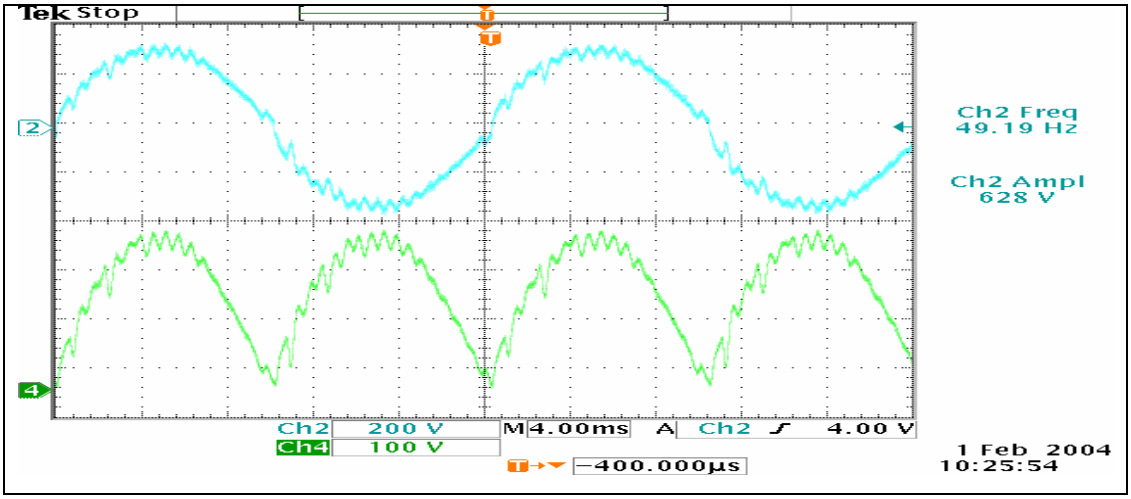

Figure 4.18 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 50 Hz.

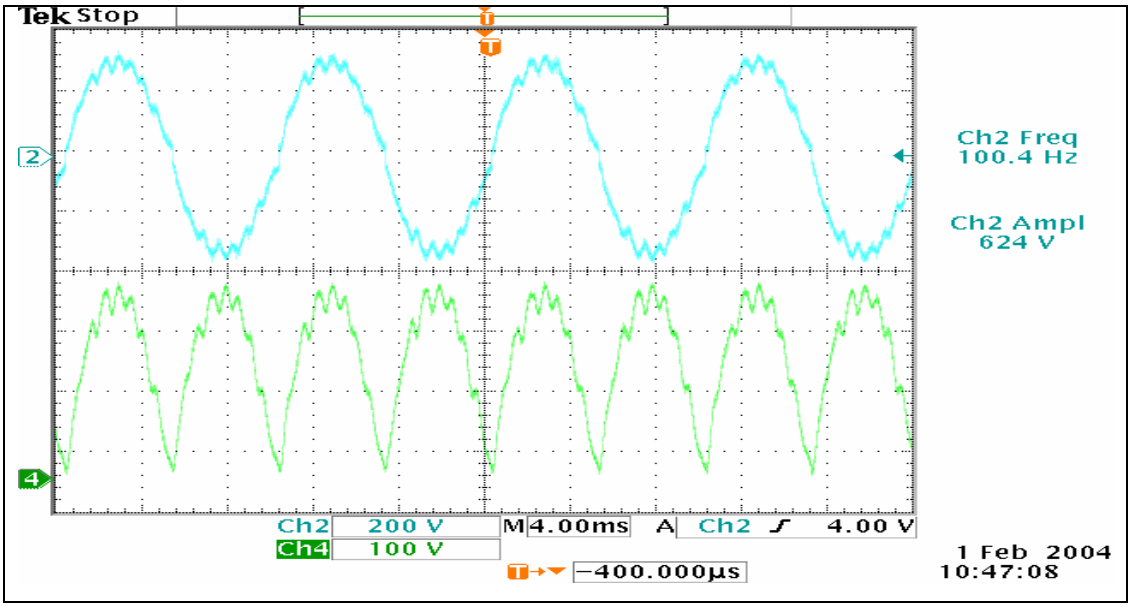

Figure 4.19 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 100 Hz.

4.4.1.2 Experimental Results for Full load Operation

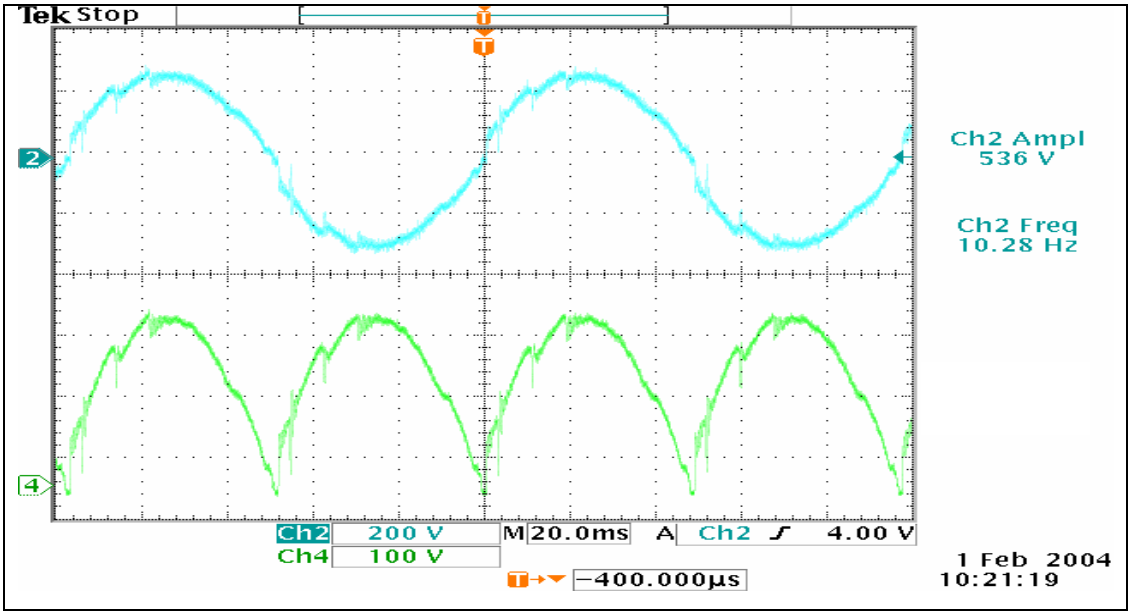

Figure 4.20 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 10 Hz.

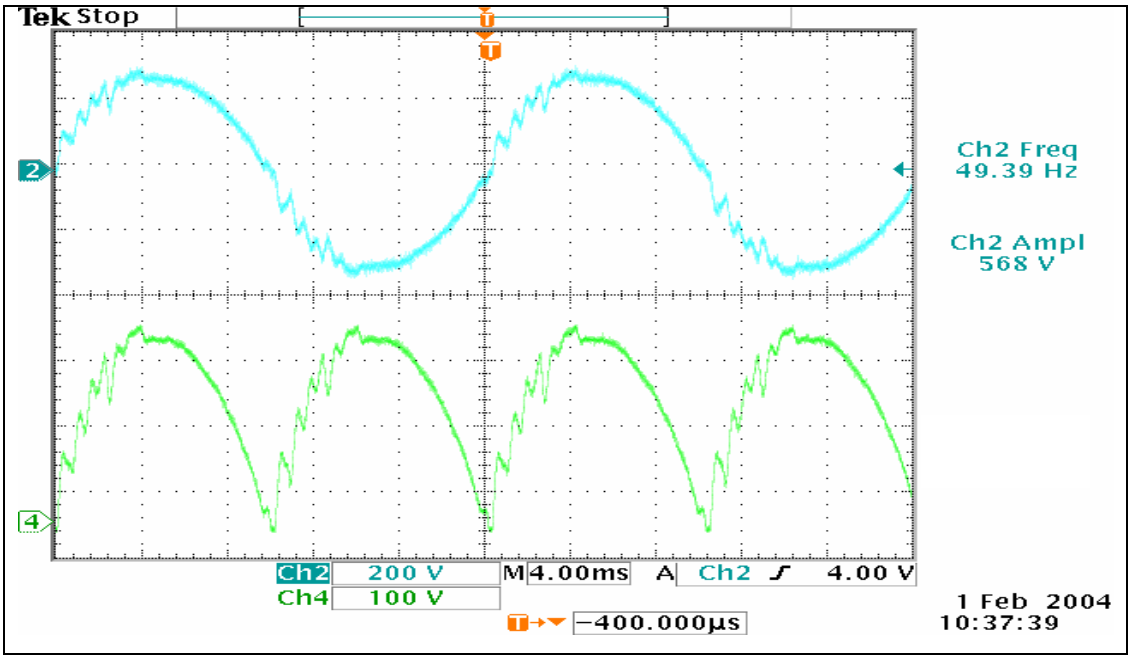

Figure 4.21 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 50 Hz.

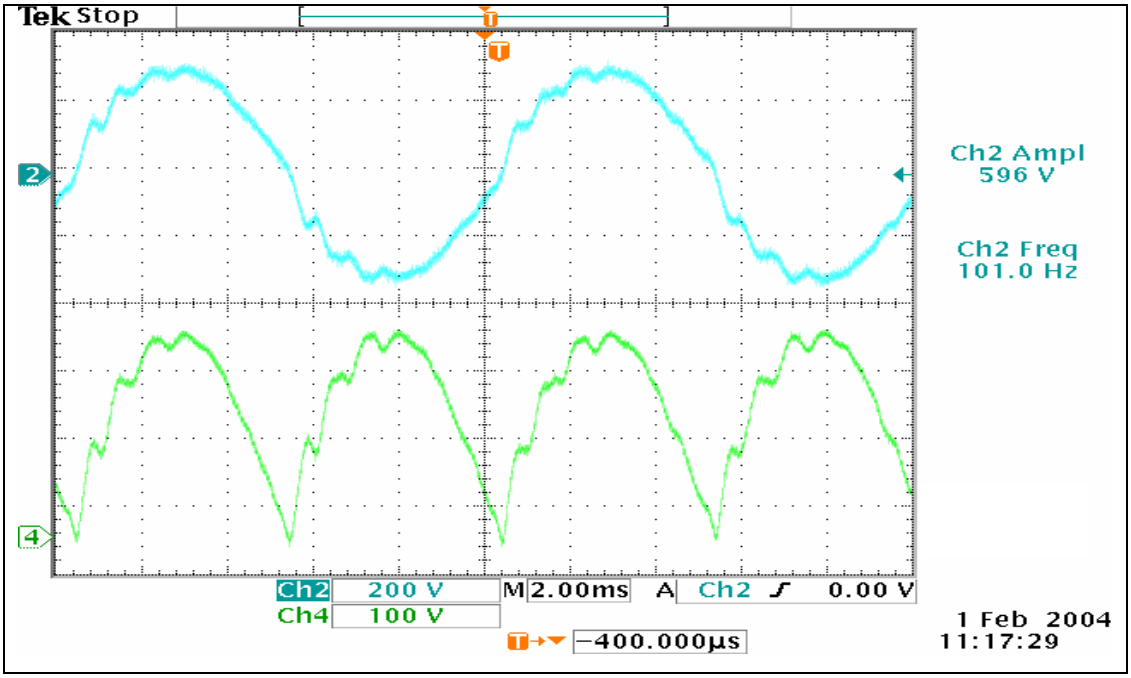

Figure 4.22 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 100 Hz.

Feed Forward Control Operation						
	No Load			Full Load		
	10 Hz	50 Hz	100 Hz	10 Hz	50 Hz	100 Hz
Magnitude Error (%)	0	0	0	14%	8%	4.5%
T.H.D (%)	7.76%	8.4%	8.32%	9.2%	9.48%	8.5%
Efficiency (%)	-	-	-	80%	85.6%	87%

Table 4.1 Performance Analysis for Feed Forward Control Operation

As it is seen from the waveforms and the performance table, the feed-forward control gave unsatisfactory results. The output tends to follow the reference but with oscillation. The frequency of the ripples on the voltage waveforms are approximately 1750 Hz. The cut-off frequency of the DC-DC converter filter is 1650 Hz. The possible reason of these ripples is the high gain of the DC-DC converter filter at the cut-off frequency in open loop case. The distortions on the waveforms are above the acceptable limits.

4.4.2 Experimental Results of Closed Loop Control Operation

As the feed forward control gave unsatisfactory results, the voltage on the rectified DC-link is regulated by a fed-back loop as taking voltage samples at each switching cycle, comparing with reference, calculating the instant error, regulating it in a PI control loop and then generating necessary switching signals. Same measurements and analysis done in section 4.4.1 are applied for closed loop operation experiments.

4.4.2.1 Experimental Results for No-Load Operation

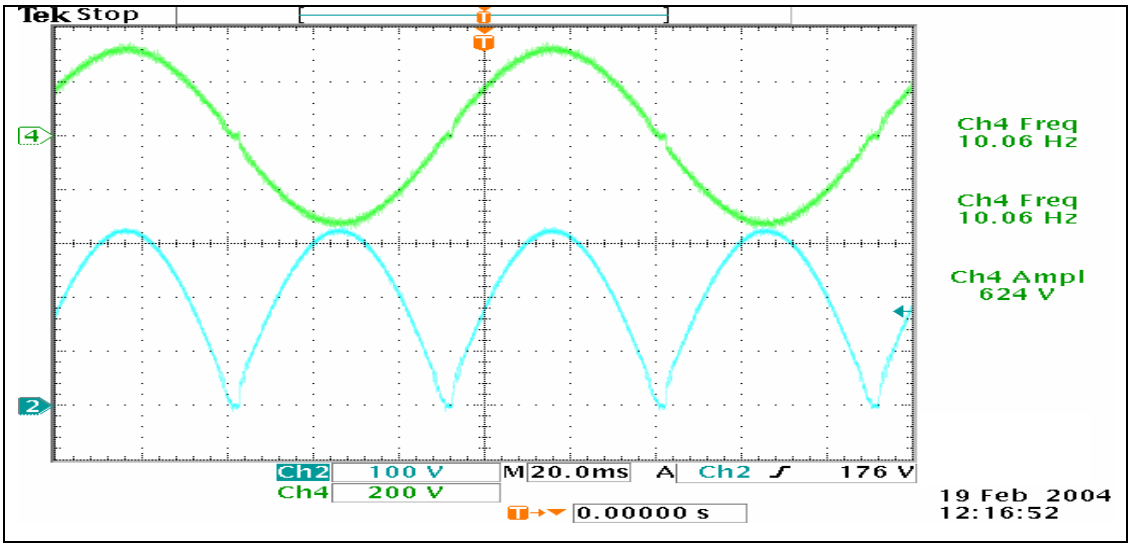

Figure 4.23 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 10 Hz.

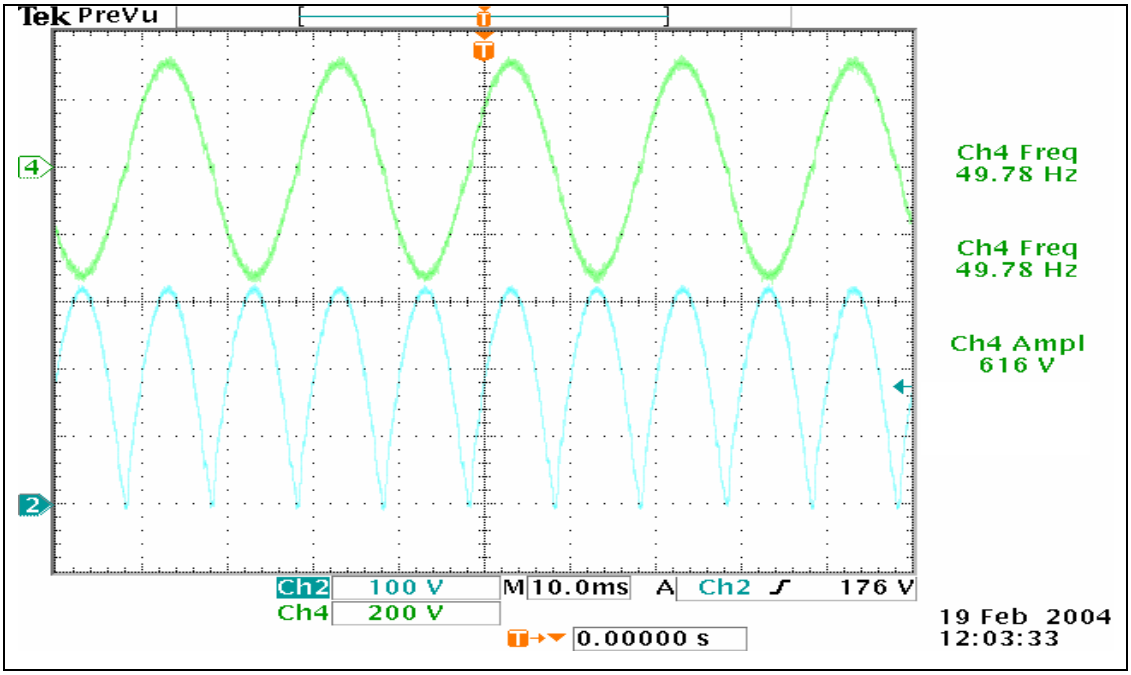

Figure 4.24 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 50 Hz.

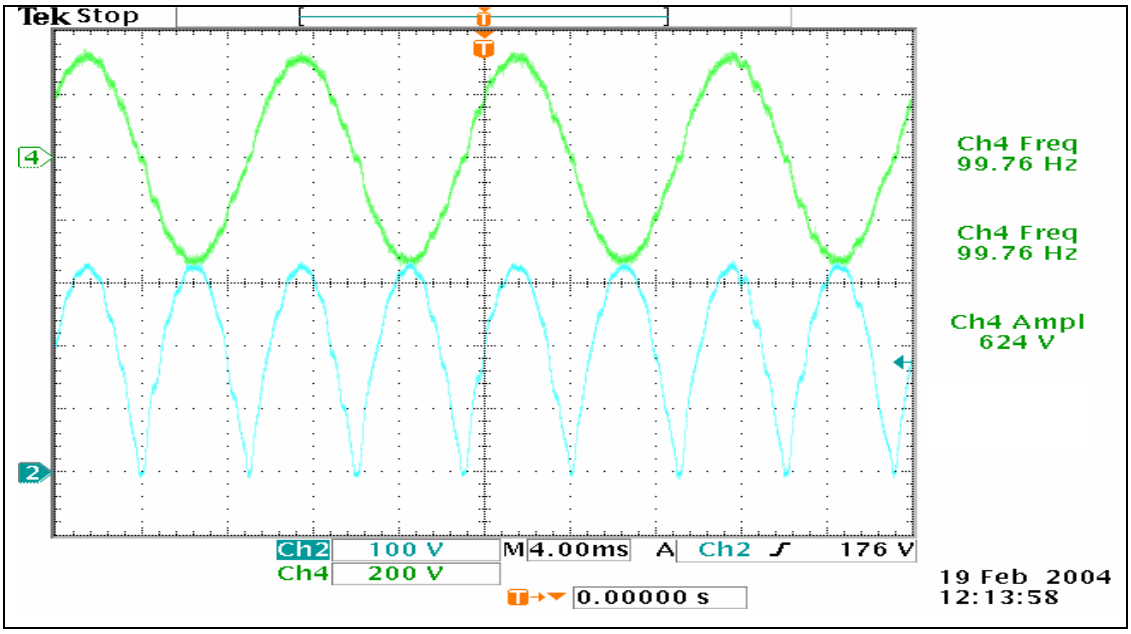

Figure 4.25 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 100 Hz.

4.4.2.2 Experimental Results for Full load Operation

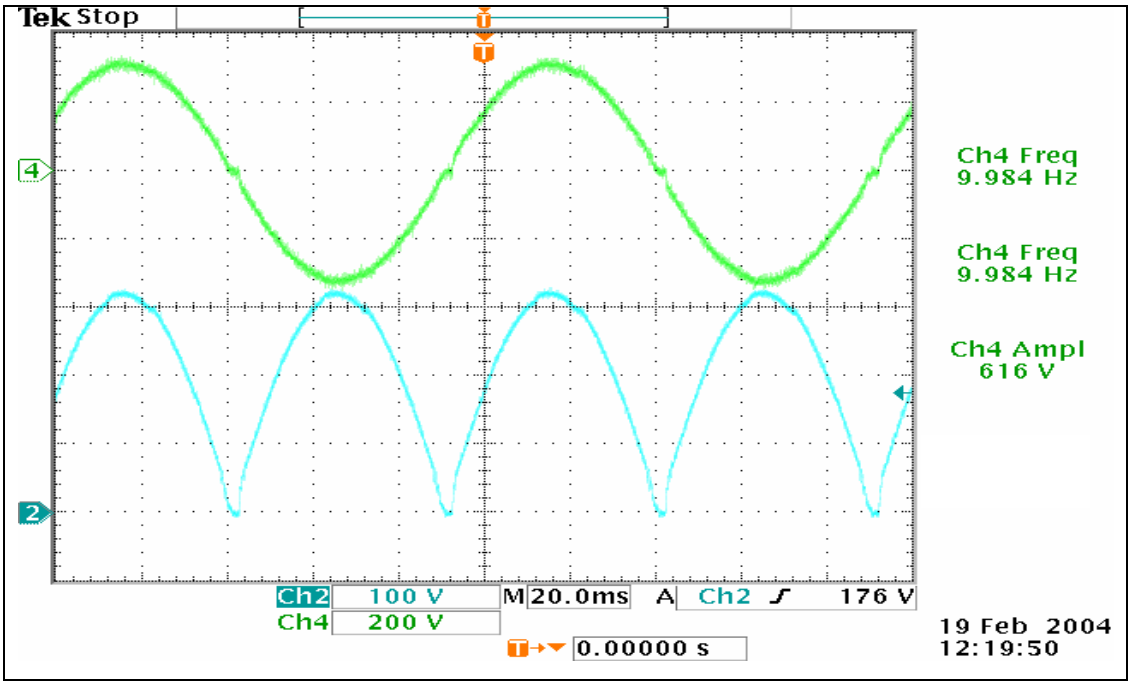

Figure 4.26 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 10 Hz.

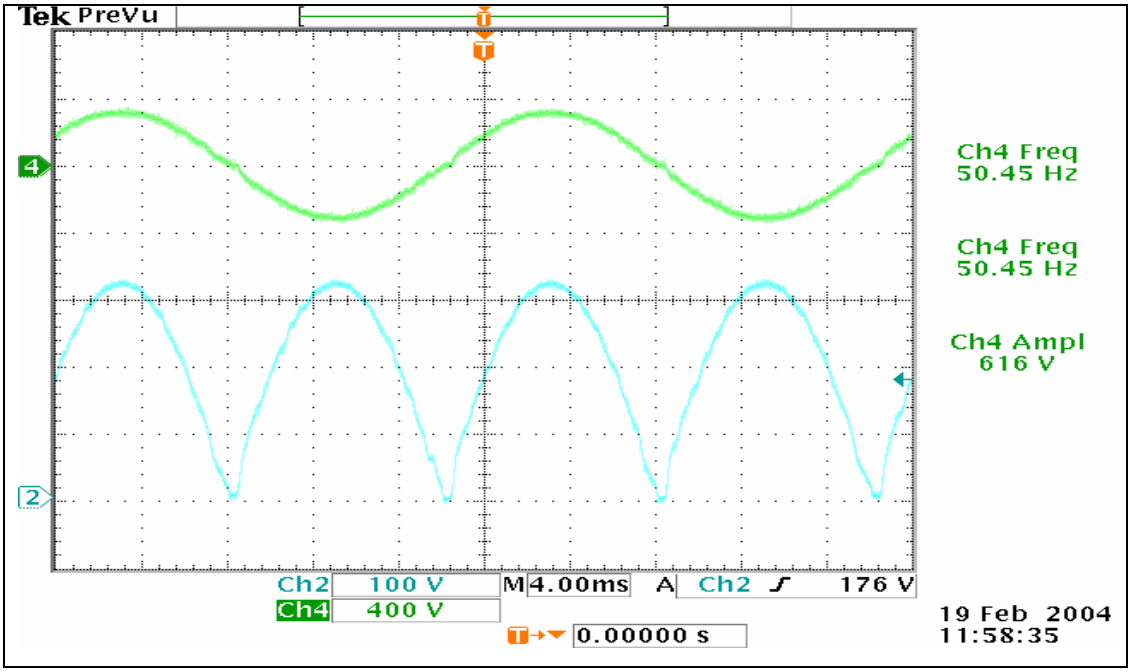

Figure 4.27 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 50 Hz.

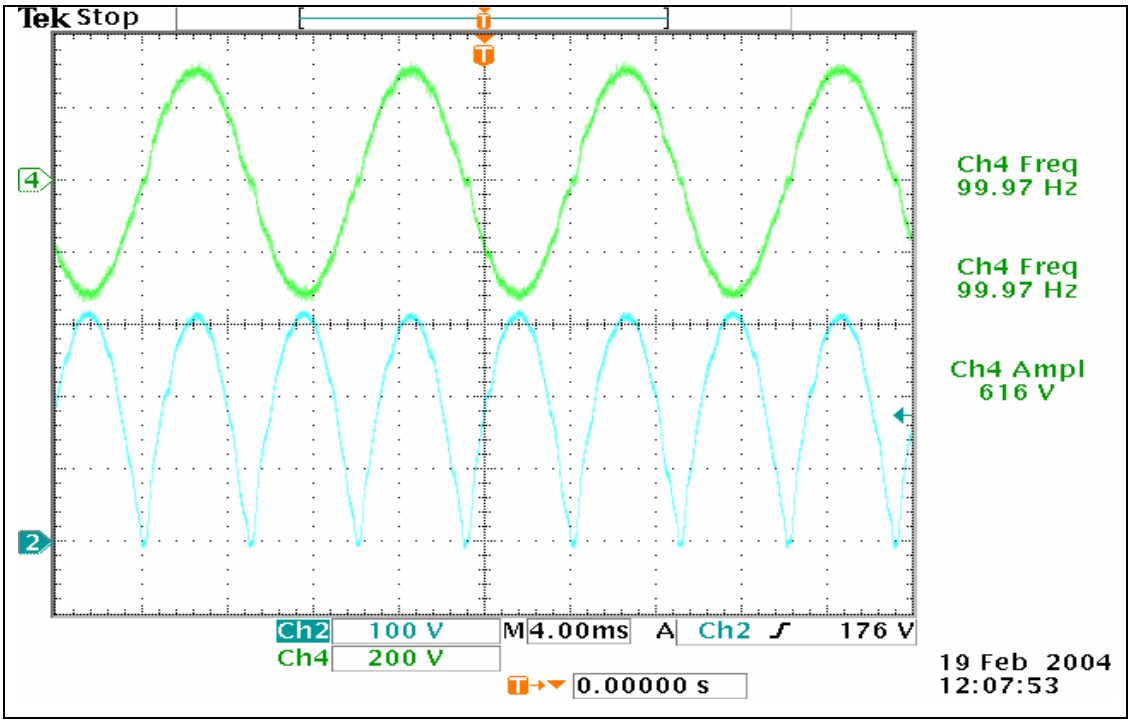

Figure 4.28 Rectified DC-link (upper waveform) and load voltages (lower waveform) at 100 Hz

Closed Loop Control Operation						
	No Load			Full Load		
	10 Hz	50 Hz	100 Hz	10 Hz	50 Hz	100 Hz
Magnitude Error (%)	0	0	0	1.9%	0.95%	0.95%
T.H.D (%)	1.21%	1.53%	1.93%	1.35%	1.71%	2.25%
Efficiency (%)	-	-	-	88.75%	89.7%	93.4%

.

Table 4.2 Performance Analysis for Closed Control Operation

The results for closed loop operation are much better then the ones obtained for the feed forward operation. THD and magnitude errors are decreased to acceptable levels. The existing small magnitude errors are caused by the voltage drop on the output stage mosfets. Also the efficiency of the system operating in closed loop mode is increased.

While calculating the input power, the current flowing into the input DC-link capacitor is used. As the input DC-link capacitor is too big (2200 μF) the frequency of the current is low and only flows whenever the input DC-link capacitor voltage tends to drop. Such a current waveform is shown in figure 4.29

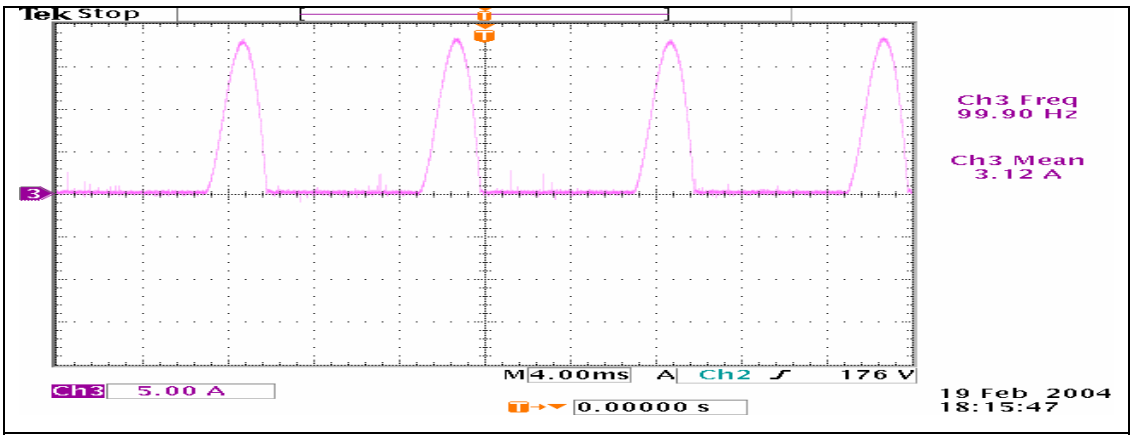

Figure 4.29 Input DC-Link capacitor current

4.4.3 Determination of the Level of the Minimum Achievable Voltage

In motor drive applications the output voltage is applied to the motor is generally a linear function of the frequency. At lower frequencies voltage level must be decreased to lower levels to preserve the V/f ratio. However going down to lower voltage values is a problem for digital controllers. In order to determine the level of minimum voltage achievable, the inverter is operated at 5 Hz and 10 Hz keeping the V/f level at 50 Hz (220V/50Hz). The results are shown in figures 4.30 and 4.31

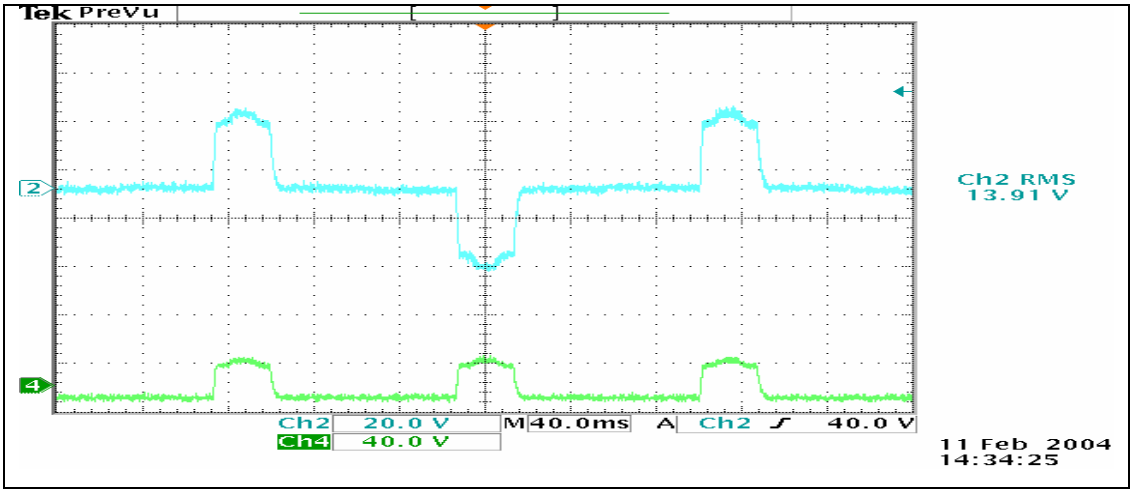

Figure 4.30 Constant V/f operation for 5 Hz and 22V_{rms} Upper waveform is load voltage and the lower one is rectified DC-link voltage

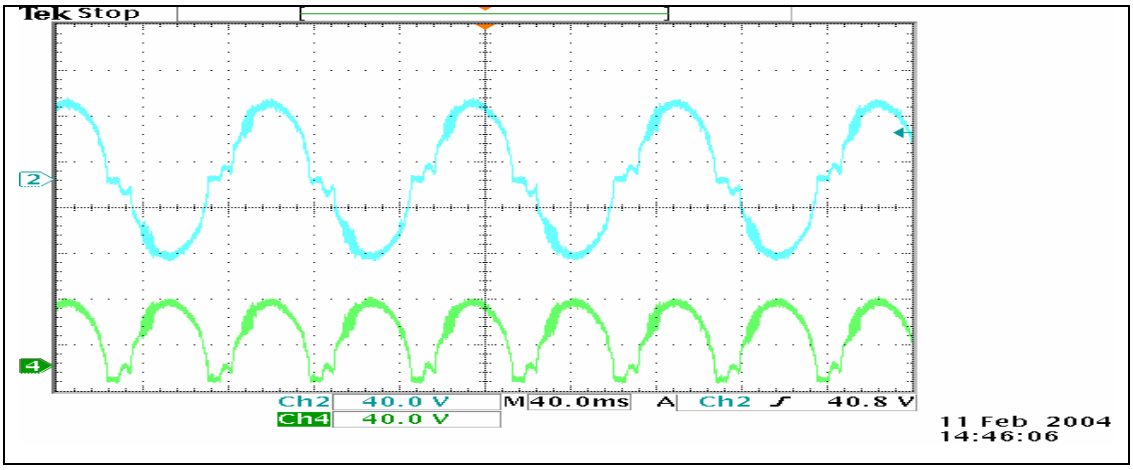

Figure 4.31 Constant V/f operation for 10 Hz and 44 Vrms Upper waveform is load voltage and the lower one is rectified DC-link voltage

As shown in the above figures the output voltage waveforms are distorted even if closed loop control is applied. In order to understand the causes of the distortion, actual PWM generating principle should be reviewed.

In theory, the maximum duty cycle of each switch in the DC-DC converter can be unity. But in actual case (especially for two switches in one lag case), two switches should never fired at the same time in order to prevent any short circuit situation. To realize this time delay called "dead time" is injected between two switching signals that is 4-5 μs thus reducing the achievable maximum and minimum duty cycles.

In this study dead time is adjusted to be 2.6 μs also switching period is 66 μs (for switching frequency of 15000Hz). So 5 μs of the period becomes useless. Because there are two dead time durations in a switching period. Minimum achievable duty cycle is then 5/66 = 0.075. The input DC link is 400 V so minimum achievable output voltage level of the DC-DC converter is 30V. As the voltage reference is reduced below 30 V the controller applies 0 signal to the IGBT's. This is clearly seen in figure 4.30 for 5 Hz and 22V operation. For 10 Hz, 44V operation the system tends to follow the reference but as not good as higher voltage references. Below 10V the output voltage can no longer follow the reference voltage.

For lower voltage values the switching frequency is to be decreased in order to widen the switching period and so the ratio of dead time to switching period is decreased providing smaller duty cycle values and much satisfactory results for the lower voltage levels.

4.4.4 The Effect of Power Factor on Inverter Operation

In this section the system is operated at full load (1kVA) at different power factors such as pf = 0, 0.3, 0.8 and 1 at 50 Hz. Results are as shown in figures 4.32, 4.33, 4.34 and 4.35 respectively.

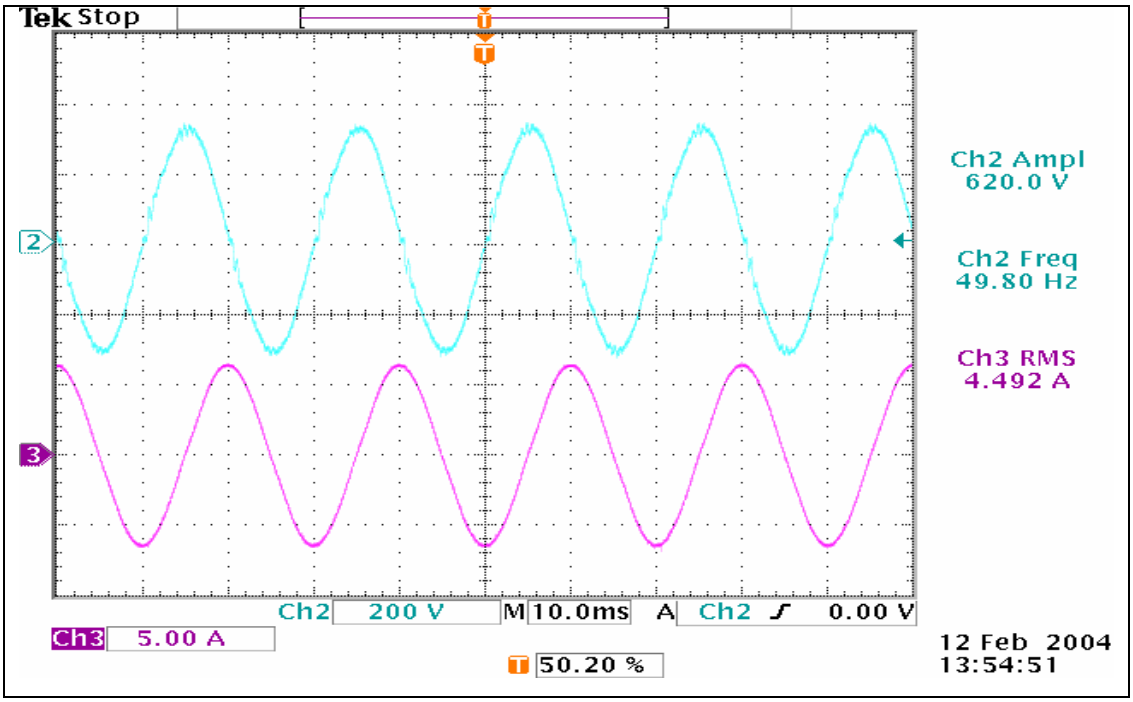

Figure 4.32 Load Voltage and current at 1 kVA with pf = 0

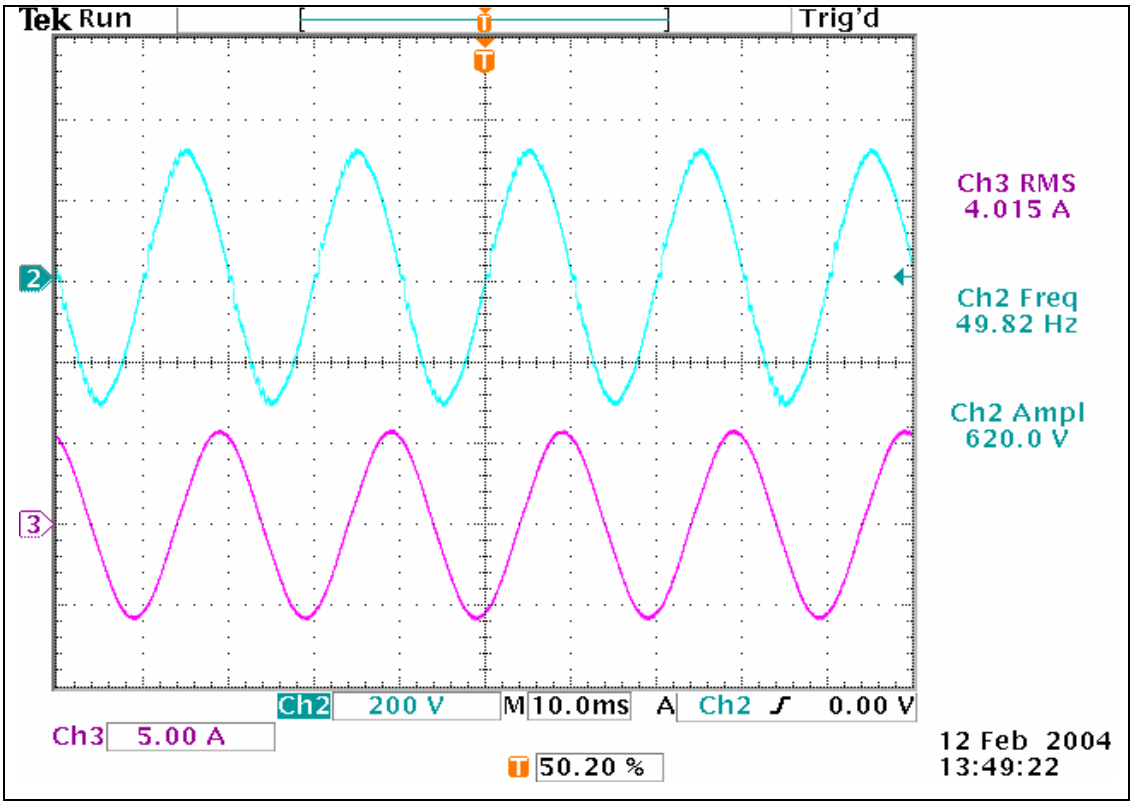

Figure 4.33 Load Voltage and current at 1kVA with pf = 0.

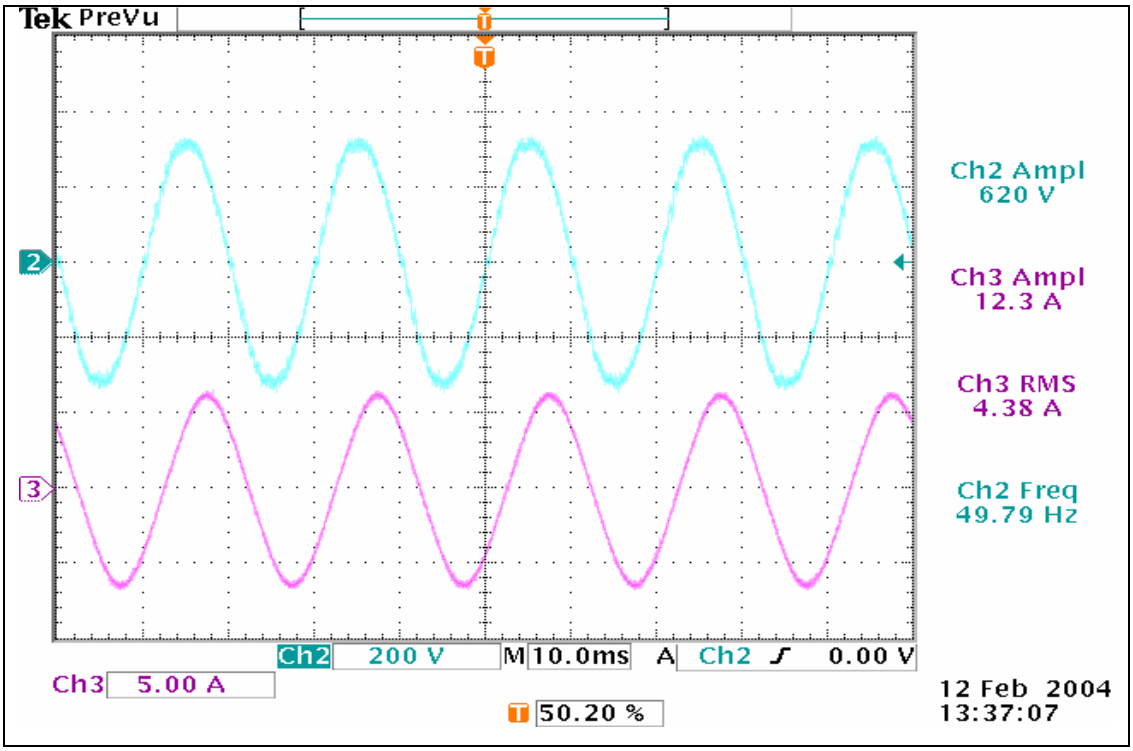

Figure 4.34 Load Voltage and current at 1 kVA with pf = 0.8

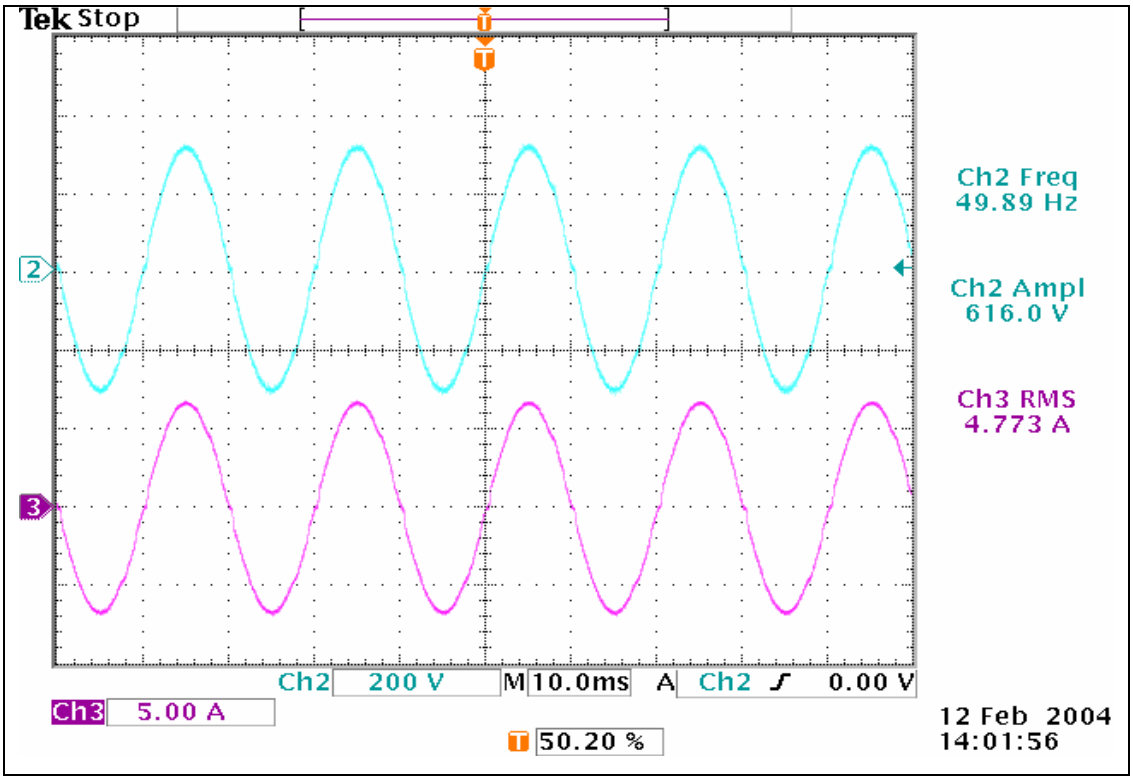

Figure 4.35 Load Voltage and current at 1 kVA with pf = 1

Table 4.3 Performance Analysis at different Load power factor values

Effect of Load Power Factor Variations				
	pf = 0	**pf = 0.3**	**pf = 0.8**	**pf = 1**
Magnitude Error (%)	**0.64 %**	**0.64%**	**0.64%**	**1.29%**
T.H.D (%)	**2.55 %**	**2.16 %**	**1.65 %**	**1.39 %**

As it is seen both from the figures 4.31, 4.32, 4.33, and 4.34, and table 4.3, the inverter operation does not affected with the variation of the load power factor. The worst case, pf = 0 has the highest distortion and as the pf decreases to 1 distortion also decreases. This is the result of increasing inductive current flowing into the rectified DC-link capacitor.

4.4.5 Stresses on the Semiconductor Switch

The voltage and current level on the DC-DC converter IGBT is obtained and given in figures 4.36, 4.37 and 4.38. The turn-on and turn-off characteristics of the IGBT are given in figure 4.39. The problem is the voltage and the current rating of the switches used in the DC-DC converter.

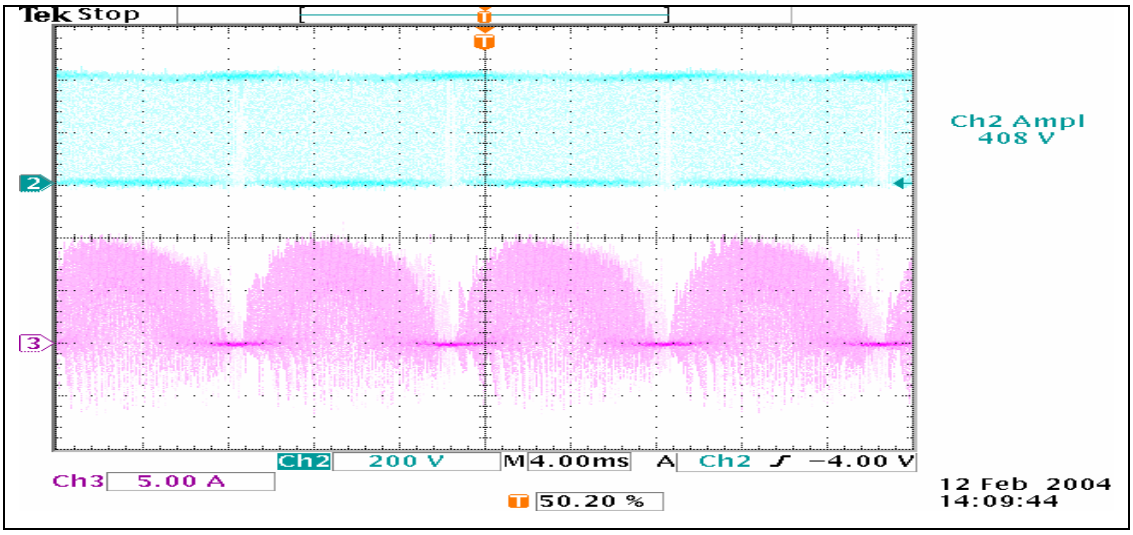

Figure 4.36 Voltage and Current on the DC-DC converter IGBT

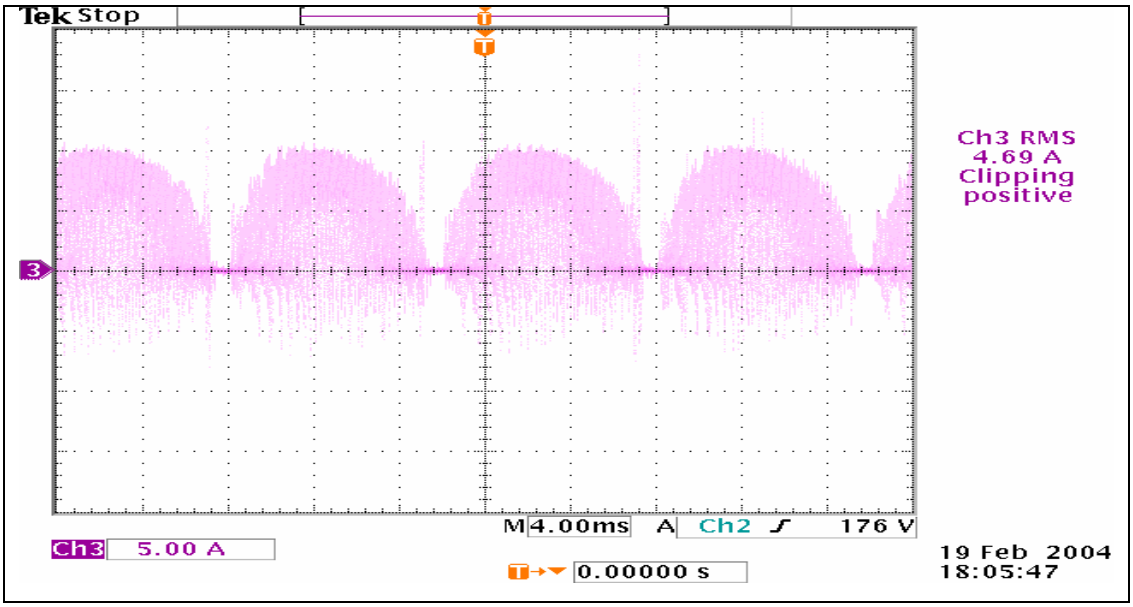

Figure 4.37 IGBT Current for full load (1 kVA) at pf = 1

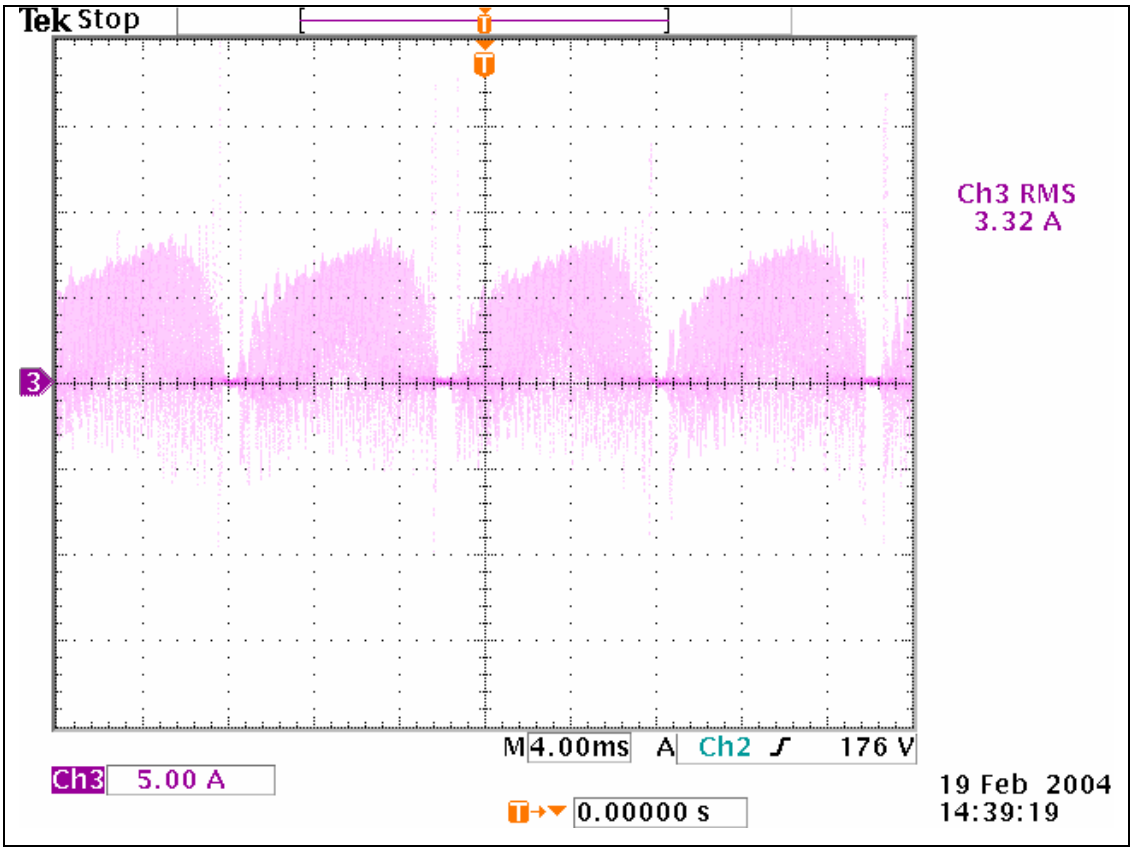

Figure 4.38 IGBT Current for full load (1 kVA) at pf = 0.8

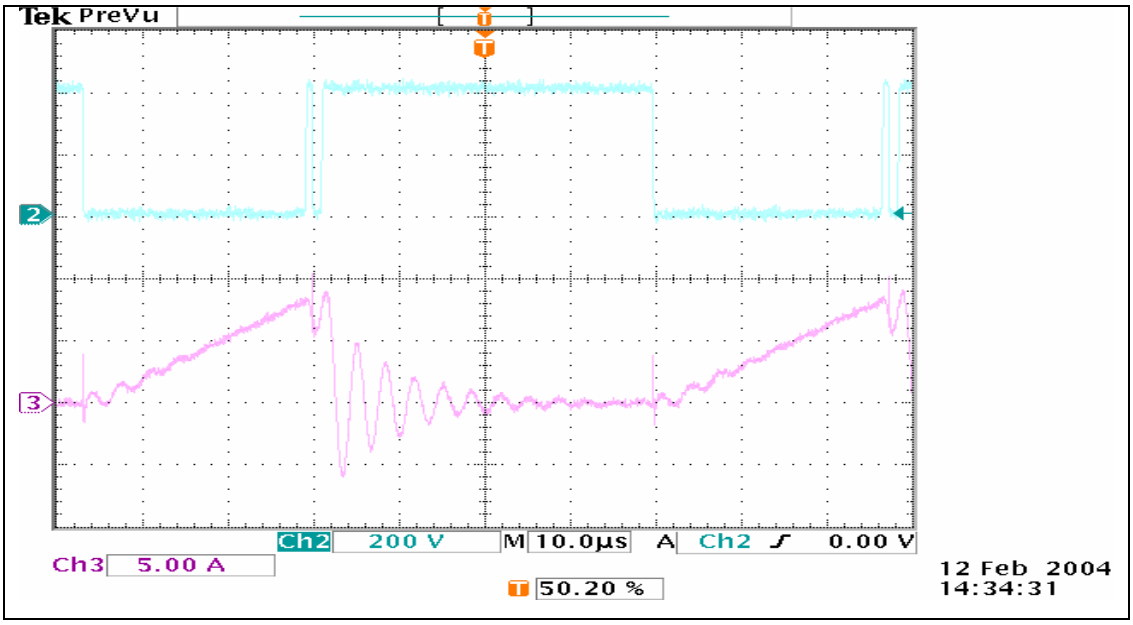

Figure 4.39 Turn on and turn off characteristics of the DC-DC converter IGBT

As seen in figure 4.36 the maximum voltage level on the IGBT is input DC link voltage and the maximum current level is approximately 9 A when the load is 1 kVA. The maximum voltage of the switches is the DC-link voltage, and as the input capacitor is too big, there are no ripples or spikes on the switches. Also figures 4.37 and 4.38 shows the IGBT currents for full load (1 kVA) at pf = 1, and pf = 0.8 respectively. The maximum peak current is also approximately 9 A for pf = 1 and 8 A for pf = 0.8. rms values of these currents are 4.69A and 3.32A for pf=1 and pf=0.8 respectively which are proper values for the chosen power levels. The peak currents are approximately two times of the rms currents. These results show that the switches used in the DC-DC converter stage have ratings slightly higher than the ones used in a conventional DC-AC inverter.

4.4.6 Inductor Losses at 15000 Hz

As discussed in chapter 3, the filter inductor in DC-DC converter stage is designed using ferrite core, however in experimental study, since the ordered inductor was not available on time, an air core conventional inductor is used. The inductor has 60 turns with a solid conductor has an area of 2.5 mm^2. As a result of

high frequency operation, a solid conductor inductor has higher resistance than a bundled conductor. Thus the inductor losses are expected to be higher. The AC resistance of the inductor is calculated at 15000 Hz and also knowing the rms inductor current, the inductor loses will be calculated by the following formula

$$P_{ind} = I_{rms}^2 . R_{ac(15000\ Hz)}$$

The inductor loss is calculated for two extreme condition (pf = 0 and pf = 1) at full load (1 kVA). For pf = 0 I_{rms} = 5.1 A, and for pf = 1 I_{rms} = 4.98 A and the resistance is 2.35Ω so

$$P_{ind,pf=0} = 5.1^2 x 2.35 = 61.12W$$
$$P_{ind,pf=1} = 4.98^2 x 2.35 = 58.28W$$

If the actual designed inductor have been used, the inductor loss would have been P_{ind} = 3.527 W as calculated in sections3.2.5 and 3.2.6. The efficiencies for closed loop operation than would be

Expected and Measured Efficiency Values for Closed Loop Control Operation						
	No Load			**Full Load**		
	10 Hz	**50 Hz**	**100 Hz**	**10 Hz**	**50 Hz**	**100 Hz**
Efficiency With Ideal Inductor (%)	**-**	**-**	**-**	**92.74%**	**93.73%**	**97.6%**
Efficiency Measured with the Existing Inductor (%)	**-**	**-**	**-**	**88.75%**	**89.7%**	**93.4%**

Table 4.4 Expected and Measured Efficiency Values for Closed Loop Control Operation

4.4.7 Sinusoidal Power Filters in the Market

Some passive sinusoidal filters are available in the industry. However they have some disadvantages compared with the proposed method in this study. First of all the size of the inductor used in that filters at the same power level is 7-20 times greater in value then the one used in this study. For example the dimensions of one such filter is as given in Table 4.5. Note that the volume of this filter is 4 times larger than the filter used here. Also the frequency range of the commercial inductors is often quite limited. The data sheets of two sinusoidal filters are given in Appendix A.6

Filter Inductance	Height (mm)	Width (mm)	Length (mm)
Commercial (DEO 100)	107	53	41
Used in this thesis	56	19	59

Table 4.5 Physical Dimensions of the filter Inductors.

4.4.7 Conclusions

As shown in figures for feed forward control section, the output voltages both for no load and full load (1 kVA) tend to follow the reference voltage but the distortion of the waveforms is considerable. At no load the peak output voltage has almost the same value as reference voltage. However at full load operation the magnitude of the output voltage decreases below the reference voltage as a result of the voltage decrease in the input DC link voltage. The reduction of the voltage increases at lower frequencies as shown in table 4.1. If the THD levels are examined it is seen that the distortion of the waveforms are approximately same. Also it is clear that the distortion level is increasing with the load. The distortion levels of the output voltages are given in table 4.1. The results are clearly not acceptable for practical conditions. Also the efficiency of the system increases with the increased frequency.

The closed loop control operation experiments gave much better results in comparison with the feed forward case as found in the simulations. The output voltage follows the reference voltage for both no load and full load (1 kVA) cases without any oscillations and with distortion levels are within acceptable limits. Magnitude error, THD, and efficiency of the system with closed loop control are given in table 4.2. As the rectified DC-link voltage is regulated the magnitude error of the system is reduced to negligible values. The existing small error results from the voltage drop on the output inverter switches. THD values are increased as the load is increased and the efficiency of the system is also increased compared to the open loop case. Efficiency increases with the increasing frequency. The distortion level is also increased with the increasing frequency. As the frequency of the output voltage increases, the number of samples taken within a period is decreased and with decreased number of voltage feed-back samples the controller can not track the reference as perfect as it does at low frequencies. The reason of the increasing distortion level can be summarized in that way.

As pointed out in section 4.4.6, the designed actual DC-DC converter filter inductor couldn't be used in the experiments as a result of manufacturing problems. Following this an air core solid conductor inductor had to be used. The losses of that inductor are also calculated in section 4.4.6 and this is far above the expected loss calculated in section 3.2.5. Thus the efficiency of the system with actual inductor is supposed to be higher than measured as given in table 4.4.

Also the system is operated in order to determine the effect of load power factor variations on the capability of the converter to follow the specified reference voltage. The output waveforms for different power factors were obtained with low distortion levels as indicated in table 4.3. The distortion level increases with the reduced power factor. Because as the power factor decreased the amount of the reactive current flowing into the rectified DC-link capacitor increases and the waveform of the rectified DC-link voltage is distorted a little bit compared to resistive load case (pf=1).

CHAPTER 5

CONCLUSION

5.1 General

As discussed in the introduction part of the thesis, conventional ac motor drivers and power supplies use some modulation techniques in order to keep the output current sinusoidal regardless of the output voltage. Output voltage of a conventional driver or power supply is either a square-wave or in the case of a PWM inverter, composed of high frequency pulses, typically in the 6 kHz – 20 kHz range. In both cases there are some drawbacks. Square-wave inverters' output voltages contain high-amplitude low frequency harmonics. In PWM inverters the harmonics of the output voltage are carried to higher frequencies eliminating lower order harmonics but this also introduces some additional problems such as acoustic noise, additional iron losses, switching losses, insulation problems etc.

An ideal inverter should have a purely sinusoidal voltage and current outputs. In this study, an idea of an inverter has been proposed which can produce a low distortion sinusoidal output voltage.

The proposed idea in this thesis is to generate rectified sinusoids and form a variable frequency and amplitude DC-link. This link is called the "rectified DC-link". The output stage of the proposed inverter is an H bridge which inverts these rectified sinusoids in order to form the sinusoidal output. In this thesis a single phase implementation of the proposed inverter configuration is targeted in order to identify possible problems and investigate the performance of the inverter.

The investigation of possible circuit topologies for obtaining the "rectified DC link" and inverting this waveform is found to be utilizing a synchronous buck converter along with an H-bridge inverter. Software indicated that a closed loop control was essential to obtain the desired voltage magnitude and shape.

The proposed circuit is implemented by using the DSP software development kit of Technosoft MCK 2407A. Naturally a microcontroller with far smaller capabilities could do the necessary task. Other details of the implementation are described in the related sections. Necessary software for controlling the system have also been developed and loaded into the DSP board controller.

In chapter four, experimental studies have been conducted on the implemented system configuration. A series of tests have been performed in the laboratory to identify the system performance at steady state conditions.

5.2 Experimental Results

First feed forward control operation of the system is studied. The output voltage waveforms are found to have THD content above the acceptable levels for no load operation. The distortion further increased for full load operation. The results are given in table 4.1.

As the feed forward control was insufficient, a feedback loop is added to the control scheme from the rectified DC-link. Then the performance of the circuit is measured once again at 10, 50 and 100 Hz. In closed loop operation, the performance of the circuit is found to be very good. In other words the distortion of the output voltage is found to be less than 2%.

The magnitude error is very small too. They are in the order of 1.95% at the worst case. This is mainly because of the voltage drop on the output transistors. The efficiency of the system is found to be somewhat small due to the filter inductance

losses. However it is found that the efficiency reaches very high levels if a proper inductor with a proper core is used.

The effect of the load power factor on the system operation is also investigated at 50Hz. It is shown that the output voltage followed the reference under full load (1 kVA) condition for pf = 0, 0.3, 0.8, and 1, however a slight increase in the distortion level is obtained with the decreasing power factor.

The minimum voltage capability of the inverter is also investigated. It is shown that for low voltage values (lower then 10V), the output voltage can no longer track the reference as a result of the dead-time between switching signals. This problem can be solved by reducing the switching frequency for lower voltage levels.

Semiconductor switch stresses are also studied. The IGBT's of the DC-DC converter are found to have the same ratings as transistors of a conventional inverter. The size of the filter at the output of the DC-DC converter is also compared with a power filter that should be used to obtain a sinusoidal voltage waveform at the output of a PWM inverter.

It is found that the filter inductor size needed in the proposed configuration is one fourth of the volume of the inductor employed in the conventional inverter case. The capacitor size of a conventional filter is 2.2 μF as proposed by the filter manufacturer. This value is one fourth in value but naturally not in size. However capacitor size is not very large in any case.

In summary, it can be concluded that by using the proposed topology, two extra transistors need to be used, as compared to conventional PWM inverter. In return the inverter transistors of the proposed circuit operate at low frequency less than (400 Hz). Therefore these are likely to cost far less. The filter used in the proposed circuit is smaller and the overall filter cost is likely to be somewhat less than the one used in the PWM inverter sinusoidal filter. In other words the overall

cost of the topology proposed here may be marginally higher but an important size advantage is possible.

For very high power applications the proposed topology is very advantageous cost wise and size wise since the output transistors are of low frequency type and the filter becomes much smaller.

5.3 Conclusion and Future Work

At the end of this study, variable frequency and amplitude voltage and current waveforms with low distortion levels are obtained which an ideal inverter should have at its output. Major contribution of this study is to obtain the sinusoidal waveforms with a novel approach. The advantages and disadvantages of the system are as follows

Advantages:

- Low distortion sinusoidal output voltage
- Sinusoidal input current possible
- Small size of filter elements (both inductor and capacitor)
- Low Losses

Disadvantages:

- # of switches increased. (but sinusoidal input current is possible, note that for conventional inverters additional switches are needed for this purpose)

The future work on this study will consist of

- Higher frequency operation
- Solution of low frequency distortion problem
- Investigation of dynamic load response of the system

- A 3-phase inverter implementation
- Development of advanced control algorithms that will increase the control bandwidth and reliability
- Development of better and more reliable protection circuits
- Implementation of input power factor correction algorithms to the existing software

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APPENDIX A

DATA SHEETS OF THE COMPONENTS AND FULL PROGRAM CODES

In order to understand the concept, detailed information about the components and full program codes of both inductance design software and system control software are given below.

A.1 Flow Charts and Source Code of The Controller Program Written in C language

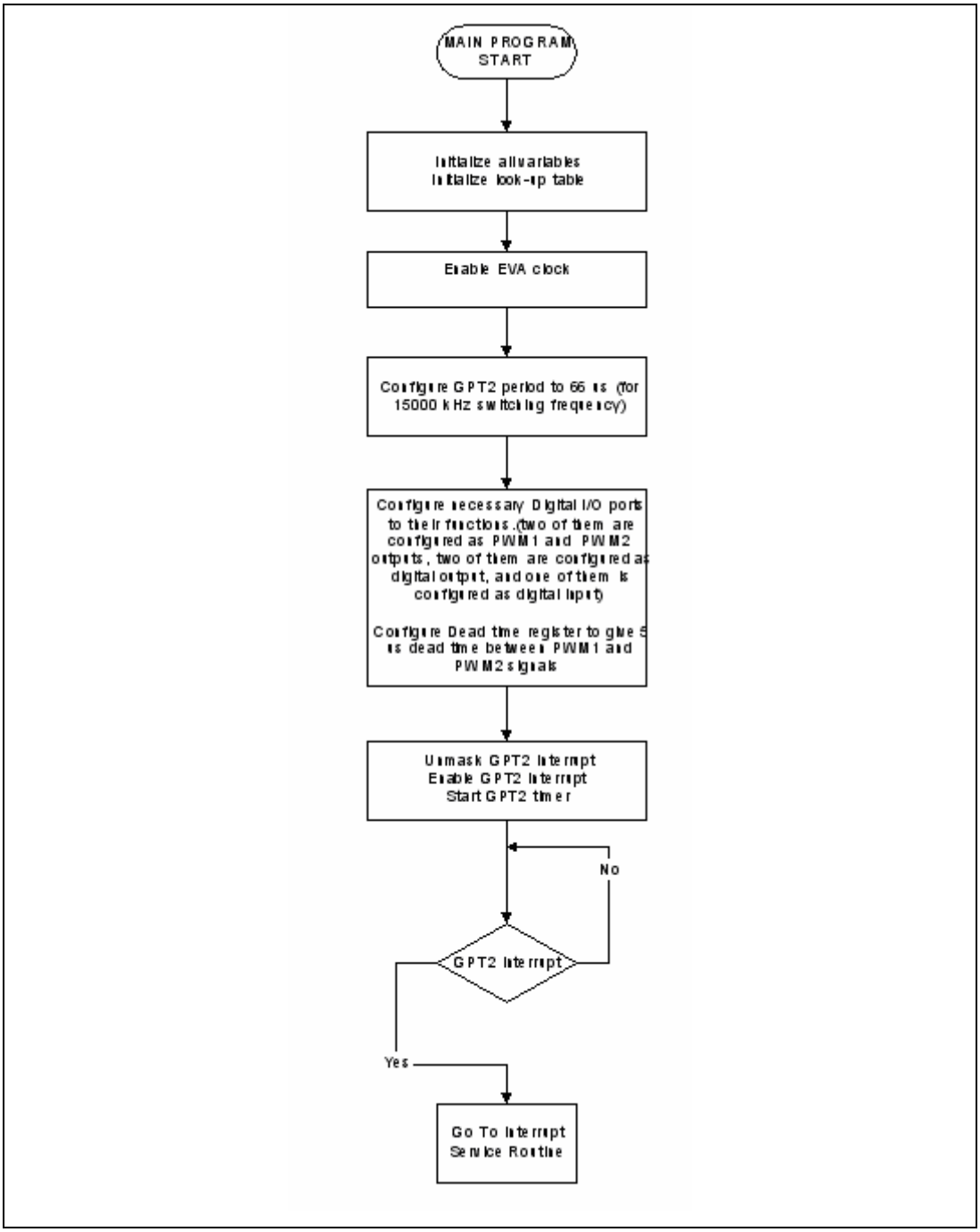


Figure A.1 Flow Chart of the main program for open loop control.

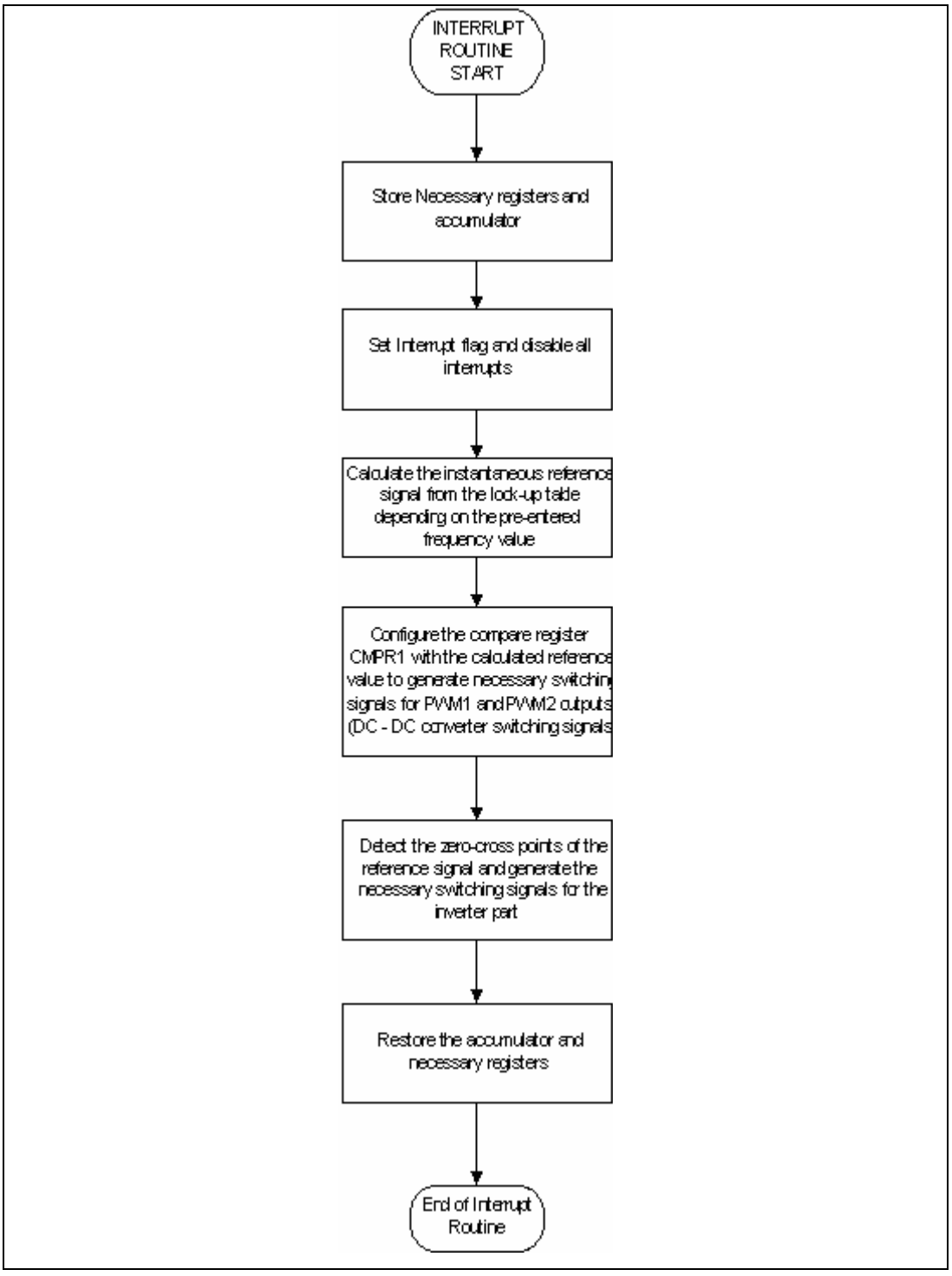


Figure A.2 Flow Chart of the interrupt service routine for open loop control.

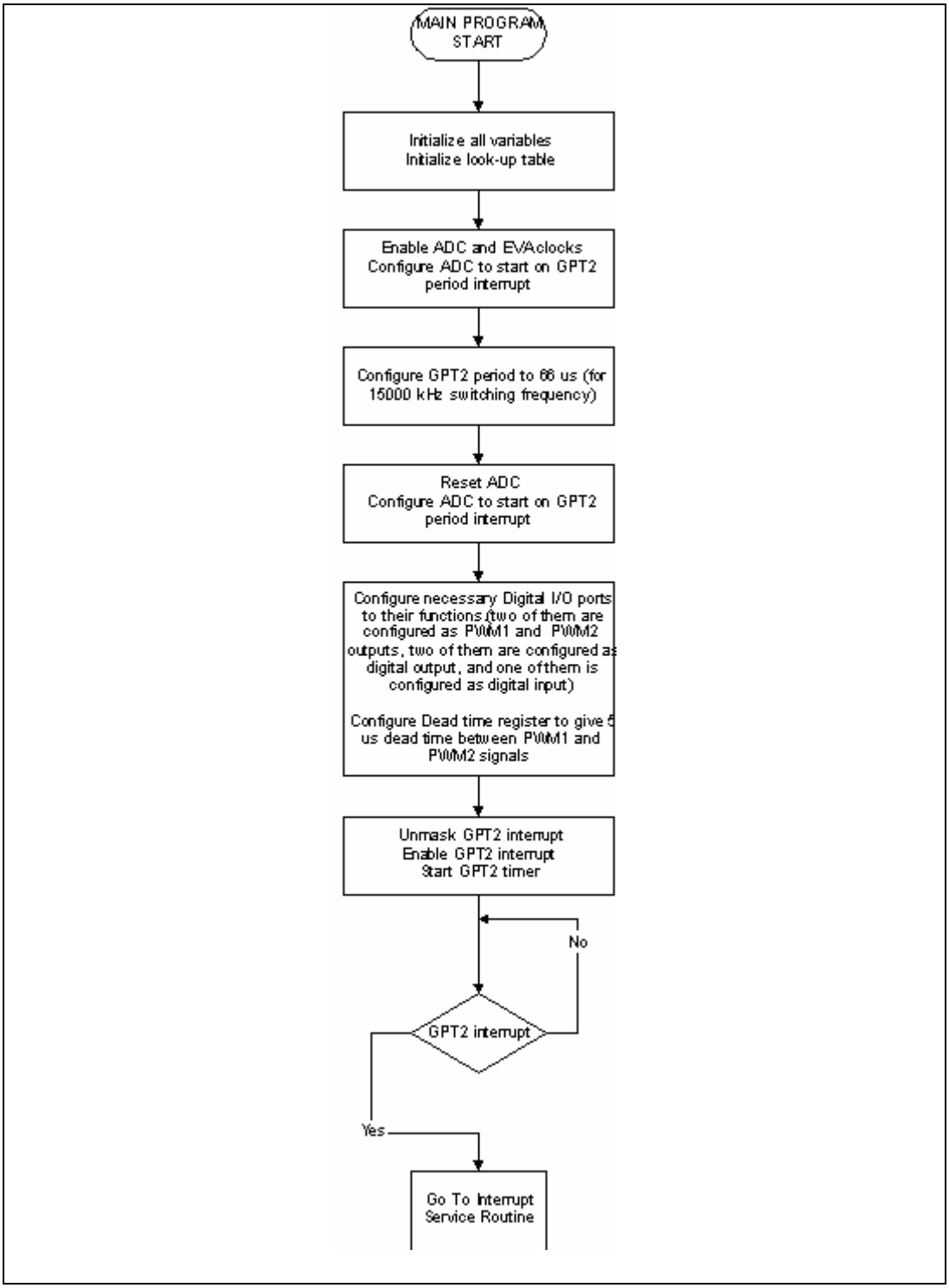


Figure A3. Flow Chart of the main program for closed loop control.

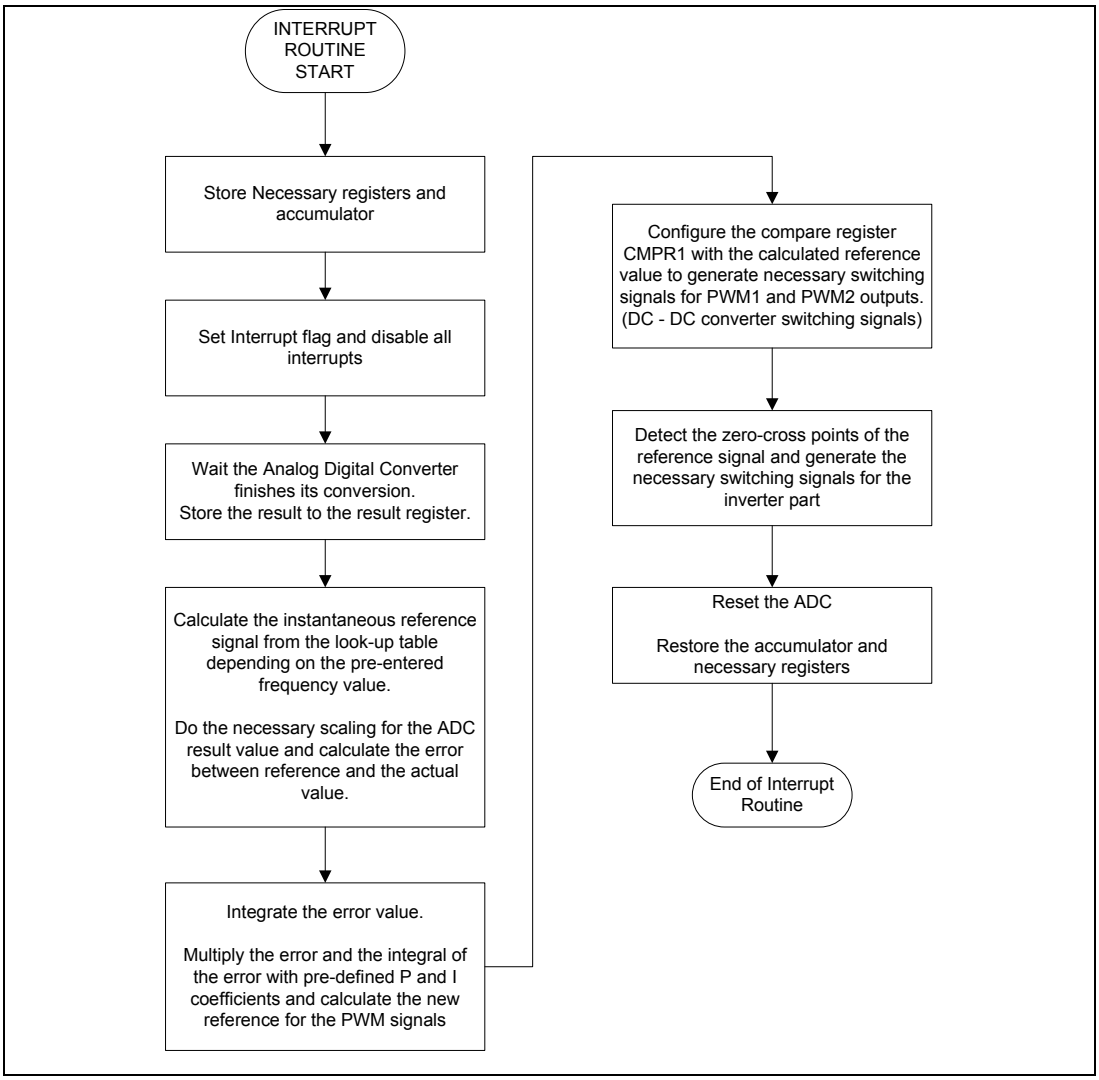


Figure A4. Flow Chart of the interrupt service routine for closed loop control.

```
#include "vect240.h"
#include "f2407_c.h"
#define MON2407 (int(*)(void))0x0300
#define END_APPL   asm (" setc INTM");\
                                asm (" LDP  #0E0h");\
                                asm (" SPLK #004Fh, 07029h");
/*#define SETBIT(REG,BIT) (REG|(1<<BIT));
#define CLRBIT(REG,BIT) (REG&=~(1<<BIT));
#define TOGGLEBIT(REG,BIT) (REG^=(1<<BIT));
#define TESTBIT(REG,BIT) (REG & (1<<BIT));*/
const float sine[] = {  0,     0.018, 0.035, 0.052, 0.070, 0.087, 0.105, 0.122, 0.139, 0.156,
                        0.174, 0.191, 0.208, 0.225, 0.242, 0.259, 0.276, 0.292, 0.309, 0.326,
                        0.342, 0.358, 0.375, 0.391, 0.407, 0.423, 0.438, 0.454, 0.469, 0.485,
                        0.500, 0.515, 0.530, 0.545, 0.559, 0.574, 0.588, 0.602, 0.616, 0.629,
                        0.643, 0.656, 0.669, 0.682, 0.695, 0.707, 0.719, 0.731, 0.743, 0.755,
                        0.766, 0.777, 0.788, 0.799, 0.810, 0.819, 0.829, 0.839, 0.848, 0.857,
                        0.866, 0.875, 0.883, 0.891, 0.899, 0.906, 0.914, 0.921, 0.927, 0.934,
                        0.940, 0.946, 0.951, 0.956, 0.961, 0.966, 0.970, 0.974, 0.978, 0.982,
                        0.985, 0.988, 0.990, 0.993, 0.995, 0.996, 0.998, 0.999, 0.999, 1    ,
                        1,     1,     0.999, 0.999, 0.998, 0.996, 0.995, 0.993, 0.990, 0.988,
                        0.985, 0.982, 0.978, 0.974, 0.970, 0.966, 0.961, 0.956, 0.951, 0.946,
                        0.940, 0.934, 0.927, 0.921, 0.914, 0.906, 0.899, 0.891, 0.883, 0.875,
                        0.866, 0.857, 0.848, 0.839, 0.829, 0.819, 0.810, 0.799, 0.788, 0.777,
                        0.766, 0.755, 0.743, 0.731, 0.719, 0.707, 0.695, 0.682, 0.669, 0.656,
                        0.643, 0.629, 0.616, 0.602, 0.588, 0.574, 0.559, 0.545, 0.530, 0.515,
                        0.500, 0.485, 0.469, 0.454, 0.438, 0.423, 0.407, 0.391, 0.375, 0.358,
                        0.342, 0.326, 0.309, 0.292, 0.276, 0.259, 0.242, 0.225, 0.208, 0.191,
                        0.174, 0.156, 0.139, 0.122, 0.105, 0.087, 0.070, 0.052, 0.035, 0.018,
                        0 };
unsigned int ort;
float er;
float ier;
float lm;
int pb;
int n;
float c;
float f;
float k;
int k1;
float p;
int ret_val_mon;
extern void t2per_ISR_ASM();
int deadtime(int);
int dt;
float err;
void main(void)
{
        ret_val_mon = 1;        /* must be initialized  */
        *SCSR1 = (*SCSR1 | 0x0084); /*ADC and EVA  clock enabled on system control and status register*/
```

```
*WDCR = 0x00E8;     /*watchdog reset*/
*GPTCONA =  0x0400 ; /*start ADC on T2 period int general purpose timer control register*/
*T2PR = 0x012C;    /*15000 Hz T2 freq*/
*T2CNT = 0x0000;   /*reset GPT2 counter*/
*T2CON = 0x1000;    /*timer in continuous up mode with prescaler x1*/
*T1PR = 0x07AD;    /*15000 Hz T2 freq*/
*T1CNT = 0x0000;   /*reset GPT2 counter*/
*DBTCONA = 0x09F0;
*ACTRA = 0x0006;
*T1CON = 0x1000;
*tpint2vec = (unsigned int)&t2per_ISR_ASM; /*load ISR address to Int. vector in on-hip block B2*/
*ADCTRL1 = 0x4000; /*reset ADC*/
asm (" NOP ");
*ADCTRL1 = 0x1010; /*free run, prescaler 1,start-stop mode,cascaded mode, calibration disabled, self-test
disabled.*/
*ADCTRL2 = 0x4100; /*reset SEQ1 and EVM A trigger starts conversion*/
*MAX_CONV = 0x0000;
*CHSELSEQ1 = 0x0000;
*CHSELSEQ2 = 0x0000;
*CHSELSEQ3 = 0x0000;
*CHSELSEQ4 = 0x0000;
/*IO mux control register is configured to its first function as PWM1 "secondary is IOPA6"*/
*MCRA = (*MCRA | 0x00E0);
*PBDATDIR = *PBDATDIR | 0xC0C0; /*configure IOPF3 as output*/
*PBDATDIR = *PBDATDIR & 0xC080;
*PADATDIR = *PADATDIR | 0x0000; /*configure IOPA5 as input*/
*IMR =  0x0014;                 /* INT3 & INT5 unmasked */
*EVAIMRB = 0x0001;        /*T2 period interrupt enabled*/
n = 0;          /*initialize all variables*/
c = 0;
k = 0;
k1 = 0;
f = 50*1.6;
p = 0;
 ort = 0;
err = 0;
lm = 0;
er = 0;
ier = 0;
*CMPR1 = 0x0000;
*COMCONA = (*COMCONA | 0x8000);
*COMCONA = (*COMCONA | 0x0200);
*T2CON =  0x1040;   /*start timer*/
*T1CON =  0x1040;   /*start timer*/
asm (" CLRC INTM ");
for ( ; ;)
                {
                        ret_val_mon = (*MON2407)();/*communication and monitor program*/
                }
```

```
                    END_APPL  /*restoring accumulator and necessary registers*/
}
 void timer (void)
{

        if ((*PADATDIR & 0x0020) == 0x0000)
{
        while ((*ADCTRL2 & 0x1000) != 0x0000)
        {
        asm (" NOP ");      /*(waiting the adc finishes the conversion)*/
        }
        lm = (*RESULT0*0.7);
        k = 0.0258*f*n;
        k1 = k;
        c = 6976/f;
        p = 0xFF00*sine[k1];
        p = (p+0xFF00*sine[k1])/2;
        p = (p+0xFF00*sine[k1])/2;
        if ((p - lm) <= 0)
        {
        *CMPR1 = 0x004F ;
        ier = ier - ier*0.8;
        }
        else
        {
                if ((p - lm)*0.032 >= 1572)
                {
                *CMPR1 = 0x0624;
                ier = ier + (p - lm)*0.032;
                }
                else
                {
                ier = ier + (p - lm)*0.032;
                *CMPR1 = (((p - lm)*0.032)+(ier*0.003)) ;
          }
        }

        if (n < c)
{
        if (n == 0)
        {
                pb = *PBDATDIR & 0x0080;
                if (pb==0)
                {
                *PBDATDIR = *PBDATDIR ^ 0x0040;
                deadtime(1);
        *PBDATDIR = *PBDATDIR ^ 0x0080;
                }
                else
```

```
                        {
                        *PBDATDIR = *PBDATDIR ^ 0x0080;
                        deadtime(1);
                        *PBDATDIR = *PBDATDIR ^ 0x0040;
                        }
    n++;
            }
            else
            {
              n++;
            }
}
            else
{
                        n=0;
}
  *ADCTRL2 = *ADCTRL2 | 0X4000;
            *EVAIFRB = (*EVAIFRB | 0x0001); /*clear timer 2 period interrupt flag*/
}
else
{
            while ((*ADCTRL2 & 0x1000) != 0x0000)
            {
            asm (" NOP ");      /*(waiting the adc finishes the conversion)*/
            }
            *CMPR1 = 0x0000;
  *ADCTRL2 = *ADCTRL2 | 0X4000;
            *EVAIFRB = (*EVAIFRB | 0x0001); /*clear timer 2 period interrupt flag*/
}
}
int deadtime(ar)
int ar;
{
int n1;
n1=0;
while(n1<ar)
{
                        n1++;
}
}
            .text
            .global _t2per_ISR_ASM
            .global _timer
_t2per_ISR_ASM:
            CALL _timer;
;           End interrupt service routine
            MAR     *, AR1                                          ; ARP=1, AR1=TOS+5
            MAR     *-                  ; AR1--, AR1=TOS+4
            LACL    *-                  ; retore ACCL, AR1=TOS+3
```

```
ADD     *-,16                   ; retore ACCH, AR1=TOS+2
LST     #0, *-                  ; restore ST0, AR1=TOS+1
LST     #1, *-                  ; restore ST1, AR1=TOS
CLRC    INTM
RET
```

A.2 Source Code of The Inductor Design Software

```
peakV=input('Enter Peak voltage in Volts>');
freq=input('Enter line frequency in Hz>');
R=input('Enter Load Resistance in Ohms>');
clc;
close all;
clear all;
kcu=0.3;
Jrms=210;
Bp=0.35;
f=15000;
T=1/f;
Vs=530;
D=Vo/Vs;
i=1;
Idc=Vo/R
for L=0:0.000025:0.01
   Imax(i)=Vo*((1/R+((1-D)*T)/(2*L)));
   Imin(i)=Vo*((1/R-((1-D)*T)/(2*L)));
   Ipp(i)=Imax(i)-Imin(i);
   bb(i)=Imax(i)-D*Imin(i);
   Bc(i)=Bp;
   cc=(Ipp(i)^2/3*(1-D^3)-Ipp(i)*bb(i)*(1-D^2)+bb(i)^2*(1-D))/(1-D)^2;
   ccc=(Ipp(i)^2/3+Ipp(i)*Imin(i)+Imin(i)^2)*D;
   IRMS(i)=sqrt(cc+ccc);
   AP(i)= 10000*(L*Imax(i)*IRMS(i))./(kcu*Jrms*Bc(i));
        if Imin(i) < 0
            t1=-(Imin(i))*D*T/Ipp(i);
            t3=Imax(i)*(1-D)*T/Ipp(i);
            t2=D*T-t1;
            t=t1+t2+t3;
            t4=T-t;
            IDC(i)= (((Imax(i).*(t2+t3))./2)+((Imin(i).*(t1+t4))./2)).*15000;
    Irms(i)=(sqrt((1/T)*((Imax(i)^2/3*(t2+t3))+(Imin(i)^2/3*(t1+t4)))));
            AP(i)= 10000*(L*Imax(i)*Irms(i))./(kcu*Jrms*Bc(i));
        else
            Irms(i)=(sqrt((((Imax(i)-Imin(i))^2*D)/3)+(((Imax(i)-Imin(i))^2*(1-D))/3))+Imin(i));
            AP(i)= 10000*(L*Imax(i)*Irms(i))./(kcu*Jrms*Bc(i));
        end
   L1(i)=L;
   i=i+1;
end
plot(L1,Imax);
hold on
plot(L1,AP,'r');
hold on
figure
plot(L1,IRMS,'g');
```

A.3 Data Sheets of the Components

FUJI ELECTRIC

2MBI 50N-120

2-Pack IGBT
1200 V
50 A

IGBT MODULE (N series)

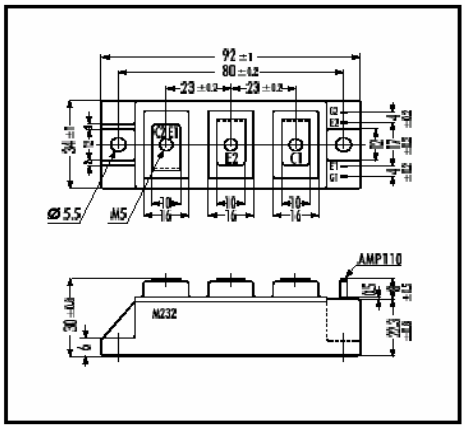
■ Features

- *Square RBSOA*
- *Low Saturation Voltage*
- *Less Total Power Dissipation*
- *Improved FWD Characteristic*
- *Minimized Internal Stray Inductance*
- *Overcurrent Limiting Function (4~5 Times Rated Current)*

■ Applications

- *High Power Switching*
- *A.C. Motor Controls*
- *D.C. Motor Controls*
- *Uninterruptible Power Supply*

■ Outline Drawing



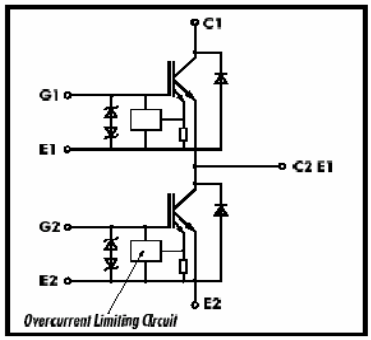
■ Maximum Ratings and Characteristics

• Absolute Maximum Ratings (T_c=25°C)

Items		Symbols	Ratings	Units
Collector-Emitter Voltage		V_{CES}	1200	V
Gate -Emitter Voltage		V_{GES}	± 20	V
Collector Current	Continuous	I_C	50	A
	1ms	$I_{C\ PULSE}$	100	
	Continuous	$-I_C$	50	
	1ms	$-I_{C\ PULSE}$	100	
Max. Power Dissipation		P_C	400	W
Operating Temperature		T_j	+150	°C
Storage Temperature		T_{stg}	-40 ~ +125	°C
Isolation Voltage	A.C. 1min.	V_{is}	2500	V
Screw Torque		Mounting *1	3.5	Nm
		Terminals *2	3.5	

Note: *1:Recommendable Value: 2.5 ~ 3.5 Nm (M5)

■ Equivalent Circuit



• Electrical Characteristics (at T_j=25°C)

Items	Symbols	Test Conditions	Min.	Typ.	Max.	Units
Zero Gate Voltage Collector Current	I_{CES}	V_{GE}=0V V_{CE}=1200V			1.0	mA
Gate-Emitter Leackage Current	I_{GES}	V_{CE}=0V V_{GE}=± 20V			15	µA
Gate-Emitter Threshold Voltage	$V_{GE(th)}$	V_{CE}=20V I_C=50mA	4.5		7.5	V
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	V_{GE}=15V I_C=50A			3.3	V
Input capacitance	C_{ies}	V_{GE}=0V		8000		pF
Output capacitance	C_{oes}	V_{CE}=10V		2900		
Reverse Transfer capacitance	C_{res}	f=1MHz		2580		
Turn-on Time	t_{ON}	V_{CC}=600V		0.65	1.2	µs
	t_r	I_C=50A		0.25	0.6	
Turn-off Time	t_{OFF}	V_{GE}=± 15V		0.85	1.5	
	t_f	R_G=24Ω		0.35	0.5	
Diode Forward On-Voltage	V_F	I_F=50A V_{GE}=0V			3.0	V
Reverse Recovery Time	t_{rr}	I_F=50A			350	ns

• Thermal Characteristics

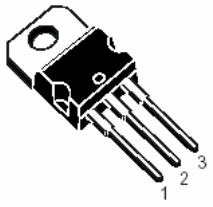
Items	Symbols	Test Conditions	Min.	Typ.	Max.	Units
Thermal Resistance	$R_{th(j-c)}$	IGBT			0.31	°C/W
	$R_{th(j-c)}$	Diode			0.85	
	$R_{th(c-f)}$	With Thermal Compound		0.05		

IRF740

N-CHANNEL 400V - 0.46Ω - 10A TO-220
PowerMESH™II MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF740	400 V	< 0.55 Ω	10 A

- TYPICAL $R_{DS}(on)$ = 0.46Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW GATE CHARGE
- VERY LOW INTRINSIC CAPACITANCES

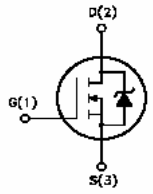


TO-220

DESCRIPTION

The PowerMESH™II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns swithing speed, gate charge and ruggedness.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	400	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	400	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuos) at T_C = 25°C	10	A
I_D	Drain Current (continuos) at T_C = 100°C	6.3	A
I_{DM} (●)	Drain Current (pulsed)	40	A
P_{TOT}	Total Dissipation at T_C = 25°C	125	W
	Derating Factor	1.0	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	4.0	V/ns
T_{stg}	Storage Temperature	– 65 to 150	°C
T_j	Max. Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(1)I_{SD} ≤10A, di/dt ≤120A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$

P Material

μ_i 2500 ± 25%

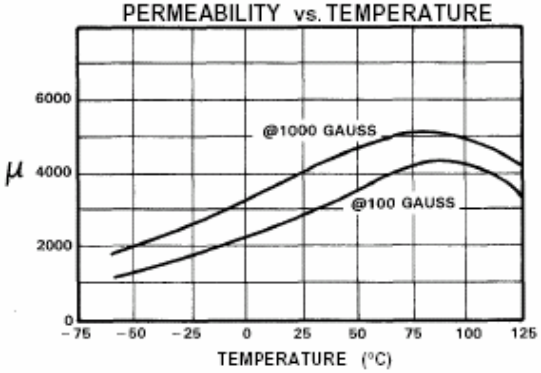
Saturation Flux Density - gausses 5000 (at 15 oersted, 25° C) (500 mT)

Coercive Force - oersted 0.18 (14A/m)

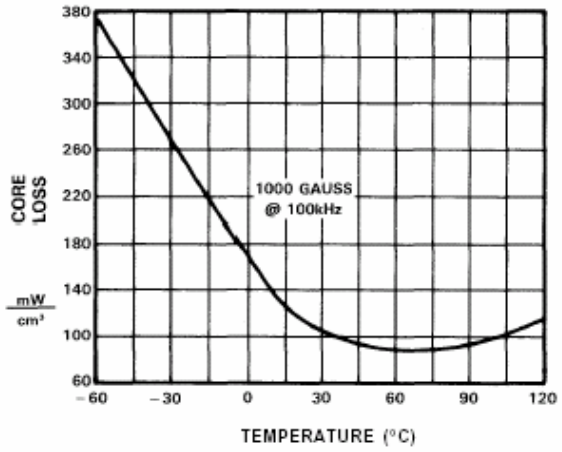
Curie Temperature . . . . . 230°C

Note: The core loss curves are developed from empirical data. For best results and highest accuracy, use them. The formula on page 2.11 yields a fair approximation and can be useful in computer programs.

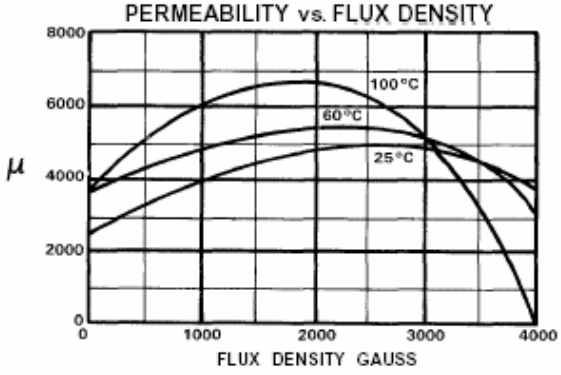
PERMEABILITY vs. TEMPERATURE



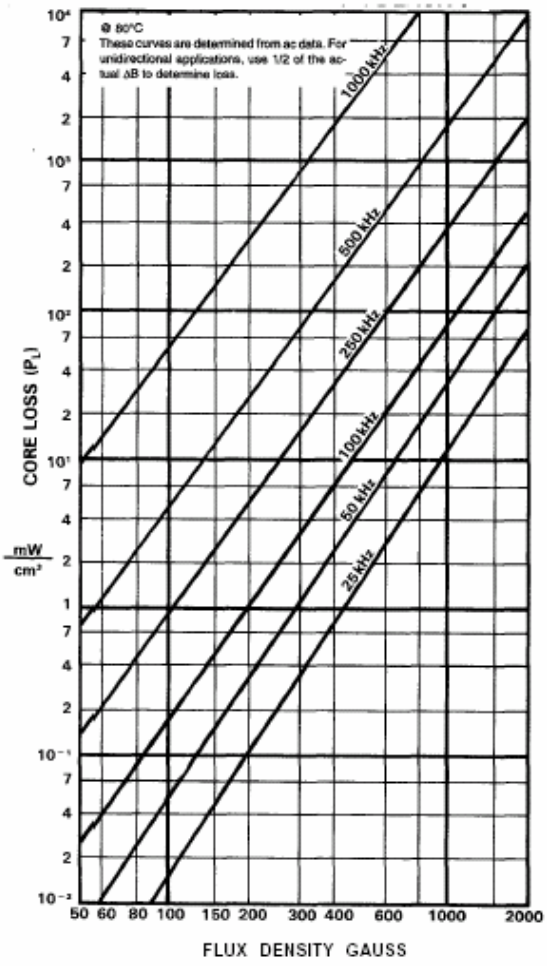
CORE LOSS vs. TEMPERATURE



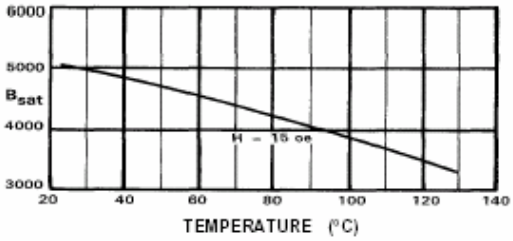
PERMEABILITY vs. FLUX DENSITY



CORE LOSS vs FLUX DENSITY



FLUX DENSITY vs. TEMPERATURE



CORE LOSS INFORMATION

Included on Pages 2.4-2.10 are material characteristics for the various **Magnetics** power and inductor materials. For computer programming purposes, the core loss curves can be represented by the equation below. The factors indicated in the chart are split into discrete frequency ranges, so that the equation offers a close approximation to the core loss curves on the above pages.

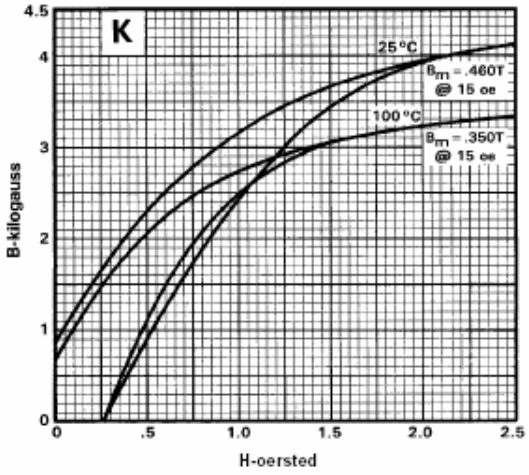
CORE LOSS EQUATION: $P_L = af^c B^d$

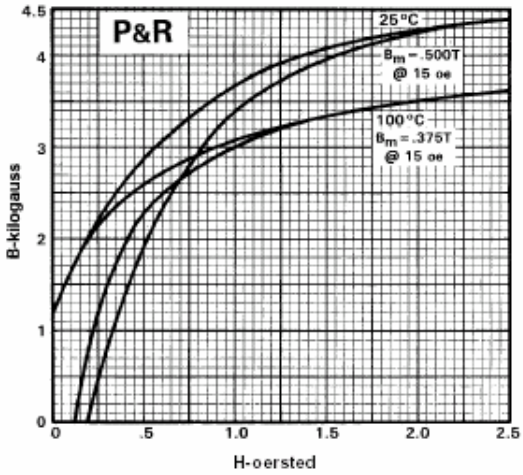
P_L is in mW/cm^3
B is in kG
f is in kHz

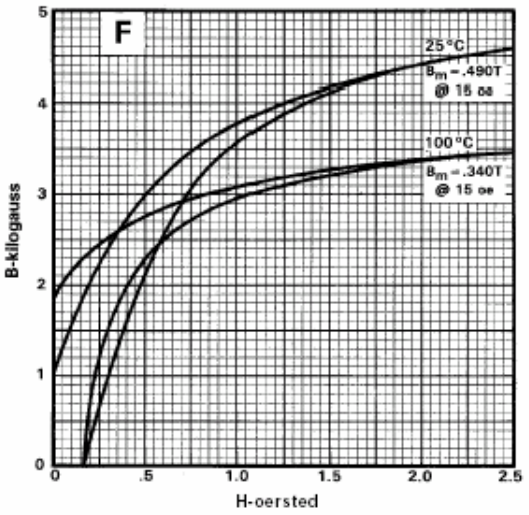
FACTORS APPLIED TO THE ABOVE FORMULA

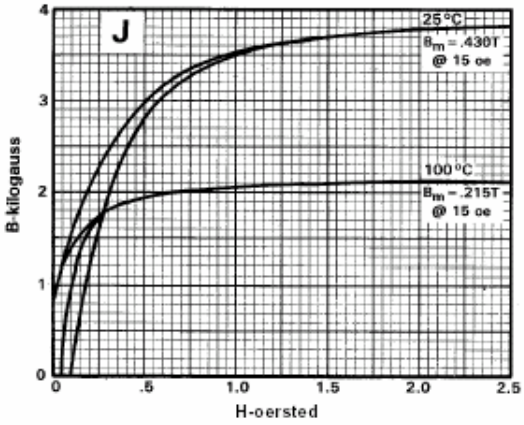
		a	c	d
K Material	f<500 kHz	0.0530	1.60	3.15
	500 kHz≤f<1 MHz	0.00113	2.19	3.10
	f≥1 MHz	$1.77*10^{-9}$	4.13	2.98
R Material	f<100 kHz	0.074	1.43	2.85
	100 kHz≤f<500 kHz	0.036	1.64	2.68
	f≥500 kHz	0.014	1.84	2.28
P Material	f<100 kHz	0.158	1.36	2.86
	100kHz≤f<500 kHz	0.0434	1.63	2.62
	f≥500 kHz	$7.36*10^{-7}$	3.47	2.54
F Material	f≤10 kHz	0.790	1.06	2.85
	10 kHz≤f<100 kHz	0.0717	1.72	2.66
	100 kHz≤f<500 kHz	0.0573	1.66	2.68
	f≥500 kHz	0.0126	1.88	2.29
J Material	f≤20 kHz	0.245	1.39	2.50
	f>20 kHz	0.00458	2.42	2.50
W Material	f≤20 kHz	0.300	1.26	2.60
	f>20 kHz	0.00382	2.32	2.62
H Material	f≤20 kHz	0.148	1.50	2.25
	f>20 kHz	0.135	1.62	2.15

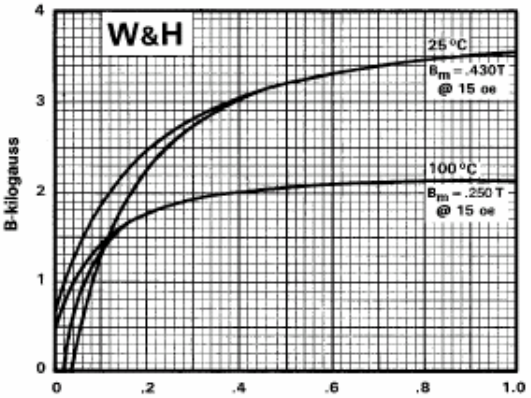
B vs. H Curves (dc)











CONVERSION TABLE

Multiply number of	by	to obtain
Oersteds	79.5	A/m
Oersteds	.795	A/cm
Gausses	.1	milli Teslas
Gausses	10^{-4}	Teslas
Teslas	10^{4}	Gausses

E Cores

45015 TO 48020

See pages
11.1 - Lamination Sizes
12.1 - EC Cores
12.4 - ETD Cores

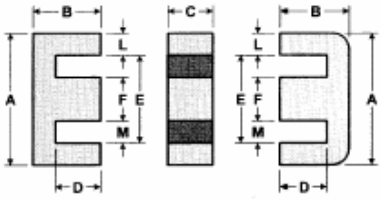


Figure 1 Figure A Figure 2

Lamination Size Cores, See page 11.1

45724-EC •

Part Number (1)	FIG.	MECHANICAL DIMENSIONS - Inches mm = ( ) A	B	C	D (min.)	E (min.)	F	L	M
45021-EC Metric E50	1A	1.95 ± .025 (49.5)	.839 ± .012 (21.3)	.575 ± .015 (14.6)	.492 (12.5)	1.359 (34.5)	.575 ± .015 (14.6)	.290 ± .010 (7.37)	.3975 ± .012 (10.1)
45528-EC DIN 55/21	1A	2.16 ± .025 (54.9)	1.085 ± .015 (27.6)	.812 ± .015 (20.6)	.730 (18.5)	1.476 (37.5)	.660 ± .015 (16.8)	.330 ± .015 (8.38)	.420 ± .015 (10.7)
45530-EC DIN 55/25	1A	2.16 ± .025 (54.9)	1.085 ± .015 (27.6)	.969 ± .015 (24.61)	.730 (18.5)	1.476 (37.5)	.660 ± .015 (15.62)	.330 ± .015 (8.38)	.420 ± .015 (10.7)
46016-EC Metric E60	2A	2.362 ± .031 (59.99)	.878 ± .012 (22.3)	.615 ± .015 (15.62)	.543 (13.8)	1.732 (44)	.615 ± .015 (15.62)	.303 ± .010 (7.70)	.5705 ± .010 (14.49)
47228-EC F11	1A	2.85 ± .030 (72.4)	1.100 ± .013 (27.9)	.750 ± .013 (19.0)	.700 (17.8)	2.072 (52.6)	.750 ± .015 (19.0)	.375 ± .015 (9.53)	.665 min. (16.9)
48020-EC Metric E80	1A	3.150 ± .035 (80)	1.500 ± .013 (38.1)	.780 ± .012 (19.8)	1.110 (28.2)	2.334 (59.3)	.780 ± .012 (19.8)	390 nom. (9.9)	.780 min. (19.8)

MAGNETIC DATA

TO ORDER SEE NOTE ↓

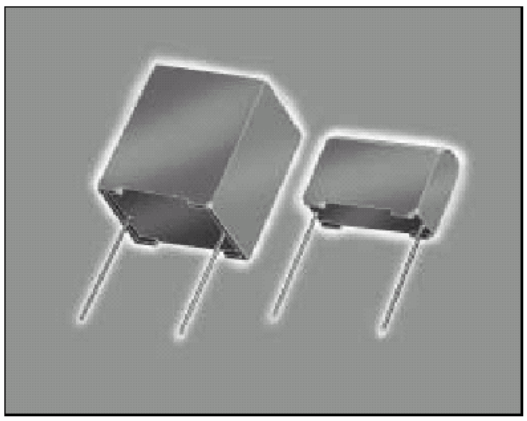
PART NUMBER (Note 1)	COMBI-NATION	AL VALUES MH/1000 Turns MATERIALS μ μ2300 R (min.)	μ μ2500 P (min.)	μ μ3000 F ±25%	μ μ5000 J (min.)	μ l_e (cm)	A_e (cm^2)	MINIMUM AREA (cm^2)	V_e (cm^3)	SET NOM. Wt. (gms)	BOBBIN WINDOW AREA (cm^2)	WaAc (cm^4) (Note 2)
45021-EC	E-E	4,600	5,000	8,000	8,010	9.29	2.25	2.13	20.9	108	1.78	4.00
45528-EC	E-E	4,720	5,130	8,220	9,375	12.3	3.50	3.46	43.1	212	2.83	9.91
45530-EC	E-E	5,640	6,130	9,800	11,190	12.3	4.17	4.13	51.4	255	2.83	11.8
46016-EC	E-E	4,300	4,680	6,590	7,445	11.0	2.48	2.40	27.2	135	2.89	7.16
47228-EC	E-E	4,470	4,860	7,780	8,885	13.7	3.68	3.63	50.3	264	4.02	14.8
48020-EC	E-E	3,505	3,810	6,000	6,940	18.5	3.89	3.82	72.1	357	7.91	30.8

FOR PREFERRED PARTS, SEE INSIDE BACK COVER

1. (a) When ordering, add material code to part number. E.g., F-45015-EC.
   (b) Any practical gap is available. See pages 1.6 and 1.7.
   (c) Cores are sold per piece. (Multiply sets x 2). Gapped pieces are normally packed separately from ungapped pieces. If desired in sets, this must be specified.
2. Product of window area and core area.

Medium Power Film Capacitors

FFB



The FFB series uses a non-impregnated metallized polypropylene or polyester dielectric with the controlled self-healing process, specially treated to have a very high dielectric strength in operating conditions up to 100°C.

The FFB has been designed for printed circuit board mounting. Furthermore, their performances allow to be a very interesting alternative to electrolytic technology because they can withstand much higher levels of surge voltage.

APPLICATIONS

The FFB capacitor is particularly designed for DC filtering, low reactive power.

GENERAL CHARACTERISTICS

Climatic category	55/100/56 (IEC 68)
Test voltage between terminals @ 25°C	1.5 x $V_n$dc

STANDARDS

IEC 1071-1, IEC 1071-2: Power electronic capacitors
IEC 60 384-16: Fixed metallized polypropylene film dielectric DC capacitors
IEC 60 384-16-1: Fixed metallized polypropylene film dielectric DC capacitors Assessment level E
IEC 60 384-17: Fixed metallized polypropylene film dielectric AC and pulse capacitors
IEC 60 384-17-1: Fixed metallized polypropylene film dielectric AC and pulse capacitors Assessment level E

WORKING TEMPERATURE

(according to the power to be dissipated) -55°C to +100°C

LIFETIME EXPECTANCY

One unique feature of this technology (as opposed to electrolytics) is how the capacitor reacts at the end of its lifetime. Whereas, with an electrolytic, there is a strong risk of explosion of the case. However, with our line of film capacitors, the capacitor will simply experience at the end of life a loss of capacitance of about 5%, with no risk of explosion.

Please note that this is theoretical, however, as the capacitor continues to be functional even after this 5% decrease.

HOT SPOT TEMPERATURE CALCULATION

You can calculate the maximum operating (hot spot) temperature of this capacitor in the following manner:

The loss factor of the capacitor is made up of the sum of two components. The first represents electrical losses in the dielectric and the second component represents Joule effect in the connection and foils (Rs.C.2 π f).

For all applications, the temperature in the hot spot capacitor must be lower than 100°C.

$$\theta_{hot\ spot} = \theta_{ambient} + [tg\delta_0 \cdot Q + R_S \cdot (I_{rms})^2] \cdot R_{th}$$

With:

Q : Reactive power in Var
R_S in Ohm
I_{rms} in Ampere
R_{th} : Rth ambient / hot spot in °C/W
tg $\delta_{ii} \cdot (10^{-4})$ is the tangent of loss angle (see tan δ_0 page 3)

PACKAGING

Self-extinguishing plastic case (V0 = in accordance with UL 94) filled thermosetting resin.

Self-extinguishing thermosetting resin (V0 = in accordance with UL 94; M2F1 = in accordance with NF F 16-101).

Medium Power Film Capacitors

FFB

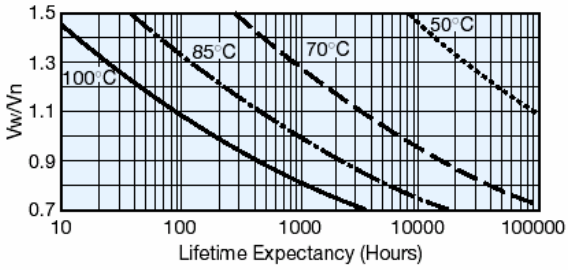
DC FILTERING FOR LOW VOLTAGE

POLYESTER DIELECTRIC

TABLE OF VALUES

Capacitance (µF)	Box Kind	I_{rms} max. (A)	R_s (mΩ)	R_{th} (°C/W)	Part Number
$V_n$dc 75V	**Vrms max.: 45 volts**				
33	PO	3	3	40.7	FFB14D0336K--
47	18	4.3	2	33.3	FFB24D0476K--
68	19	6.2	1.7	29.9	FFB34D0686K--
82	26	7.4	1.6	26.7	FFB44D0826K--
110	R68 (2 terminals)	10	1.4	22.9	FFB54D0117K--
110	R68 (4 terminals)	10	1.4	22.9	FFB54D0117KJC
$V_n$dc 100V	**Vrms max.: 60 volts**				
20	PO	2.6	3	40.5	FFB14E0206K--
27	18	3.5	2.5	33.3	FFB24E0276K--
39	19	5	2	29.8	FFB34E0396K--
47	26	6	1.7	26.6	FFB44E0476K--
68	R68 (2 terminals)	9	1.4	22.8	FFB54E0686K--
68	R68 (4 terminals)	9	1.4	22.8	FFB54E0686KJC
$V_n$dc 300V	**Vrms max.: 90 volts**				
7.5	PO	2.4	16	40.7	FFB14H0755K--
11	18	3.6	11	33.5	FFB24H0116K--
16	19	5.2	8	29.9	FFB34H0166K--
18	26	6	7	27.1	FFB44H0186K--
27	R68 (2 terminals)	9	5	22.9	FFB54H0276K--
27	R68 (4 terminals)	9	5	22.9	FFB54H0276KJC
$V_n$dc 400V	**Vrms max.: 105 volts**				
6.2	PO	2.5	17	40.5	FFB14I0625K--
7.5	18	3.1	14	33.5	FFB24I0755K--
12	19	5	9	29.9	FFB34I0126K--
15	26	6.2	7	26.4	FFB44I0156K--
20	R68 (2 terminals)	8.2	5.5	22.8	FFB54I0206K--
20	R68 (4 terminals)	8.2	5.5	22.8	FFB54I0206KJC

LIFETIME EXPECTANCY vs V_W/V_n AND HOT SPOT TEMPERATURE



Vw = Working DC Voltage

Vn = Rated DC Voltage

1. Introduction

The insulated gate bipolar transistor (IGBT) is increasingly being used in small, low-noise, high-performance power supplies, inverters, uninterruptable power supplies (UPS), and motor speed controls.

Fuji's Hybrid IC driver for IGBTs was developed to take full advantage of the IGBT.

2. Features

- Various series

  Standard series: For up to 10 kHz operation

  High-speed series: For up to 40 kHz operation

  These series cover the full range of IGBT products.
- Built-in photocoupler for high isolation voltage: 2500 V AC for one minute
- Single supply operation
- Built-in overcurrent protection circuit
- Overcurrent detection output
- SIL package for high-density mounting

3. Applications

- General-purpose inverter and motor control
- Servo control
- Uninterruptable power supplies (UPS)
- Welding machines

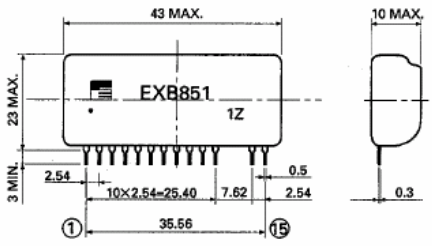
4. Comprehensive Chart

IGBT	600 V IGBT drive		1200 V IGBT drive	
	Up to 150A	Up to 400A	Up to 75A	Up to 300A
Standard type	EXB850	EXB851	EXB850	EXB851
High-speed type	EXB840	EXB841	EXB840	EXB841

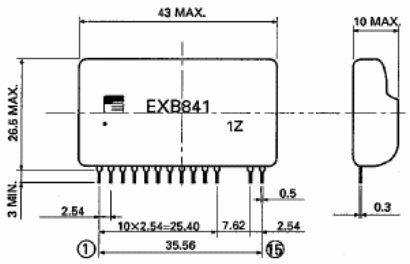
Notes: 1. Standard type: Signal delay in drive circuit; Up to 4μs (max.)
2. High-speed type: Signal delay in drive circuit; Up to 1.5μs (max.)

5. Dimensions, mm

- EXB850
- EXB840

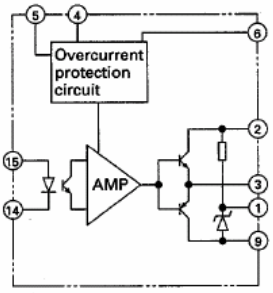


- EXB851
- EXB841

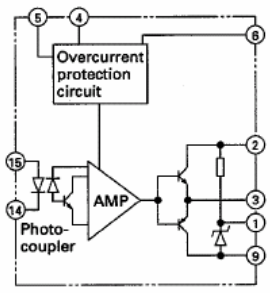


6. Functional Block Diagrams

EXB850, 851



EXB840, 841



Notation common to all EXB series

Pin number	Description
①	Connected to smoothing capacitor for reverse bias power supply
②	Power supply (+20 V)
③	Drive output
④	For connecting an external capacitor to protect against malfunction of the overcurrent protection circuit. (The capacitor is not needed in most cases.)
⑤	Overcurrent detection output
⑥	Collector voltage monitoring
⑦ ⑧	Not connected
⑨	Power supply (0 V)
⑩ ⑪	Not connected
⑭	Drive signal input (–)
⑮	Drive signal input (+)

7. Ratings and Characteristics

■ Absolute maximum ratings (Ta = 25°C)

Item	Symbol	Condition	Rating		Unit
			EXB850, EXB840 (Medium capacity)	EXB851, EXB841 (Large capacity)	
Supply voltage	V cc		25		V
Photocoupler input current	I in		25		mA
Forward bias output current	I g1	PW = 2 µs, duty at 0.05 or less	1.5	4.0	A
Reverse bias output current	I g2	PW = 2 µs, duty at 0.05 or less	1.5	4.0	A
Input/Output isolation voltage	V ISO	AC 50/60 Hz, 1 minute	2500		V
Operating surface temperature	T c		–25 to +85		°C
Storage temperature	T stg		–25 to +125		°C

■ Recommended operating conditions

Item	Symbol	Recommended operating conditions				Unit
		Standard type		High-speed type		
		EXB850	EXB851	EXB840	EXB841	
Supply voltage	V cc	20 $^{+2}_{-0}$				V
Photocoupler input current	I in	5		10		mA

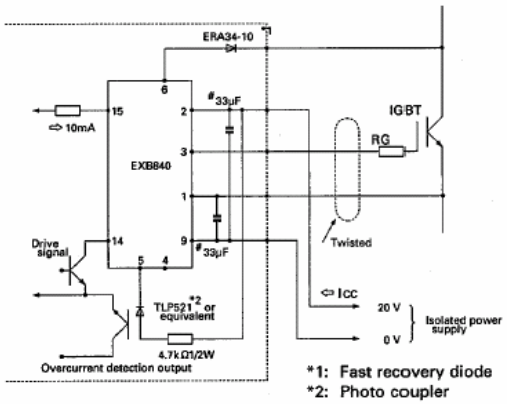
3 EXB840 Application Circuits

EXB840 is a hybrid IC capable of driving up to 150A for 600 V IGBT and up to 75A for a 1200 V IGBT. Since the signal delay in the drive circuit is 1µs or less, the hybrid IC is suitable for switching at up to about 40 kHz.

Note the following when using the hybrid IC:

- The IGBT's gate-emitter drive loop wiring must be shorter than one meter.
- The IGBT's gate-emitter drive wiring should be twisted.
- If a large voltage spike is generated at the collector of the IGBT, increase the IGBT's gate series resistor(RG).
- The 33 µF (#) capacitor absorbs changes in the supply voltage caused by the power supply wiring impedance. It is not a power supply filter capacitor.

Control circuit PC board



*1: Fast recovery diode
*2: Photo coupler

- High-Performance Static CMOS Technology
  - 25-ns Instruction Cycle Time (40 MHz)
  - 40-MIPS Performance
  - Low-Power 3.3-V Design
- Based on TMS320C2xx DSP CPU Core
  - Code-Compatible With F243/F241/C242
  - Instruction Set and Module Compatible With F240/C240
- Flash (LF) and ROM (LC) Device Options
  - LF240xA: LF2407A, LF2406A, LF2403A, LF2402A
  - LC240xA: LC2406A, LC2404A, LC2402A
- On-Chip Memory
  - Up to 32K Words x 16 Bits of Flash EEPROM (4 Sectors) or ROM
  - Programmable "Code-Security" Feature for the On-Chip Flash/ROM
  - Up to 2.5K Words x 16 Bits of Data/Program RAM
    - 544 Words of Dual-Access RAM
    - Up to 2K Words of Single-Access RAM
- Boot ROM (LF240xA Devices)
  - SCI/SPI Bootloader
- Up to Two Event-Manager (EV) Modules (EVA and EVB), Each Includes:
  - Two 16-Bit General-Purpose Timers
  - Eight 16-Bit Pulse-Width Modulation (PWM) Channels Which Enable:
    - Three-Phase Inverter Control
    - Center- or Edge-Alignment of PWM Channels
    - Emergency PWM Channel Shutdown With External $\overline{\text{PDPINTx}}$ Pin
  - Programmable Deadband (Deadtime) Prevents Shoot-Through Faults
  - Three Capture Units for Time-Stamping of External Events
  - Input Qualifier for Select Pins
  - On-Chip Position Encoder Interface Circuitry
  - Synchronized A-to-D Conversion
  - Designed for AC Induction, BLDC, Switched Reluctance, and Stepper Motor Control
  - Applicable for Multiple Motor and/or Converter Control
- External Memory Interface (LF2407A)
  - 192K Words x 16 Bits of Total Memory: 64K Program, 64K Data, 64K I/O
- Watchdog (WD) Timer Module
- 10-Bit Analog-to-Digital Converter (ADC)
  - 8 or 16 Multiplexed Input Channels
  - 375 ns or 500 ns MIN Conversion Time
  - Selectable Twin 8-State Sequencers Triggered by Two Event Managers
- Controller Area Network (CAN) 2.0B Module (LF2407A, 2406A, LF2403A)
- Serial Communications Interface (SCI)
- 16-Bit Serial Peripheral Interface (SPI) (LF2407A, 2406A, LC2404A, LF2403A)
- Phase-Locked-Loop (PLL)-Based Clock Generation
- Up to 40 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins
- Up to Five External Interrupts (Power Drive Protection, Reset, Two Maskable Interrupts)
- Power Management:
  - Three Power-Down Modes
  - Ability to Power Down Each Peripheral Independently
- Real-Time JTAG-Compliant Scan-Based Emulation, IEEE Standard 1149.1† (JTAG)
- Development Tools Include:
  - Texas Instruments (TI) ANSI C Compiler, Assembler/Linker, and Code Composer Studio™ Debugger
  - Evaluation Modules
  - Scan-Based Self-Emulation (XDS510™)
  - Broad Third-Party Digital Motor Control Support
- Package Options
  - 144-Pin LQFP PGE (LF2407A)
  - 100-Pin LQFP PZ (2406A, LC2404A)
  - 64-Pin TQFP PAG (LF2403A)
  - 64-Pin QFP PG (2402A)
- Extended Temperature Options (A and S)
  - A: – 40°C to 85°C
  - S: – 40°C to 125°C

† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port; however, boundary scan is not supported in this device family.

TEXAS INSTRUMENTS

A.4 Simulation model

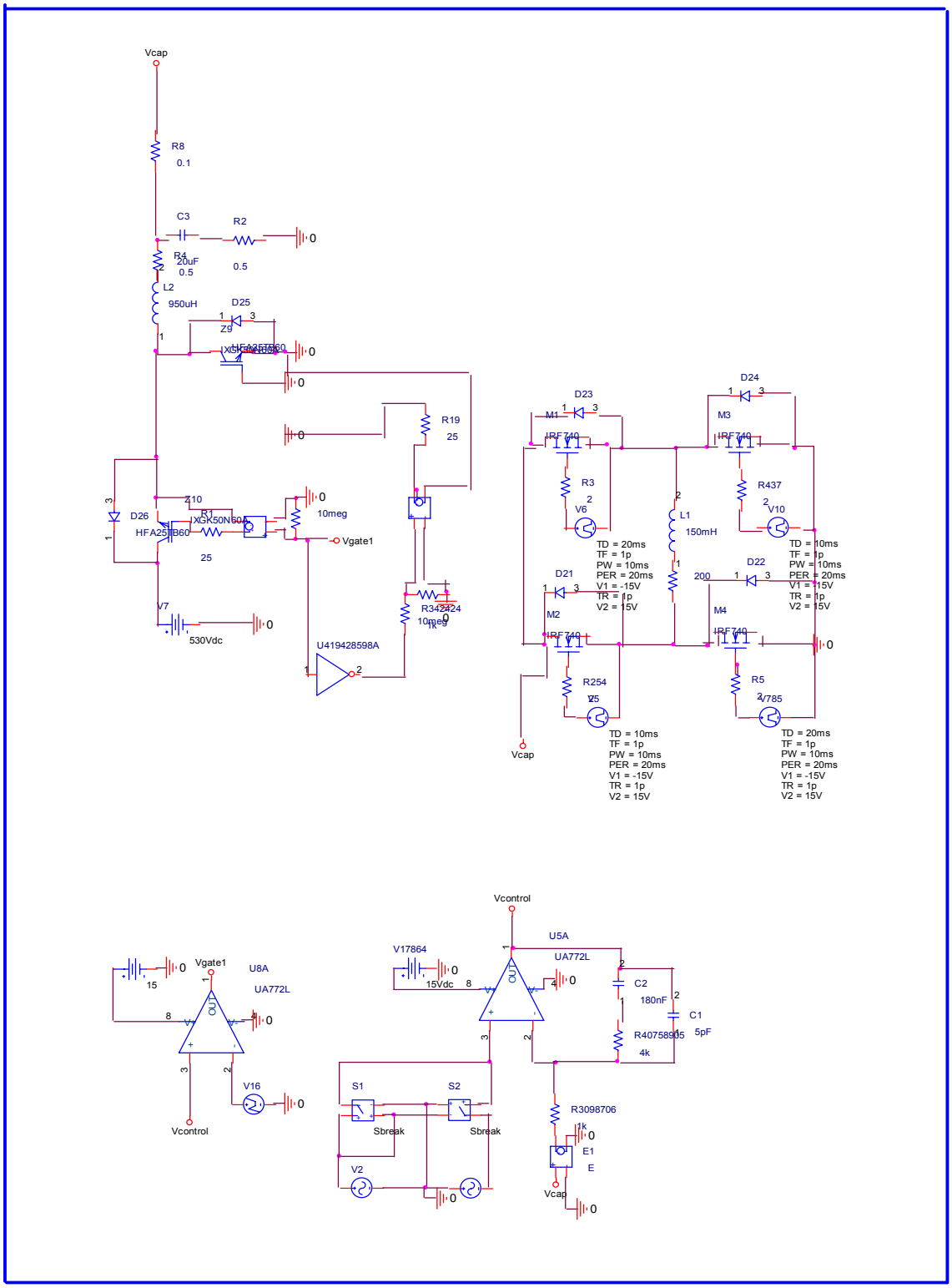


Figure A-5 Simulation Model

A.5 Determination of Suitable Topology for the Output Stage

Seven different circuit topologies have been proposed. These topologies are variations of well-known H-Bridge inverters.

Also it is important to emphasize that the switches of the output stage are switched at low frequencies, thus reducing losses and cost. First thyristorized topologies are examined because of their low costs. Then IGBT and MOSFETs are examined.

Initially mode by mode analysis is applied to the circuits and it is seen that five of the topologies can satisfactorily operate for purely resistive load. However when the load is changed to be inductive, only two of them seemed to be working properly in all situations. Two of them could not work for both resistive and the inductive loads.

It must be noted that all of the switches used at the output stage are low speed switches.

In order to simplify the problem, the issue of obtaining sinusoidal input currents to the input stage is not considered in this study. During the analysis the input part, that is the full rectified sinusoid generator, is assumed to be ideal and conducting current in both directions. The load is first assumed to be purely resistive and than a combined resistive+inductive load is considered.

A.5.1 Full Controlled H-Bridge Inverters

In this section different full controlled bridge inverters are examined. Although all of them have four controlled switches, the type of that circuit devices changes and also some of them has anti-parallel diodes. In order to specify the differences, individual circuits are named as topology 1, 2 … etc.

A.5.1.1 Topology One of the Full Controlled Bridge Inverter

The first topology of full controlled bridge inverter consists of four tyristors as shown in figure A.6. That is, all of the switches are controllable at this time. This circuit operates well when the load is purely resistive. T1 and T4 switches are turned on for one cycle, and T3 and T2 for the next cycle.

For inductive load, this circuit fails. After T1 and T4 switches are turned on, because of the lagging current, these switches can not be turned off even if the gate signals are removed. So a sinusoidal signal can not be obtained at the terminals of the load.

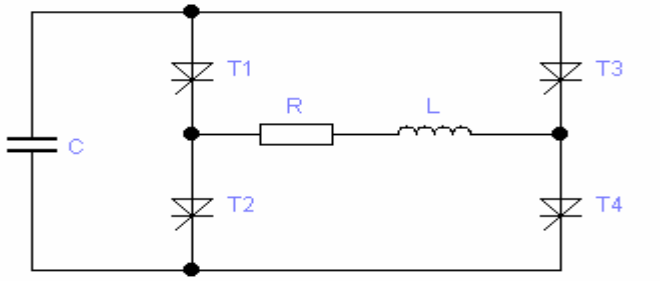


Figure A.6 First topology consists of four tyristors

A.5.1.2 Topology Two of the Full Controlled H-Bridge Inverter

The second topology of full controlled bridge inverter is a modified version of the four thyristorized circuit. At this time four anti-parallel diodes are added as shown in figure A.7

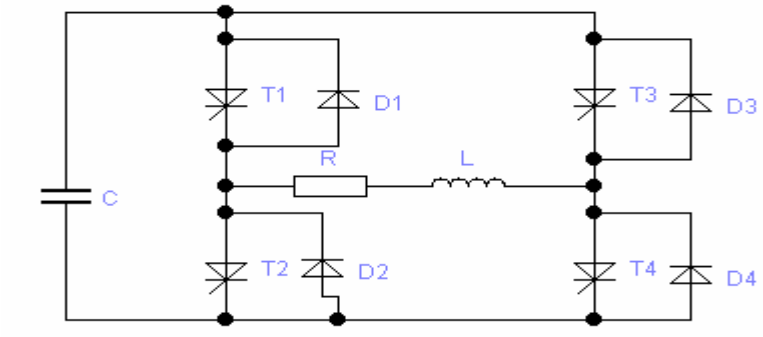


Figure A.7 Four anti-parallel diodes are added to topology one

This circuit operates well for the purely resistive load. But in spite of the freewheeling diodes the circuit does not operate when the load is inductive.

At the first sight it is thought that (assume positive current and voltage) the reactive current can be commutated from T1 and T4 switches to D2 and D3 diodes. But it is not the case. The same problem with topology one is still exists. The thyristors can not be turned off while there is a current flowing through them.

A.5.1.3 Topology Three of the Full Controlled H-Bridge Inverter

The third topology of full controlled bridge inverter consists of two tyristors and two transistors (or GTO's) as shown in figure A.8.

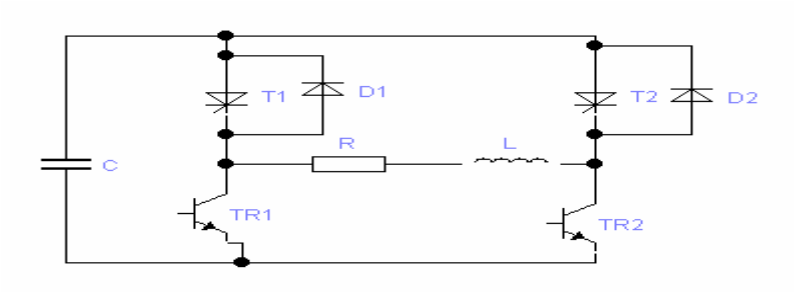


Figure A.8 Third topology consists of two tyristors and two transistors

For resistive load the circuit works well. Let's look at what will happen when an inductive load is connected.

At the first mode, T1 and TR2 are turned on and the voltage and the current are positive as shown in figure A.9.

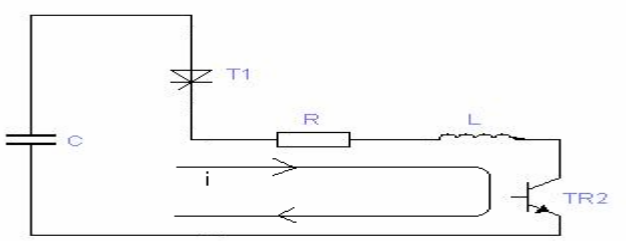


Figure A.9 T1 and TR2 are turned on

At the second mode, the load voltage must be the reversed of the input voltage so the cross elements (T2 and TR1 must be turned on). But as the current is lagging T1 can not be turned off even TR2 can be. At this time the load current closes its path through D2 as shown in figure A.10. Because TR1 and T2 can not go into conduction as it can not draw negative current. The load is shorted so load voltage is zero until the current in T1 reverses its direction. This is not what we want. This topology also fails.

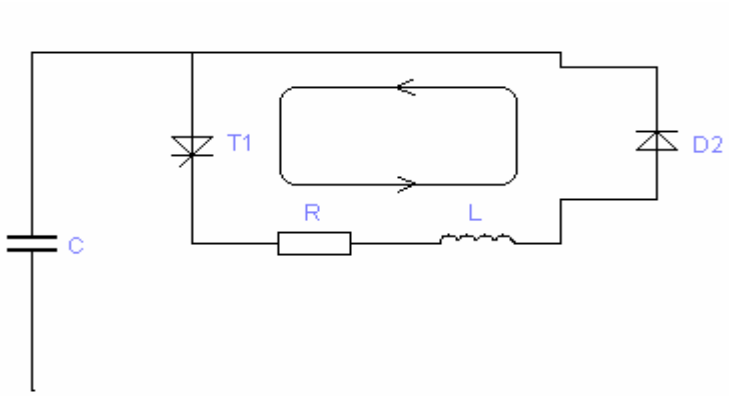


Figure A.10 load current closes its path through D2

A.5.1.4 Topology Four of the Full Controlled H-Bridge Inverter

The fourth topology of full controlled bridge inverter consists of four transistors. GTO's can also be used but they are produced for very high power applications in the ranges of megawatts so BJT's, Mosfets, and IGBT s are suitable for low power application. Note that the cost effective solution is to use BJT s.

The circuit shown in figure A.11 works properly when the load is purely resistive. In the case of an inductive load, the circuit has some problems. Initially TR1 and TR4 are in conduction. When the source voltage drops to zero TR1 and TR4 are turned off and the cross switches TR2 and TR3 are turned on. At this point that is the switching instant, the current is first forced to drop to zero and than immediately change direction. Due to the high di/dt, there is a huge voltage spike occurs on the load.

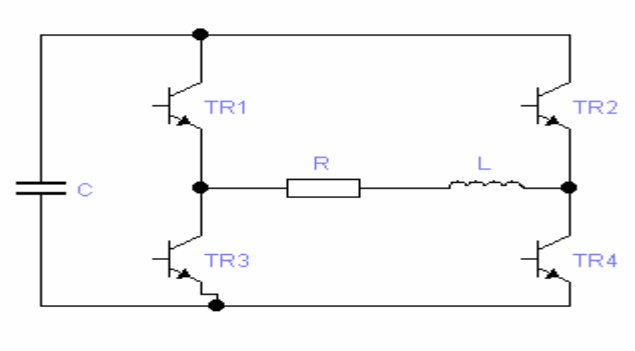


Figure A.11 Fourth topology consists of four transistors

This problem will be solved by providing a path to the reactive current. This is achieved by connecting anti-parallel diodes to the transistors as shown in figure A.12. During the mode by mode analysis, I assume that the capacitor voltage is kept constant.

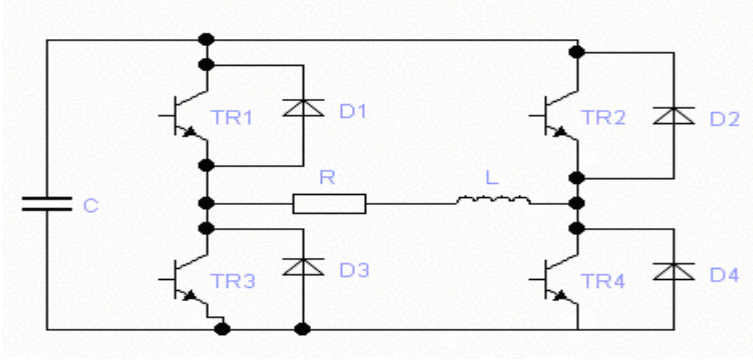


Figure A.12 Anti-parallel diodes connected to topology shown in figure A.11

Mode 1:

The voltage and the current are positive. TR1 and TR4 are on. The load voltage is the input voltage minus the voltage drops on the transistors as shown in figure A.13.

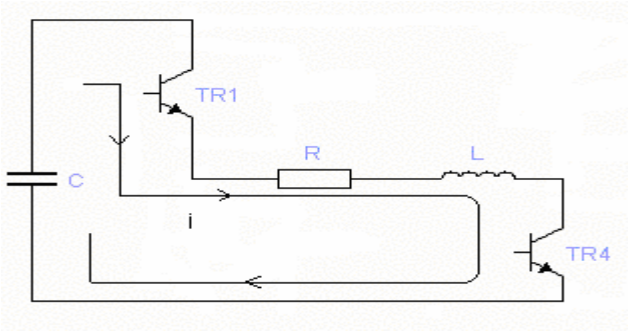


Figure A.13 TR1 and TR4 are on

Mode 2:

The voltage is negative but the current is still positive. TR1 and TR4 are turned off. The current continues to flow through D2 and D3 and even if the gate signals are applied, TR2 and TR3 can not be turned on. The load voltage is the reverse of the input voltage minus the voltage drops on the diodes. This mode continues until the load current becomes zero as shown in figure A.14.

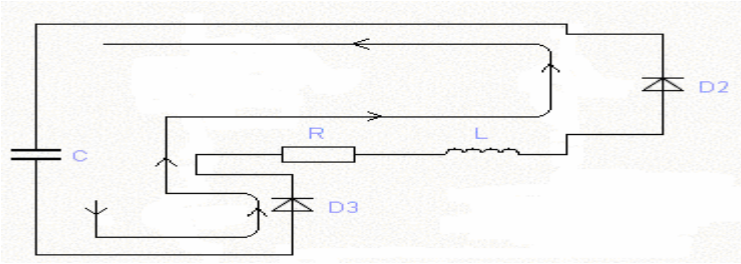


Figure A.14 D2 and D3 are on

Mode 3:

Both the voltage and the current are negative. TR2 and TR3 are on as shown in figure A.15. The load voltage is the reverse of the input voltage minus the voltage drops on the transistors.

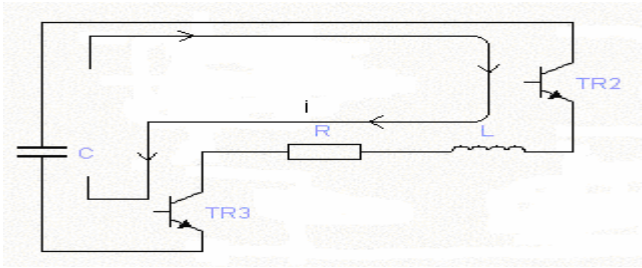


Figure A.15 TR2 and TR3 are on

Mode 4:

The voltage is now positive but the current is still negative. TR2 and TR3 are turned off. The current continues to flow through D1 and D4 and even the gate signals are applied, TR1 and TR4 can not be turned on as shown in figure A.16. The load voltage is the input voltage minus the voltage drops on the diodes. This mode continues until the load current becomes zero.

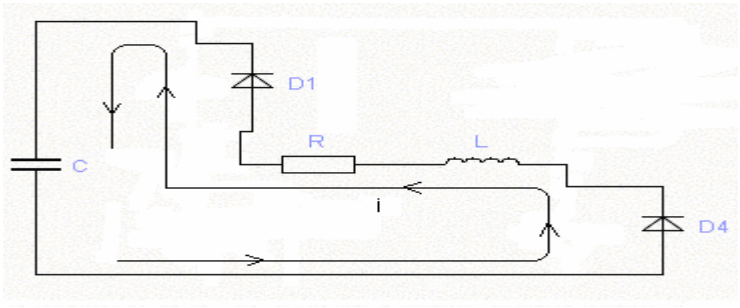


Figure A.16 D1 and D4 are on

The theoretical voltage and current waveforms indicating the operation modes for inductive load are shown in Figure A.17

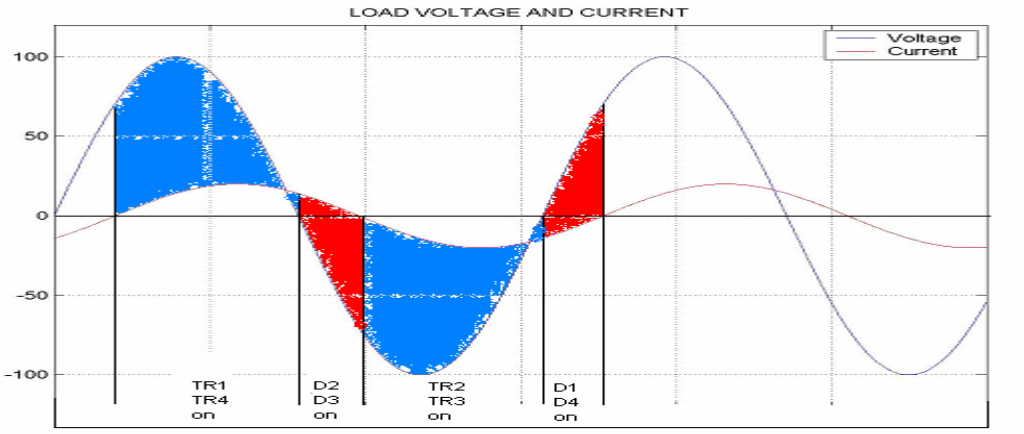


Figure A.17 Theoretical voltage and current waveforms indicating the operation modes for inductive load

A.5.1.5 Topology Five of the Full Controlled H-Bridge Inverter

The fifth topology of full controlled inverter's is a mid-point connection inverter, consists of only two transistors but two capacitors at the input as shown in figure A.18. During the mode by mode analysis, I assume that the capacitor voltages are same and kept constant. This circuit works properly for in-phase load voltage and current.

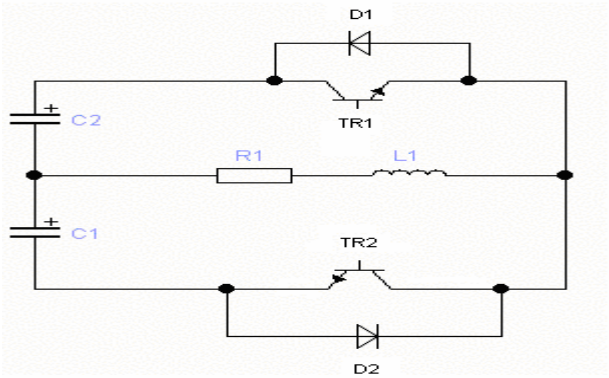


Figure A.18 Fifth topology consists of two transistors, two capacitors at the input

For inductive load;

Mode 1:

The voltage and the current are positive. TR1 is on. The load voltage is the input voltage minus the voltage drop on the transistor as shown in figure A.19.

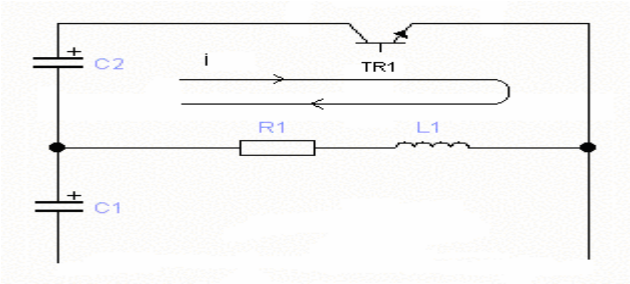


Figure A.19 TR1 is on

Mode 2:

The voltage is negative but the current is still positive. TR1 is turned off. The current continues to flow through D2 and even the gate signals are applied, TR2 can not be turned on as shown in figure A.20. The load voltage is the reverse of the input voltage minus the voltage drop on the diode. This mode continues until the load current becomes zero.

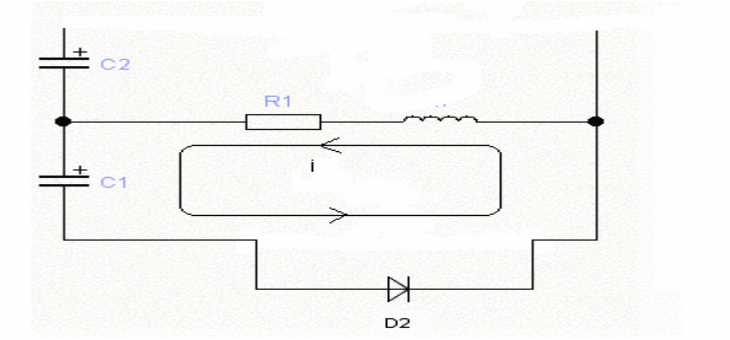


Figure A.20 D2 is on

Mode 3:

Both the voltage and the current are negative. TR2 is on as shown in figure A.21. The load voltage is the reverse of the input voltage minus the voltage drop on the transistor.

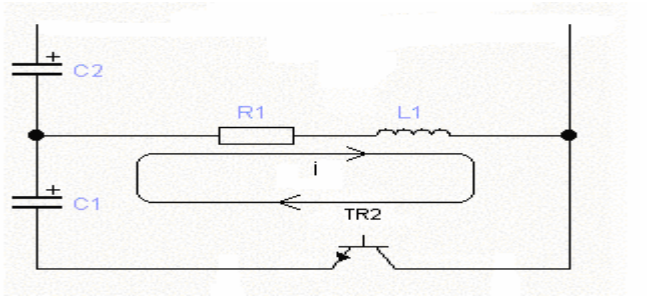


Figure A.21 TR2 is on

Mode 4:

The voltage is now positive but the current is still negative. TR2 is turned off. The current continues to flow through D1 and even the gate signals are applied, TR1 can not be turned on as shown in figure A.22. The load voltage is the input voltage minus the voltage drop on the diode. This mode continues until the load current becomes zero.

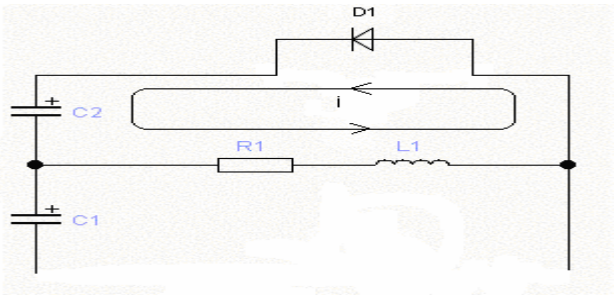


Figure A.22 D1 is on

The theoretical voltage and current waveforms indicating the operation modes for inductive load are as shown in figure A.23. Note that, under the given assumptions, the waveforms are same with topology six except for the amplitude of the input voltage levels. It is the half of the bridge inverter topologies as two capacitors are connected in series. But this topology uses half the number of semiconductor switches used in other full controlled bridge inverters.

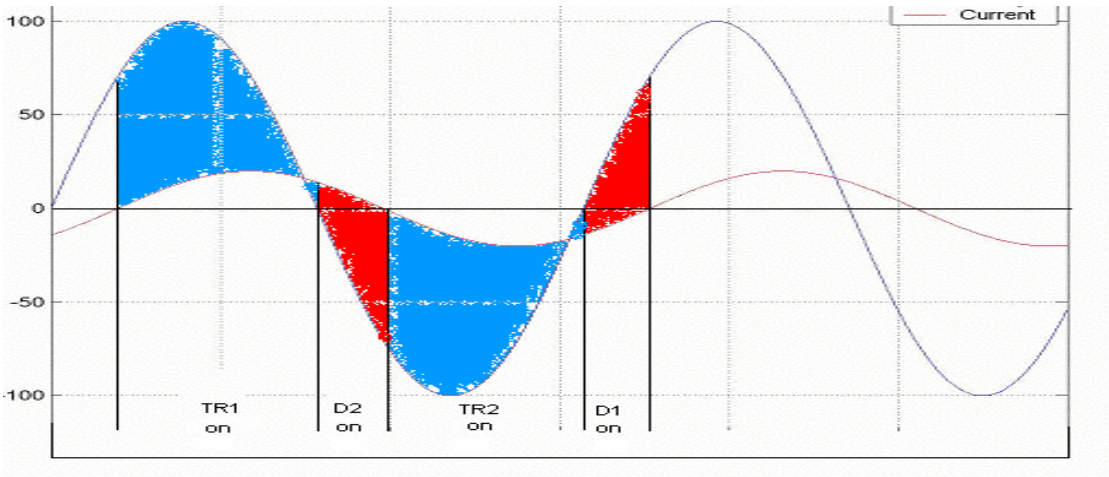


Figure A.23 Theoretical voltage and current waveforms indicating the operation modes for inductive load

Topology two would also be suitable for our application. But force commutation circuits must be used to turn off the thyristors which means additional cost and volume. That's why this topology is rejected.

Under the given assumptions, the results are satisfactory for circuit topologies four and five of the full controlled bridge inverters. But when the practical facts are taken into account (the non ideal capacitor voltages), topology five of the full controlled H-bridge inverter seems to be difficult to implement practically. So, topology four of the full controlled bridge inverter is chosen as the inverter stage for the further analysis.

A.6 Sinusoidal Filters Available in the Market

RED
INDUCTIVE COMPONENTS
SETZERMANN

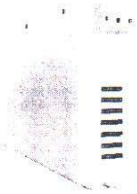
Sinusfilter (3 x 400 V)
Sinusoidal Filter (3 x 400 V)
Filtre sinus (3 x 400 V)

Baureihe CNW 930
Type CNW 935/..

Anwendungen:
Sinusformung des Ausgangsstromes an einem Frequenzumrichterausgang. Zur Lebensdauerverl[illegible] der Motorisolation, Geräuschminderung.

Applications:
Sine wave creation of the output current on the [illegible] of a frequency drive.
Longer lifetime of motor insulation, noise reduct[illegible]

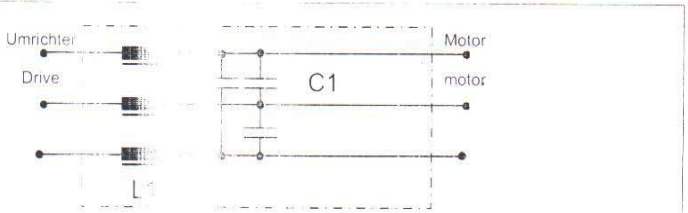
Applications:
Formation de sinus du courant de sortie à la sort[illegible] convertisseur de fréquence. Durée de vie plus lo[illegible] l'isolation du moteur.



Prüfspannung/ Test voltage/ Tension d'essai
L-L 2100 V, DC 1 s L-PE 2700 V, DC 1s
Klimakategorie/ Climatic category/ Catégorie climatique
DIN IEC 68 Teil 1 25/085/21

Überlast / Overload / Surcharge
1,5 x I_{Nenn} 1 min / h

Schaltung • Circuit • Circuit



Vorteile:
- Geringe Erwärmung
- Sehr geräuscharm
- Einfacher Anschluß
- Anpassung an Motorleitungen bis 1000 Meter möglich
- Einsparung der geschirmten Leitung möglich
- Höhere Taktfrequenz bis 16 kHz möglich
- Abgestimmte Einbaumaße mit Netzfilter und Bremswiderstand

Benef[illegible]
- Lo[illegible]
- lov[illegible]
- sim[illegible] tion
- ada[illegible] dor cables up to 10[illegible] le
- in [illegible] ses the need for scr[illegible] es is avoided
- hig[illegible] quency up to 16 kH[illegible]
- mo[illegible] nsions adapted to tho[illegible] filter and braking res[illegible]

Ses avantages:
- Faible échauffement
- à bruit faible
- assemblage facile et rapide
- adaptation aux câbles, de moteur possible jusqu'à 1000 m
- dans la plupart des cas l'utilisation des câbles blindés est évitée
- fréquence de cycles possible jusqu'à 16 kHz
- dimensions de montage adaptées aux filtre de réseau et résistance de freinage

RED
INDUCTIVE COMPONENTS
SETZERMANN

Technische Daten • Technical data • Données techniques

Type	BV-Nummer	für Motorleistung bis [kW]	für Nennstrom bis [3 x A]	ΣL [mH]	C [µF]
CNW 935/6	944800	2.2	6,0	7,2	2,2
CNW 935/10	944801	4.0	10,0	4,8	4,4
CNW 935/16	944802	5.5	16,0	3,5	6,6
CNW 935/25	944803	11.0	25,0	2,1	6,6
CNW 935/32	944804	15.0	32,0	1,8	6,6

Nennspannung: 3 x 400V
Frequenz: 50/60 Hz

Rated voltage: 3 x 400V
Frequency: 50/60 Hz

Courant nominal: 3 x 400V
Fréquence: 50/60 Hz

Andere Leistungen / Nennströme auf Anfrage!

Die Ausgangsfilter sind auf Motorleitungen bis zu 200 m ausgerichtet. Bei längeren Leitungen wird eine geringe Anpassung durchgeführt. Geben Sie dazu bitte die Länge und den Typ der Leitung an. Wichtig ist es, darauf zu achten die Ein- und Ausgangsklemmen nicht zu tauschen. Das Anschließen der Kondensatoren direkt an den Umrichter Ausgang kann zu einer Schädigung der Schaltung führen.	The output filters are designed for motor cables up to 200 m, with longer cables a small adaption will be effected. Just let us know the cable type and length. It is important to ensure that the input and output terminals are not exchanged. Direct connection of the capacitors on the inverter output may damage the circuit.	Les filtres de sortie sont conçus pour des câbles de moteur jusqu'à 200 m de longueur. A partir de 200 m une petite adaption est effectué. A ce propos, veuillez indiquer la longeur et le type de câble. Il faut absolument observer que les bornes de l'entrée et à la sortie ne soient pas interchangées. La connection des condensateurs directe à la sortie du convertisseur peut endommager le circuit.

A Spannungsverlauf ohne Sinusfilter

B Spannungsverlauf mit Sinusfilter

Der Transformator.
Tauscher

Sinusfilter, Motorfilter, dreiphasig

Sinusfilter (3 x 400V) als Tiefpassfilter aus Drossel und Kondensator für Frequenzumrichter nach EN 61558, VDE 0570

Einsatzmöglichkeiten

Geregelte Drehstrom-Antriebe mit Frequenzumrichter für Druckmaschinen, Holz-/Kunststoff-Maschinen, Textilmaschinen, Verpackungsmaschinen, Werkzeugmaschinen. Fertigungs-automaten, Förder-, Kran- und Transporttechnik, Bahnfahrzeuge, Mahlwerke, Rührwerke, Pumpen, Verdichter, Gebläse, Ventilatoren und Chemische Verfahrenstechnik, Bordnetzanlagen, Prüfeinrichtungen, Windkraft- und Solaranlagen

Beschreibung

Drossel mit Kondensator zur Sinusformung des Ausgangsstromes an einen Frequenzumrichterausgang.
Zur Lebensdauerverlängerung der Motorisolation durch reduziertes du/dt und Geräuschminderung.
Betrieb von Motoren über lange Zuleitungen, Einsparung einer geschirmten Leitung möglich, günstigere EMV-Werte.

Sinusoidal filter, motor filters, three-phase

Sinusoidal filter (3 x 400V) as low-pass filter with reactor and capacitor for frequency inverter to EN 61558, VDE 0570

applications

controlled threephase drives with frequency inverter for printmachines, wood/plastics machines, textilmachines, packingmachines, machine-tools, automatic productionmachines, conveying machines, cranes, railway/trains, grinding-mills, mixer-machines, pumping apparatus, ventilators and chemical industries. test equipments, windpowerplants and solarenergy plants.

description

Reactor with capacitor for sine wave creation of the output current of a frequency drive.
Longer lifetime of motor insulation with reduction of du/dt and parasitic noise reduction.
Use of motors with long cables possible, in most cases a screened cable it not necessary, better EMC datas.

Technische Daten

Sinusdrossel mit Kondensator nach EN 61558, VDE 0570
Frequenzbereich: 0 Hz bis 120 Hz
Schaltfrequenz 3 kHz bis 8 kHz
Bereich der Bemessungsspannung: bis 3 x 400 V
(höhere Werte auf Anfrage)
Additive Umrichtermehrbelastung: typ. + 10 % des Bemessungsstroms
Prüfspannung: Wicklung - Kern: 2,5 kV
gute EMV-Verhältnisse
große thermische Stabilität
Isolationsklasse: F
max. Umgebungstemperatur: 40°C
Überlast: 1,5 x I Nenn 1 Min/h
Brandschutzklasse: UL94V0
Vorbereitet für Schutzklasse I
Schutzart: IP00
Nennströme von 2,5A bis 610A
Drossel 2 x im Vakuum getränkt
Klemmen berührungssicher nach VBG4, oder
Flachanschluss für Bolzen oder zum Stecken, nicht berührsicher

technical datas

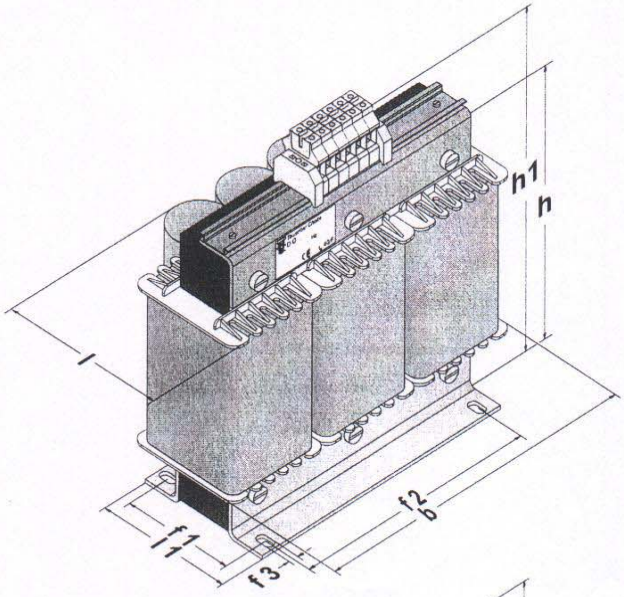
Sinewave reactor with capacitor according EN 61558, VDE 0570
frequency range: 0 Hz to 120 Hz
switching frequency 3 kHz to 8 kHz
range of rated voltage: until 3x 400 V
(higher values on request),
additve load of inverter: type + 10 % of rated current
test- voltage: winding - core: 2,5 kV
good EMI conditions
high thermic stability
temperature class: F
max. ambient temperature: 40°C
over load: 1,5 I 1 min/h
fire class: UL94V0
prepared for protection index I
protective class: IP00
current from 2,5A until 610A
chokes 2 x laquered under vacuum
block terminals safe according VBG4 or
flat termination with bolt or for plugging, not touch safe

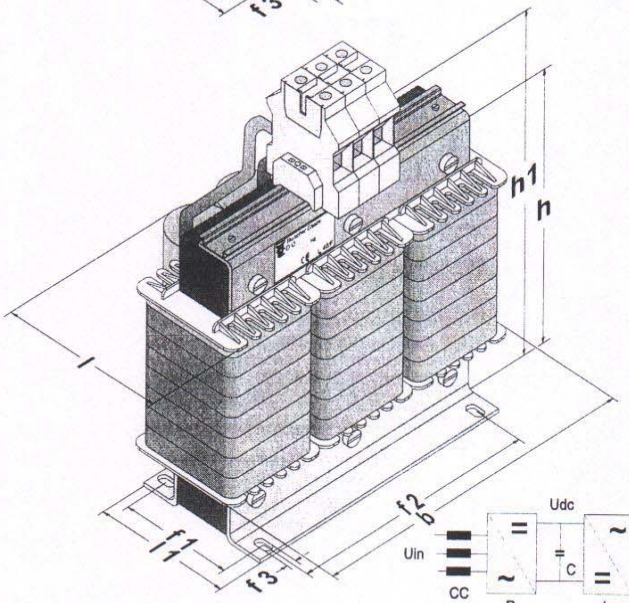
Der Transformator.
Tauscher

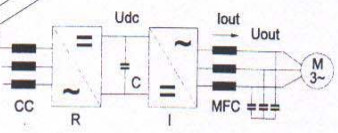
Sinusfilter, Motorfilter, dreiphasig

Sinusoidal filter, motor filters, three-phase

CE







Legende:		legend:
MFC	Motordrossel	motor filter choke
FC	Filterkondensatoren	filter capacitors
M	Motor	motor
CC	Kommutierungsdrossel	commutation choke
R	Gleichrichter	rectifyer
I	Inverter	inverter

Der Transformator.
Tauscher

Sinusfilter, Motorfilter, dreiphasig

Sinusoidal filter, motor filters, three-phase

Type type	Bemess-ungsstrom rated current A	Induktivität pro Phase inductance at 1phase mH	Energie energy 0,5 x L x I² mWs	für Motor-nennleistung for motor rated power kW	Abmessungen dimensions in mm					Montage-löcher mounting in mm			Kupfer-gewicht copper weight kg	Gesamt-gewicht total weight kg
					b	l	l1	h	h1	f1	f2	f3		
DEO 100/100/21	2,5	22	69	1,1	122	52	53	107	140	39	90	4,8	0,7	2,1
DEO 100/100/21	4	10,5	84	1,5	122	52	53	107	140	39	90	4,8	0,7	2,1
DEO 100/100/31	6	6,1	110	2,2	122	64	63	107	140	49	90	4,8	0,7	2,8
DEO 125/125/26,5	8	4,6	147	3,0	152	66	67	133	168	50	113	5,8	0,7	4,1
DEO 125/125/41,5	10	4,4	220	4,0	152	83	82	133	168	65	113	5,8	1,7	5,9
DEO 125/125/41,5	12	4,1	295	5,5	152	83	82	133	168	65	113	5,8	1,7	5,9
DEO 125/125/41,5	16	2,5	320	7,5	152	83	82	133	168	65	113	5,8	1,7	5,9
DEO 150/150/41,5	18	2,5	405	7,5	183	90	86	157	190	67	136	7	2,7	8,8
DEO 150/150/51,5	24	1,6	461	11	183	90	96	157	190	77	136	7	3,2	10,7
DEO 190/190/40	30	1,9	855	15	231	96	91	198	240	71	176	7	5,2	14,6
DEO 200/200/51	37	1,4	958	18,5	243	112	107	208	260	81	185	9	6,6	19,9
DEO 200/200/61	48	1,2	1382	22	243	122	117	208	260	91	185	9	8,4	26,8
DEO 200/200/71	60	0,95	1710	30	243	134	127	208	260	101	185	9	8,4	26,8
DEO 250/250/52	75	0,8	2250	37	305	122	124	260	320	94	224	10	11,7	33,0
DEO 250/250/77	90	0,6	2430	45	305	153	149	260	320	119	224	10	13,9	45,0
DEO 300/300/63	115	0,5	3306	55	370	156	155	306	380	125	264	10	18,6	56,0
DEO 300/300/78	150	0,5	5625	75	370	173	170	306	380	140	264	10	20,0	66,0
DEO 300/300/93	180	0,4	6480	90	370	189	185	306	380	155	264	10	27,8	83,0
DEO 350/350/103	200	0,4	8000	110	430	199	205	362	440	173	316	12	47	130
DEO 350/350/103	250	0,3	9375	132	430	199	205	362	440	173	316	12	47	130
DEO 400/400/110	325	0,3	15844	160	490	231	232	415	490	214	356	15	77	180
DEO 400/400/140	440	0,2	19360	250	490	275	252	415	490	214	356	15	77	225
DEO 500/500/150	510	0,17	22109	315	600	277	230	500	570	200	450	18	47	261
DEO 500/500/175	610	0,14	26047	355	600	288	255	500	570	225	450	18	55	305